

## 11.3 Gbps Modulator Driver

Check for Samples: [ONET1141L](#)

### FEATURES

- Digitally Selectable Output Amplitude up to 2.0VPP Single-Ended
- Digitally Selectable Bias Current up to 145mA Source
- 2-wire Digital Interface with Integrated DACs and ADC for Control and Diagnostic Management
- Automatic Power Control (APC) Loop
- Adjustable Rise and Fall Times
- Programmable Input Equalizer
- Cross-Point Control
- Selectable Monitor PD Current Range and Polarity

- Includes Laser Safety Features
- Single 3.3V Supply
- –40°C to 100°C Operation
- Surface Mount Small Footprint 4mm x 4mm 24 Pin RoHS Compliant QFN Package

### APPLICATIONS

- 10 Gigabit Ethernet Optical Transmitters
- SONET OC-192/SDH STM-64 Optical Transmitters
- 10G-EPON and XG-PON
- SFP+ and XFP Transceiver Modules
- XENPAK, XPAK, X2 and 300-pin MSA Transponder Modules

### DESCRIPTION

The ONET1141L is a high-speed, 3.3V electroabsorption modulator driver designed to bias and modulate an electroabsorptive modulated laser (EML) at data rates from 1 Gbps up to 11.3 Gbps.

The device provides a two-wire serial interface which allows digital control of the modulation and bias currents, eliminating the need for external components. Output waveform control, in the form of cross-point adjustment and rise and fall time adjustment are available to improve the optical eye mask margin. An optional input equalizer can be used for equalization of up to 150mm (6") of microstrip or stripline transmission line on FR4 printed circuit boards. The device contains internal analog to digital and digital to analog converters to eliminate the need for special purpose microcontrollers.

The ONET1141L includes an integrated automatic power control (APC) loop which compensates for variations in laser average optical power over voltage and temperature and circuitry to support laser safety and transceiver management systems.

The modulator driver is characterized for operation from –40°C to 100°C case temperatures and is available in a small footprint 4mm x 4mm 24 pin RoHS compliant QFN package.



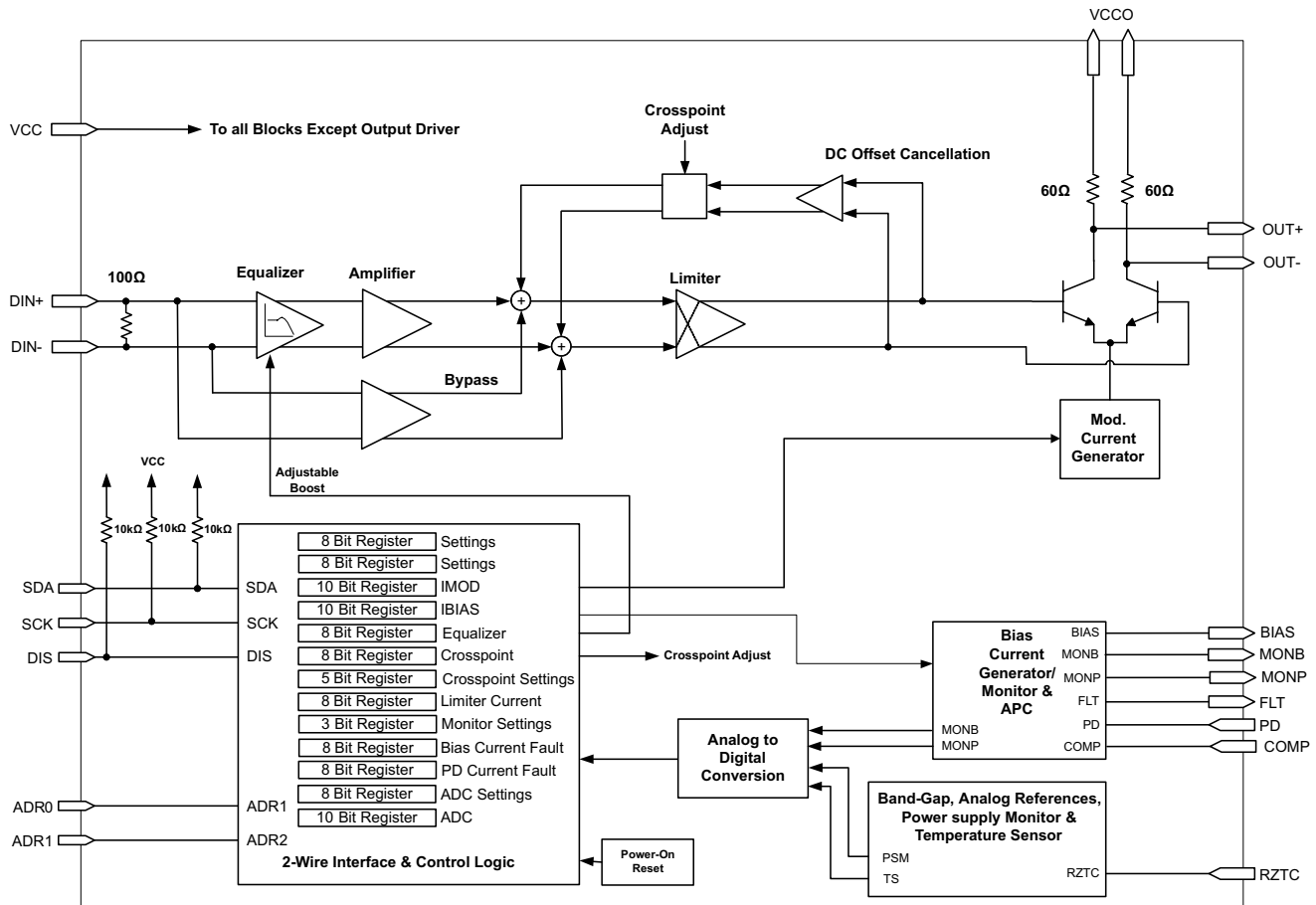
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## BLOCK DIAGRAM

A simplified block diagram of the ONET1141L is shown in Figure 1. The modulator driver consists of an input equalizer with selectable bypass, a limiter, an output driver, DC offset cancellation with cross point control, power-on reset circuitry, a 2-wire serial interface including a control logic block, a modulation current generator, a bias current generator with automatic power control loop, an analog to digital converter and an analog reference block.

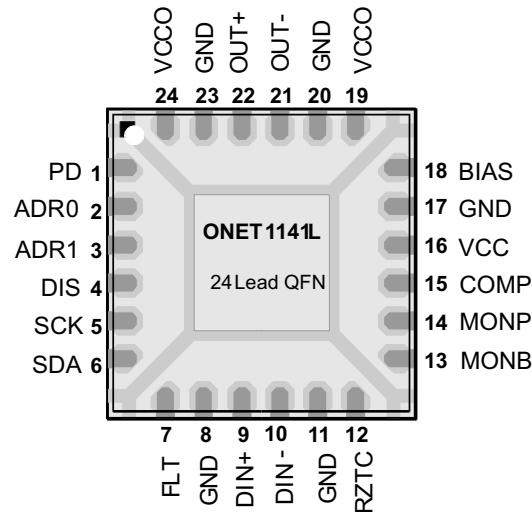


**Figure 1. Simplified Block Diagram of the ONET1141L**

## PACKAGE

The ONET1141L is packaged in a small footprint 4mm X 4mm 24 pin RoHS compliant QFN package with a lead pitch of 0.5mm. The pin out is shown below.

24 PIN QFN PACKAGE, 4mm x 4mm  
(TOP VIEW)



PIN FUNCTIONS

| NO.                   |      | TYPE           | DESCRIPTION   |
|-----------------------|------|----------------|---|
| PIN                   | NAME |                |   |
| 1                     | PD   | Analog         | Photodiode input. Pin can source or sink current dependent on register setting.   |
| 2                     | ADR0 | Digital-in     | 2-wire interface address programming pin. Leave this pad open for a default address of 0001000. Pulling the pin to VCC changes the 1 <sup>st</sup> address bit to a 1 (address = 0001001)   |
| 3                     | ADR1 | Digital-in     | 2-wire interface address programming pin. Leave this pad open for a default address of 0001000. Pulling the pin to VCC changes the 2 <sup>nd</sup> address bit to a 1 (address = 0001010)   |
| 4                     | DIS  | Digital-in     | Disables both bias and modulation currents when set to high state. Includes a 10kΩ or 40kΩ pull-up resistor to VCC. Toggle to reset a fault condition.  |
| 5                     | SCK  | Digital-in     | 2-wire interface serial clock input. Includes a 10kΩ or 40kΩ pull-up resistor to VCC.   |
| 6                     | SDA  | Digital-in/out | 2-wire interface serial data input/output. Includes a 10kΩ or 40kΩ pull-up resistor to VCC.   |
| 7                     | FLT  | Digital-out    | Fault detection flag. High level indicates that a fault has occurred. Open drain output. Requires an external 4.7kΩ to 10kΩ pull-up resistor to VCC for proper operation.   |
| 8, 11, 17, 20, 23, EP | GND  | Supply         | Circuit ground. Exposed die pad (EP) must be grounded.  |
| 9                     | DIN+ | Analog-in      | Non-inverted data input. On-chip differentially 100Ω terminated to DIN-. Must be AC coupled.  |
| 10                    | DIN- | Analog-in      | Inverted data input. On-chip differentially 100Ω terminated to DIN+. Must be AC coupled.  |
| 12                    | RZTC | Analog         | Connect external zero TC 28.7kΩ resistor to ground (GND). Used to generate a defined zero TC reference current for internal DACs.   |
| 13                    | MONB | Analog-out     | Bias current monitor. Sources a 1% replica of the bias current. Connect an external resistor to ground (GND) to use the analog monitor (DMONB = 0). If the voltage at this pin exceeds 1.16V a fault is triggered. Typically choose a resistor to give MONB voltage of 0.8V at the maximum desired bias current. If the digital monitor function is used (DMONB = 1) the resistor must be removed.                                  |
| 14                    | MONP | Analog-out     | Photodiode current monitor. Sources a 12.5% replica of the photodiode current when PDRNG = 1X, a 25% replica when PDRNG = 01 and a 50% replica when PDRNG = 00. Connect an external resistor (5kΩ typical) to ground (GND) to use the analog monitor (DMONP = 0). If the voltage at this pin exceeds 1.16V a fault is triggered when MONPFLT = 1. If the digital monitor function is used (DMONP = 1) the resistor must be removed. |
| 15                    | COMP | Analog         | Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01μF capacitor to ground.   |
| 16                    | VCC  | Supply         | 3.3V ± 10% supply voltage.  |
| 18                    | BIAS | Analog         | Sinks or sources the bias current for the laser in both APC and open loop modes.  |
| 19, 24                | VCCO | Supply         | 3.3V ± 10% supply voltage for the output stage.   |
| 21                    | OUT- | CML-out        | Inverted data output.   |
| 22                    | OUT+ | CML-out        | Non-inverted data output.   |

## ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|  |   | VALUE |     | UNIT     |
|--|---|-------|-----|----------|
|  |   | MIN   | MAX |          |
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>   | -0.3  | 4.0 | V        |
| V <sub>ADR0</sub> , V <sub>ADR1</sub> , V <sub>DIS</sub> , V <sub>RZTC</sub> ,<br>V <sub>SCK</sub> , V <sub>SDA</sub> , V <sub>DIN+</sub> , V <sub>DIN-</sub> , V <sub>FLT</sub> ,<br>V <sub>MONB</sub> , V <sub>MONP</sub> , V <sub>COMP</sub> , V <sub>PD</sub> ,<br>V <sub>BIAS</sub> , V <sub>OUT+</sub> , V <sub>OUT-</sub> | Voltage at ADR0, ADR1, DIS, RZTC, SCK, SDA, DIN+, DIN-, FLT, MONB,<br>MONP, COMP, PD, BIAS, OUT+, OUT- <sup>(2)</sup> | -0.3  | 4.0 | V        |
| I <sub>DIN-</sub> , I <sub>DIN+</sub>  | Maximum current at input pins   |       | 25  | mA       |
| I <sub>OUT+</sub> , I <sub>OUT-</sub>  | Maximum current at output pins  |       | 120 | mA       |
| I <sub>BIAS-MAX</sub>  | Maximum bias current  |       | 180 | mA       |
| ESD  | ESD rating at all pins  |       | 2   | kV (HBM) |
| T <sub>J,max</sub>   | Maximum junction temperature  |       | 125 | °C       |
| T <sub>STG</sub>   | Storage temperature range   | -65   | 150 | °C       |
| T <sub>C</sub>   | Case temperature  | -40   | 110 | °C       |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                   |                                       |  | MIN  | TYP  | MAX  | UNIT              |
|-------------------|---------------------------------------|--|------|------|------|-------------------|
| V <sub>CC</sub>   | Supply voltage                        |  | 2.97 | 3.3  | 3.63 | V                 |
| V <sub>IH</sub>   | Digital input high voltage            | DIS, SCK, SDA  | 2.0  |      |      | V                 |
| V <sub>IL</sub>   | Digital input low voltage             | DIS, SCK, SDA  |      |      | 0.8  | V                 |
|                   | Photodiode current range              | Control bit PDRNG = 1X, step size = 3 μA             |      | 3080 |      | μA                |
|                   |                                       | Control bit PDRNG = 01, step size = 1.5 μA           |      | 1540 |      |                   |
|                   |                                       | Control bit PDRNG = 00, step size = 0.75 μA          |      | 770  |      |                   |
| R <sub>RZTC</sub> | Zero TC resistor value <sup>(1)</sup> | 1.16V bandgap bias across resistor, E96, 1% accuracy | 28.4 | 28.7 | 29   | kΩ                |
| V <sub>IN</sub>   | Differential input voltage swing      | EQENA = 1  | 160  |      | 1000 | mV <sub>p-p</sub> |
|                   |                                       | EQENA = 0  | 400  |      | 1000 |                   |
| t <sub>R-IN</sub> | Input rise time                       | 20%–80%  |      | 30   | 55   | ps                |
| t <sub>F-IN</sub> | Input fall time                       | 20%–80%  |      | 30   | 55   | ps                |
| T <sub>C</sub>    | Temperature at thermal pad            |  | -40  |      | 100  | °C                |

- (1) Changing the value will alter the DAC ranges.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, with 50Ω output load, open loop operation,  $V_{OUT} = 2.0V_{pp}$ ,  $I_{BIAS} = 80\text{ mA}$ , and  $R_{RZTC} = 28.7k\Omega$  unless otherwise noted. Typical operating condition is at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$

| PARAMETER       | CONDITION                                   | MIN  | TYP | MAX  | UNIT  |                |    |
|-----------------|---|--|-----|------|-------|----------------|----|
| $V_{CC}$        | Supply voltage                              | 2.97   | 3.3 | 3.63 | V     |                |    |
| $I_{VCC}$       | Supply current                              | $V_{OUT} = 2.0V_{pp}$ , $I_{BIAS} = 0\text{mA}$ , $EQENA = 0$                            |     | 143  | 170   | mA             |    |
|                 |   | $V_{OUT} = 2.0V_{pp}$ , $I_{BIAS} = 0\text{mA}$ , $EQENA = 1$                            |     | 151  | 182   |                |    |
|                 |   | Output off (DIS = HIGH), $V_{OUT} = 2.0V_{pp}$ , $I_{BIAS} = 80\text{ mA}$ , $EQENA = 0$ |     | 40   |       |                |    |
| $R_{IN}$        | Data input resistance                       | Differential between DIN+ / DIN-   |     | 82   | 100   | 118            | Ω  |
| $R_{OUT}$       | Output resistance                           | Single-ended at OUT+ or OUT-   |     | 50   | 60    | 70             | Ω  |
|                 | Digital input current                       | SCK, SDA, pull up to VCC   |     | 2    | 360   | 470            | μA |
|                 | Digital input current                       | DIS, pull up to VCC  |     | 2    | 360   | 470            | μA |
| $V_{OH}$        | Digital output high voltage                 | FLT, pull-up to $V_{CC}$ , $I_{SOURCE} = 50\text{ μA}$                                   |     | 2.4  |       |                | V  |
| $V_{OL}$        | Digital output low voltage                  | FLT, pull-up to $V_{CC}$ , $I_{SINK} = 350\text{ μA}$                                    |     |      |       | 0.4            | V  |
| $I_{BIAS-MIN}$  | Minimum bias current                        | See (1)  |     |      |       | 5              | mA |
| $I_{BIAS-MAX}$  | Maximum bias current                        | Source. $BIASPOL = 0$ , DAC set to maximum, open and closed loop                         |     | 145  | 160   |                | mA |
|                 |   | Sink. $BIASPOL = 1$ , DAC set to maximum, open and closed loop                           |     | 93   | 105   |                |    |
| $I_{BIAS-DIS}$  | Bias current during disable                 |  |     |      |       | 100            | μA |
|                 | Average power stability                     | APC loop enabled   |     |      | ±0.5  |                | dB |
|                 | Bias pin compliance voltage                 | Source. $BIASPOL = 0$  |     | 0.9  |       |                | V  |
|                 |   | Sink. $BIASPOL = 1$  |     |      |       | $V_{CC} - 0.9$ |    |
|                 | Temperature sensor accuracy                 | With 1-point external mid scale calibration  |     |      | ±3    |                | °C |
| $V_{PD}$        | Photodiode reverse bias voltage             | APC active, $I_{PD} = \text{max}$  |     | 1.3  | 2.3   |                | V  |
|                 | Photodiode fault current level              | Percent of target $I_{PD}$ (2)   |     |      | 150%  |                |    |
|                 | Photodiode current monitor ratio            | $I_{MONP} / I_{PD}$ with control bit PDRNG = 1X  |     | 10%  | 12.5% | 15%            |    |
|                 |   | $I_{MONP} / I_{PD}$ with control bit PDRNG = 01  |     | 20%  | 25%   | 30%            |    |
|                 |   | $I_{MONP} / I_{PD}$ with control bit PDRNG = 00  |     | 40%  | 50%   | 60%            |    |
|                 | Monitor diode DMI accuracy                  | With external calibration at 200 μA  |     | -10% |       | 10%            |    |
|                 | Bias current monitor ratio                  | $I_{MONB} / I_{BIAS}$ (nominal 1/100 = 1%)   |     | 0.9% | 1.0%  | 1.1%           |    |
|                 | Bias current DMI accuracy                   | Bias current ≥ 30 mA   |     |      | ±10%  |                |    |
|                 | Power supply monitor accuracy               | With external mid scale calibration  |     | -2%  |       | 2%             |    |
| $V_{CC-RST}$    | $V_{CC}$ reset threshold voltage            | $V_{CC}$ voltage level which triggers power-on reset                                     |     |      | 2.5   | 2.8            | V  |
| $V_{CC-RSTHYS}$ | $V_{CC}$ reset threshold voltage hysteresis |  |     |      | 100   |                | mV |
| $V_{MONB-FLT}$  | Fault voltage at MONB                       | Fault occurs if voltage at MONB exceeds value  |     | 1.1  | 1.16  | 1.24           | V  |

(1) The bias current can be set below the specified minimum according to the corresponding register setting, however in closed loop operation settings below the specified value may trigger a fault.

(2) Assured by simulation over process, supply and temperature variation.

## AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, with 50Ω output load, open loop operation,  $V_{OUT} = 2.0V_{pp}$ ,  $I_{BIAS} = 80\text{ mA}$ , and  $R_{RZTC} = 28.7k\Omega$  unless otherwise noted. Typical operating condition is at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$

| PARAMETER      |   | CONDITION  | MIN | TYP  | MAX | UNIT              |
|----------------|---|--|-----|------|-----|-------------------|
| SDD11          | Differential input return gain              | 0.01 GHz $f < 5$ GHz   |     | -15  |     | dB                |
|                |   | 5 GHz $< f < 11.1$ GHz   |     | -8   |     |                   |
| SCD11          | Differential to common mode conversion gain | 0.01 GHz $< f < 11.1$ GHz  |     | -20  |     | dB                |
| $t_{R-OUT}$    | Output rise time                            | 20%–80%, $t_{R-IN} < 40$ ps, 50Ω load, single-ended, crosspoint = 50%  |     | 28   | 40  | ps                |
| $t_{F-OUT}$    | Output fall time                            | 20%–80%, $t_{F-IN} < 40$ ps, 50Ω load, single-ended, crosspoint = 50%  |     | 28   | 40  | ps                |
| $V_{O-MIN}$    | Minimum output amplitude                    | 50Ω load, single-ended   |     |      | 200 | mVpp              |
| $V_{O-MAX}$    | Maximum output amplitude                    | 50Ω load, single-ended   | 2.0 |      |     | Vpp               |
|                | Output Amplitude Stability                  | 50Ω load, single-ended   |     |      | 250 | mV                |
| $V_{MOD-STEP}$ | Modulation voltage step size                | 50Ω load, 10 Bit Register  |     | 2.5  |     | mV                |
| DJ             | Deterministic output jitter                 | EQENA = 1 with maximum equalization, K28.5 pattern at 11.3 Gbps, 160mVpp, 600mVpp, 1000mVpp differential input voltage, single-ended output                                    |     | 5    | 15  | PS <sub>p-p</sub> |
|                |   | EQENA = 1, K28.5 pattern at 11.3 Gbps, maximum equalization with 6" transmission line at the input, 160mVpp, 600mVpp, 1000mVpp input to transmission line, single-ended output |     | 7    |     |                   |
| RJ             | Random output jitter                        |  |     | 0.2  | 0.6 | PS <sub>RMS</sub> |
| $T_{APC}$      | APC time constant                           | $C_{APC} 0.01\ \mu F$ , $I_{PD} = 100\ \mu A$ , PD coupling ratio CR = 40 <sup>(1)</sup>   |     | 120  |     | μs                |
|                | High cross point control range              | 50Ω load, single-ended   |     | 75%  |     |                   |
|                | Low cross point control range               | 50Ω load, single-ended   |     | 30%  |     |                   |
|                | Cross point stability                       | 50Ω load, single-ended, $V_{IN} \geq 400mV_{pp}$   |     | ±5%  |     |                   |
| $T_{OFF}$      | Transmitter disable time                    | Rising edge of DIS to $I_{BIAS} \leq 0.1 \times I_{BIAS-NOMINAL}$ <sup>(1)</sup>   |     | 0.05 | 5   | μs                |
| $T_{ON}$       | Disable negate time                         | Falling edge of DIS to $I_{BIAS} \geq 0.9 \times I_{BIAS-NOMINAL}$ <sup>(1)</sup>  |     |      | 1   | ms                |
| $T_{INIT1}$    | Power-on to initialize                      | Power-on to registers ready to be loaded   |     | 1    | 10  | ms                |
| $T_{INIT2}$    | Initialize to transmit                      | Register load STOP command to part ready to transmit valid data <sup>(1)</sup>   |     |      | 2   | ms                |
| $T_{RESET}$    | DIS pulse width                             | Time DIS must held high to reset part <sup>(1)</sup>   | 100 |      |     | ns                |
| $T_{FAULT}$    | Fault assert time                           | Time from fault condition to FLT high <sup>(1)</sup>   |     |      | 50  | μs                |

(1) Assured by simulation over process, supply and temperature variation.

## DETAILED DESCRIPTION

### EQUALIZER

The data signal is applied to an input equalizer by means of the input signal pins DIN+/DIN–, which provide on-chip differential 100Ω line-termination. The equalizer is enabled by setting EQENA = 1 (bit 1 of register 0). Equalization of up to 150mm (6”) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is digitally controlled by the two-wire interface and control logic block and is dependant on the register settings EQADJ[0..7] (register 6). The equalizer can be turned off and bypassed by setting EQENA = 0 and the supply current is reduced. For details about the equalizer settings, see [Table 19](#).

### LIMITER

By limiting the output signal of the equalizer to a fixed value, the limiter removes any overshoot after the input equalization and provides the input signal for the output driver. Adjustments to the limiter bias current and emitter follower current can be made to trade off the rise and fall times and supply current. The limiter bias current is adjusted through LIMCSGN (bit 7 of register 9) and LIMC[0..2] (bits 4, 5 and 6 of register 9). The emitter follower current is adjusted through EFCSGN (bit 3 of register 9) and EFC[0..2] (bits 0, 1 and 2 of register 9).

### HIGH-SPEED OUTPUT DRIVER

The modulation current is sunk from the common emitter node of the limiting output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages are connected to the output pins OUT+ and OUT–. The collectors have internal 60Ω back termination resistors to VCCO. The outputs are optimized to drive a 50Ω single-ended load and to obtain the maximum single-ended output voltage of 2.0Vpp, AC coupling and inductive pull-ups to VCC are required.

The polarity of the output pins can be inverted by setting the output polarity switch bit, POL (bit 2 of register 0) to 1.

### MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The circuit is digitally controlled by the 2-wire interface block.

A 10-bit wide control bus, MODC[0..9] (registers 2 and 3), is used to set the desired modulation current, and therefore, the output voltage. The modulation current can be increased by setting HCENA = 1 (bit 4 of register 1) and enabling the high modulation current mode, however, the single-ended output voltage should be kept below 2Vpp for the best performance.

The modulation current can be disabled by setting the DIS input pin to a high level or setting ENA = 0 (bit 7 of register 0). The modulation current is also disabled in a fault condition if the internal fault detection enable register flag FLTEN is set to 1 (bit 3 of register 0).

### DC OFFSET CANCELLATION AND CROSS POINT CONTROL

The ONET1141L has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled by setting OCDIS = 1 (bit 3 of register 1). To adjust the eye crossing point, set CPENA = 1 (bit 2 of register 8). The crossing point can be moved toward the one level by setting CPSGN = 1 (bit 7 of register 7) and it can be moved toward the zero level by setting CPSGN = 0. The percentage of shift depends upon the register settings CPADJ[0..6] (register 7), and the cross point adjustment range bits CPRNG[0..1] (register 8). Setting CPRNG1 = 0 and CPRNG0 = 0 results in minimum adjustment capability and setting CPRNG1 = 1 and CPRNG0 = 1 results in maximum adjustment capability.

## BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the 2-wire interface. In open loop operation, selected by setting OLENA = 1 (bit 4 of register 0) the bias current is set directly by the 10-bit wide control word BIASC[0..9] (registers 4 and 5). In automatic power control mode, selected by setting OLENA = 0, the bias current depends on the register settings BIASC[0..9] and the coupling ratio (CR) between the laser bias current and the photodiode current.  $CR = I_{BIAS}/I_{PD}$ . If the photodiode anode is connected to the PD pin (PD pin is sinking current), set PDPOL = 1 (bit 0 of register 0) and if the photodiode cathode is connected to the PD pin (PD pin is sourcing current), set PDPOL = 0.

Three photodiode current ranges can be selected by means of the PDRNG[0..1] bits (register 0). The photodiode range should be chosen to keep the laser bias control DAC, BIASC[0..9], close to the center of its range. This keeps the laser bias current set point resolution high. For details regarding the bias current setting in open-loop as well as in closed-loop mode, see [Table 19](#).

The ONET1141L has the ability to source or sink the bias current. The default condition is for the BIAS pin to source the current (BIASPOL = 0). To act as a sink, set BIASPOL = 1 (bit 2 of register 1).

The bias current is monitored using a current mirror with a gain equal to 1/100. By connecting a resistor between MONB and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The bias current can also be monitored as a 10 bit unsigned digital word through the 2-wire interface by setting DMONB = 1 (bit 0 of register 10) and removing the resistor to ground.

## ANALOG REFERENCE AND TEMPERATURE SENSOR

The ONET1141L modulator driver is supplied by a single  $3.3V \pm 10\%$  supply voltage connected to the VCC and VCCO pins. This voltage is referred to ground (GND) and can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground. This resistor is used to generate a precise, zero-TC current which is required as a reference current for the on-chip DACs.

The ONET1141L provides an on-chip temperature sensor which can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

## POWER-ON RESET

The ONET1141L has power on reset circuitry which ensures that all registers are reset to zero during startup. After the power-on to initialize time ( $t_{INIT1}$ ), the internal registers are ready to be loaded. The part is ready to transmit data after the initialize to transmit time ( $t_{INIT2}$ ), assuming that the chip enable bit ENA is set to 1 and the disable pin DIS is low. The DIS pin has an internal 10k $\Omega$  pull up resistor so the pin must be pulled low to enable the outputs. The ONET1141L can be disabled using either the ENA control register bit or the disable pin DIS. In both cases the internal registers are not reset. After the disable pin DIS is set low and/or the enable bit ENA is set back to 1, the part returns to its prior output settings.

To reduce the disable time, only the output stage can be disabled by setting DISMODE = 1 (bit 1 of register 1).

## ANALOG TO DIGITAL CONVERTER

The ONET1141L has an internal 10 bit analog to digital converter (ADC) that converts the analog monitors for temperature, power supply voltage, bias current and photodiode current into a 10 bit unsigned digital word. The first 8 most significant bits (MSBs) are available in register 14 and the 2 least significant bits (LSBs) are available in register 15. Depending on the accuracy required, 8 bits or 10 bits can be read. However, due to the architecture of the 2-wire interface, in order to read the 2 registers, 2 separate read commands have to be sent.

The ADC is enabled by default so to monitor a particular parameter, select the parameter with ADCSEL[0..1] (bits 0 and 1 of register 13). [Table 1](#) shows the ADCSEL bits and the parameter that is monitored.



**Table 1. ADC Selection Bits and the Monitored Parameter**

| ADCSEL1 | ADCSEL0 | Monitored Parameter |
|---------|---------|---------------------|
| 0       | 0       | Temperature         |
| 0       | 1       | Supply voltage      |
| 1       | 0       | Photodiode current  |
| 1       | 1       | Bias current        |

To digitally monitor the photodiode current, ensure that DMONP = 1 (bit 1 of register 10) and that a resistor is not connected to the MONP pin. To digitally monitor the bias current, ensure that DMONB = 1 (bit 0 of register 10) and that a resistor is not connected to the MONB pin. If it is not desired to use the ADC to monitor the various parameters then the ADC can be disabled by setting ADCDIS = 1 (bit 7 of register 13) and OSCDIS = 1 (bit 6 of register 13).

The digital word read from the ADC can be converted to its analog equivalent through the following formulas:

**Temperature Without a Mid-Point Calibration**

$$\text{Temperature } (^{\circ}\text{C}) = (\text{ADCx} - 264) / 6 \quad (1)$$

**Temperature With a Mid-Point Calibration**

$$\text{Temperature } (^{\circ}\text{C}) = (\text{T\_cal} (^{\circ}\text{C}) + 273) \times (\text{ADCx} + 1362) / (\text{ADC\_cal} + 1362) - 273 \quad (2)$$

**Power Supply Voltage**

$$\text{Power supply voltage (V)} = 2.25 \times (\text{ADCx} + 1380) / 1409 \quad (3)$$

**Photodiode Current Monitor**

$$\text{IPD } (\mu\text{A}) = 1.3 \times \text{ADCx} \quad (4)$$

**Bias Current Monitor**

$$\text{Source mode: IBIAS (mA)} = 0.177 \times \text{ADCx}$$

$$\text{Sink mode: IBIAS (mA)} = 0.19 \times \text{ADCx} \quad (5)$$

Where:

ADCx = the decimal value read from the ADC

T\_cal = the calibration temperature

ADC\_cal = the decimal value read from the ADC at the calibration temperature

**2-WIRE INTERFACE AND CONTROL LOGIC**

The ONET1141L uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCK pins have internal 10kΩ pull ups to VCC. If a common interface is used to control multiple parts, the internal pull ups can be set to 40kΩ by setting TWITERM to 1 (bit 7 of register 1). This will also set the internal pullup on the DIS pin to 40 kΩ.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET1141L is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data write transmission is as follows:

1. START command
2. 7 bit slave address (0001000) followed by an eighth bit (value = 0) which is the data write bit (W).
3. 8 bit register address
4. 8 bit register data word
5. STOP command

The first 2 bits of the slave address can be changed to 1 by grounding the ADR0 and ADR1 pins.

Regarding timing, the ONET1141L is I<sup>2</sup>C compatible. The typical timing is shown in Figure 2 and complete data write and read transfers are shown in Figure 3. Parameters for Figure 2 are defined in Table 2.

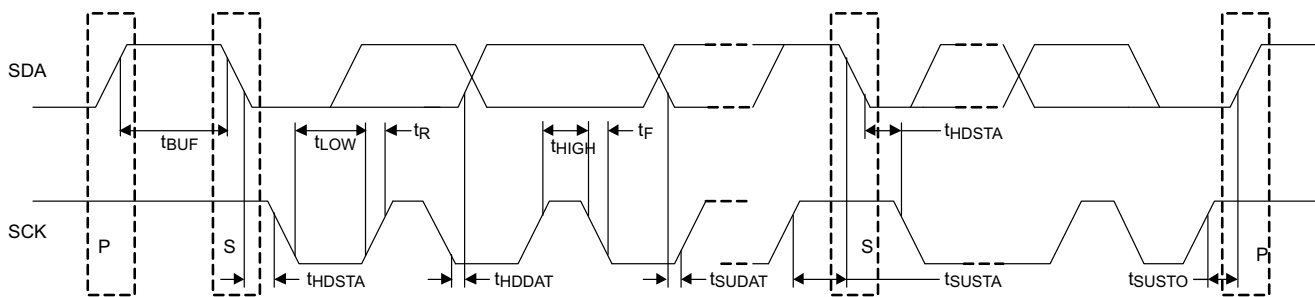
**Bus Idle:** Both SDA and SCK lines remain HIGH

**Start Data Transfer:** A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

**Data Transfer:** Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

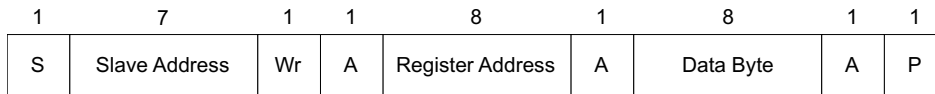


**Figure 2. I<sup>2</sup>C Timing Diagram**

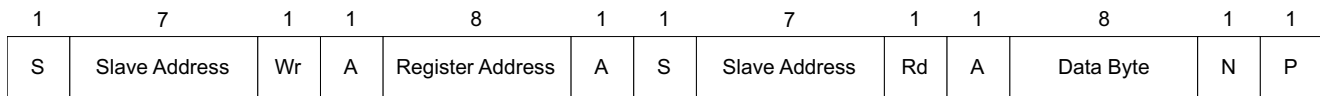
**Table 2. Timing Diagram Definitions**

| SYMBOL             | PARAMETER   | MIN | MAX | UNIT |
|--------------------|---|-----|-----|------|
| f <sub>SCK</sub>   | SCK clock frequency   |     | 400 | kHz  |
| t <sub>BUF</sub>   | Bus free time between STOP and START conditions   | 1.3 |     | μs   |
| t <sub>HDSTA</sub> | Hold time after repeated START condition. After this period, the first clock pulse is generated | 0.6 |     | μs   |
| t <sub>LOW</sub>   | Low period of the SCK clock   | 1.3 |     | μs   |
| t <sub>HIGH</sub>  | High period of the SCK clock  | 0.6 |     | μs   |
| t <sub>SUSTA</sub> | Setup time for a repeated START condition   | 0.6 |     | μs   |
| t <sub>HDDAT</sub> | Data HOLD time  | 0   |     | μs   |
| t <sub>SUDAT</sub> | Data setup time   | 100 |     | ns   |
| t <sub>R</sub>     | Rise time of both SDA and SCK signals   |     | 300 | ns   |
| t <sub>F</sub>     | Fall time of both SDA and SCK signals   |     | 300 | ns   |
| t <sub>SUSTO</sub> | Setup time for STOP condition   | 0.6 |     | μs   |

## Write Sequence



## Read Sequence



## Legend

|    |                           |
|----|---------------------------|
| S  | Start Condition           |
| Wr | Write Bit (bit value = 0) |
| Rd | Read Bit (bit value = 1)  |
| A  | Acknowledge               |
| N  | Not Acknowledge           |
| P  | Stop Condition            |

**Figure 3. Programming Sequence**
**REGISTER MAPPING**

The register mapping for register addresses 0 (0x00) through 15 (0x0F) are shown in [Table 3](#) through [Table 18](#). [Table 19](#) describes the circuit functionality based on the register settings.

**Table 3. Register 0 (0x00) Mapping – Control Settings**

| register address 0 (0x00) |        |        |       |       |       |       |       |
|---------------------------|--------|--------|-------|-------|-------|-------|-------|
| bit 7                     | bit 6  | bit 5  | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| ENA                       | PDRNG1 | PDRNG0 | OLENA | FLTEN | POL   | EQENA | PDPOL |

**Table 4. Register 1 (0x01) Mapping – Control Settings**

| register address 1 (0x01) |          |          |       |       |         |         |        |
|---------------------------|----------|----------|-------|-------|---------|---------|--------|
| bit 7                     | bit 6    | bit 5    | bit 4 | bit 3 | bit 2   | bit 1   | bit 0  |
| TWITERM                   | HIEFCENA | HIEQGENA | HCENA | OCDIS | BIASPOL | DISMODE | LOGENA |

**Table 5. Register 2 (0x02) Mapping – Modulation Current**

| register address 2 (0x02) |       |       |       |       |       |       |       |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7                     | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| –                         | –     | –     | –     | –     | –     | MODC1 | MODC0 |

**Table 6. Register 3 (0x03) Mapping – Modulation Current**

| register address 3 (0x03) |       |       |       |       |       |       |       |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7                     | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| MODC9                     | MODC8 | MODC7 | MODC6 | MODC5 | MODC4 | MODC3 | MODC2 |

**Table 7. Register 4 (0x04) Mapping – Bias Current**

| register address 4 (0x04) |       |       |       |       |       |        |        |
|---------------------------|-------|-------|-------|-------|-------|--------|--------|
| bit 7                     | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1  | bit 0  |
| –                         | –     | –     | –     | –     | –     | BIASC1 | BIASC0 |

**Table 8. Register 5 (0x05) Mapping – Bias Current**

| register address 5 (0x05) |        |        |        |        |        |        |        |
|---------------------------|--------|--------|--------|--------|--------|--------|--------|
| bit 7                     | bit 6  | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
| BIASC9                    | BIASC8 | BIASC7 | BIASC6 | BIASC5 | BIASC4 | BIASC3 | BIASC2 |

**Table 9. Register 6 (0x06) Mapping – Equalizer Adjust**

| register address 6 (0x06) |        |        |        |        |        |        |        |
|---------------------------|--------|--------|--------|--------|--------|--------|--------|
| bit 7                     | bit 6  | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
| EQADJ7                    | EQADJ6 | EQADJ5 | EQADJ4 | EQADJ3 | EQADJ2 | EQADJ1 | EQADJ0 |

**Table 10. Register 7 (0x07) Mapping – Cross Point Adjust**

| register address 7 (0x07) |        |        |        |        |        |        |        |
|---------------------------|--------|--------|--------|--------|--------|--------|--------|
| bit 7                     | bit 6  | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
| CPSGN                     | CPADJ6 | CPADJ5 | CPADJ4 | CPADJ3 | CPADJ2 | CPADJ1 | CPADJ0 |

**Table 11. Register 8 (0x08) Mapping – Cross Point Control Settings**

| register address 8 (0x08) |       |       |       |       |       |        |        |
|---------------------------|-------|-------|-------|-------|-------|--------|--------|
| bit 7                     | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1  | bit 0  |
| IDRV                      | –     | –     | CPREF | –     | CPENA | CPRNG1 | CPRNG0 |

**Table 12. Register 9 (0x09) Mapping – Limiter Bias Current Adjust**

| register address 9 (0x09) |       |       |       |        |       |       |       |
|---------------------------|-------|-------|-------|--------|-------|-------|-------|
| bit 7                     | bit 6 | bit 5 | bit 4 | bit 3  | bit 2 | bit 1 | bit 0 |
| LIMCSGN                   | LMC2  | LIMC1 | LIMC0 | EFCSGN | EFC2  | EFC1  | EFC0  |

**Table 13. Register 10 (0x0A) Mapping – Monitor Settings**

| register address 10 (0x0A) |       |       |       |       |         |       |       |
|----------------------------|-------|-------|-------|-------|---------|-------|-------|
| bit 7                      | bit 6 | bit 5 | bit 4 | bit 3 | bit 2   | bit 1 | bit 0 |
| –                          | –     | –     | –     | –     | MONPFLT | DMONP | DMONB |

**Table 14. Register 11 (0x0B) Mapping – Bias Monitor Fault Settings**

| register address 11 (0x0B) |       |       |       |       |       |       |       |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7                      | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| BMF7                       | BMF6  | BMF5  | BMF4  | BMF3  | BMF2  | BMF1  | BMF0  |

**Table 15. Register 12 (0x0C) Mapping – Power Monitor Fault Settings**

| register address 12 (0x0C) |       |       |       |       |       |       |       |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7                      | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| PMF7                       | PMF6  | PMF5  | PMF4  | PMF3  | PMF2  | PMF1  | PMF0  |

**Table 16. Register 13 (0x0D) Mapping – ADC Settings**

| register address 13 (0x0D) |        |       |       |       |       |         |         |
|----------------------------|--------|-------|-------|-------|-------|---------|---------|
| bit 7                      | bit 6  | bit 5 | bit 4 | bit 3 | bit 2 | bit 1   | bit 0   |
| ADCDIS                     | OSCDIS | –     | –     | –     | –     | ADCSEL1 | ADCSEL0 |

**Table 17. Register 14 (0x0E) Mapping – ADC Output (Read Only)**

| register address 14 (0x0E) |       |       |       |       |       |       |       |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7                      | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| ADC9                       | ADC8  | ADC7  | ADC6  | ADC5  | ADC4  | ADC3  | ADC2  |

**Table 18. Register 15 (0x0F) Mapping – ADC Output (Read Only)**

| register address 15 (0x0F) |       |       |       |       |       |       |       |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7                      | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| –                          | –     | –     | –     | –     | –     | ADC1  | ADC0  |

**Table 19. Register Functionality**

| REGISTER | BIT    | SYMBOL           | FUNCTION  |
|----------|--------|------------------|---|
| 0        | 7      | ENA              | <b>Enable chip bit</b><br>1 = Chip enabled. Can be toggled low to reset a fault condition.<br>0 = Chip disabled   |
|          | 6<br>5 | PDRNG1<br>PDRNG0 | <b>Photodiode current range bits</b><br>1X: up to 3080µA / 3µA resolution<br>01: up to 1540µA / 1.5µA resolution<br>00: up to 770µA / 0.75µA resolution |
|          | 4      | OLENA            | <b>Open loop enable bit</b><br>1 = Open loop bias current control,<br>0 = Closed loop bias current control  |
|          | 3      | FLTEN            | <b>Fault detection enable bit</b><br>1 = Fault detection on<br>0 = Fault detection off  |
|          | 2      | POL              | <b>Output polarity switch bit</b><br>1: pin 22 = OUT- and pin 21= OUT+<br>0: pin 22 = OUT+ and pin 21 = OUT-  |
|          | 1      | EQENA            | <b>Equalizer enable bit</b><br>1 = Equalizer is enabled<br>0 = Equalizer is disabled and bypassed   |
|          | 0      | PDPOL            | <b>Photodiode polarity bit</b><br>1 = Photodiode cathode connected to V <sub>CC</sub><br>0 = Photodiode anode connected to GND                          |

**Table 19. Register Functionality (continued)**

| REGISTER | BIT | SYMBOL   | FUNCTION   |
|----------|-----|----------|--|
| 1        | 7   | TWITERM  | <b>Two wire interface input termination select bit</b><br>1 = 40kΩ selected<br>0 = 10kΩ selected   |
|          | 6   | HIEFCENA | <b>High emitter follower drive current enable bit</b><br>1 = High current enabled<br>0 = High current disabled   |
|          | 5   | HIEQGENA | <b>High gain enable for EQ stage (with EQENA = 1)</b><br>1 = High gain enabled<br>0 = High gain disabled   |
|          | 4   | HCENA    | <b>High modulation current enable bit</b><br>1 = High modulation current enabled<br>0 = High modulation current disabled   |
|          | 3   | OCDIS    | <b>Offset cancellation disable bit</b><br>1 = DC offset cancellation is disabled<br>0 = DC offset cancellation is enabled  |
|          | 2   | BIASPOL  | <b>Bias current polarity bit</b><br>1 = Bias pin sinks current<br>0 = Bias pin sources current   |
|          | 1   | DISMODE  | <b>Disable mode setting bit</b><br>1 = Only the output stage is disabled (fast disable mode)<br>0 = Major parts of the signal path are disabled  |
|          | 0   | LOGENA   | <b>Low gain enable for input amplifier (with EQENA = 0)</b><br>1 = Low gain enabled<br>0 = Default gain  |
| 3        | 7   | MODC9    | <b>Modulation current setting: sets the output voltage</b><br><br>Output Voltage: 2.3Vpp / 2.5mV steps   |
|          | 6   | MODC8    |  |
|          | 5   | MODC7    |  |
|          | 4   | MODC6    |  |
|          | 3   | MODC5    |  |
|          | 2   | MODC4    |  |
|          | 1   | MODC3    |  |
|          | 0   | MODC2    |  |
| 2        | 1   | MODC1    |  |
|          | 0   | MODC0    |  |
| 5        | 7   | BIASC9   | <b>Bias current settings</b><br><b>Closed loop (APC):</b><br>Coupling ratio $CR = I_{BIAS} / I_{PD}$ , $BIASC = 0..1023$ , $I_{BIAS} \leq 150mA$ :<br><br>PDRNG = 00 (see above); $I_{BIAS} = 0.75\mu A \times CR \times BIASC$<br>PDRNG = 01 (see above); $I_{BIAS} = 1.5\mu A \times CR \times BIASC$<br>PDRNG = 1X (see above); $I_{BIAS} = 3\mu A \times CR \times BIASC$<br><br><b>Open loop:</b> |
|          | 6   | BIASC8   |  |
|          | 5   | BIASC7   |  |
|          | 4   | BIASC6   |  |
|          | 3   | BIASC5   |  |
|          | 2   | BIASC4   |  |
|          | 1   | BIASC3   |  |
|          | 0   | BIASC2   |  |
| 4        | 1   | BIASC1   | $I_{BIAS} \sim 150\mu A \times BIASC$ in source mode<br>$I_{BIAS} \sim 100\mu A \times BIASC$ in sink mode   |
|          | 0   | BIASC0   |  |

**Table 19. Register Functionality (continued)**

| REGISTER | BIT | SYMBOL         | FUNCTION   |
|----------|-----|----------------|--|
| 6        | 7   | EQADJ7         | <b>Equalizer adjustment setting</b>  |
|          | 6   | EQADJ6         |  |
|          | 5   | EQADJ5         |  |
|          | 4   | EQADJ4         |  |
|          | 3   | EQADJ3         |  |
|          | 2   | EQADJ2         |  |
|          | 1   | EQADJ1         |  |
|          | 0   | EQADJ0         |  |
| 7        | 7   | CPSGN          | Eye cross-point adjustment setting   |
|          | 6   | CPADJ6         | CPSGN = 1 (positive shift)   |
|          | 5   | CPADJ5         | Maximum shift for 1111111  |
|          | 4   | CPADJ4         | Minimum shift for 0000000  |
|          | 3   | CPADJ3         | CPSGN = 0 (negative shift)   |
|          | 2   | CPADJ2         | Maximum shift for 1111111  |
|          | 1   | CPADJ1         | Minimum shift for 0000000  |
|          | 0   | CPADJ0         |  |
| 8        | 7   | IDRV           | <b>Output Driver Tail Current Bit</b><br>1 = Output driver tail current is increased<br>0 = Output driver tail current is set to default   |
|          | 6   | -              |  |
|          | 5   | -              |  |
|          | 4   | CPREF          | <b>Cross point temperature coefficient selection bit</b><br>1 = Reverses the behavior<br>and EQENA = 1: temperature coefficient disabled<br>and EQENA = 0: temperature coefficient enabled<br>0 = Default condition<br>and EQENA = 1: temperature coefficient enabled<br>and EQENA = 0: temperature coefficient disabled |
|          | 3   | -              |  |
|          | 2   | CPENA          | <b>Cross point adjustment enable bit</b><br>1 = Cross point adjustment is enabled<br>0 = Cross point adjustment is disabled  |
|          | 1   | CPRNG1         | <b>Cross point adjustment range bits</b><br>Minimum adjustment range for 00<br>Maximum adjustment range for 11   |
|          | 0   | CPRNG0         |  |
| 9        | 7   | <b>LIMCSGN</b> | Limiter bias current sign bit<br>1 = Decrease limiter bias current<br>0 = Increase limiter bias current  |
|          | 6   | LIMC2          | <b>Limiter bias current selection bits</b><br>000 = No change<br>111 = Maximum current change  |
|          | 5   | LIMC1          |  |
|          | 4   | LIMC0          |  |
|          | 3   | EFCSGN         | <b>Emitter follower sign bit</b><br>1 = Decrease emitter follower current<br>0 = Increase emitter follower current   |
|          | 2   | EFC2           | Emitter follower current selection bits<br>000 = No change<br>111 = Maximum current change   |
|          | 1   | EFC1           |  |
|          | 0   | EFC0           |  |

**Table 19. Register Functionality (continued)**

| REGISTER | BIT | SYMBOL  | FUNCTION  |
|----------|-----|---------|---|
| 10       | 7   | -       |   |
|          | 6   | -       |   |
|          | 5   | -       |   |
|          | 4   | -       |   |
|          | 3   | -       |   |
|          | 2   | MONPFLT | <b>Analog photodiode current monitor fault trigger bit</b><br>1 = Fault trigger on MONP pin is enabled<br>0 = Fault trigger on MONP pin is disabled   |
|          | 1   | DMONP   | <b>Digital photodiode current monitor selection bit (MONP)</b><br>1 = Digital photodiode monitor is active (external resistor must not be installed)<br>0 = Analog photodiode monitor is active (external resistor is required) |
|          | 0   | DMONB   | <b>Digital bias current monitor selection bit (MONB)</b><br>1 = Digital bias current monitor is active (external resistor must not be installed)<br>0 = Analog bias current monitor is active (external resistor is required)   |
| 11       | 7   | BMF7    | <b>Bias current monitor fault threshold</b><br>With DMONB = 1<br>Register sets the value of the bias current that will trigger a fault.<br>The external resistor on the MONB pin must be removed to use this feature.           |
|          | 6   | BMF6    |   |
|          | 5   | BMF5    |   |
|          | 4   | BMF4    |   |
|          | 3   | BMF3    |   |
|          | 2   | BMF2    |   |
|          | 1   | BMF1    |   |
|          | 0   | BMF0    |   |
| 12       | 7   | PMF7    | <b>Power monitor fault threshold</b><br>With DMONP = 1<br>Register sets the value of the photodiode current that will trigger a fault<br>The external resistor on the MONP pin must be removed to use this feature.             |
|          | 6   | PMF6    |   |
|          | 5   | PMF5    |   |
|          | 4   | PMF4    |   |
|          | 3   | PMF3    |   |
|          | 2   | PMF2    |   |
|          | 1   | PMF1    |   |
|          | 0   | PMF0    |   |
| 13       | 7   | ADCDIS  | <b>ADC disable bit</b><br>1 = ADC disabled<br>0 = ADC enabled   |
|          | 6   | OSCDIS  | <b>ADC oscillator bit</b><br>1 = Oscillator disabled<br>0 = Oscillator enabled  |
|          | 5   |         |   |
|          | 4   |         |   |
|          | 3   |         |   |
|          | 2   |         |   |
|          | 1   | ADCSEL1 | <b>ADC input selection bits</b><br>00 selects the temperature sensor<br>01 selects the power supply monitor<br>10 selects MONP<br>11 selects MONB   |
|          | 0   | ADCSEL0 |   |



**Table 19. Register Functionality (continued)**

| REGISTER | BIT | SYMBOL     | FUNCTION   |
|----------|-----|------------|--|
| 14       | 7   | ADC9 (MSB) | Digital representation of the ADC input source (read only) |
|          | 6   | ADC8       |  |
|          | 5   | ADC7       |  |
|          | 4   | ADC6       |  |
|          | 3   | ADC5       |  |
|          | 2   | ADC4       |  |
|          | 1   | ADC3       |  |
|          | 0   | ADC2       |  |
| 15       | 7   | -          |  |
|          | 6   | -          |  |
|          | 5   | -          |  |
|          | 4   | -          |  |
|          | 3   | -          |  |
|          | 2   | -          |  |
|          | 1   | ADC1       |  |
|          | 0   | ADC0 (LSB) |  |

## LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET1141L provides built in laser safety features. The following fault conditions are detected:

1. Voltage at MONB exceeds the voltage at RZTC (1.16V) or, alternately, if DMONB = 1 and the bias current exceeds the bias current monitor fault threshold set by BMF[0..7] (register 11). When using the digital monitor, the resistor to ground must be removed.
2. Voltage at MONP exceeds the voltage at RZTC (1.16V) and the analog photodiode current monitor fault trigger bit, MONPFLT (bit 2 of register 10), is set to 1. Alternately, a fault can be triggered if DMONP = 1 and the photodiode current exceeds the photodiode current monitor fault threshold set by PMF[0..7] (register 12). When using the digital monitor, the resistor to ground must be removed.
3. Photodiode current exceeds 150% of its set value,
4. Bias control DAC drops in value by more than 50% in one step.

If one or more fault conditions occur and the fault enable bit FLTEN is set to 1, the ONET1141L responds by:

1. Setting the bias current to zero.
2. Setting the modulation current to zero.
3. Asserting and latching the FLT pin.

Fault recovery is performed by the following procedure:

1. The disable pin DIS and/or the internal enable control bit ENA are toggled for at least the fault latch reset time.
2. The FLT pin de-asserts while the disable pin DIS is asserted or the enable bit ENA is de-asserted.
3. If the fault condition is no longer present, the part will return to normal operation with its prior output settings after the disable negate time.
4. If the fault condition is still present, FLT re-asserts once DIS is set to a low level and the part will not return to normal operation.

**TYPICAL CHARACTERISTICS**

Typical operating condition is at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $I_{BIASC} = 80mA$ ,  $V_{OUT} = 2V_{PP}$ ,  $V_{IN} = 400mV_{pp}$  (unless otherwise noted).

**DETERMINISTIC JITTER  
vs  
MODULATION CURRENT**

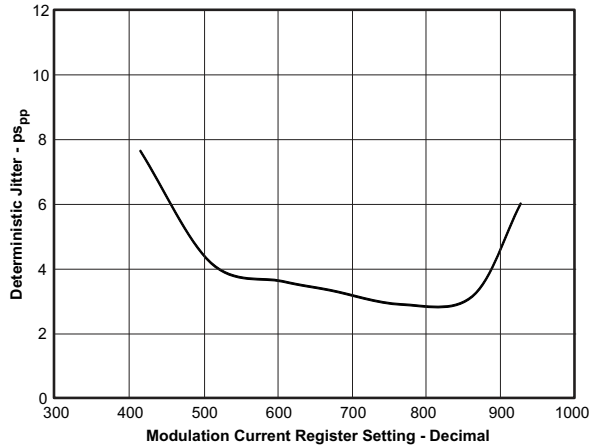


Figure 4.

**DETERMINISTIC JITTER  
vs  
TEMPERATURE**

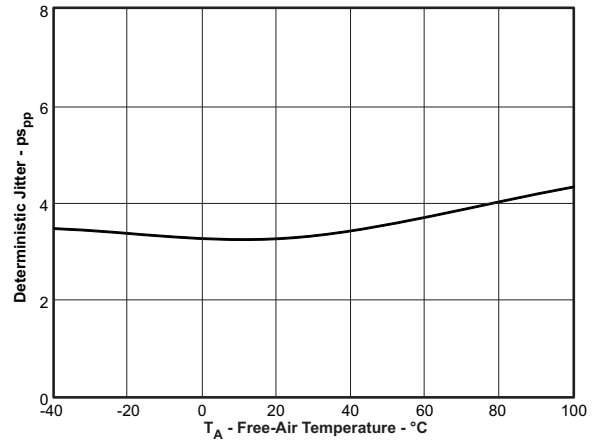


Figure 5.

**RANDOM JITTER  
vs  
MODULATION CURRENT**

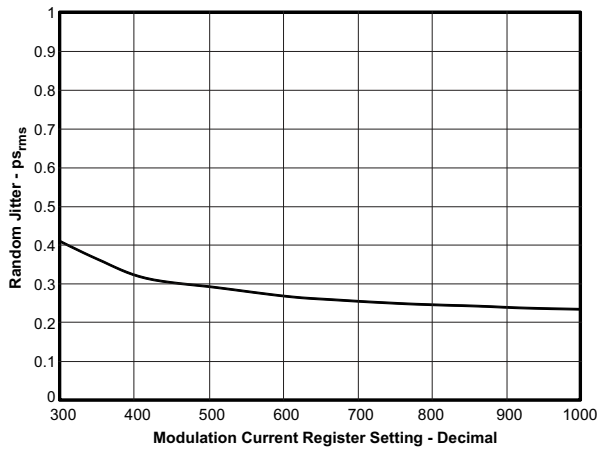


Figure 6.

**RANDOM JITTER  
vs  
TEMPERATURE**

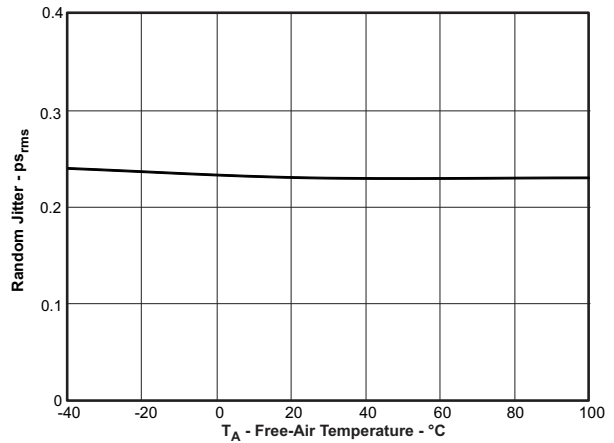
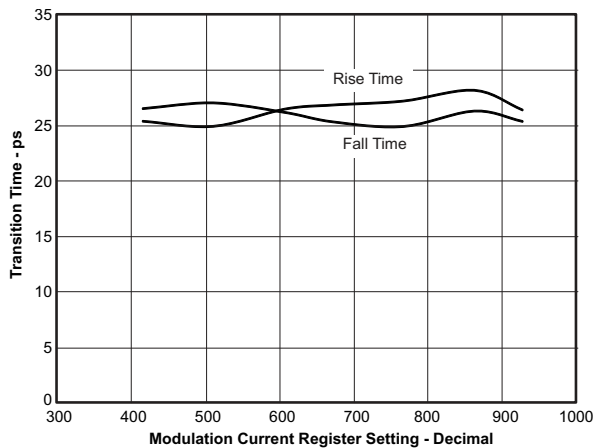


Figure 7.

**TYPICAL CHARACTERISTICS (continued)**

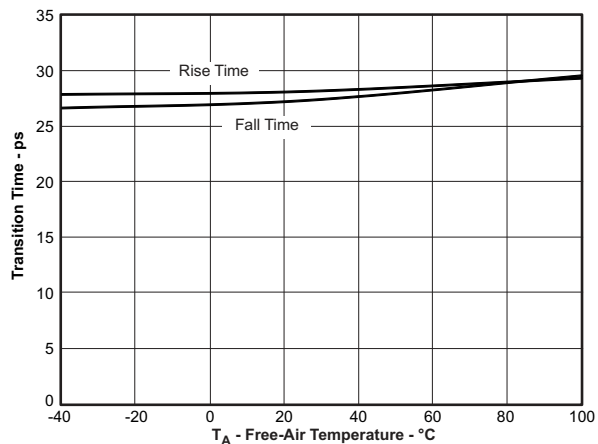
Typical operating condition is at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $I_{BIASC} = 80mA$ ,  $V_{OUT} = 2V_{PP}$ ,  $V_{IN} = 400mV_{pp}$  (unless otherwise noted).

**RISE-TIME AND FALL-TIME  
vs  
MODULATION CURRENT**



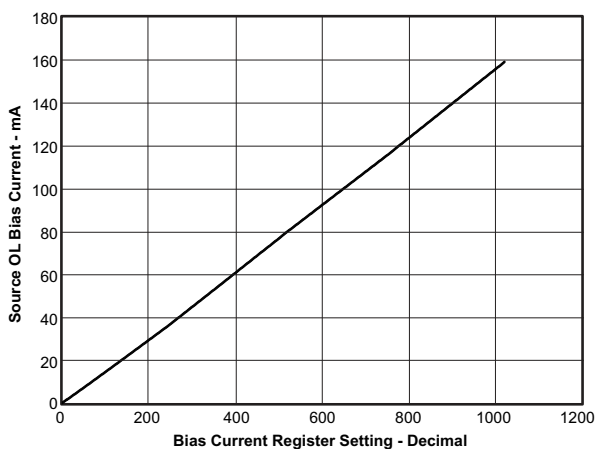
**Figure 8.**

**RISE-TIME AND FALL-TIME  
vs  
TEMPERATURE**



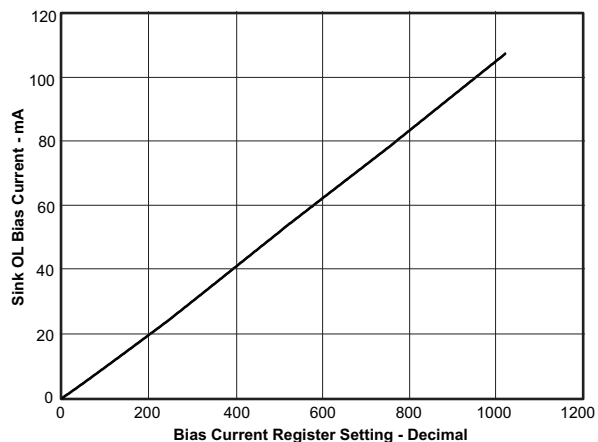
**Figure 9.**

**BIAS CURRENT IN OPEN LOOP MODE  
vs  
BIAS CURRENT REGISTER SETTING**



**Figure 10.**

**BIAS CURRENT IN OPEN LOOP MODE  
vs  
BIAS CURRENT REGISTER SETTING**

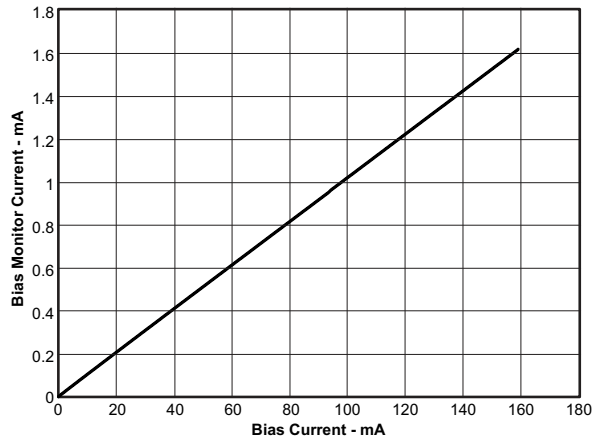


**Figure 11.**

**TYPICAL CHARACTERISTICS (continued)**

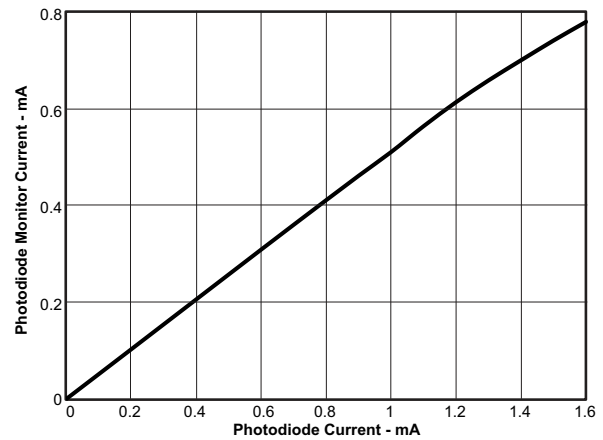
Typical operating condition is at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $I_{BIASC} = 80mA$ ,  $V_{OUT} = 2V_{PP}$ ,  $V_{IN} = 400mV_{pp}$  (unless otherwise noted).

**BIAS MONITOR CURRENT  
vs  
BIAS CURRENT**



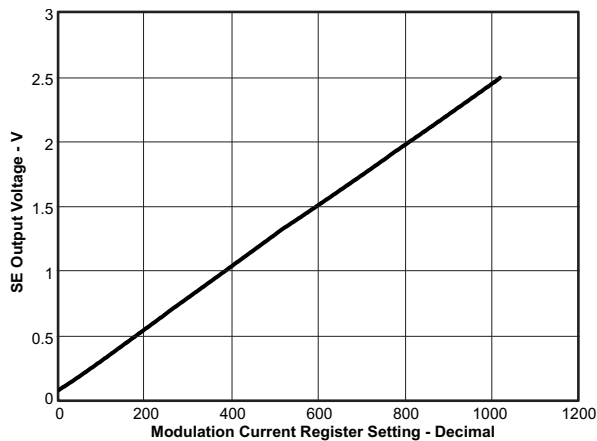
**Figure 12.**

**PHOTODIODE MONITOR CURRENT  
vs  
PHOTODIODE CURRENT**



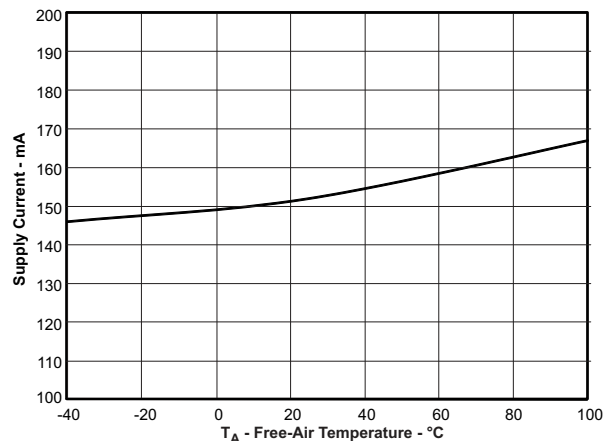
**Figure 13.**

**OUTPUT VOLTAGE  
vs  
MODC REGISTER SETTING**



**Figure 14.**

**SUPPLY CURRENT  
vs  
TEMPERATURE**



**Figure 15.**

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $I_{BIASC} = 80mA$ ,  $V_{OUT} = 2V_{PP}$ ,  $V_{IN} = 400mV_{pp}$  (unless otherwise noted).

**EYE-DIAGRAM AT 10.31GBPS**  
 $V_{OUT}=2V_{PP}$ , EQ Set to 00

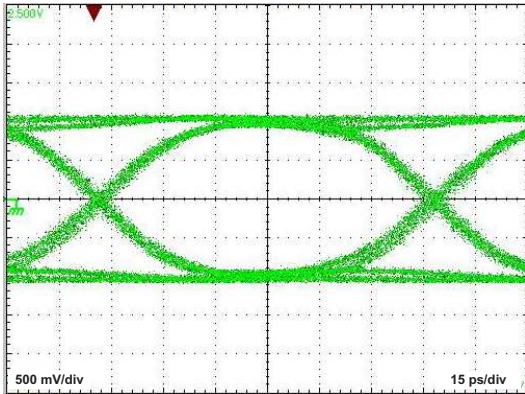


Figure 16.

**EYE-DIAGRAM AT 11.3GBPS**  
 $V_{OUT}=2V_{PP}$ , EQ Set to 00, 50% Cross Point

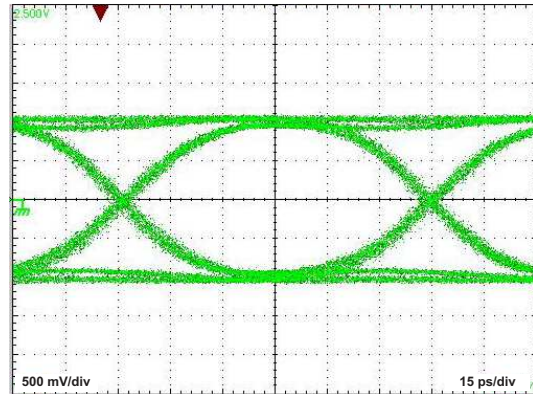


Figure 17.

**EYE-DIAGRAM AT 11.3GBPS**  
 $V_{OUT}=2V_{PP}$ , EQ Set to 00, 30% Cross Point

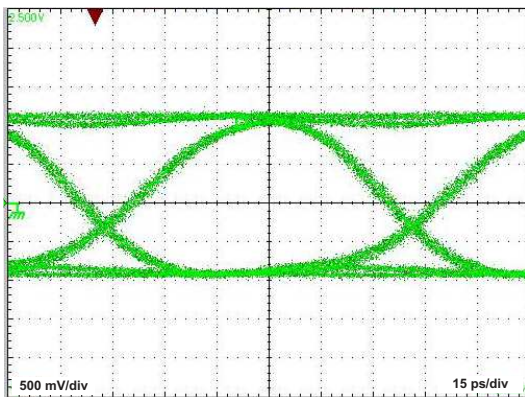


Figure 18.

**EYE-DIAGRAM AT 11.3GBPS**  
 $V_{OUT}=2V_{PP}$ , EQ Set to 00, 70% Cross Point

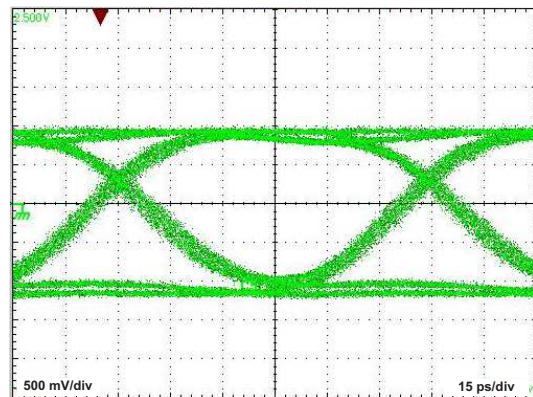


Figure 19.

**EYE-DIAGRAM AT 11.3GBPS**  
 $V_{OUT}=2V_{PP}$ , EQ Set to 00,  
6" OF FR4 AT INPUTS

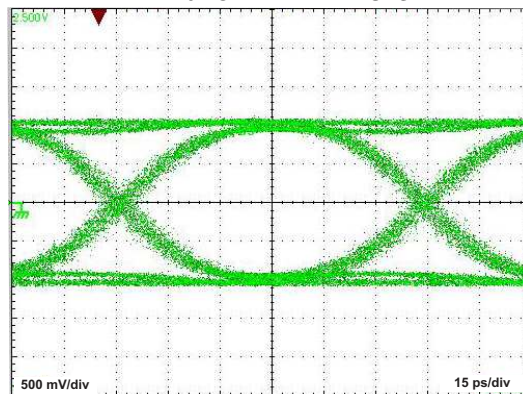


Figure 20.

## APPLICATION INFORMATION

Figure 21 and Figure 22 show typical application circuits using the ONET1141L. The modulator must be AC coupled to the driver for proper operation. The laser driver is controlled via the 2-wire interface SDA/SCK by a microcontroller. In a typical application, the FLT, MONB and MONP outputs are also connected to the microcontroller for transceiver management purposes.

The component values in Figure 21 and Figure 22 are typical examples and may be varied according to the intended application.

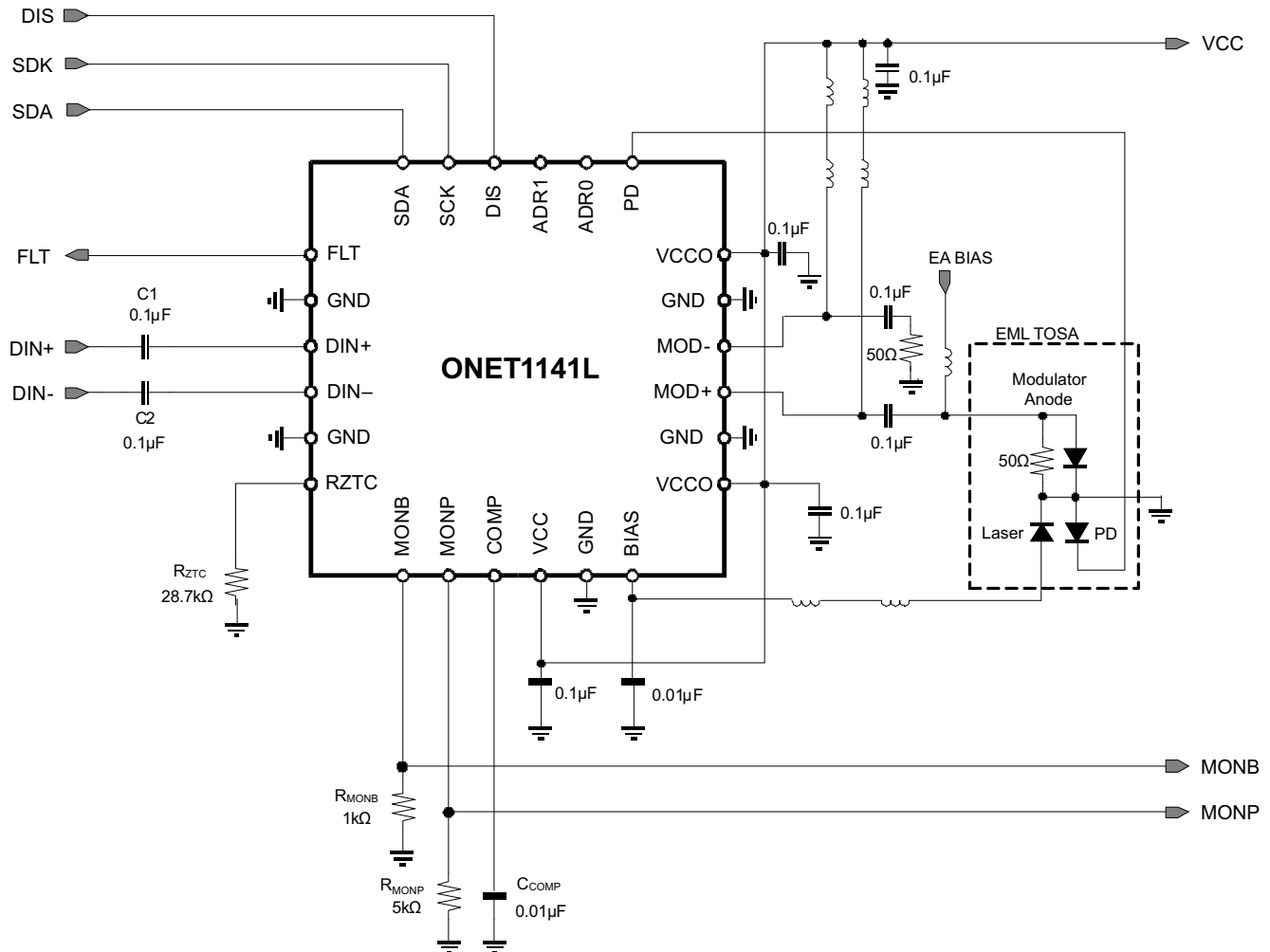


Figure 21. AC Coupled Drive with PD Monitor Cathode Available

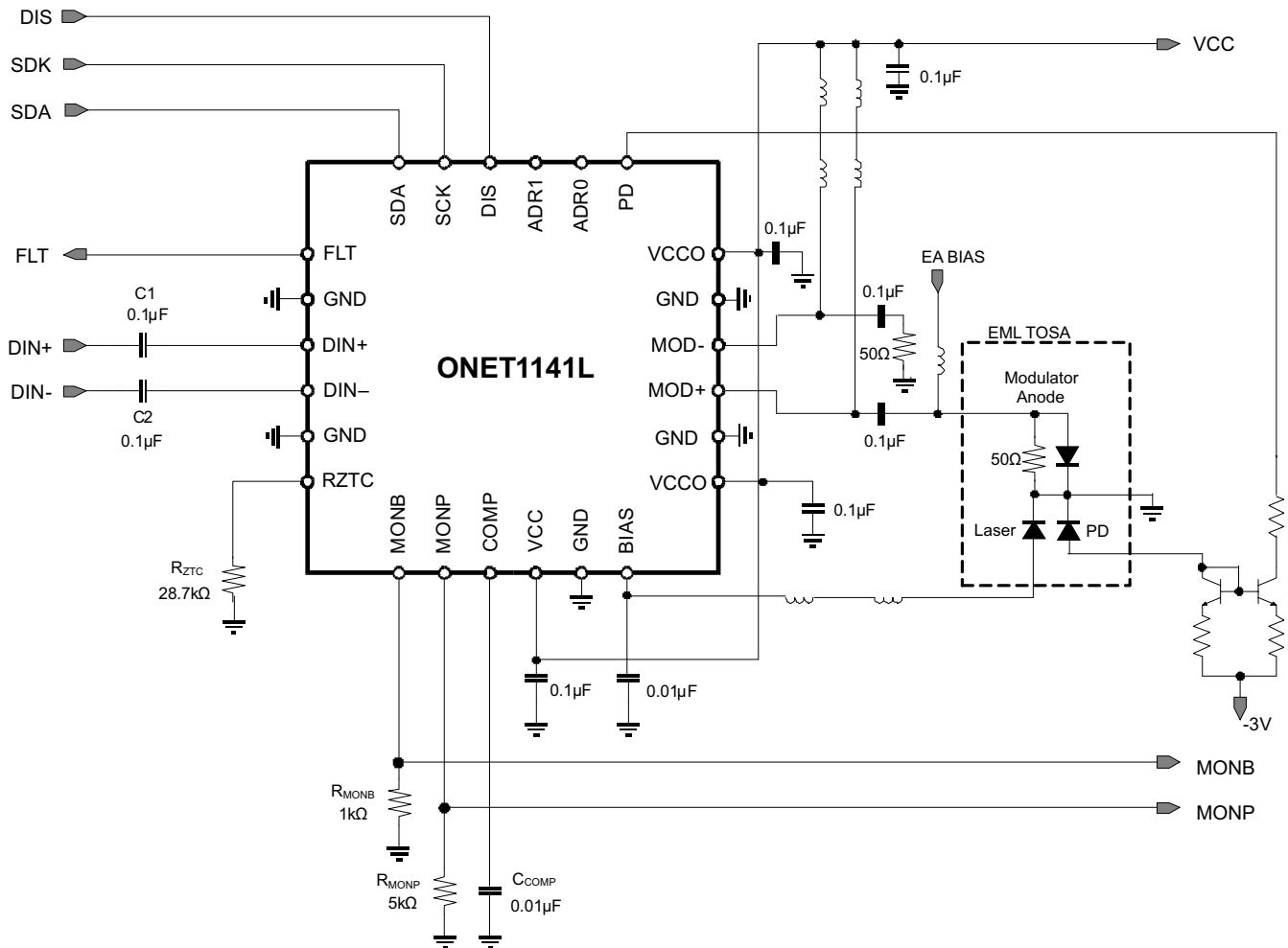




Figure 22. AC Coupled Drive with PD Monitor Anode Available

### Layout Guidelines

For optimum performance, use 50Ω transmission lines (100Ω differential) for connecting the signal source to the DIN+ and DIN- pins and 50Ω transmission lines (100Ω differential) for connecting the modulation current outputs, MOD+ and MOD-, to the laser. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| ONET1141LRGER    | ACTIVE        | VQFN         | RGE             | 24   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 100   | ONET<br>1141L           |  |
| ONET1141LRGET    | ACTIVE        | VQFN         | RGE             | 24   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 100   | ONET<br>1141L           |  |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ONET1141LRGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.3     | 4.3     | 1.5     | 8.0     | 12.0   | Q2            |
| ONET1141LRGET | VQFN         | RGE             | 24   | 250  | 330.0              | 12.4               | 4.3     | 4.3     | 1.5     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

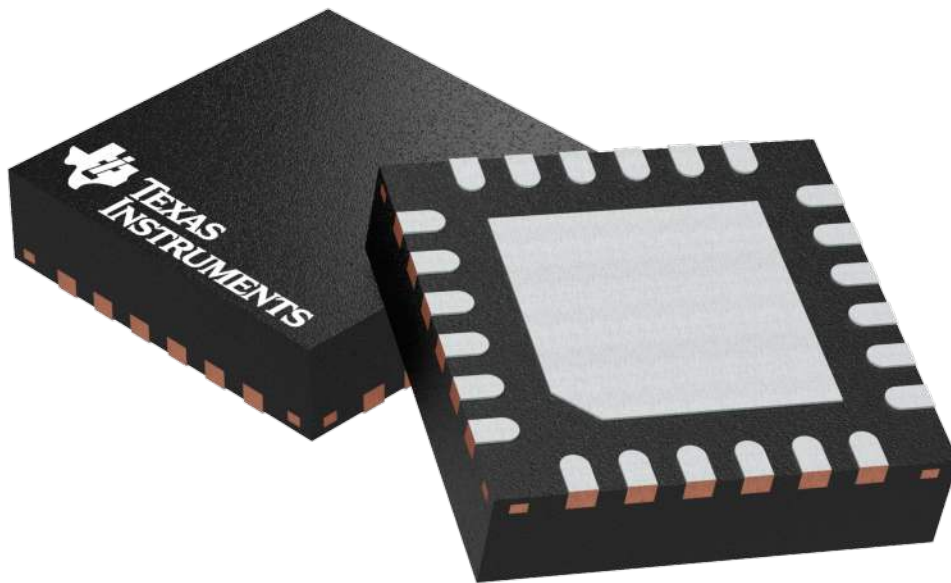
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ONET1141LRGER | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 38.0        |
| ONET1141LRGET | VQFN         | RGE             | 24   | 250  | 367.0       | 367.0      | 38.0        |

**RGE 24**

**GENERIC PACKAGE VIEW**

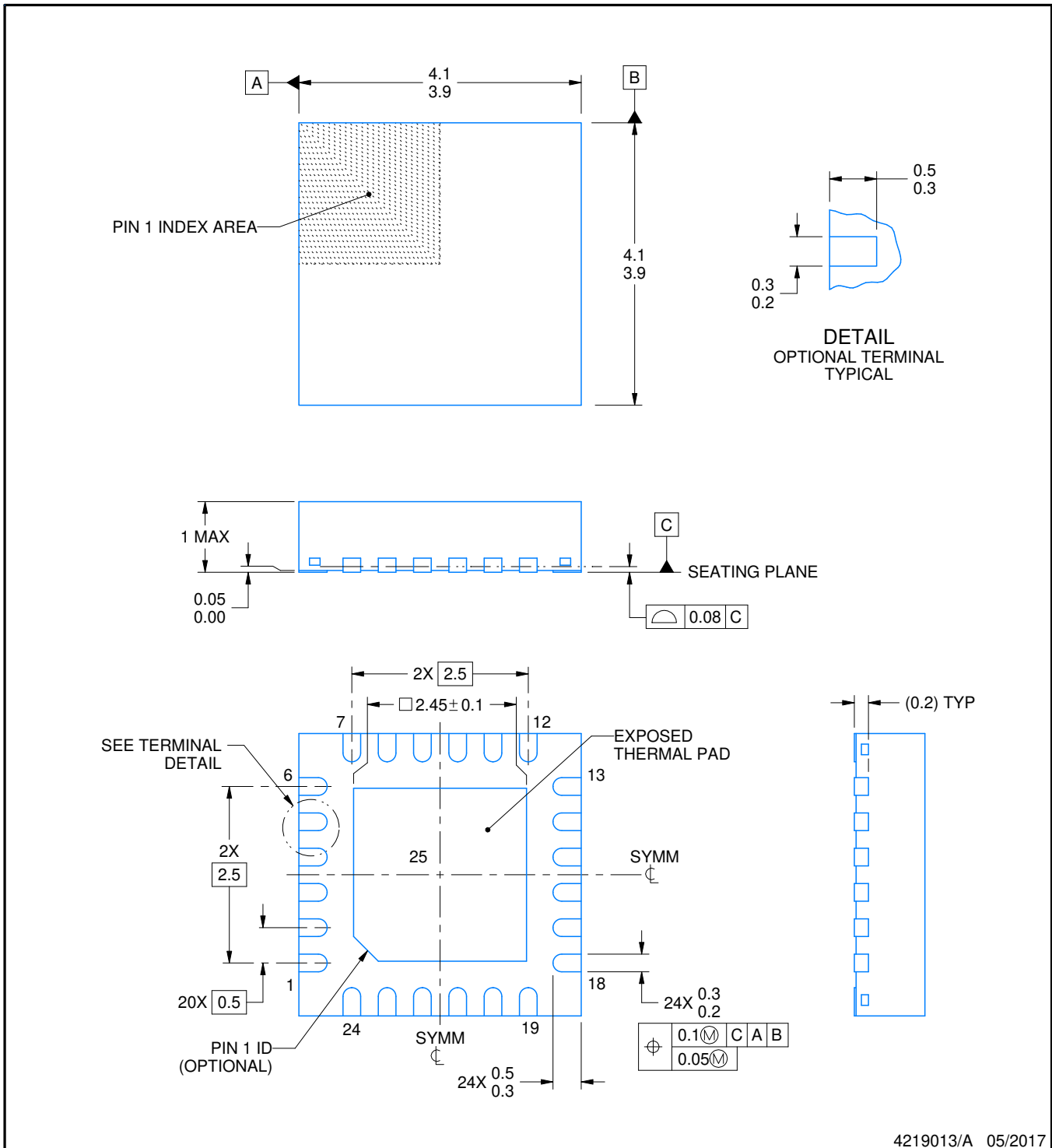
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

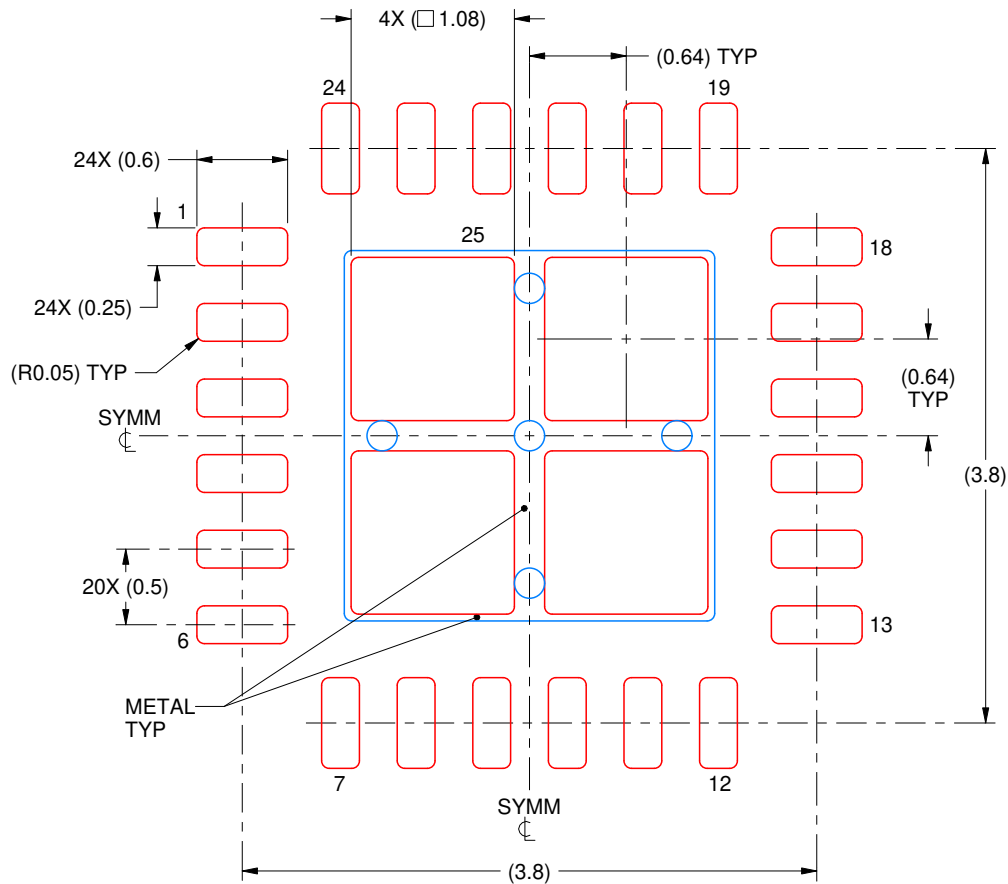


# EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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