TPS562231 4.5-V to 17-V Input, 2-A Synchronous Step-Down Buck Converter in SOT563

1 Features

- 2-A converter integrated 95-mΩ and 55-mΩ FETs
- D-CAP3™ Mode Control with fast transient response
- Input voltage range: 4.5 V to 17 V
- Output voltage range: 0.6 V to 7 V
- Pulse skip mode
- 850-kHz switching frequency
- Low shutdown current less than 2 µA (typical)
- 2% feedback voltage accuracy (25ºC)
- Startup from pre-biased output voltage
- Cycle-by-cycle over current limit
- Hiccup-mode over current protection
- Non-latch UVP and TSD protections
- 6-pin SOT563 package
- Precision enable
- Pin-to-pin compatible with TPS563231

2 Applications

- Standard 12-V rail supplies
- Digital TV power supply
- Embedded systems
- Networking home terminal
- Digital set top box (STB)
- Surveillance
- E-Meter

3 Description

The TPS562231 is a simple, easy-to-use, 2-A synchronous step-down converter in SOT563 package.

The device is optimized to operate with minimum external component counts, and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP3 mode control providing a fast transient response and supporting both low-equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

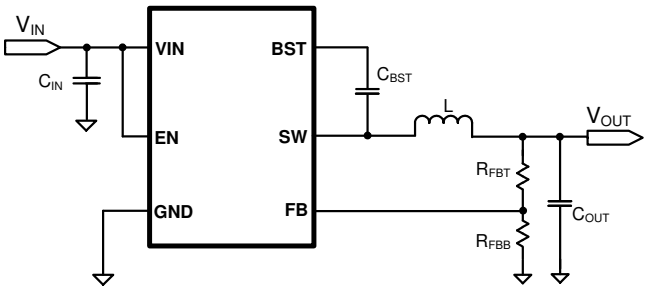
During light load operation, TPS562231 operates in pulse skip mode (PSM), which maintains high efficiency. The TPS562231 is available in a 6-pin 1.6-mm × 1.6-mm SOT563 (DRL) package, and specified from a –40°C to 125°C junction temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS562231	DRL (6)	1.60 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



TPS562231 Efficiency

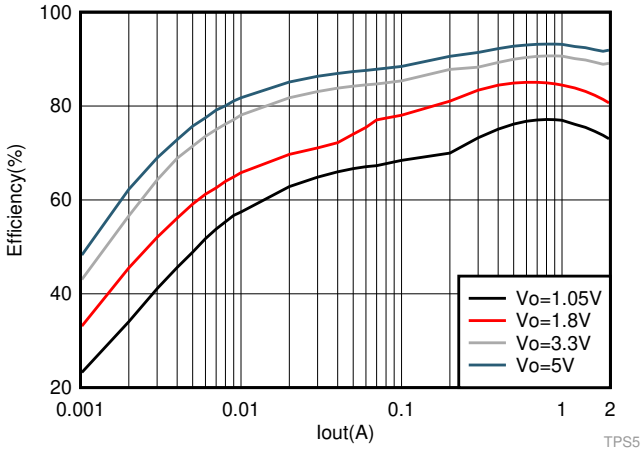


Table of Contents

4 Revision History

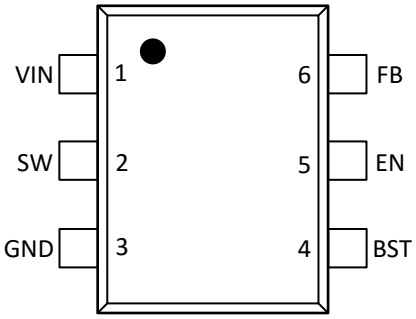
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B	Page
• Changed FB I/O Type from 'O' to 'I'	4

Changes from Original (February 2019) to Revision A	Page
• Changed marketing status from Advance Information to initial release.	1

5 Pin Configuration and Functions

DRL Package
6-Pin SOT563
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between BST and SW pins.
EN	5	I	Enable input control. High = On, Low = Off. Can be connected to VIN. Do not float. Adjust the input undervoltage lockout with EN resistor divider.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
GND	3	—	Power ground terminals, connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. Path to C_{IN} must as short as possible.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	1	I	Input voltage supply pin. The drain terminal of high-side power NFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	19	V
	BST	–0.3	24.5	V
	BST (10 ns transient)	–0.3	26.5	V
	BST to SW	–0.3	5.5	V
	FB	–0.3	5.5	V
	EN	-0.3	VIN + 0.3	
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	4.5	17	V
	BST	–0.1	22	V
	BST to SW	–0.1	5	
	EN	–0.1	VIN	
	FB	–0.1	4.5	
	SW	–1.8	17	
Operating junction temperature	T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS562231 DRL 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	135.8	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	45.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	23.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
I_{VIN}	Operating – non-switching supply current	V_{EN} = 5 V, V_{FB} = 0.7 V		220	300	µA
I_{VINSDN}	Shutdown supply current	V_{EN} = 0 V		2	12	µA
V_{IN_UVLO}	Undervoltage lockout thresholds	Rising threshold		4.0	4.3	V
		Falling threshold	3.3	3.6		
		Hysteresis		0.4		
ENABLE (EN PIN)						
V_{ENH}	EN high-level input voltage		1.1	1.24	1.42	V
V_{ENL}	EN low-level input voltage		1	1.13	1.3	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		1000		kΩ
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	V_{IN} = 4.5 V to 17 V, T_J = 25 °C	588	600	612	mV
		V_{IN} = 4.5 V to 17 V, T_J = –40°C to 125°C		600		mV
I_{FB}	V_{FB} input current	V_{FB} = 0.6 V		0	±100	nA
MOSFET						
R_{DSON_H}	High-side switch resistance	T_J = 25°C, V_{BST} – V_{SW} = 5.5 V		95		mΩ
R_{DSON_L}	Low-side switch resistance	T_J = 25°C		55		mΩ
CURRENT LIMIT						
I_{OC_LS}	Low side FET source current limit		2.3	2.8	3.3	A
I_{ZC}	Zero cross current detection	TPS562231		0		A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		160		°C
		Hysteresis		25		
ON-TIME TIMER CONTROL						
$t_{ON(MIN)}$	Minimum on time(1)			80		ns
$t_{OFF(MIN)}$	Minimum off time(1)	V_{FB} = 0.5 V		250		ns
SOFT START						
Tss	Soft-start time	Internal soft-start time		1.5		ms
FREQUENCY						
F_{sw}	Switching frequency	V_{IN} = 12 V, V_{OUT} = 3.3 V, CCM mode		850		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{UVP}	Output UVP falling threshold	Hiccup detect		65		%
T_{HICCUP_WAIT}	UVP propagation delay			0.6		ms
T_{HICCUP_RE}	Hiccup time before restart			24		ms

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

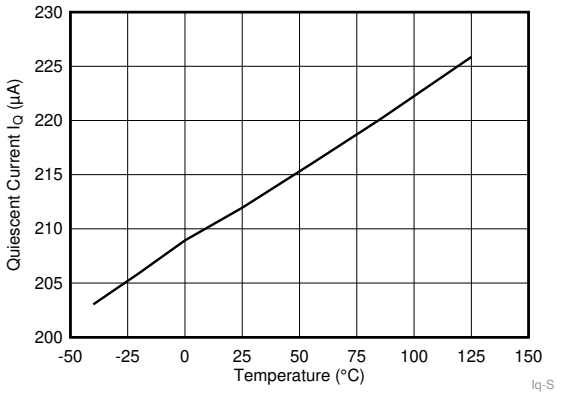


Figure 1. I_Q vs Junction Temperature

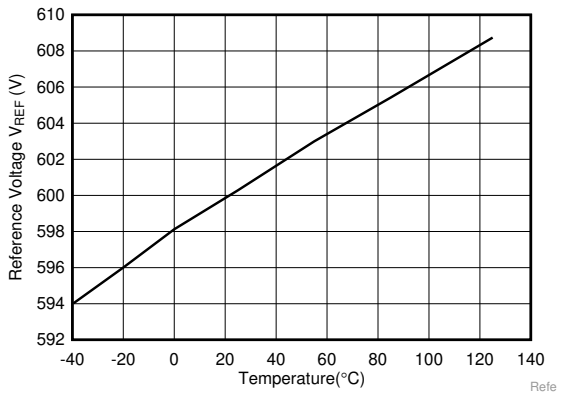


Figure 2. V_{REF} Voltage vs Junction Temperature

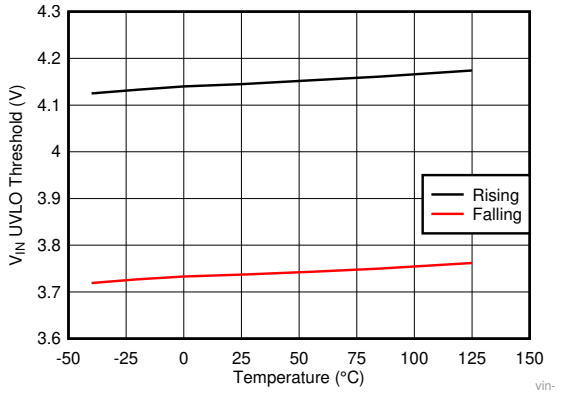


Figure 3. V_{IN} UVLO vs Junction Temperature

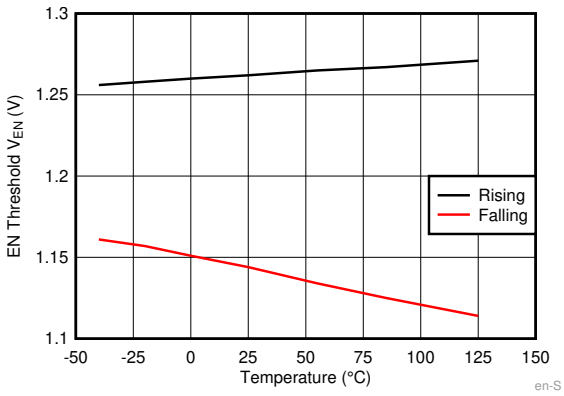


Figure 4. EN Pin UVLO vs Junction Temperature

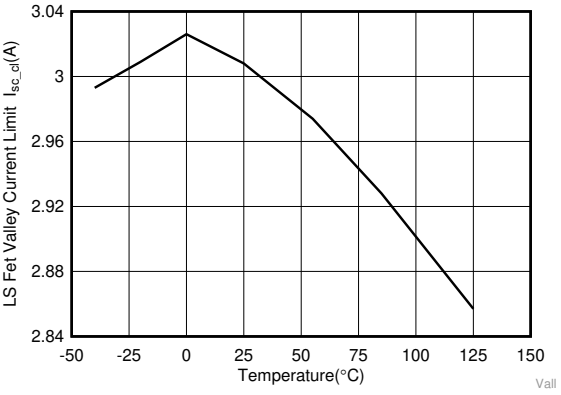


Figure 5. Current Limit vs Junction Temperature

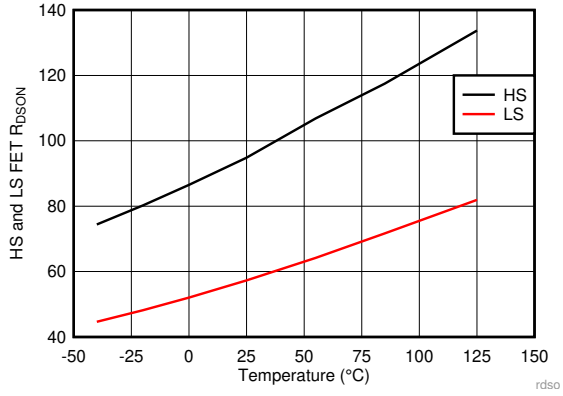


Figure 6. R_{DS-ON} vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

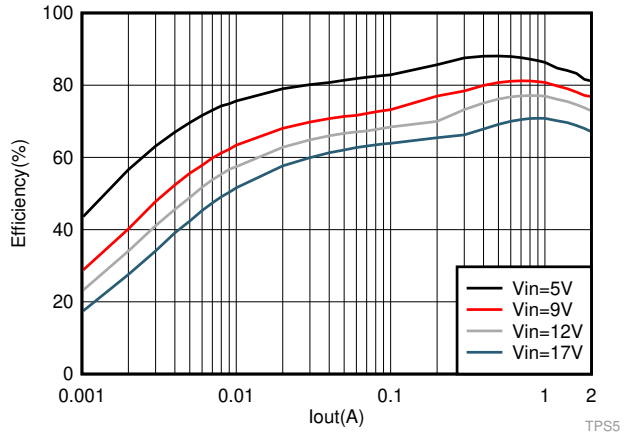


Figure 7. TPS562231 V_{OUT} = 1.05 V Efficiency

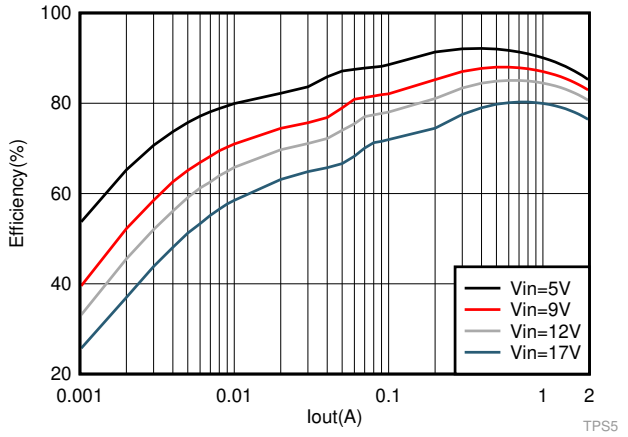


Figure 8. TPS562231 V_{OUT} = 1.8 V Efficiency

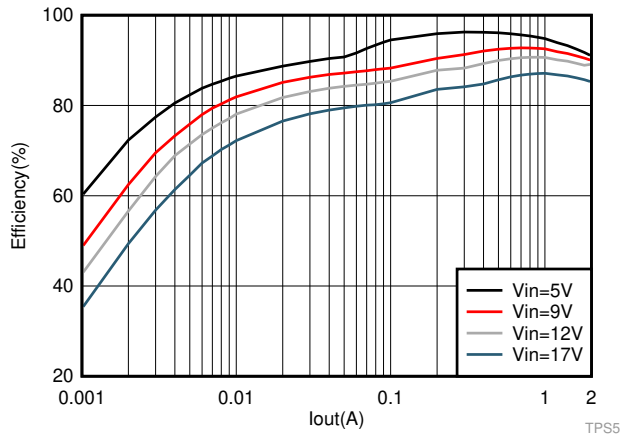


Figure 9. TPS562231 V_{OUT} = 3.3 V Efficiency

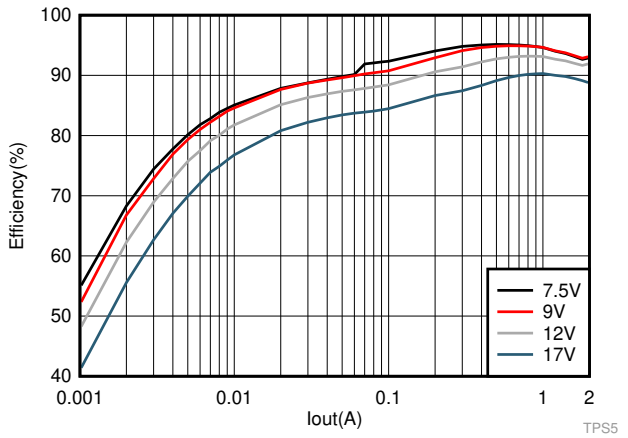


Figure 10. TPS562231 V_{OUT} = 5 V Efficiency

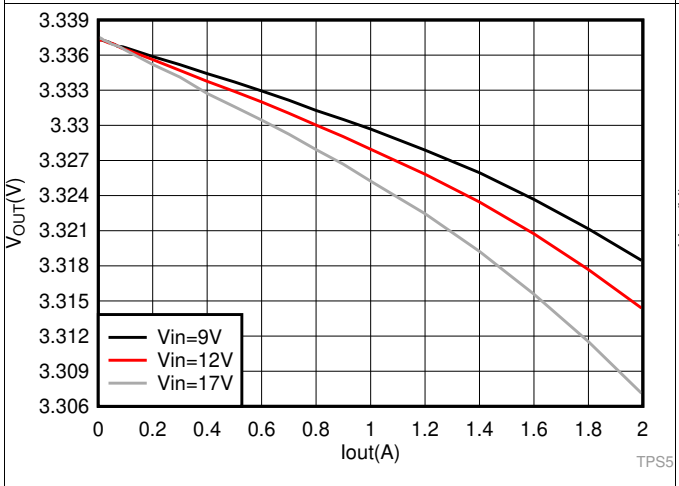


Figure 11. TPS562231 V_{OUT} = 3.3V Load Regulation

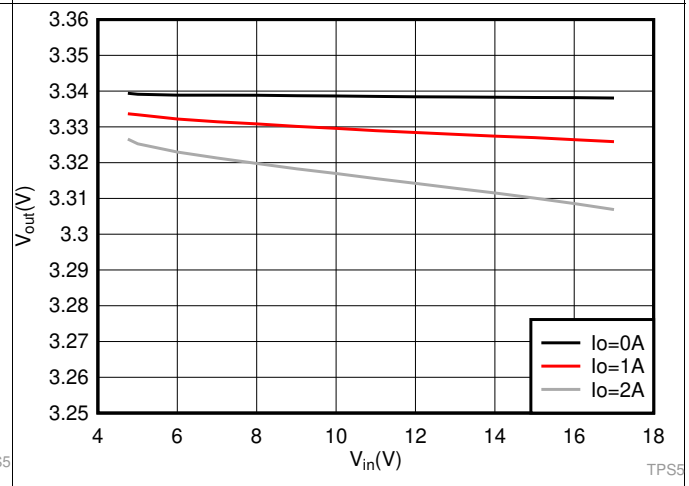


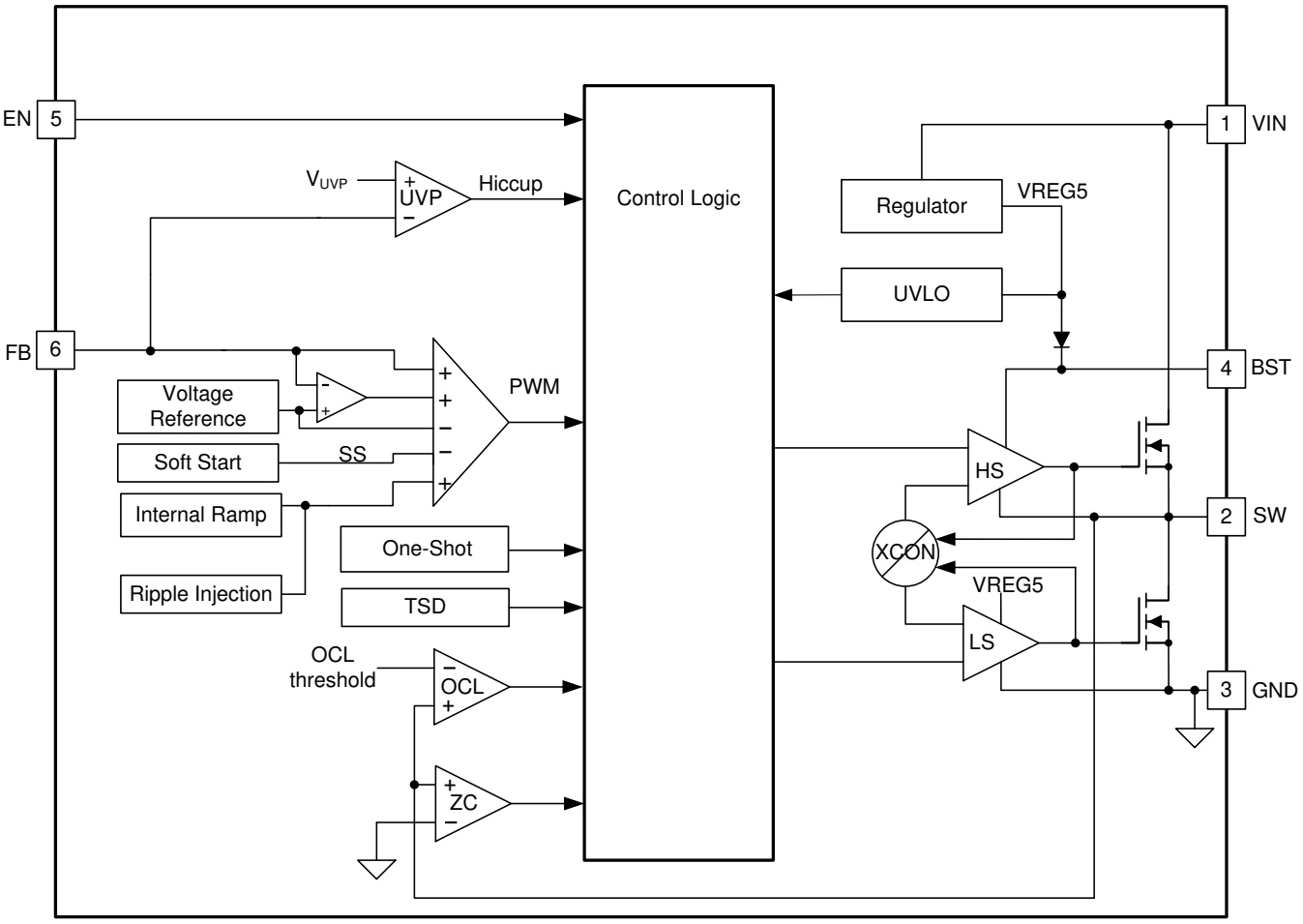
Figure 12. TPS562231 V_{OUT} = 3.3 V Line Regulation

7 Detailed Description

7.1 Overview

The TPS562231 is a 2-A synchronous step-down converter. The proprietary D-CAP3 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP3 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562231 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal on-shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN}, and inversely proportional to the output voltage, V_{OUT}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The on-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 mode control.

Feature Description (continued)

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS562231 has an internal 1.5-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage from 0 V to 0.6 V linearly.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Over Current and Short Circuit Protection

The TPS562231 is protected from over-current conditions by cycle-by-cycle current limit on the valley of the inductor current. Hiccup mode will be activated if a fault condition persists to prevent over-heating.

The current going through low-side (LS) MOSFET is sensed and monitored. When the LS MOSFET turns on, the inductor current begins to ramp down. The LS MOSFET will not be turned OFF if its current is above the LS current limit I_{LS_LIMIT} even the feedback voltage, V_{FB}, drops below the reference voltage V_{REF}. The LS MOSFET is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS MOSFET is turned OFF and the HS switch is turned on after a dead time.

As the inductor current is limited by I_{LS_LIMT}, the output voltage tends to drop as the inductor current may be smaller than the load current. Hiccup current protection mode is activated once the V_{FB} drops below the UVP threshold after a delay time (600 µs typically). In hiccup mode, the regulator is shut down and kept off for 24 ms typically before the TPS562231 try to start again. If over-current or short-circuit fault condition still exist, hiccup will repeat until the fault condition is removed. Hiccup mode reduces power dissipation under severe over-current conditions, prevents over-heating and potential damage to the device.

7.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPS562231. When V_{EN} is below its threshold (1.13 V typically), the device is in shutdown mode. The switching regulator is turned off and the quiescent current drops to 2.0 µA typically. The TPS562231 also employ V_{IN} under voltage lock out protection. If V_{IN} voltage is below its UVLO threshold (3.6 V typically), the regulator is turned off.

7.4.2 Continuous Conduction Mode (CCM)

Continuous Conduction Mode (CCM) operation is employed when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is pseud fixed, output voltage ripple will be at a minimum in this mode and the maximum output current of 2 A can be supplied.

Device Functional Modes (continued)

7.4.3 Pulse Skip Mode (PSM, TPS562231)

The TPS562231 is designed with Advanced Eco-mode™ to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The low-side MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation current I_{OUT_LL} can be calculated in Equation 1.

$$I_{OUT\_LL} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

As the load current continues to decrease, the switching frequency also decreases. The on-time starts to decrease once the switching frequency is lower than 250 kHz. The on-time can be about 22% reduced at most for extremely light load condition. This function is employed to achieve smaller ripple at extremely light load condition.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The devices are typical step-down DC-DC converters. It typically uses to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 2 A. The following design procedure can be used to select component values for the TPS562231. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The TPS562231 only require a few external components to convert from a higher variable voltage supply to a fixed output voltage. Figure 13 shows a basic schematic of 3.3-V output application. This section provides the design procedure.

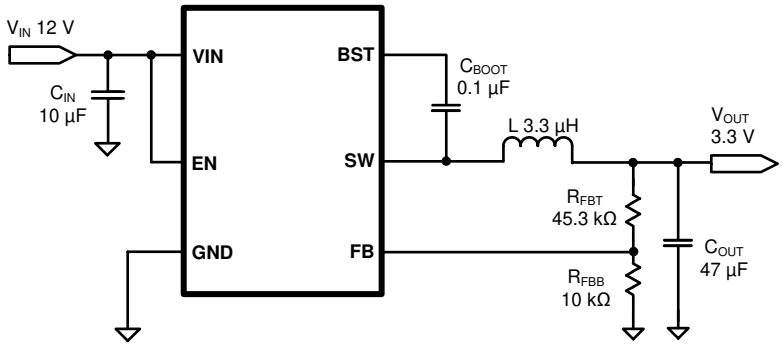


Figure 13. TPS562231 3.3V/2-A Reference Design

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	3.3 V
Transient response, 2-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	2 A
Operating frequency	850 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. 1% tolerance or better divider resistors is recommended. Start by using Equation 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \quad (2)$$

Choose the value of R_{FBB} to be 10 kΩ. With the desired output voltage set to 3.3 V and the V_{REF} = 0.6 V, the R_{FBT} value can then be calculated using Equation 2. The formula yields to a value 45.3 kΩ of R_{FBT}.

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	6.65	10.0	1	1.2	4.7	20 to 68
1.05	7.5	10.0	1	1.2	4.7	20 to 68
1.2	10	10.0	1.2	1.5	4.7	20 to 68
1.5	15	10.0	1.5	1.5	4.7	20 to 68
1.8	20	10.0	1.5	2.2	4.7	20 to 68
2.5	31.6	10.0	2.2	2.2	4.7	20 to 68
3.3	45.3	10.0	2.2	3.3	4.7	20 to 68
5	73.2	10.0	3.3	4.7	4.7	20 to 68
6.5	97.6	10.0	3.3	4.7	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{L\_PP} = \frac{V_{OUT}}{V_{IN\_MAX}} \times \frac{V_{IN\_MAX} - V_{OUT}}{L \times f_{SW}} \quad (4)$$

$$I_{L\_PK} = I_{OUT} + \frac{I_{L\_PP}}{2} \quad (5)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{L\_PP}^2} \quad (6)$$

For this design example, the calculated peak current is 2.43 A and the calculated RMS current is 2.01A. The inductor used is a WE 74437349033 with a peak current rating of 13.5 A and an RMS current rating of 5 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562231 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{C\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (7)$$

For this design two Murata GRM21BR61A226ME44L 22-µF/10-V output capacitors are used in parallel. The typical ESR is 3mΩ each. The calculated RMS current is 0.39 A and each output capacitor is rated for 5 A.

8.2.2.3 Input Capacitor Selection

The TPS562231 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10-µF for the decoupling capacitor. An additional 0.1-µF capacitor from VIN pin to GND pin is also recommended to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage, 25 V or higher voltage rating is recommended.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BST to SW pin for proper operation. 10 V or higher voltage rating is recommended.

8.2.3 Application Curves

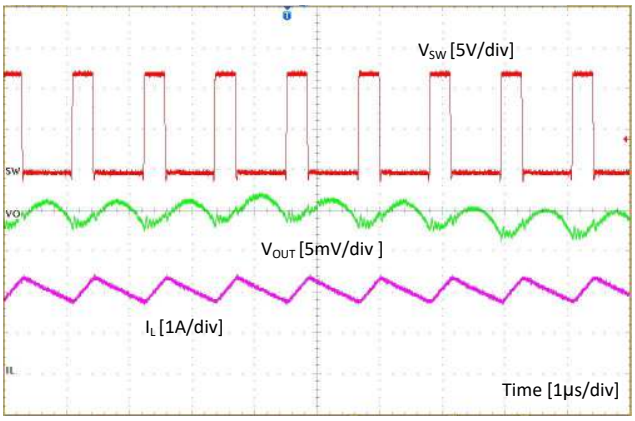


Figure 14. CCM Mode

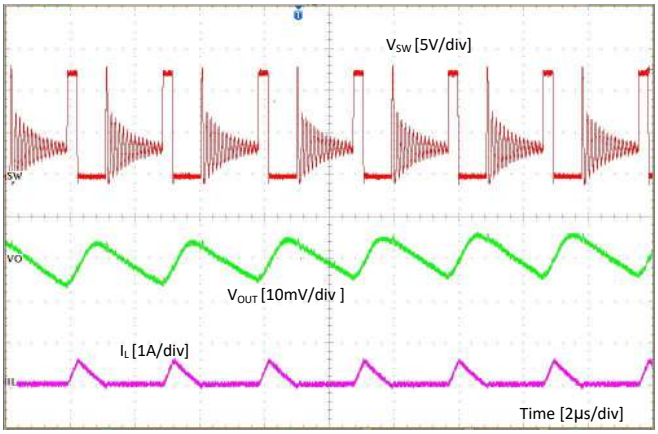


Figure 15. DCM Mode

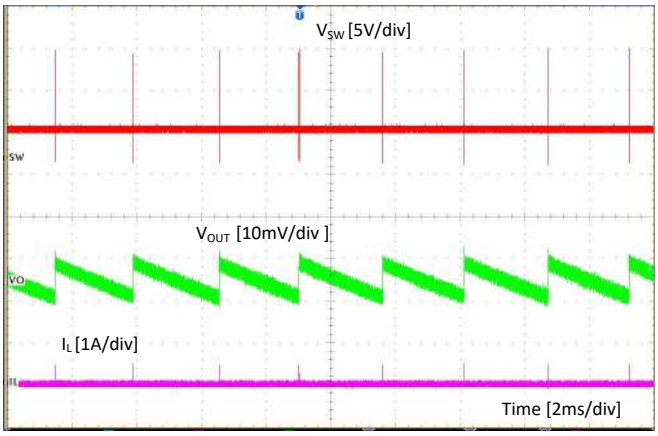


Figure 16. PSM Mode

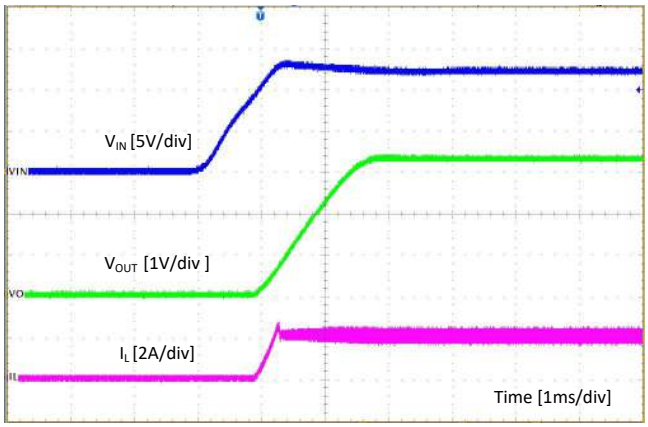


Figure 17. Start-up by V_{IN}

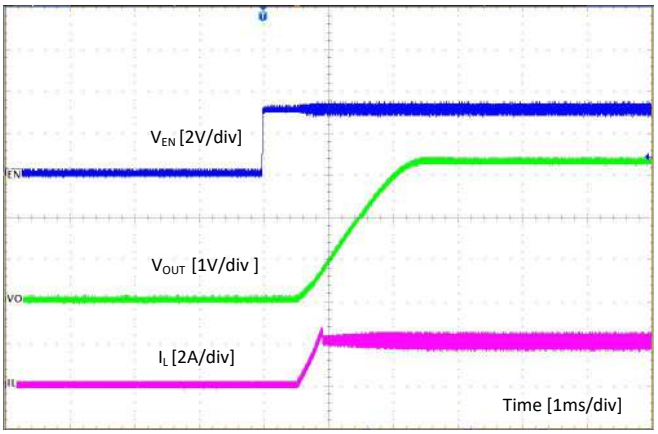


Figure 18. Start-up by EN

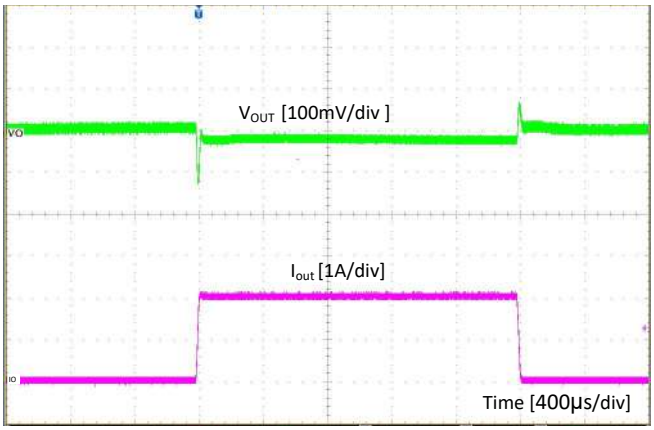


Figure 19. Load Transient

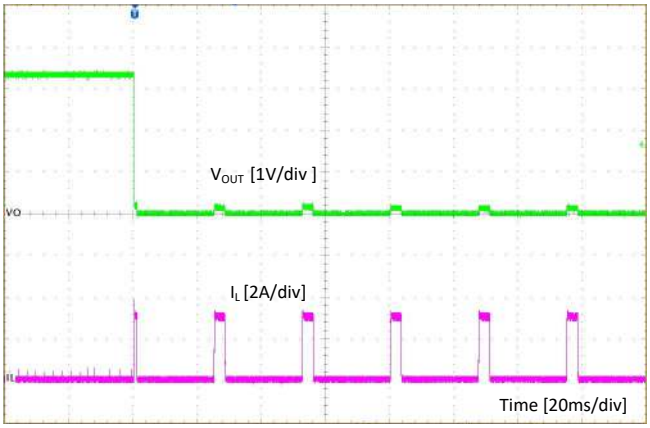


Figure 20. Short Protection

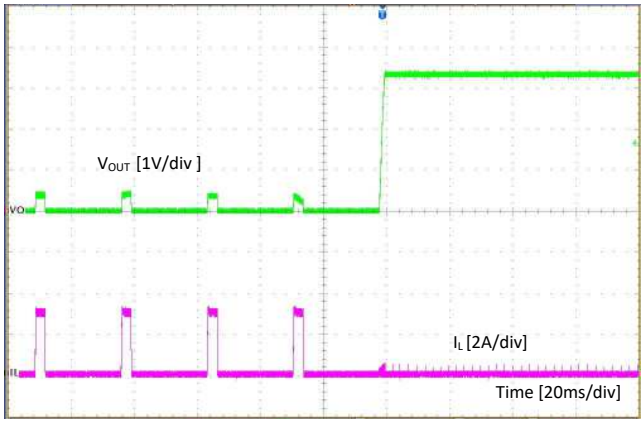


Figure 21. Short Recovery

9 Power Supply Recommendations

TPS562231 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 70%. Using that criteria, the minimum recommended input voltage is V_O / 0.7.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

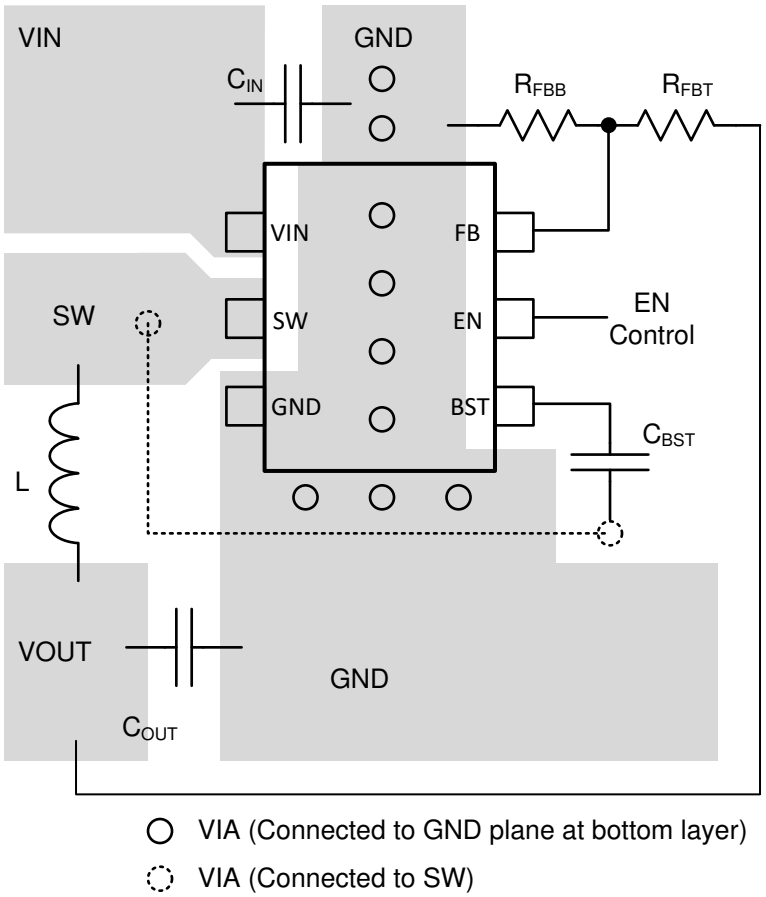


Figure 22. TPS562231 Layout

11 Device and Documentation Support

11.1 Device Support

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

D-CAP3, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS562231DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	2231	Samples
TPS562231DRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	2231	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

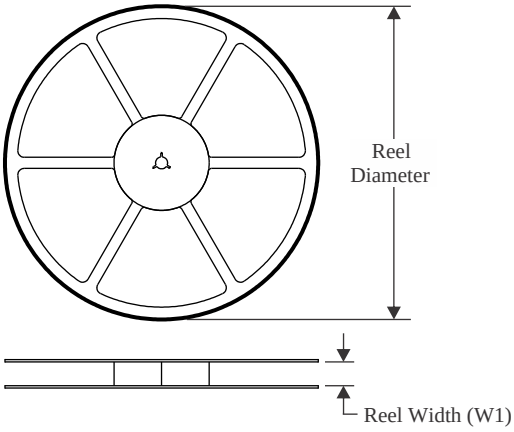
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

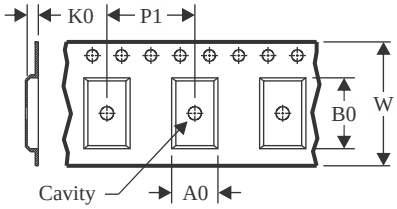
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

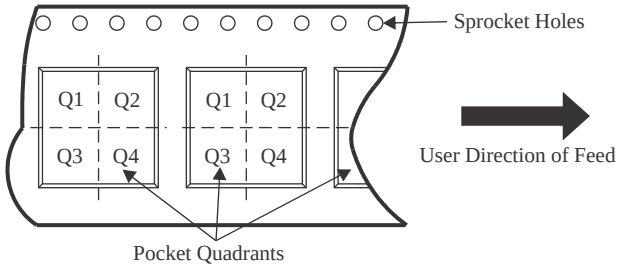


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

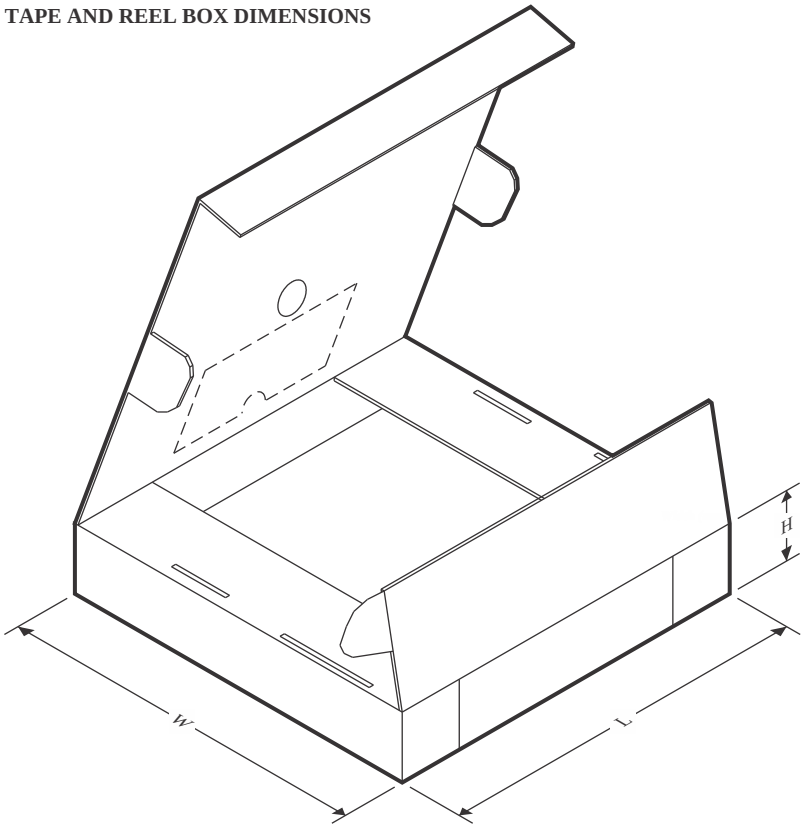
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS562231DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS562231DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS562231DRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS562231DRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

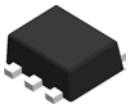
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS562231DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS562231DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS562231DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TPS562231DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0

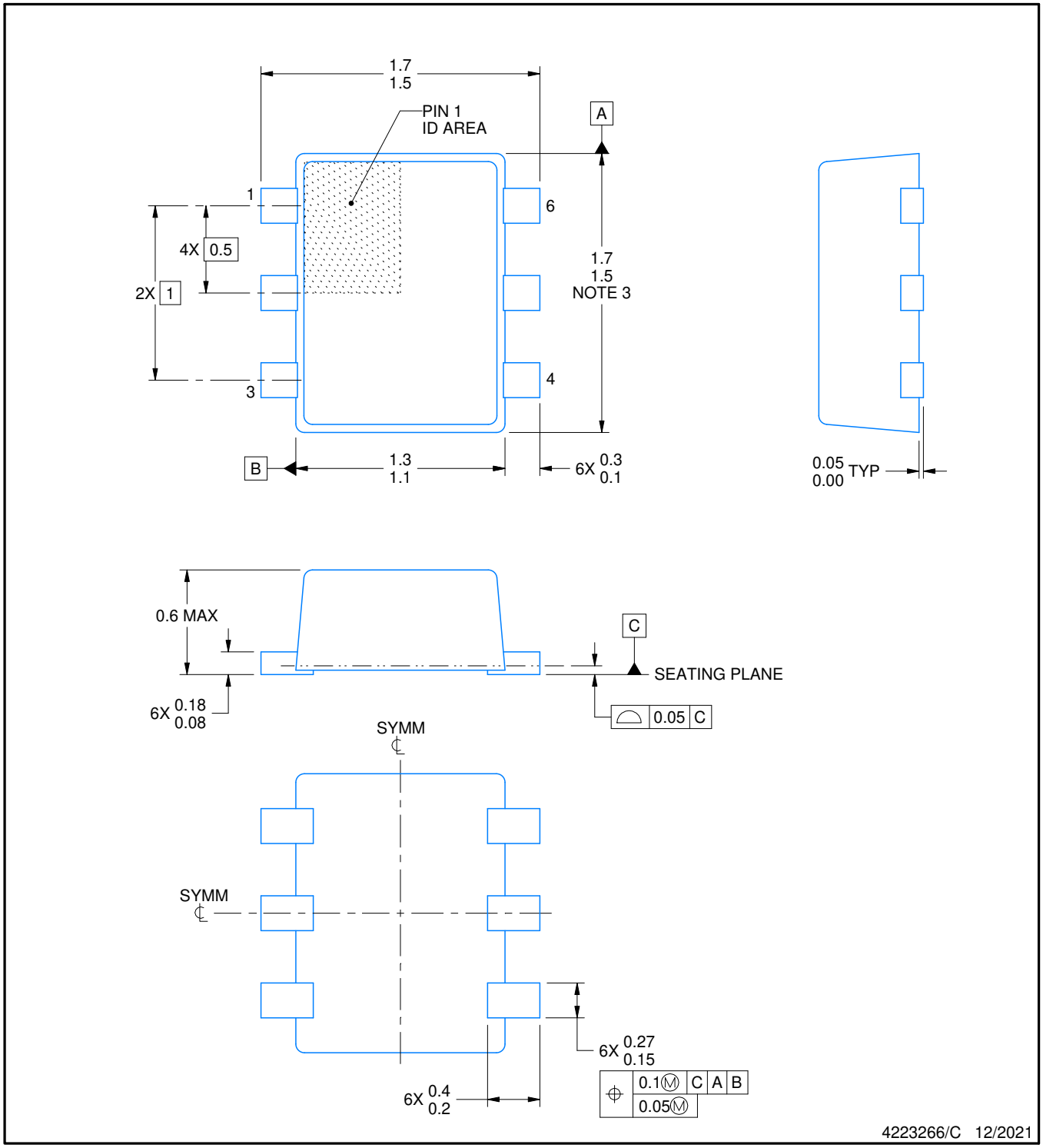
DRL0006A



PACKAGE OUTLINE

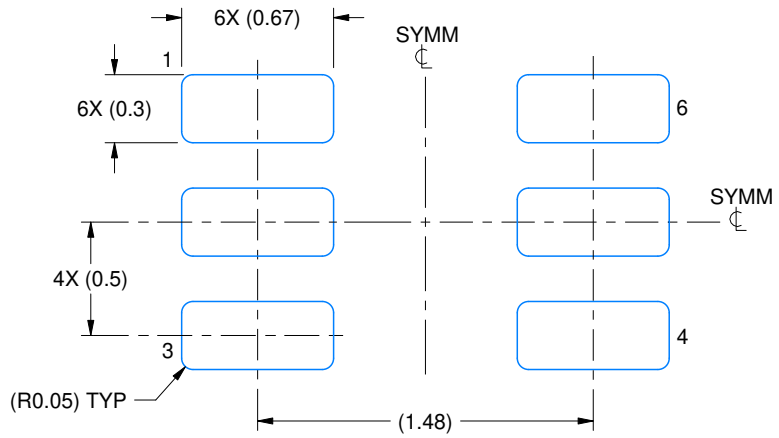
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

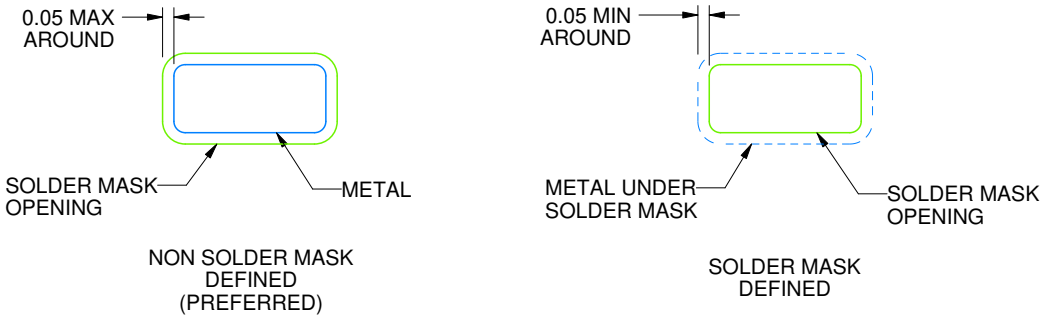


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X

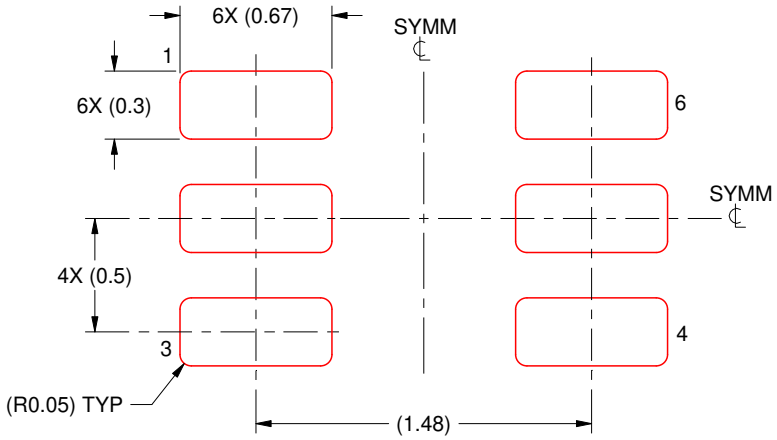


SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265