3-CH, 18V, Synchronous Step-Down Converter

General Description

The RT7273 features three synchronous wide input range high efficiency Buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5V, 9V or 12V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8V and the input supply minus 1V. Each converter features an enable pin that allows a delayed start-up for sequencing purposes, a soft-start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit pin (RLIMx) to adjust current limit by selecting an external resistor. The COMP pin allows optimizing transient versus dc accuracy response with a simple RC compensation.

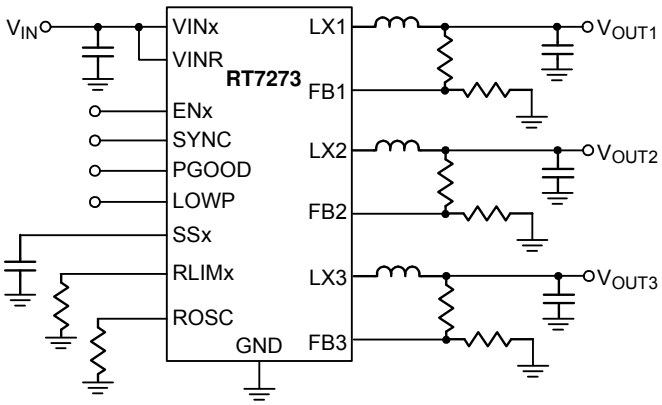
The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or be synchronized to an external clock connected to SYNC pin if needed. The switching converters are designed to operate from 300kHz to 2.2MHz. The converters operate with 180° phase between CH 1 and CH 2, CH 3 (CH 2 and CH 3 ran in phase) to minimize the input filter requirements.

The RT7273 also features a low power mode enabled by an external signal, which allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

Features

- **Wide Input Supply Voltage Range : 4.5V to 18V**
- **Output Range : 0.8V to (VIN – 1V)**
- **Fully Integrated Triple-Buck**
  - **Maximum Current 3.5A/2.5A/2.5A**
  - **Continuous Operation 3A/2A/2A**
- **High Efficiency**
- **Switching Frequency**
  - **300kHz to 2.2MHz Set by External Resistor**
- **External Synchronization Pin for Oscillator**
- **External Enable/Sequencing Pins**
- **Adjustable Cycle-By-Cycle Current Limit Set by External Resistor**
- **Soft-Start**
- **Current Mode Control with Simple Compensation Circuit**
- **Power Good Indicator**
- **Discontinuous Operating Mode at Light Load when LOWP = High**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



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Applications

- Set Top Boxes
- Blu-ray DVD
- DVR
- DTV
- Car Audio/Video
- Security Camera

Marking Information

RT7273GQW : Product Number

YMDNN : Date Code

Ordering Information

RT7273 □□□

Pin 1 Orientation***
(2) : Quadrant 2, Follow EIA-481-D

Package Type
QW : WQFN-40L 6x6 (W-Type)
(Exposed Pad-Option 2)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

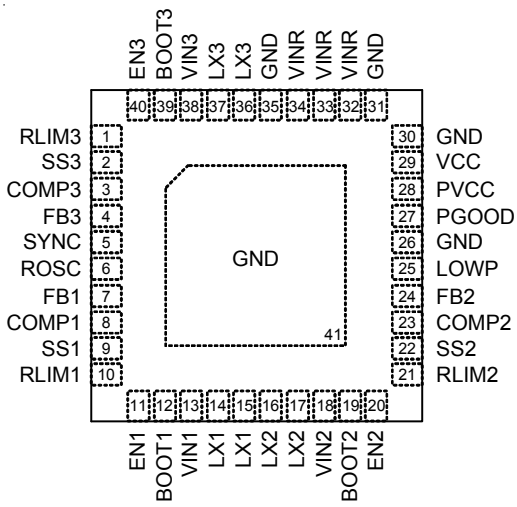
***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



WQFN-40L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	RLIM3	Current Limit Setting for CH 3. Connect a resistor from RLIM3 to GND to set the peak current limit on the output inductor.
2	SS3	Soft-Start Time Setting for CH 3. Connect a capacitor to this pin and GND for soft-start time setting.
3	COMP3	Compensation Node for CH 3. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
4	FB3	Feedback Voltage Input for CH 3.
5	SYNC	Synchronous Clock Input. Connect to GND if not used.
6	ROSC	Oscillator Setting. Connect a resistor from ROSC to GND to set the switching frequency.
7	FB1	Feedback Voltage Input for CH 1.
8	COMP1	Compensation Node for CH 1. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
9	SS1	Soft-Start Time Setting for CH 1. Connect a capacitor to this pin and GND for soft-start time setting.

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Pin No.	Pin Name	Pin Function
10	RLIM1	Current Limit Setting for CH 1. Connect a resistor from RLIM to GND to set the peak current limit on the output inductor.
11	EN1	Enable Control Input for CH 1. A low level signal on this pin disables it. If this pin is left open, a weak internal pull-up to VCC will allow automatic enables.
12	BOOT1	Bootstrap Supply for High-Side Gate Driver of CH 1. Connect a 0.1μF ceramic capacitor from this pin to LX1.
13	VIN1	Power Input for CH 1 and Connected to High-Side MOSFET Drain. Place a 10μF ceramic capacitor close to this pin.
14, 15	LX1	Switch Node of CH 1.
16, 17	LX2	Switch Node of CH 2.
18	VIN2	Power Input for CH 2. Place a 10μF ceramic capacitor close to this pin.
19	BOOT2	Bootstrap Supply for High-Side Gate Driver of CH 2. Connect a 0.1μF ceramic capacitor from this pin to LX2.
20	EN2	Enable Control Input for CH 2. A low level signal on this pin disables it. If this pin is left open, a weak internal pull-up to VCC will allow automatic enables.
21	RLIM2	Current Limit Setting for CH 2. Connect a resistor from RLIM2 to GND to set the peak current limit on the output inductor.
22	SS2	Soft-Start Time Setting for CH 2. Connect a capacitor to this pin and GND for soft-start time setting.
23	COMP2	Compensation Node for CH 2. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
24	FB2	Feedback Voltage Input for CH 2.
25	LOWP	Discontinuous Operation Mode Input (Active High).
26, 30, 31, 35, 41 (Exposed Pad)	GND	Ground. The exposed pad must be connected to GND and soldered to a large PCB copper plane for maximum power dissipation.
27	PGOOD	Power Good Indicator Output with Open-Drain.
28	PVCC	5V Power Supply Output. Connect a capacitor 10μF between this pin and GND.
29	VCC	4.6V Power Supply Output. Connect a capacitor 3.3μF between this pin and GND.
32, 33, 34	VINR	Supply Voltage Input for Internal Control Circuit.
36, 37	LX3	Switch Output for CH 3.
38	VIN3	Power Input for CH 3. Place a 10μF ceramic capacitor close to this pin.
39	BOOT3	Bootstrap Supply for High-Side Gate Driver of CH 3. Connect a 0.1μF ceramic capacitor from this pin to LX3.
40	EN3	Enable Control Input for CH 3. A low level signal on this pin disables it. If this pin is left open, a weak internal pull-up to VCC will allow automatic enables.

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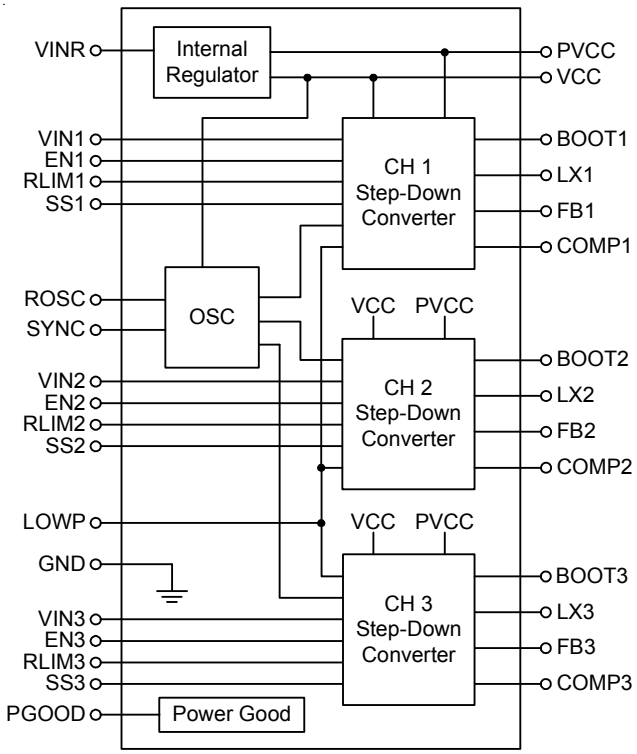
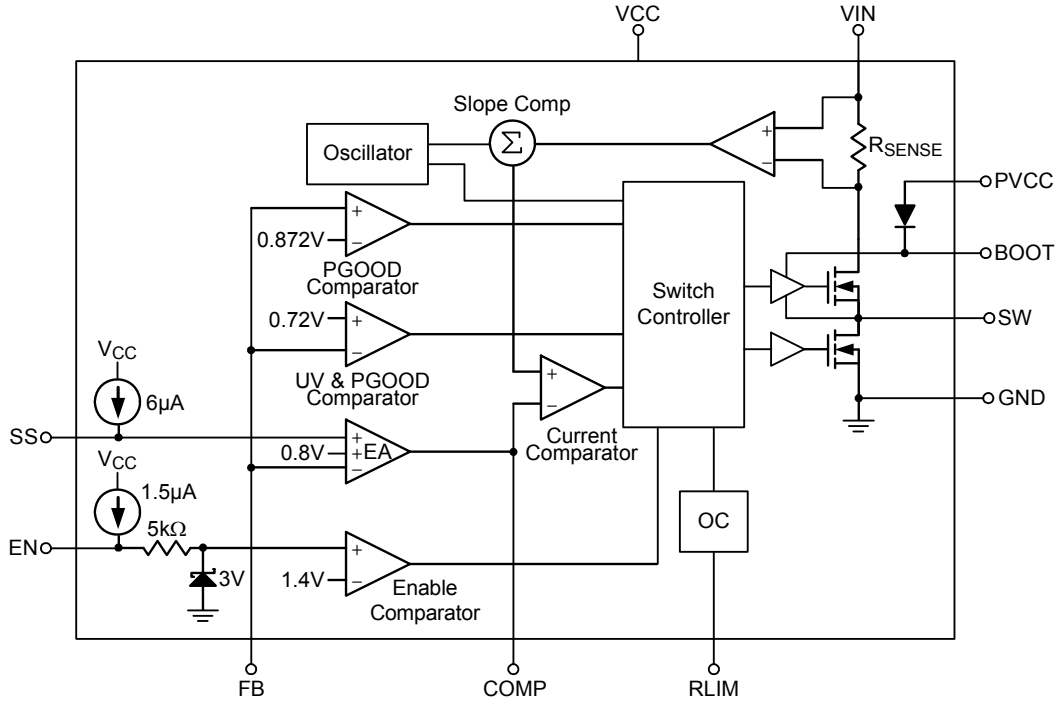
Functional Block Diagram

Whole Chip Function Block Diagram



Each Channel Function Block Diagram



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Operation

Overall

The RT7273 is a 3-CH synchronous high voltage Buck Converter that can support the input voltage range from 4.5V to 18V and the output current up to 3A/2A/2A separately. The RT7273 uses an adjustable constant frequency, current-mode architecture. In normal operation, the high-side N-MOSFET is turned on when the Switch Controller is set by the Oscillator and is turned off when the current comparator resets the Switch Controller. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on.

High-side N-MOSFET peak current is measured by internal R_{SENSE}. The Current Signal is where Slope Compensator works together with sensing voltage of R_{SENSE}. The error amplifier EA adjusts COMP voltage by comparing the feedback signal from the output voltage with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the COMP voltage then rises to allow higher inductor current to match the load current.

UV and PGOOD Comparator

If the feedback voltage (V_{FB}) is higher than 0.72V and lower than 0.872V, the two comparators' output will go low and trigger Switch Controller to generate PGOOD signal for this channel. However, the whole chip PGOOD signal will go high only if all three channels' PGOOD conditions are established. If V_{FB} is lower than UV threshold, the UV comparator's output will go high and the Switch Controller will turn off the high-side N-MOSFET. The output under-voltage protection is designed to operate in hiccup mode. This function is only available after soft-start finished.

Oscillator

The frequency of internal oscillator can be adjusted by the external resistor at ROSC pin in the range between 300kHz and 2.2MHz. It can also be synchronized by an external clock in the range between 200kHz and 2.2MHz from SYNC pin.

Enable Comparator

The internal 1.5μA pull-up current to EN pin can be used to set the power sequence of each channel by connecting a capacitor to EN pin. Internal 5kΩ resistor and Zener diode are used to clamp the input signal to 3V. Thus, the EN pin can also be connected to VIN through a 100kΩ resistor.

Soft-Start

An internal current source (6μA) charges an external capacitor connected to SS pin to build the soft-start ramp voltage. The V_{FB} voltage will track the soft-start ramp voltage during soft-start interval. The typical soft-start time is 2ms.

Over-Current Limit

Each channel can set its own over-current limit by external resistor. It is recommended that the over-current limit level should be 1.5 times larger than the maximum loading current.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN1, VIN2, VIN3, VINR ---------- –0.3V to 21V
- Switch Node Voltage, LX1, LX2, LX3 ---------- –0.3V to (VINx + 0.3V)
  < 10ns ---------- –5V to 25V
- BOOTx to LXx ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 6x6 ---------- 3.52W
- Package Thermal Resistance (Note 2)
  WQFN-40L 6x6, θ_{JA} ---------- 28.4°C/W
  WQFN-40L 6x6, θ_{JC} ---------- 5.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, f_S = 800kHz, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply UVLO and Internal Supply Voltage						
Supply Current (Shutdown)	I_{Q_SDN}	V_{EN} = 0V for All CHs	--	1.3	--	mA
Supply Current (Quiescent)	I_Q	Converters enabled, Buck1 = 3.3V, Buck2 = 2.5V, Buck3 = 7.5V	--	20	--	mA
Supply Current (LOWP enabled)	I_{Q_LOWP}	Converters enabled, Buck1 = 3.3V, Buck2 = 2.5V, Buck3 = 7.5V	--	1.5	--	mA
VIN Under-Voltage Lockout	V_{VIN_UVLO}	V_{IN} Rising	--	4.2	--	V
VIN Under-Voltage Lockout Hysteresis		V_{IN} Falling	--	200	--	mV
VIN Under-Voltage Lockout Deglitch			--	100	--	μs
Internal Biasing Supply	V_{PVCC}		--	5	--	V
Internal Biasing Supply	V_{VCC}		--	4.6	--	V
PVCC Under-Voltage Lockout	V_{PVCC_UVLO}	PVCC Rising	--	3.8	--	V
PVCC Under-Voltage Lockout Hysteresis			--	250	--	mV

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PVCC Under-Voltage Lockout Deglitch				--	100	--	μs
Enable Circuit, Soft-Start, Sync Circuit, Low Power Mode and Switching Frequency							
Enable Input Voltage	Logic-High	V_{EN_H}		1.6	--	--	V
	Logic-Low	V_{EN_L}		--	--	1.2	
ENx Pull-Up Current		I_{EN}		--	1.5	--	μA
Soft-Start Current Source		I_{SS}		--	6	--	μA
Converter Switching Frequency Range		f_{SW}		0.3	--	2.2	MHz
Frequency Setting Resistor		R_{OSC}		50	--	600	kΩ
Internal Oscillator Accuracy		f_{SW_TOL}	f_{SW} = 800kHz	−10	--	10	%
SYNC External Clock Input Voltage	Logic-High	V_{SYNC_H}		1.6	--	--	V
	Logic-Low	V_{SYNC_L}		--	--	1.2	
Synchronization Range		f_{SW_SYNC}		0.2	--	2.2	MHz
SYNC Signal Minimum Duty Cycle				10	--	--	%
SYNC Signal Maximum Duty Cycle				--	--	90	%
Low Power Mode Input Voltage	Logic-High	V_{LOWP_H}		1.6	--	--	V
	Logic-Low	V_{LOWP_L}		--	--	1.2	
Feedback							
Feedback Reference Voltage		V_{REF}		0.792	0.8	0.808	V
			$4.5V \le V_{IN} \le 18V$	0.784	0.8	0.816	
Minimum On-Time		$t_{ON(MIN)}$		--	100	--	ns
Minimum Off-Time		$t_{OFF(MIN)}$		--	100	--	ns
CH 1 On-Resistance							
Switch On-Resistance		$R_{DS(ON)1_H}$		--	95	--	mΩ
		$R_{DS(ON)1_L}$		--	50	--	
CH 2 On-Resistance							
Switch On-Resistance		$R_{DS(ON)2_H}$		--	120	--	mΩ
		$R_{DS(ON)2_L}$		--	80	--	
CH 3 On-Resistance							
Switch On-Resistance		$R_{DS(ON)3_H}$		--	120	--	mΩ
		$R_{DS(ON)3_L}$		--	80	--	
Current Limit							
Current Limit CH 1		I_{OC_CH1}		2	--	6	A
Current Limit CH 2, CH 3 Range		$I_{OC_CH2, CH3_Range}$		2	--	5	A

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit CH 1	I_{OC_CH1}	R_{LIM1} = 37kΩ	2.4	3	--	A
		R_{LIM1} = 50kΩ	3.4	4	--	
		R_{LIM1} = 63kΩ	4.25	5	--	
Current Limit CH 2, CH 3	$I_{OC_CH2, CH3}$	$R_{LIM2, LIM3}$ = 44kΩ	1.6	2	--	A
		$R_{LIM2, LIM3}$ = 69kΩ	2.55	3	--	
		$R_{LIM2, LIM3}$ = 94kΩ	3.4	4	--	
Regulation						
Line Regulation		V_{IN} = 4.5V to 18V, I_{OUT} = 1000mA	--	0.5	--	$\%V_{OUT}$
Load Regulation		I_{OUT} = 10% to 90%, I_{OUT_MAX}	--	0.5	--	$\%V_{OUT}$ /A
Error Amplifier						
Error Amplifier Transconductance	G_{EA}		--	250	--	μA/V
Comp to Current Sense Transconductance	G_{CS}		--	4	--	A/V
Power Good Reset Generator						
Under-Voltage Threshold	V_{UV_CHx}	Output Falling (device will be disabled after t_{ON_HICCUP})	--	85	--	%
		Output Rising (PGOOD will be asserted)	--	90	--	
Under-Voltage Deglitch Time	$t_{UV_DEGLITCH}$	Each Channel Buck	--	10	--	ms
Hiccup Mode On-Time	t_{ON_HICCUP}	V_{UV_CHx} asserted	--	10	--	ms
Hiccup Mode Off-Time	t_{OFF_HICCUP}	All Bucks disable during t_{OFF_HICCUP} before re-start is attempted.	--	15	--	ms
Power Good	t_{PGOOD}	Power good delay time after all bucks power-up successfully	--	640	--	ms
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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Typical Application Circuit

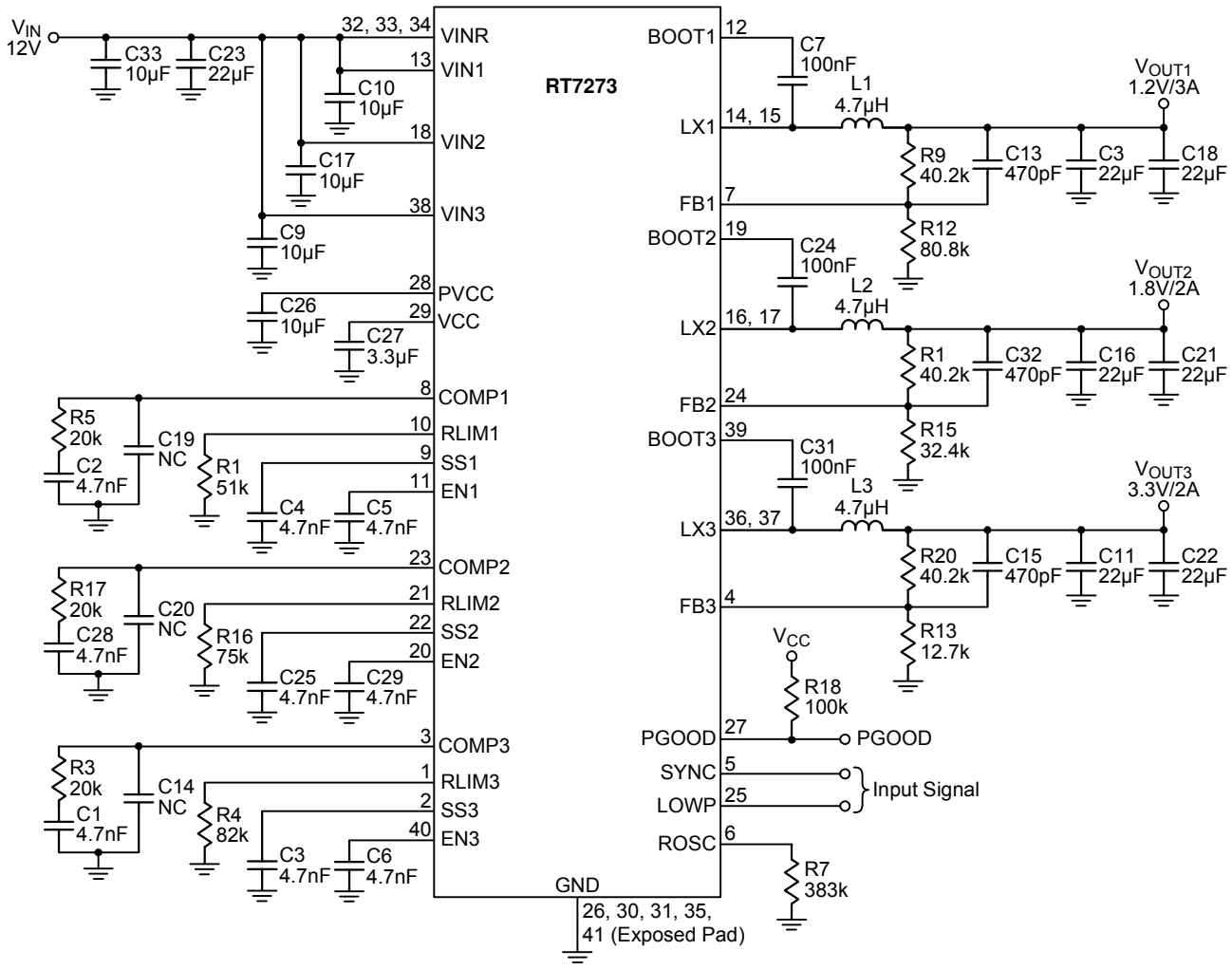

Table 1. Suggested Component Values for CH1 (V_{IN} = 12V, f_S = 500kHz)

V_{OUT} (V)	R9 (kΩ)	R12 (kΩ)	C13 (pF)	R5 (kΩ)	C2 (nF)	L1 (μH)	C3 (μF)
1.2	40.2	80.8	470	20	4.7	4.7	44
1.8	40.2	32.4	470	20	4.7	4.7	44
3.3	40.2	12.7	470	20	4.7	4.7	44
5	40.2	7.6	470	24	5.6	6.8	44
7	40.2	5.2	470	24	5.6	6.8	44

Note 5. The suggested component values can be applied to CH 2 and CH 3 as well.

Note 6. Above values are fully tested for stable operation. When making changes to output capacitors or switching frequency, please follow the guidelines in the application section.

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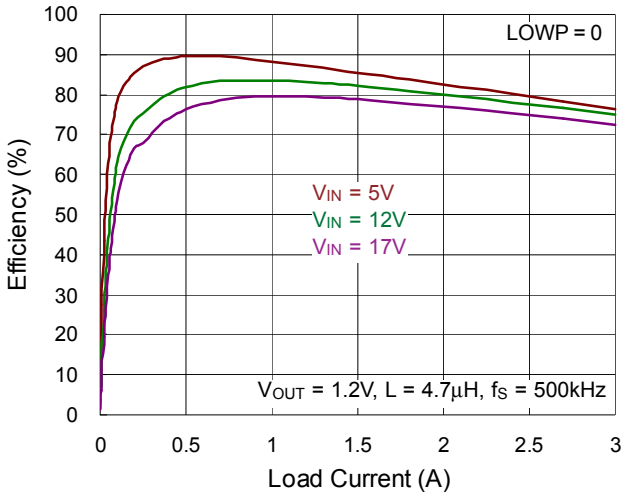
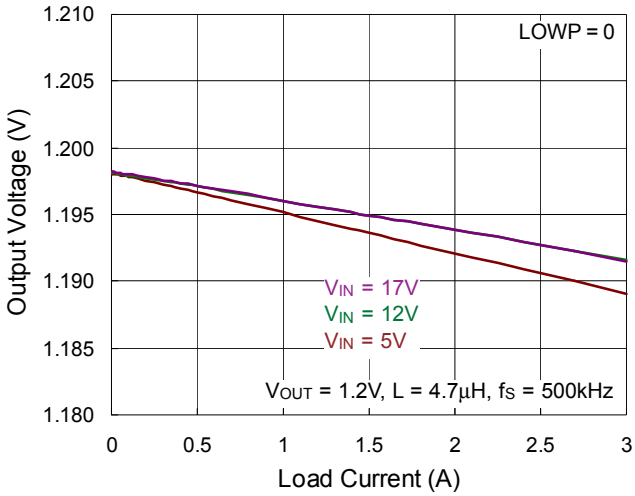
Typical Operating Characteristics

Buck 1

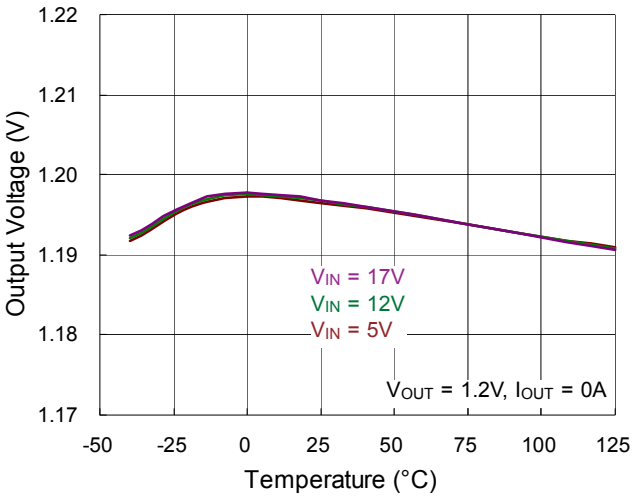
Efficiency vs. Load Current



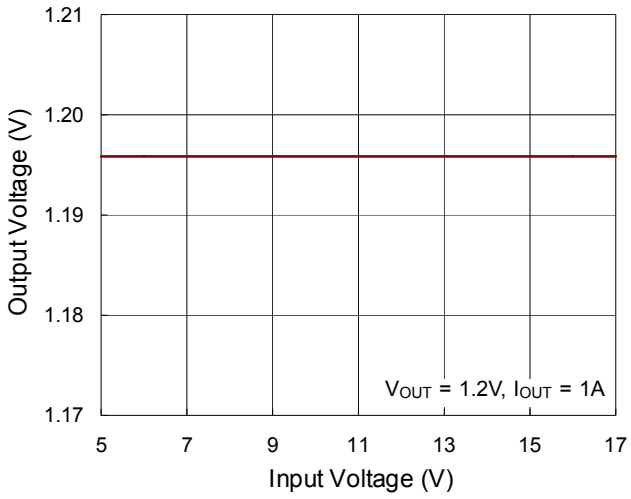
Output Voltage vs. Load Current



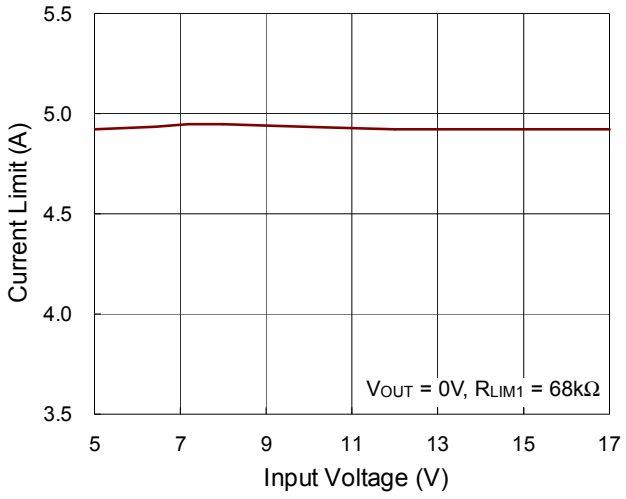
Output Voltage vs. Temperature



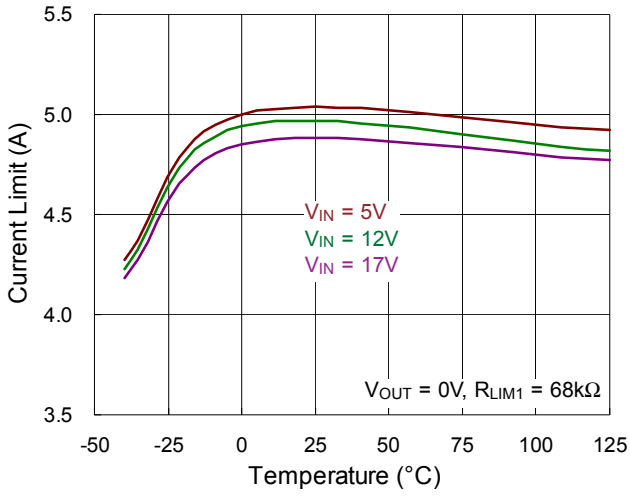
Output Voltage vs. Input Voltage



Current Limit vs. Input Voltage



Current Limit vs. Temperature



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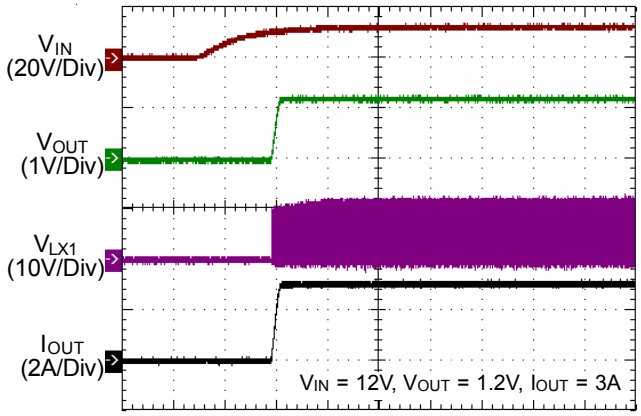
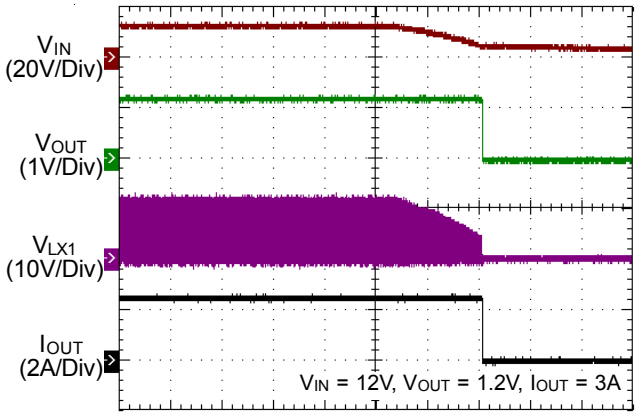
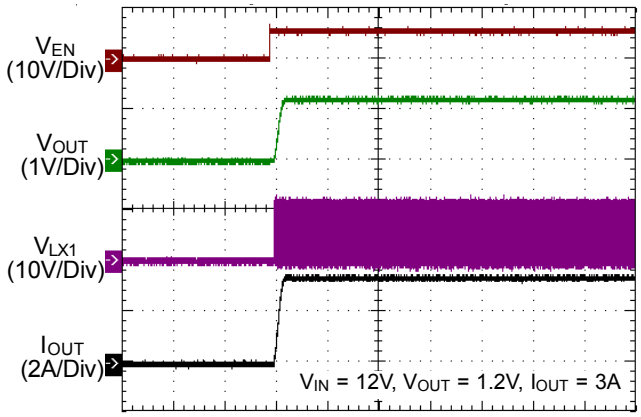
Power On from VIN



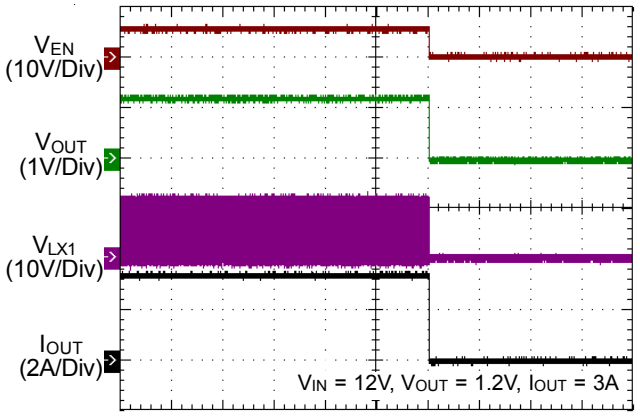
Power Off from VIN



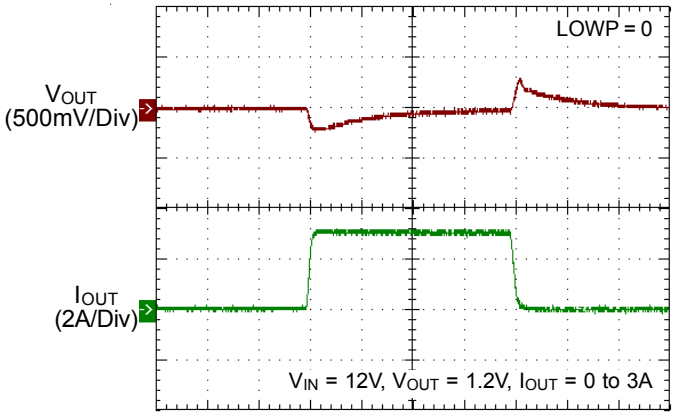
Power On from EN



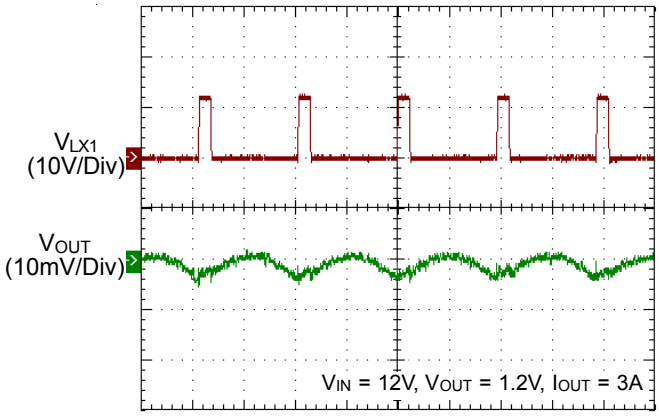
Power Off from EN



Load Transient Response



Output Ripple



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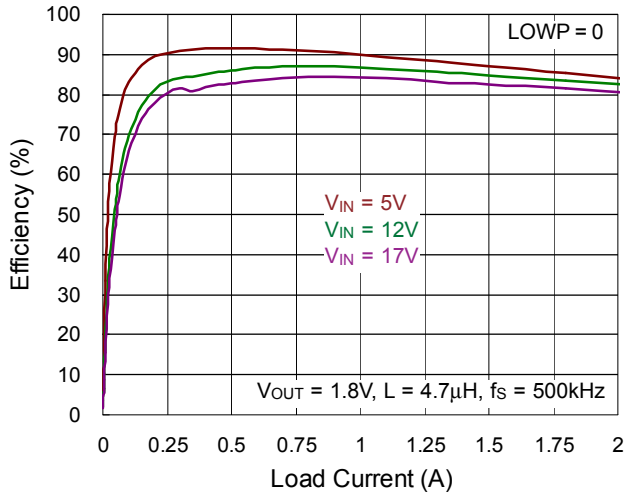
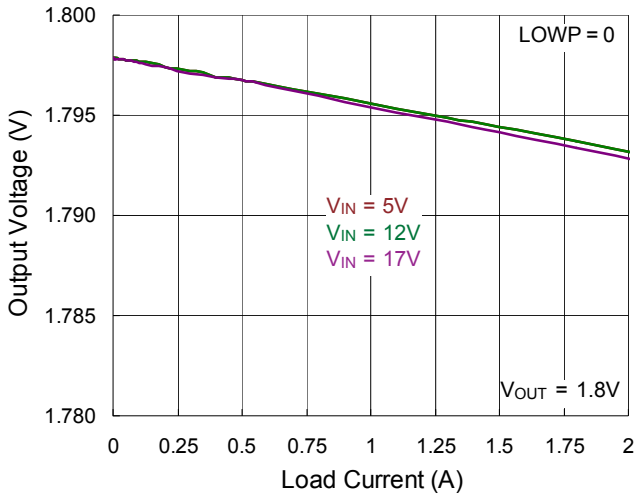
Buck 2

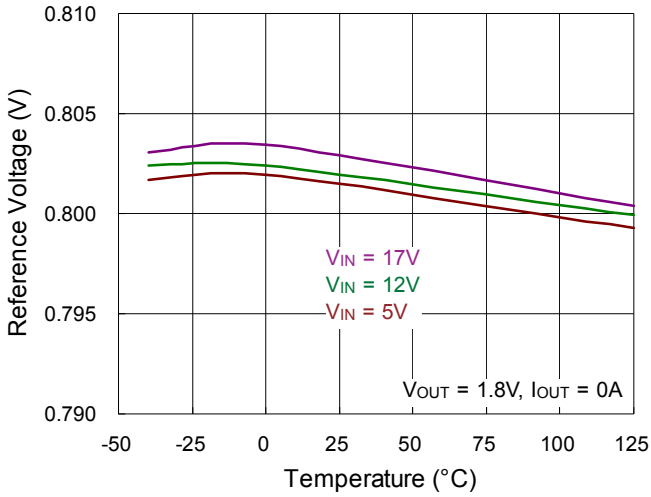
Efficiency vs. Load Current



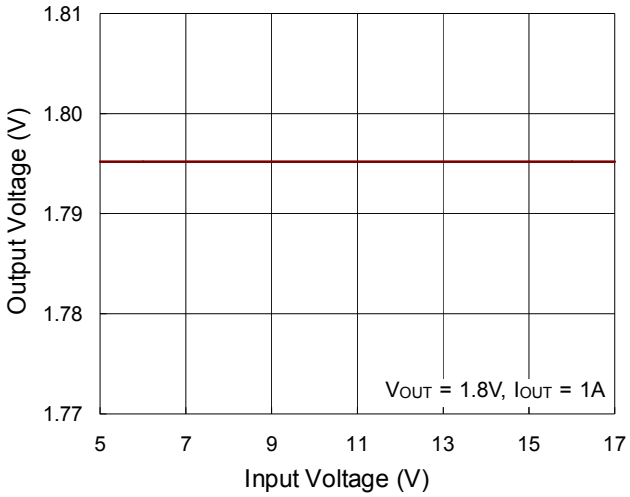
Output Voltage vs. Load Current



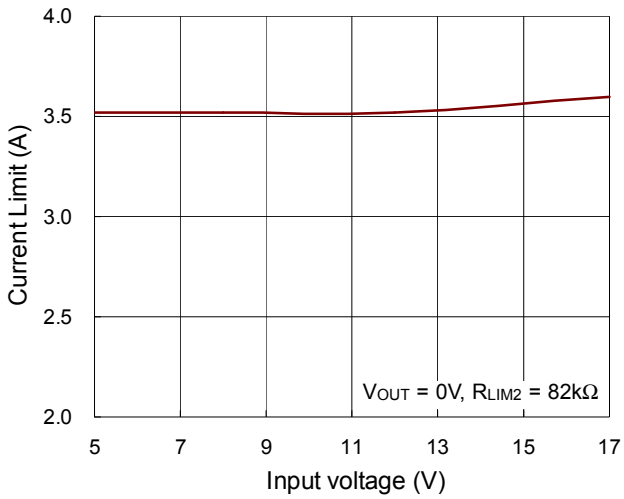
Reference Voltage vs. Temperature



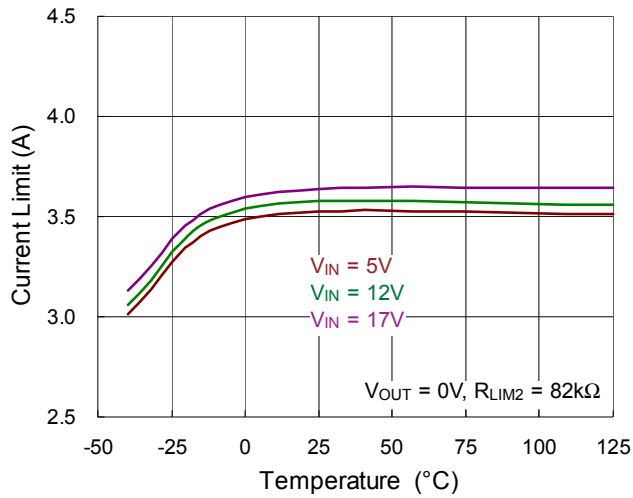
Output Voltage vs. Input Voltage



Current Limit vs. Input Voltage



Current Limit vs. Temperature



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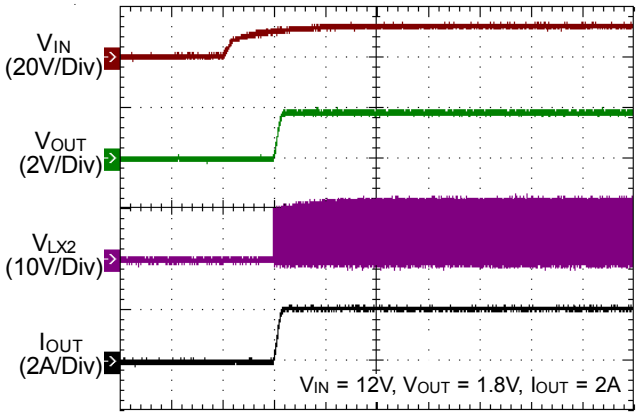
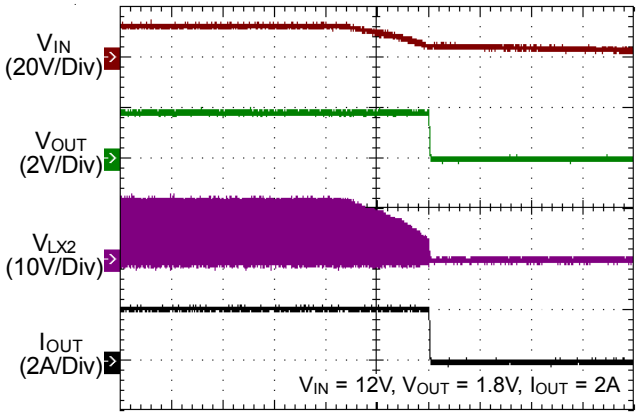
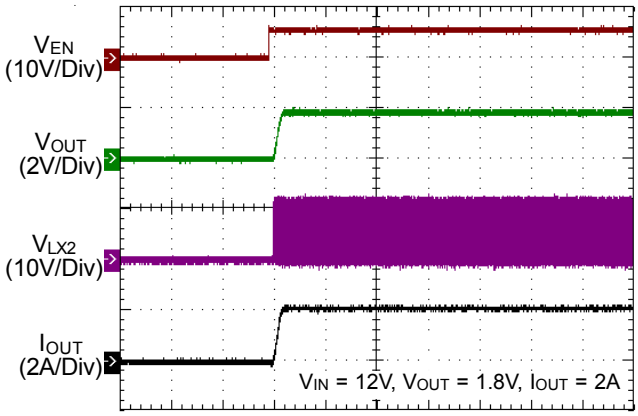
Power On from VIN



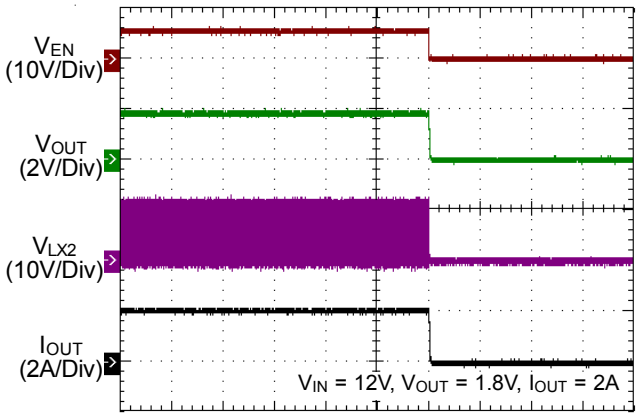
Power Off from VIN



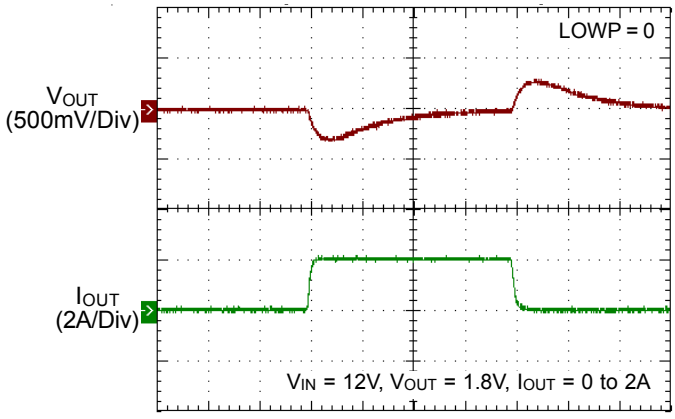
Power On from EN



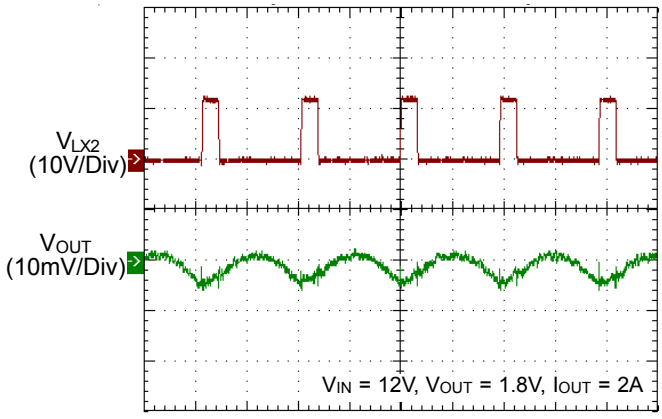
Power Off from EN



Load Transient Response



Output Ripple



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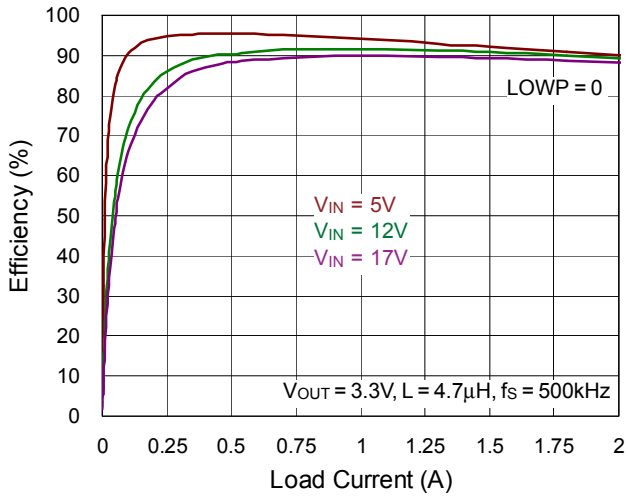
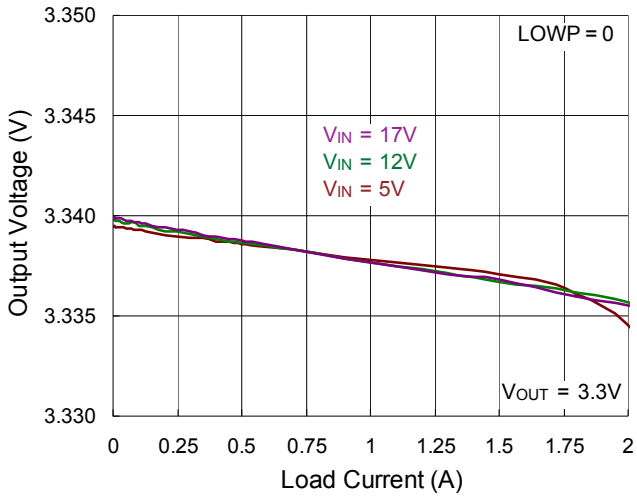
Buck 3

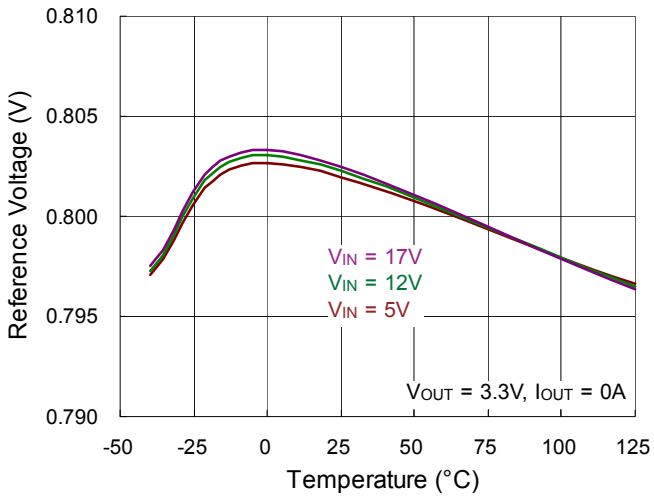
Efficiency vs. Load Current



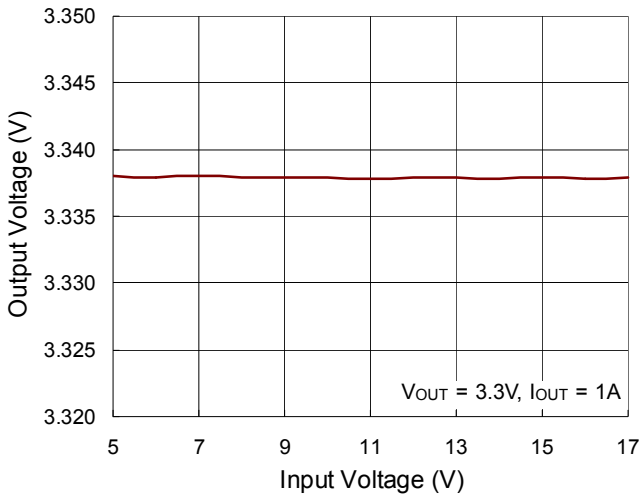
Output Voltage vs. Load Current



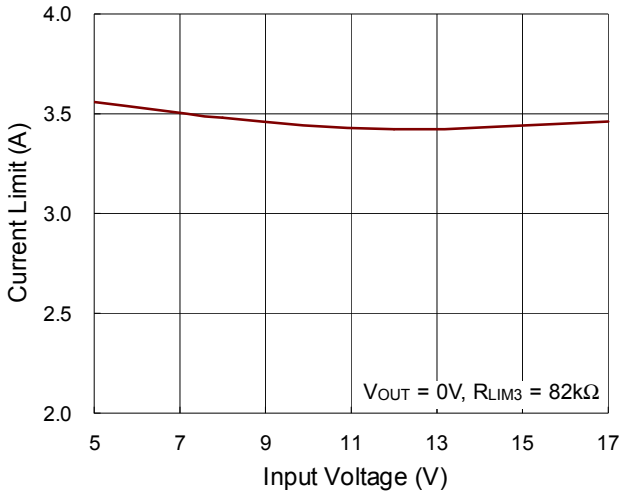
Reference Voltage vs. Temperature



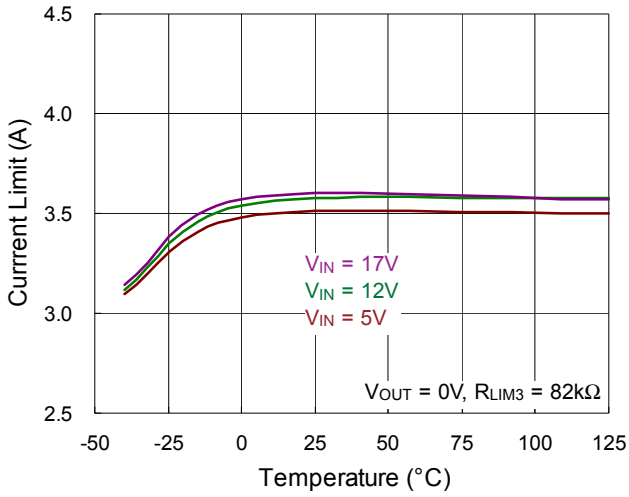
Output Voltage vs. Input Voltage



Current Limit vs. Input Voltage



Currrent Limit vs. Temperature



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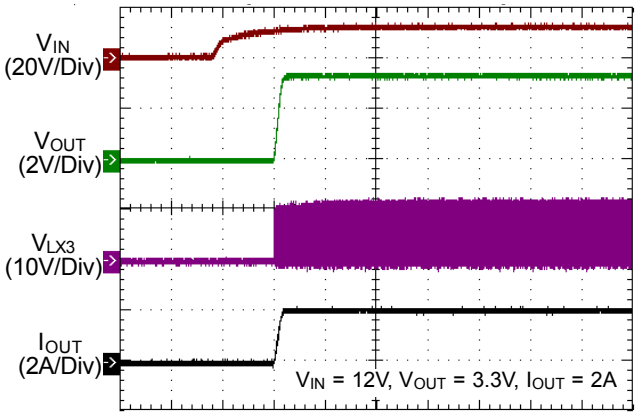
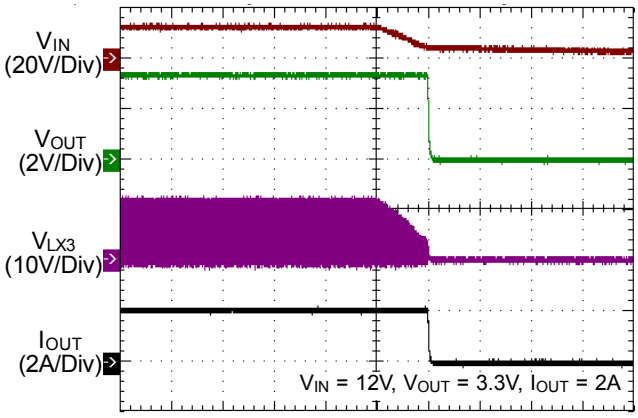
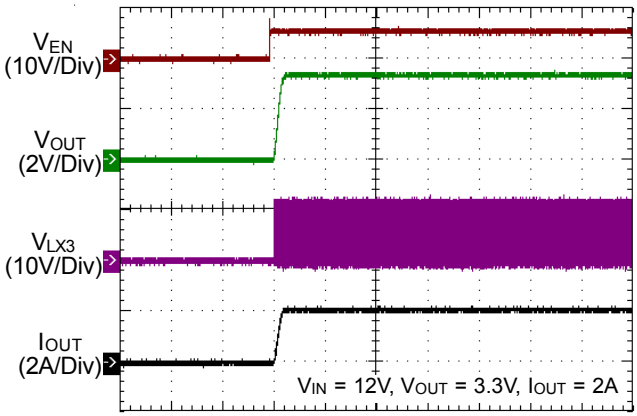
Power On from VIN



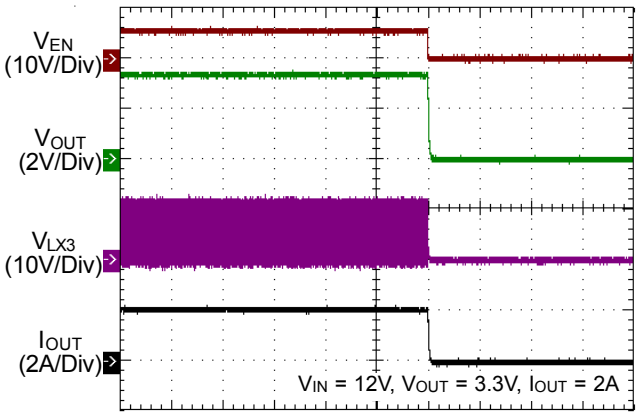
Power Off from VIN



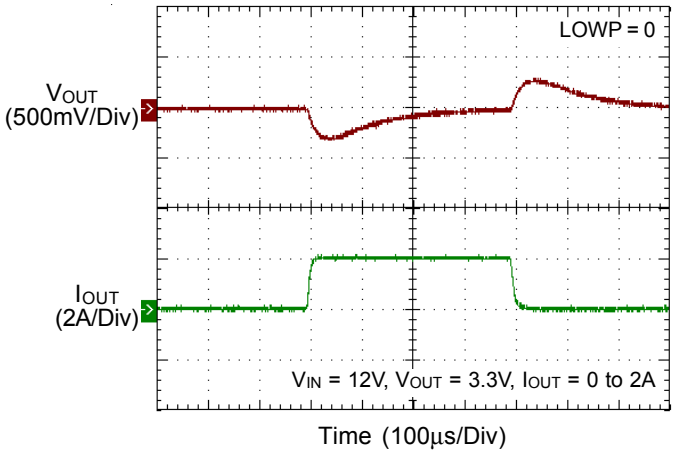
Power On from EN



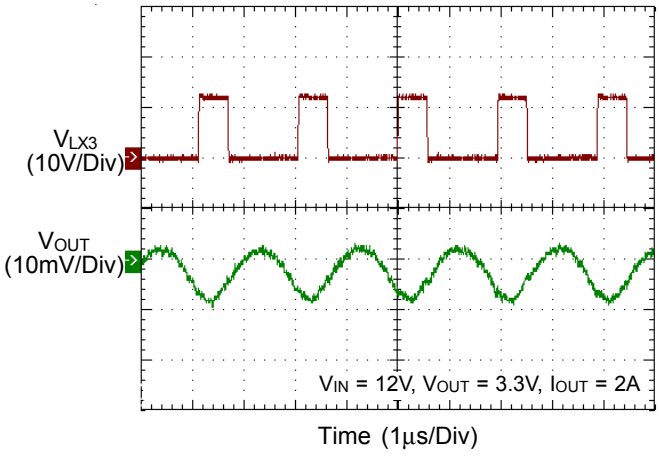
Power Off from EN



Load Transient Response



Output Ripple



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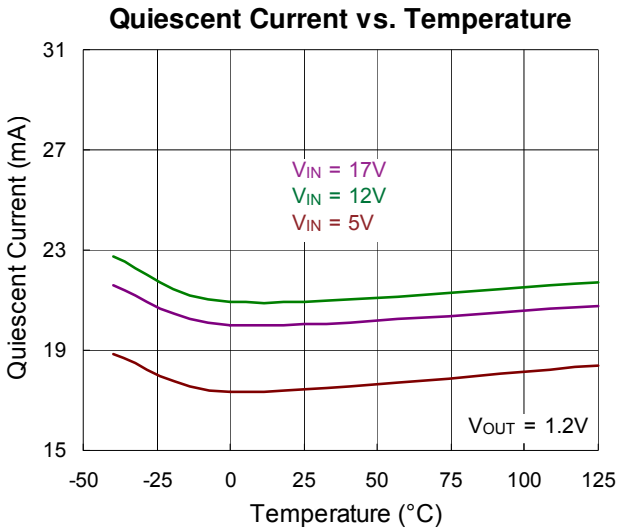
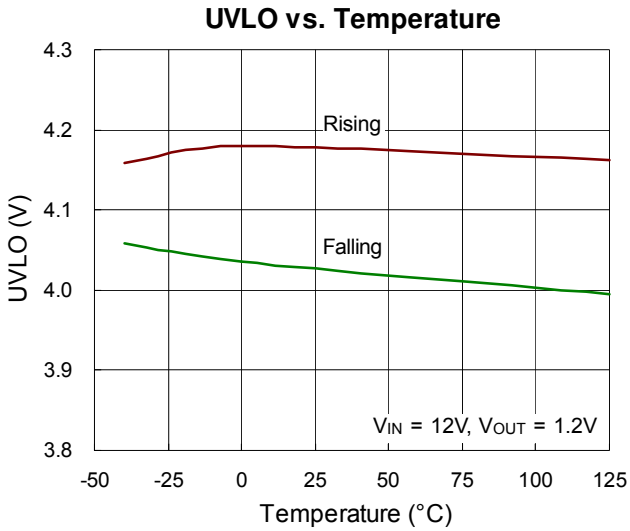
Overall





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Application Information

Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from R_{OSC} to ground. Figure 1 shows the required resistance for a given switching frequency.

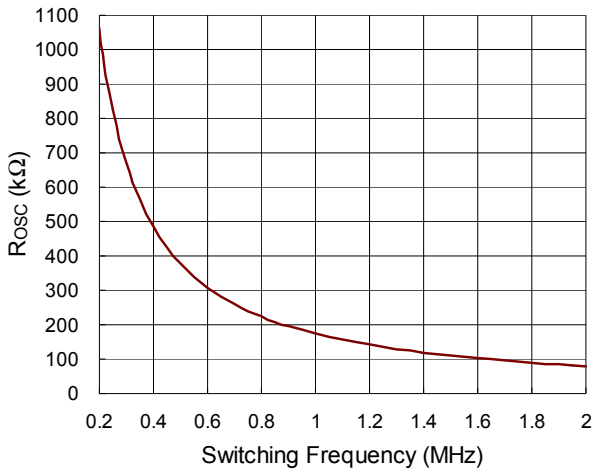

Figure 1. R_{OSC} vs. Switching Frequency

$$R_{OSC}(k\Omega) = 174 \times f^{-1.122}$$

For operation at 500kHz a 383kΩ resistor is required.

Generally, 500kHz switching frequency is a good value to achieve both small solution size and high efficiency operation. Higher frequency allows even smaller components, but the drawback is that it lowers system efficiency due to higher switch losses. Minimum on-time must also be considered : minimum duty cycle is given by $t_{ON(MIN)}$ x f_{SW}, so at higher frequency, very low output voltages may not be possible due to duty cycle limit. When increasing switching frequency, inductor value can be reduced in the same ratio, keeping current ripple constant. Higher frequency operation with smaller inductors will also require a lower value of compensation resistor.

Synchronization

The status of the SYNC pin will be ignored during start-up and the RT7273's control will only synchronize to an external signal after the PGOOD signal is asserted. The RT7273 can be easily synchronized to an external clock signal by applying a 200kHz to 2.2MHz square-wave signal to the SYNC input. After external synchronization is applied, the internal oscillator setting will be ignored. It can be higher or lower than the external clock signal. When synchronization is not applied, the SYNC pin should be connected to ground.

Out-of-Phase Operation

CH 1 has a low conduction resistance compared to CH 2 and 3. Normally CH 1 is used to drive higher system loads. CH 2 and 3 are used to drive some peripheral loads like I/O and line drivers. The combination of CH 2 and 3's loads may be on par with CH 1's. In order to reduce input ripple current, CH 2 operates in phase with CH 3; CH 1 and CH 2 operate 180 degrees out-of-phase as shown in Figure 2. This enables the system to have less input ripple, lower component cost, save board space and reduce EMI.

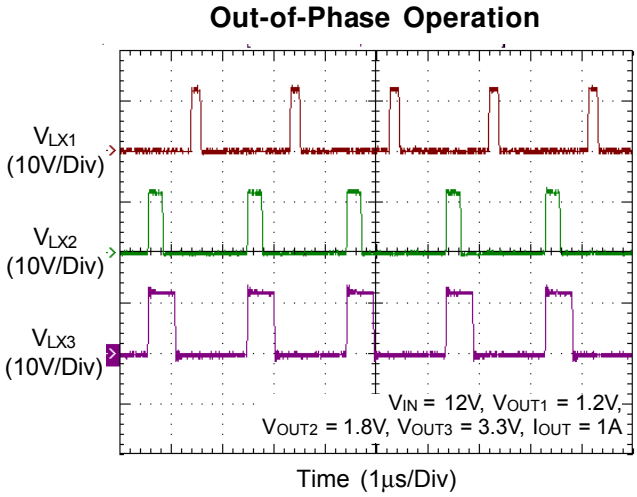

Figure 2. Switching Signals for Each Channel

Soft-Start Time

The device has an internal pull-up current source of 6μA that charges an external slow start capacitor to implement a slow start time. The equation shows how to select a slow-start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8V and the slow start charge current (I_{SS}) is 6μA. The soft-start circuit requires 1nF per 133μs to be connected at the SS pin. A 0.625ms soft-start time is implemented for all converters fitting 4.7nF to the relevant pins.

$$T_{SS}\ (ms) = V_{REF}\ (V) \times \frac{C_{SS}\ (nF)}{I_{SS}\ (\mu A)}$$

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Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin as shown in Figure 3. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with 40.2kΩ for the R1 resistor and use the equation to calculate R2.

$$R2 = R1 \times \left(\frac{0.8V}{V_{OUT} - 0.8V}\right)$$

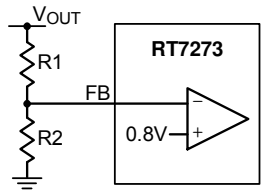

Figure 3. Voltage Divider Circuit

Bootstrap Capacitor

The device adopts three bootstrap power supply with a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1μF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Output Capacitor Selection

For the output capacitors, ceramic capacitors are recommended due to their small size and low ESR. Recommended output capacitance for all Buck channels is 44μF (two 22μF ceramic capacitors in parallel) which provides sufficiently low voltage ripple for most applications. When using different output capacitance, it is important to realize that system stability will be influenced. As a general guideline, when reducing output capacitance of a certain channel, the compensation resistor of that channel must be reduced in same ratio to maintain stable operation. As an example, when using 22μF instead of 44μF output capacitance for CH 1, the compensation resistor R5 must be reduced from 20kΩ to 10kΩ.

Power Good

The PGOOD pin is an open-drain output. The PGOOD pin is pulled low when any Buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all three Buck converters' outputs are more than 90% of its nominal output voltage and reset time of 1 second elapses.

Over-Current Limit

The RT7273 current limit trip is set as shown in Figure 4 and Figure 5.

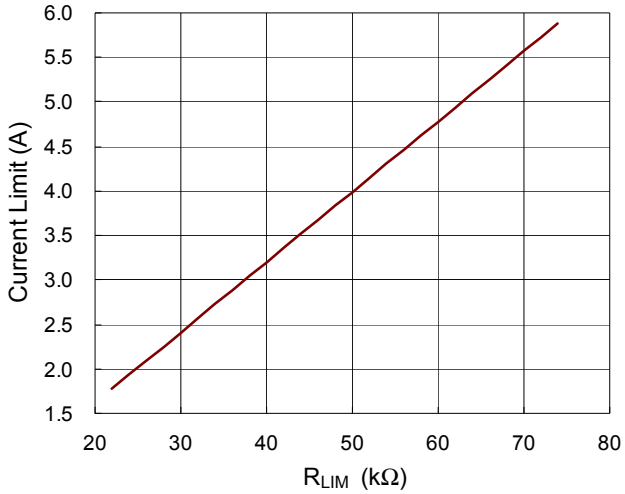

Figure 4. Channel 1 Current Limit vs. R_{LIM}

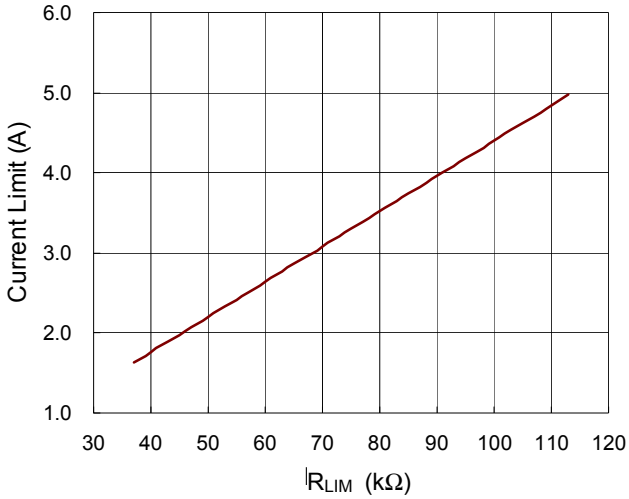

Figure 5. Channel 2 and Channel 3 Current Limit vs. R_{LIM}

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The current limit value set by the R_{LIM} resistors refers to the peak current in the inductor. Output load current is the average value of the inductor current. So when setting a current limit of a Buck channel to meet a certain max load requirement, the current limit must be set sufficiently high to include at least 50% of the inductor current ripple and 15% tolerance on the current limit.

Example : CH 1, 12V input, 1.2V output and 500kHz application, using 4.7μH inductor, and max load current is 3.1A.

Inductor ripple current = $\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$ = 0.46A , so half of the ripple = 0.23A

Max inductor peak current = 3.1 + 0.23 = 3.33A

Current limit should be at least 15% higher than 3.33A, so I_{LIM} = 4A is recommended. According to Figure 4, a 50kΩ resistor R_{LIM} is required.

All converters operate in hiccup mode under voltage protection. When an over-current or short circuit occurs lasting more than 10ms in any of the converters, all converters will be disable for 10ms. Once hiccup mode off time elapses, the start-up sequence will be tried again. A normal start-up will resume as soon as the overload or short circuit is removed. If any of the converters sees another over-current or short circuit event, the hiccup mode protection will be triggered until the failure is cleared.

No global hiccup mode will occur if an over-current or short circuit event occurs less than 10ms. Only the relevant converter affected will be protected by the cycle-by-cycle current limit during the event.

Power Sequence via Capacitor on Enable Pins

Connecting a capacitor to the EN pin of a channel will add a start-up delay for this channel. A specific start-up power sequence of Channel 1/2/3 can be achieved by using different values of capacitors on the EN1/EN2/EN3 pins. The channel start-up delay is around 1.4ms per nF capacitance on the EN pin.

Power Dissipation

For recommended operating condition specifications, the maximum junction temperature inside RT7273 is 125°C. The maximum power dissipation depends on the thermal resistance of the IC package and the PCB layout, the rate of surrounding airflow and the ambient temperature.

The following procedure can be used to calculate the junction temperature of RT7273 under continuous loading at switching frequency of 500kHz.

- Define the desired output and input voltage for each converter.
- Define the maximum continuous loading on each converter, not exceeding the maximum continuous loading.
- Find the expected losses (W) in each converter inside the RT7273 from the graphs below.

  The losses depend on the input supply, output voltage, switching frequency and the chosen converter.
- The junction temperature inside the RT7273 can be calculated by the following formula:

  $T_J = T_A + P_D \times \theta_{JA}$

where T_J is the junction temperature, T_A is the ambient temperature, P_D is the sum of losses in all converters and θ_{JA} is the junction to ambient thermal resistance.

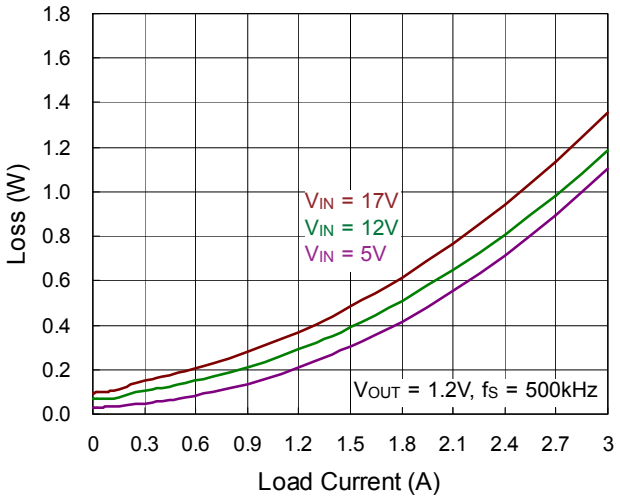

Figure 6. Channel 1 Loss vs. Load Current

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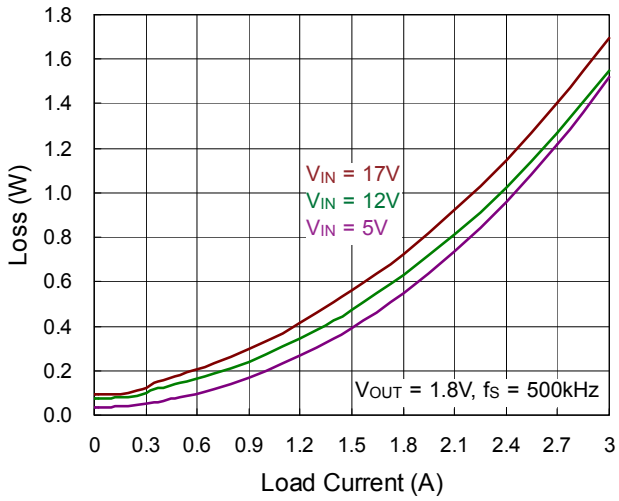

Figure 7. Channel 2 Loss vs. Load Current

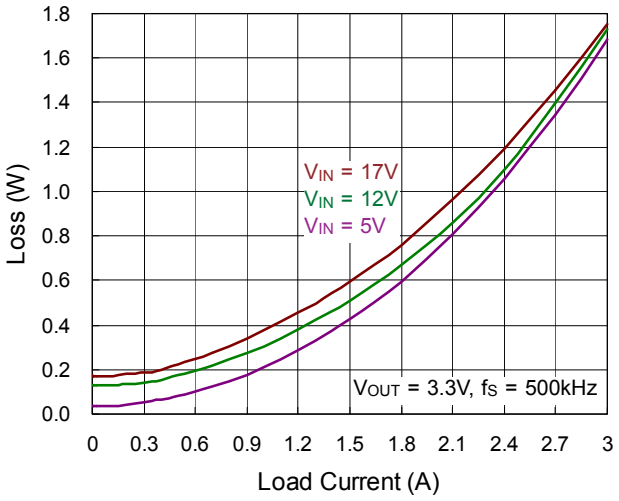

Figure 8. Channel 3 Loss vs. Load Current

Thermal Shutdown

The RT7273 includes an over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by 20°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C . The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 6x6 package, the thermal resistance, θ_{JA}, is 28.4°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.4°C/W) = 3.52W for WQFN-40L 6x6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

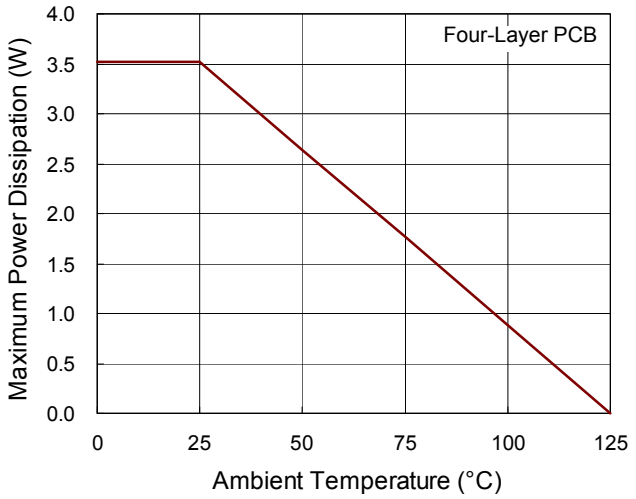

Figure 9. Derating Curve of Maximum Power Dissipation

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Layout Consideration

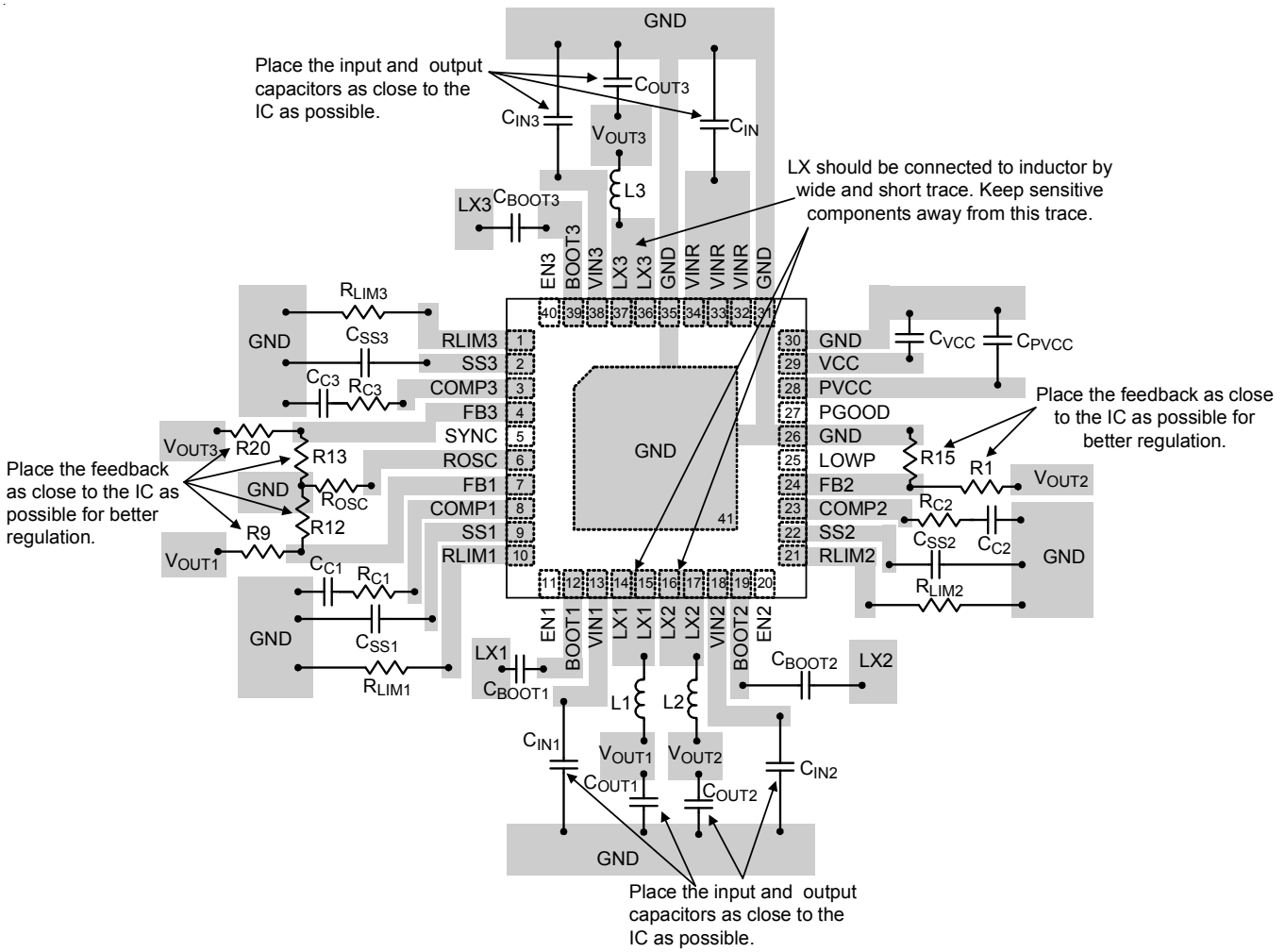

Figure 10. PCB Layout Guide

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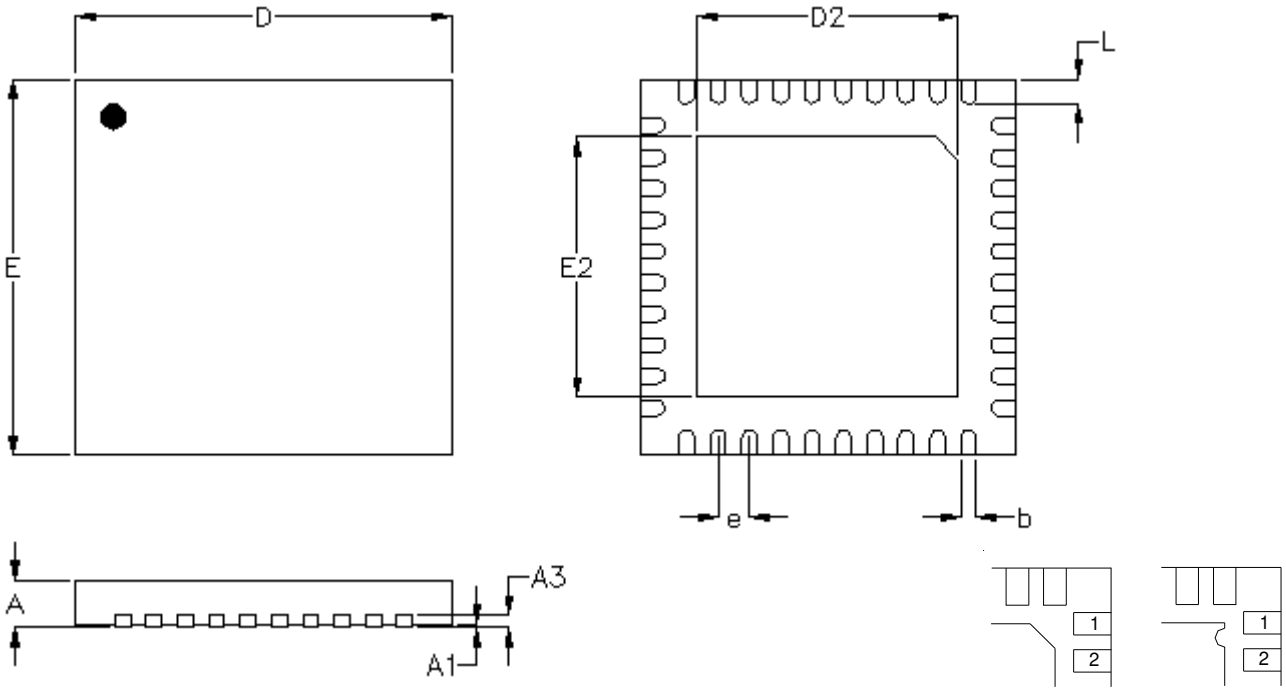
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		5.950	6.050	0.234	0.238
D2	Option1	4.000	4.750	0.157	0.187
	Option2	3.470	3.570	0.137	0.141
E		5.950	6.050	0.234	0.238
E2	Option1	4.000	4.750	0.157	0.187
	Option2	2.570	2.670	0.101	0.105
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 40L QFN 6x6 Package

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