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CCG3PA-NFET

USB Type-C Port Controller

General Description

EZ-PD™ CCG3PA-NFET is Cypress' highly integrated USB Type-C port controller with NFET-Gate driver that complies with the latest USB Type-C and PD standards and is targeted for Power adapters. CCG3PA-NFET provides additional functionalities and BOM integration advantages. CCG3PA-NFET uses Cypress' proprietary M0S8 technology with a complete Type-C USB-PD transceiver, all termination resistors required for a Type-C port, VBUS NFET gate driver and an integrated feedback control circuitry for voltage (VBUS) regulation. It is available in 24-pin QFN package.

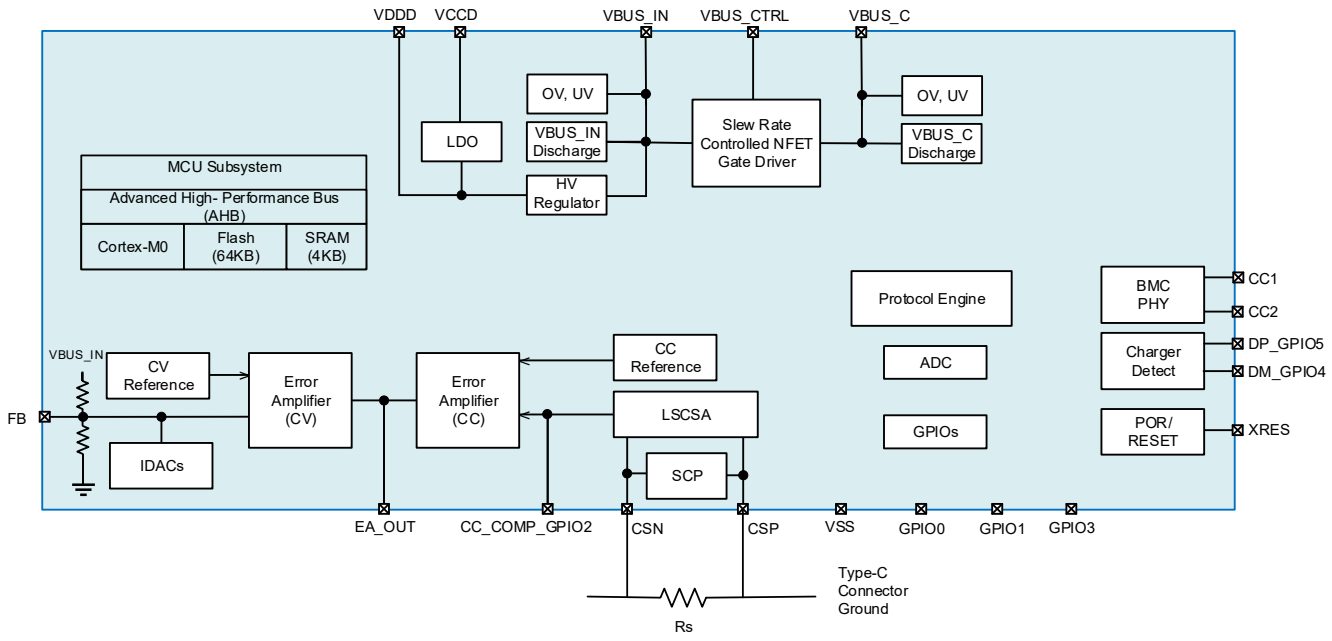
Applications

- USB PD 3.0 PPS Power Adapter[1]
- Quick Charge 4.0 Power Adapter
- Power adapters supporting both USB PD and legacy charging

Features

- Supports one USB Type-C port
- Supports USB PD2.0, PD3.0 with PPS, QC4+, QC4.0, QC3.0, QC2.0, Samsung AFC, Apple charging and BC v1.2 charging protocols
- Configurable overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), short circuit protection (SCP), and over-temperature protection (OTP)
- Integrates all termination on DP/DM lines, low-side current sense amplifier (LSCSA), 2 x VBUS discharge FETs, and a NFET gate driver to drive the load switch
- Analog regulation of secondary side feedback node (direct feedback or opto coupler)
- Supports independent constant current (CC) and constant voltage (CV) modes of operation
- Protects against accidental VBUS to CC short
- 6 GPIOs for independent functionality
- 24-QFN package with –40 °C to +105 °C extended industrial temperature range

Functional Block Diagram



Note
1. PPS supported for Opto-based feedback architecture.

Contents

Pinout

Figure 1. 24-Pin QFN Pin Map

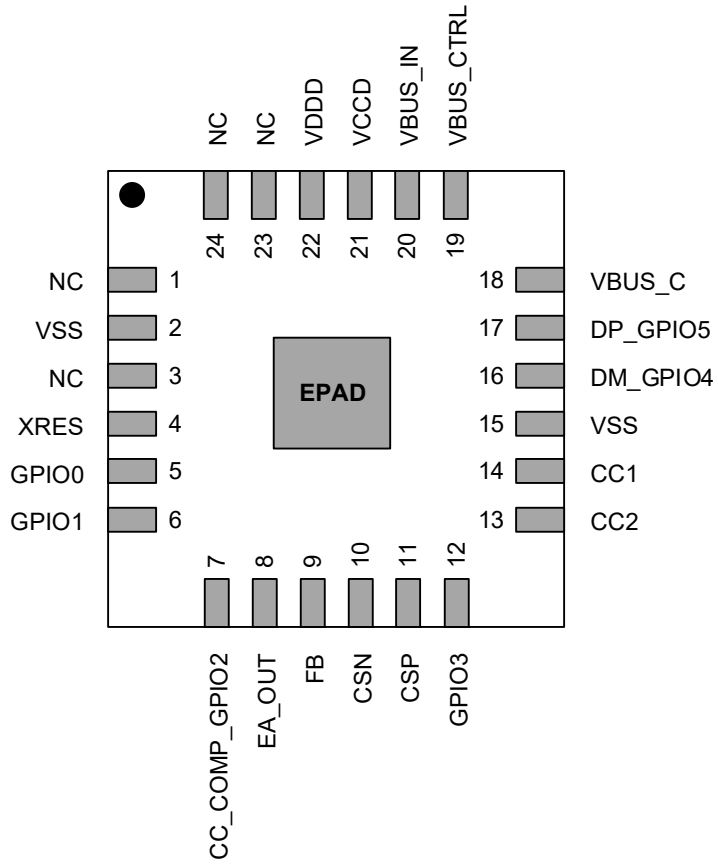


Table 1. CCG3PA-NFET Pin Description

Pin Number	Pin Name	Description
1	NC	No Connect
2	VSS	Ground
3	NC	No Connect
4	XRES	External reset input
5	GPIO0	GPIO P0.0
6	GPIO1	GPIO P0.1
7	CC_COMP_GPIO2	Pin for constant current mode compensation capacitor/GPIO P0.2
8	EA_OUT	Error amplifier output
9	FB	Error amplifier feedback
10	CSN	Low-side current sense amplifier negative input
11	CSP	Low-side current sense amplifier positive input
12	GPIO3	GPIO P0.3
13	CC2	Power delivery Communication Channel 2
14	CC1	Power delivery Communication Channel 1
15	VSS	Ground
16	DM_GPIO4	USB D-/SWD_DATA/GPIO P0.4
17	DP_GPIO5	USB D+/SWD_CLK/GPIO P0.5
18	VBUS_C	USB Type-C VBUS monitor input
19	VBUS_CTRL	Load switch NFET gate control
20	VBUS_IN	Power source input
21	VCCD	1.8-V core voltage LDO output
22	VDDD	3.0 V–5.5 V internal LDO Output
23	NC	No Connect
24	NC	No Connect
25	EPAD	EPAD for ground

Pin Description

FB, EA_OUT, CC_COMP_GPIO2

CCG3PA-NFET integrates two error amplifier blocks which handles secondary output sensing and regulation for CV and CC modes. This block is responsible for both constant voltage and constant current operations. The output of the error amplifier is routed to the EA_OUT pin. EA_OUT can further drive an opto-isolator to provide feedback to the primary controller. The negative input of the error amplifier is the feedback (FB) pin and the positive input is internal reference of 0.744 V. The FB pin has internal resistor divider of 200 kΩ and 35 kΩ, this divider sets a default voltage of 0.744 V at FB pin when VBUS_IN is at 5 V. Based on the desired VBUS_C output, the voltage at the FB pin will be varied using internal current source/sink IDACs. An external compensation network is required between FB pin and EA_OUT pin, as shown in Figure 2.

Constant current operation makes use of an internal LSCSA, the output of which feeds into an independent error amplifier as shown in Figure 2. CCG3PA-NFET error amplifier can ensure constant voltage regulation over 3.3 V to 21 V range and constant current regulation over 1 A to 3 A as required by the USB-PD PPS specification.

CC1, CC2

CC1 and CC2 are the communication channels for USB PD protocol. CCG3PA-NFET integrates a USB PD transceiver consisting of a transmitter and receiver that communicate Biphase Mark Code (BMC) encoded data over the Configuration Channel (CC) channels as per the USB-PD standard. All communication is half-duplex. The physical layer implements collision avoidance to minimize communication errors on the channel. This block includes all termination resistors (Rp) and their switches as required by the USB-PD specification. An external 390-pF capacitor is required on both the CC1 and CC2 pins.

DP_GPIO4, DM_GPIO5

The DP and DM lines are the standard USB D+ and D- lines. CCG3PA-NFET integrates a charge detect block, which handles legacy charging protocols such as BC 1.2, Quick Charge, Apple charging, and Samsung AFC. This block integrates all the terminations required for these charging protocols and no external components are required. When legacy charging is not required in the system, the same DP and DM lines can be reused as standard GPIOs.

VBUS_IN, VDDD, VCCD

CCG3PA-NFET integrates a high-voltage regulator, which is powered from the VBUS_IN rail, the output of the regulator powers the VDDD rail. The input to the regulator can range from 3.3 V minimum to 21.5 V maximum. When the input is between 5.5 V to 21.5 V, the typical output of the regulator is 5 V. For inputs from 3.3 V to 5.5 V, the regulator output is VBUS_IN – 300 mV.

The regulator can drive a maximum load current of 50 mA, which includes the chip current consumption. This regulator is not expected to drive any external loads or ICs. CCG3PA-NFET also has an internal configurable discharge path for the VBUS_IN rail, which is used to discharge the VBUS rail during negative voltage transitions.

The regulated supply VDDD, is either used to directly power some internal analog blocks or further regulated down to 1.8 V VCCD, which powers majority of the core. VDDD and VCCD is brought out on to pins to connect external capacitors for regulator stability, these are not meant to be used as power supplies.

VBUS_C, VBUS_CTRL

VBUS_C is used to monitor the voltage at the Type-C connector. VBUS_C has an internal configurable discharge path, which is used to discharge the VBUS_C rail during negative voltage transitions.

The load switch is between VBUS_IN and VBUS_C. CCG3PA-NFET integrates a NFET gate driver to control this load switch. VBUS_CTRL is the output of this gate driver. To turn off the external NFET, the gate driver drives low. To turn on the external NFET, it drives the gate to VBUS_IN + 8 V. In addition, there is a clamp circuit to limit the gate to VBUS_IN + 8 V.

CSP, CSN

CCG3PA-NFET integrates a LSCSA to monitor the load current. CSP is the positive input pin for the LSCSA and CSN is the negative input. LSCSA offers wide gain options ranging from 5 to 150. Suggested Rsense for LSCSA is 5 mΩ. LSCSA has an active offset cancellation mechanism to improve accuracy.

GPIO0, GPIO1, and GPIO3

CCG3PA-NFET has six GPIOs, out of which three are dedicated GPIOs and the rest are multiplexed with other functionalities. During power-on and reset, the I/O pins (except GPIO1) are forced to the tristate so as not to crowbar any inputs and/or cause excess turn-on current. GPIO1 is driven to zero at power-up.

XRES

The XRES pin can be used to initiate a reset, this pin is internally pulled high and needs to be pulled low externally to trigger reset.

Application Diagram

Figure 2 shows the application diagram of CCG3PA-NFET-based Power Adapter with Opto-Coupler Feedback control using 24-pin QFN device. In an opto-feedback power adapter, CCG3PA-NFET implements an independent error amplifier for constant voltage (CV) mode and an independent error amplifier for constant current (CC) mode. The feedback to the primary controller is through an opto-coupler. The current drawn through the EA_OUT pin is proportional to the potential difference between FB pin and the internal CV reference voltage for CV mode and between CC_COMP pin and the internal CC reference voltage for CC mode.

For CV mode, if VBUS needs to be changed from default 5 V, using internal IDACs and an CV error amplifier, CCG3PA-NFET draws a proportional current through the EA_OUT pin. This in turn gets coupled to the primary controller through the opto-coupler.

For CC mode, in order to keep current at the certain level, using internal IDACs and an CC error amplifier, CCG3PA-NFET draws a proportional current through the EA_OUT pin to change the voltage output. This in turn gets coupled to the primary controller through the opto-coupler.

Figure 2. CCG3PA-NFET Based Power Adapter Application Diagram with Opto Coupler Feedback Control (24-pin QFN Device)

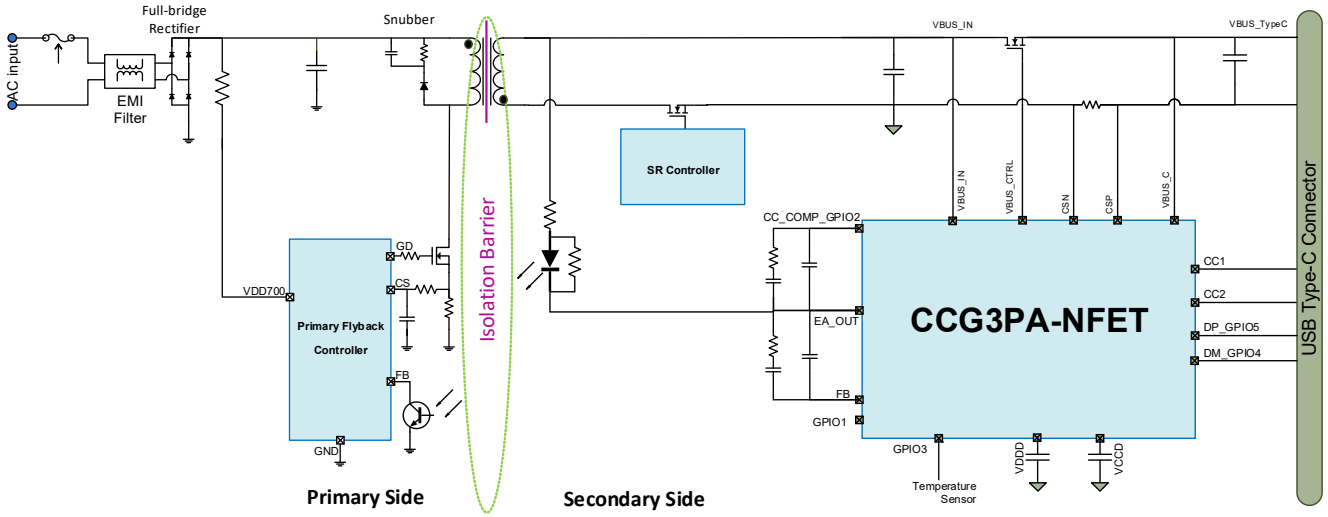
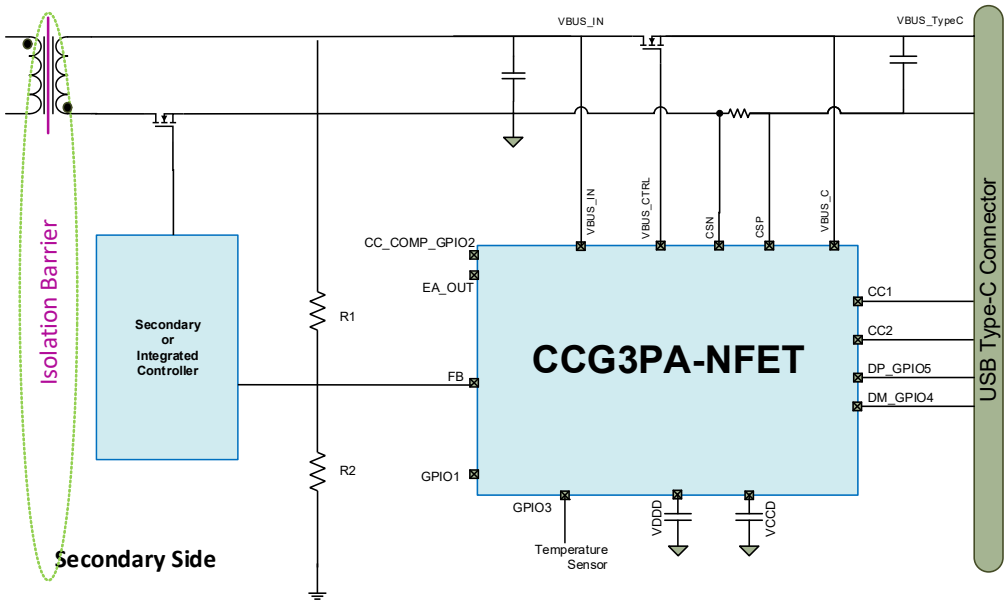


Figure 3 shows the application diagram of CCG3PA-NFET based power adapter with Direct Feedback control. In this application, VBUS is maintained at a constant voltage. The default value of VBUS upon power up (which is usually at 5 V) is set up by choosing the appropriate resistor divider that will set the FB node at a voltage expected by the secondary controller.

Feedback node is regulated using internal IDACs. Whenever a change in VBUS voltage is needed, CCG3PA-NFET will either source or sink a proportional current at feedback node, based on the amount of voltage change needed.

Figure 3. CCG3PA-NFET Based Power Adapter Application Diagram with Direct Feedback Control



Functional Description

MCU Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3PA-NFET is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG3PA-NFET has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3PA-NFET device has a flash module with one bank of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

SROM

A supervisory ROM that contains boot and configuration routines

Fault Protection

VBUS UVP and OVP

VBUS undervoltage and overvoltage faults are monitored using internal VBUS_IN/VBUS_C resistor dividers. The fault thresholds and response times are configurable in CCG3PA-NFET. Configurability includes choosing between auto-restart or latch-off options for each fault.

VBUS OCP and SCP

VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. Same as OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. Configurability includes choosing between auto-restart or latch-off options for each fault.

OTP

Over temperature monitoring is done using an external thermistor and internal ADC. The thermistor can be connected to GPIO3. Once the temperature exceeds the configured Over temperature limit, the USB-C port is disabled and the device waits for the temperature to drop below the set limit to re-enable the port. The corresponding temperature limits to report the error as well as recover from the error are user configurable. The user also has an option to enable or disable the Over temperature protection functionality.

ESD Protection

CCG3PA-NFET offers ESD protection on all the pins. The ESD protection level is 2.2 kV HBM and 500 V CDM.

VBUS to CC Short Protection

CCG3PA-NFET offers protection against accidental short from VBUS_C pin short to CC.

Power Modes

CCG3PA-NFET supports three power modes - Active, Sleep, and Deep Sleep. Transitions between these modes is handled by the device depending on the operating conditions.

CCG3PA-NFET Programming and Bootloading

CCG3PA-NFET is offered in two combinations:

1. A programmable version where the base Firmware for the device is available in EZ-PD CCGx Power Software Development
2. A preprogrammed version where the device is already programmed with a base Firmware. The customer however can configure selected parameters using EZ-PD™ Configuration Utility

There are two ways to program application firmware into a CCG3PA-NFET device:

1. Programming the Device Flash over SWD Interface (Programmable Version)

2. Application Firmware Update over CC Interface (Programmable Version)

The CCG3PA-NFET programmable devices are programmed over SWD interface during development or during the manufacturing process of the end product. Once the end product is manufactured, the application firmware can be updated via the CC bootloader interface.

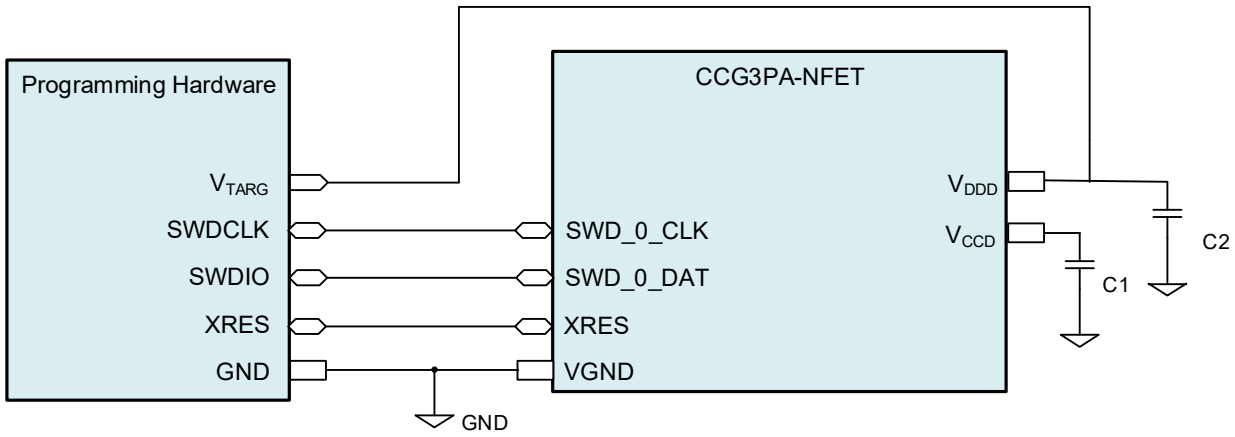
Programming the Device Flash over SWD Interface (Programmable Version)

CCG3PA-NFET family of devices can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3 and PSoC Programmer Software which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 4, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the CCG3PA-NFET device has to be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pin of CCG3PA-NFET device.

The CCG3PA-NFET device family has the XRES pin. it can programmed using Reset Mode if XRES is used. It can be programmed using Power Cycle mode if XRES is not used. Contact Cypress for further details on CYPD3XXX Programming Specifications.

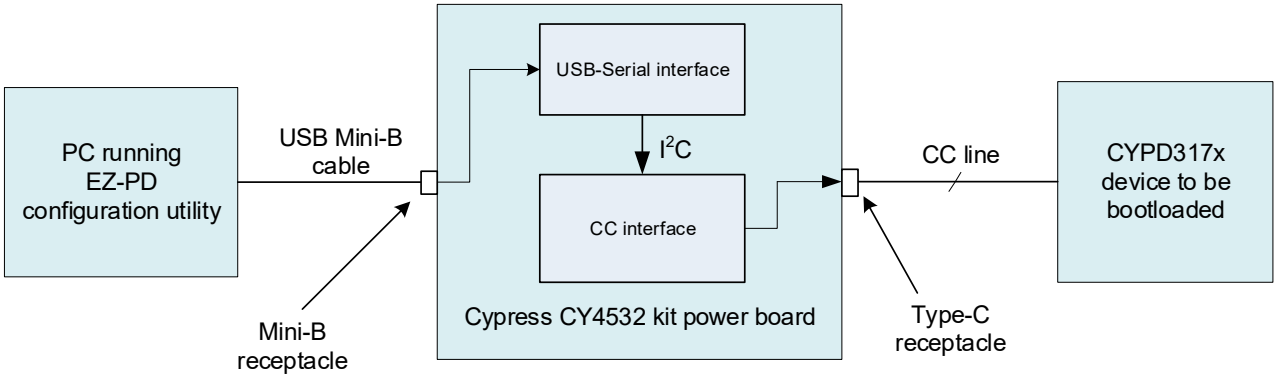
Figure 4. Connecting the Programmer to CYPD317X CCG3PA-NFET Device



Application Firmware Update over CC Interface (Programmable Version)

For bootloading CCG3PA-NFET applications, the CY4532 CCG3PA EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4532 CCG3PA EVK's Power Board is connected to the system containing CCG3PA-NFET device on one end and a Windows PC running the EZ-PD™ Configuration Utility as shown in Figure 5 on the other end to bootload the CCG3PA-NFET device.

Figure 5. Application Firmware Update over CC Interface



Application Firmware (FW) update feature over CC interface is intended for use during development and manufacturing. Cypress strongly recommends customers to use the EZ-PD Configuration Utility to turn off the Application FW Update over CC interface in the firmware that is updated into CCG3PA-NFET's flash before mass production. This prevents unauthorized firmware from being updated over CC-interface in the field. Refer to the knowledge base article KBA230192 on how to configure this in EZ-PD Configuration Utility.

If you desire to retain the Application Firmware update over CC interface feature post-production for on-field firmware updates, contact Cypress Sales for further guidelines.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[2]

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
$V_{BUS\_IN\_MAX}$	Maximum input supply voltage	–	–	24	V	–
V_{DDD_MAX}	Maximum supply voltage	–	–	6		–
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDD} + 0.5		–
$V_{CC\_PIN\_ABS}$	Maximum voltage on CC1, CC2 voltage	–	–	24		–
I_{GPIO_ABS}	Current per GPIO	–	–	25	mA	–
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
I_LU	Pin current for latch-up	–100	–	100	mA	–

Device-Level Specifications

Table 3. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR.1	V_{DDD_REG}	V_{DDD} output for 5.5 V ≤ V_{BUS_IN} ≤ 21.5 V	4.6	5.0	5.4	V	I_{LOAD} = 0-50 mA
SID.PWR.2	V_{DDD_MIN}	V_{DDD} output for 3.3 V ≤ V_{BUS_IN} ≤ 5.5 V	V_{BUS_IN} - 0.3	–	–		
SID.PWR.4	V_{BUS_IN}	Power supply input voltage	3.3	–	21.5		–
SID.PWR.6	V_{CCD}	Output voltage for core logic	–	1.8	–		–
SID.PWR.8	Cefc	Bypass capacitor for V_{CCD}	0.8	1	1.2	µF	X5R ceramic or better
SID.PWR.9	Cexc	Decoupling capacitor for V_{DDD}	1.8	–	4.7		
SID.PWR.10	Cexv	Decoupling capacitor for V_{BUS_IN}	–	1	–		Decoupling capacitor required near the IC pin.
SID.PWR.15	I_{DD_A}	Active current from V_{BUS_IN} in Type-C attached state	–	6.5	–	mA	V_{BUS_IN} = 5 V, T_A = 25 °C, CC1/CC2 in TX or RX (USB-PD communication is active)
SID.PWR.16	$I_{DD\_S\_UA}$	Sleep current from V_{BUS_IN} in Type-C attached state	–	2.5	–		V_{BUS_IN} = 5 V, T_A = 25 °C, Type-C attached, CPU OFF, PWM/EA/ADC/UVOV blocks ON. CC, Watchdog Timer (WDT) Wakeup ON
SID.PWR#16_A	$I_{\_DS\_UA}$	Deep Sleep current from V_{BUS_IN} (Type-C unattached)	–	0.75	–		V_{BUS_IN} = 5 V, T_A = 25 °C, Type-C unattached, CPU OFF, UVOV block ON, WDT Wakeup ON

Table 4. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR.14	Tsleep	Wakeup from Sleep mode	–	0	–	µs	–
SID.PWR.14A	Tdeepsleep	Wakeup from Deep Sleep mode	–	35	–	µs	–

Note

2. Usage of the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Functional Block Specifications

Table 5. ADC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral nonlinearity	–2.5	–	2.5	LSB	Reference voltage = VREF_ADC1
SYS.ADC.3	INL		–1.5	–	1.5		Reference voltage = VREF_ADC2
SYS.ADC.4	DNL	Differential nonlinearity	–2.5	–	2.5		Reference voltage = VREF_ADC1
SYS.ADC.5	DNL		–1.5	–	1.5		Reference voltage = VREF_ADC2
SYS.ADC.6	Gain Error	Gain error	–1.5	–	1.5		–
SYS.ADC.7	VREF_ADC1	ADC reference voltage	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SYS.ADC.8	VREF_ADC2		1.96	2.0	2.04		Reference voltage generate from bandgap
AC Specifications							
SID.ADC.9	Slew_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	Guaranteed by design

Table 6. Error Amplifier

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.DC.VR.1	V_R	VBUS voltage regulation accuracy	–	± 3	± 5	%	–
SID.DC.VR.2	Ika_off	Off-state EA_OUT current	–	2.2	10	µA	–
SID.DC.VR.3	Ika_on	Current through EA_OUT pin when in Sink mode for optocoupler application	–	–	5	mA	–
SID.DC.VR.4	DNL_ndac	Differential nonlinearity of NMOS DAC	–1	–	1	LSB	–
SID.DC.VR.5	INL_ndac	Integral nonlinearity of NMOS DAC	–1.5	–	1.5		–
SID.DC.VR.6	Gain_error_ndac	Gain error of NMOS DAC	–8	–	8	%	–
SID.DC.VR.7	DNL_pdac	Differential nonlinearity of PMOS DAC	–0.5	–	0.5	LSB	–
SID.DC.VR.8	INL_pdac	Integral nonlinearity of PMOS DAC	–1	–	1		–
SID.DC.VR.9	Gain_error_pdac	Gain error of PMOS DAC	–8	–	8	%	–

Table 7. LSCSA, SCP

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.LSCSA.1	Cin_inp	CSP input capacitance	–	–	10	pF	–
SID.LSCSA.2	Csa_Acc1	CSA accuracy with 5 mV < Vsense < 10 mV	–15	–	15	%	–
SID.LSCSA.3	Csa_Acc2	CSA accuracy with 10 mV < Vsense < 15 mV	–10	–	10		–
SID.LSCSA.4	Csa_Acc3	CSA accuracy with 15 mV < Vsense	–5	–	5		–
SID.LSCSA.5	SCP_6A	Short circuit trip point with threshold set to 6A	5.4	6	6.6	A	Rsense = 5 mΩ
SID.LSCSA.6	SCP_10A	Short circuit trip point with threshold set to 10A	9	10	11		
SID.LSCSA.8	Av	CSA gain values supported: 5,10, 20, 35, 50, 75, 125, 150	5	–	150		–
AC Specifications							
SID.LSCSA.AC.1	Tocp_gate	Delay from OCP threshold trip to external NFET gate turn off	–	4	20	µs	–
SID.LSCSA.AC.2	Tscp_gate	Delay from SCP threshold trip to external NFET gate turn off	–	3.1	–		1 nF NFET gate capacitance
SID.LSCSA.AC.3	Tscp_gate_1	Delay from SCP threshold trip to external NFET power gate turn off	–	7.5	–		3 nF NFET gate capacitance

Table 8. VBUS UV, OV

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.UVOV.1	VTHOV1	Over-Voltage threshold Accuracy, 4 V to 11 V	–3	–	3	%	–
SID.UVOV.2	VTHOV2	Over-Voltage threshold Accuracy, 11 V to 21.5 V	–3.2	–	3.2		–
SID.UVOV.3	VTHUV1	Under-Voltage threshold Accuracy, 3 V to 3.3 V	–4	–	4		–
SID.UVOV.4	VTHUV2	Under-Voltage threshold Accuracy, 3.3 V to 4.0 V	–3.5	–	3.5		–
SID.UVOV.5	VTHUV3	Under-Voltage threshold Accuracy, 4.0 V to 11 V	–3	–	3		–
SID.UVOV.6	VTHUV4	Under-Voltage threshold Accuracy, 11 V to 21.5 V	–2.9	–	2.9		–
AC Specifications							
SID.UVOV.AC.1	Tov_gate	Delay from OV threshold trip to external NFET Power Gate Turn off	–	–	50	µs	–

Table 9. PD Transceiver

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.PD.1	Rp_std	Downstream facing port (DFP) CC termination for default USB power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5 A USB power	166	180	194		–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0 A USB power	304	330	356		–
SID.PD.4	Vgndoffset	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to remote BMC transmitter

Table 10. VBUS Discharge

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.VBUS.DISC.1	R1	20 V NMOS ON resistance for discharge strength = 1	500	–	2000	Ω	Measured at 0.5 V
SID.VBUS.DISC.2	R2	20 V NMOS ON resistance for discharge strength = 2	250	–	1000		
SID.VBUS.DISC.3	R4	20 V NMOS ON resistance for discharge strength = 4	125	–	500		
SID.VBUS.DISC.4	R8	20 V NMOS ON resistance for discharge strength = 8	62.5	–	250		
SID.VBUS.DISC.5	R16	20 V NMOS ON resistance for discharge strength = 16	31.25	–	125		
SID.VBUS.DISC.6	Vbus_stop_error	Error percentage of final VBUS value	–	–	10	%	When VBUS is discharged to 5 V

Table 11. VBUS NFET Gate Driver

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.GD.1	GD_VGS	Gate to Source overdrive during NFET ON condition	4.5	5.75	10	V	Vbus_in = 21.5 V
SID.GD.2	GD_Rpd	Resistance when pull-down is enabled to turn off external NFET	–	0.57	2	kΩ	–
AC Specifications							
AC.GD.1	Ton	V_{BUS_ctrl} Low to High (1 V to V_{BUS} + 1 V) with 3nF external capacitance	2	5	10	ms	V_{BUS_IN} = 5 V
AC.GD.2	Toff	V_{BUS_ctrl} High to Low (90% to 10%) with 3nF external capacitance	–	7	–	µs	V_{BUS_IN} = 21.5 V

Table 12. High-Voltage Regulator

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.VREG.1	VOLTAGE_DETECT	VBUS_IN voltage detect threshold	1.7	2.1	2.4	V	–
SID.VREG.2	Tstart	Total start-up time for the regulator supply outputs	–	50	200	µs	From VBUS reaching Voltage_detect level to 95% of final value

I/O Specifications

Table 13. I/O Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID.GIO.1	I_LU	Latch-up current limits	–140	–	140	mA	–
SID.GIO.2	RPU	Pull-up resistor value	3.5	5.6	8.5	kΩ	–
SID.GIO.3	RPD	Pull-down resistor value	3.5	5.6	8.5		–
SID.GIO.4	IIL	Input leakage current	–		2	nA	–
SID.GIO.5	CPIN_A	Max pin capacitance	–	7.8	22	pF	Capacitance on DP/DM lines
SID.GIO.6	CPIN		–	3	7		Capacitance on all GPIOs, except DP/DM lines
SID.GIO.7	Voh_3V	Output voltage high level	V_{DDD} – 0.6	–	–	V	Ioh = –4 mA
SID.GIO.8	Vol_3V	Output voltage low level	–	–	0.6		Iol = 10 mA
SID.GIO.9	Vih_CMOS	Input voltage high threshold	0.7 * V_{DDD}	–	–		–
SID.GIO.10	Vil_CMOS	Input voltage low threshold	–	–	0.3 * V_{DDD}		–
SID.GIO.11	Vih_TTL	LVTTL input	2	–			–
SID.GIO.12	Vil_TTL		–	–	0.8		–
SID.GIO.13	Vhysttl	Input hysteresis LVTTL	100	–	–	mV	–
SID.GIO.14	Vhyscmos	Input hysteresis CMOS	0.05 * V_{DDD}	–	–		–
SID.GIO.15	IDIODE	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 13. I/O Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO.16	TriseF	Rise time in fast strong mode	2	–	12	ns	Cload = 25 pF
SID.GIO.17	TfallF	Fall time in fast strong mode	2	–	12		
SID.GIO.18	TriseS	Rise time in slow strong mode	10	–	60		
SID.GIO.19	TfallS	Fall time in slow strong mode	10	–	60		
SID.GIO.20	FGPIO_OUT1	GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5 V; Fast strong mode.	–	–	16	MHz	
SID.GIO.21	FGPIO_OUT2	GPIO Fout; 3V ≤ V_{DDD} ≤ 5.5 V; Slow strong mode.	7	–	–		
SID.GIO.22	FGPIO_IN	GPIO input operating frequency; 3 V ≤ V_{DDD} ≤ 5.5 V	16	–	–		–

System Resources Specifications

Table 14. Power-On Reset (POR) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.POR.1	VRISEIPOR	POR rising trip voltage	0.8	–	1.5	V	–
SID.POR.2	VFALLIPOR	POR falling trip voltage	0.7	–	1.4		–
SID.POR.3	VFALLPPOR	Brown-out-detect (BOD) trip voltage active/ sleep modes	1.48	–	1.62		–

Table 15. Flash Macro Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.MEM#1	FLASH_ERASE	Row erase time	_	_	15.5	ms	-40 °C to +85 °C T_A, ALL VDDD
SID.MEM#2	FLASH_WRITE	Row (Block) write time (erase & program)	_	_	20		-40 °C to +85 °C T_A, ALL VDDD
SID.MEM#5	FLASH_ROW_PGM	Row program time after erase	_	_	7		25 °C to 55 °C, ALL VDDD
SID178	TBULKERASE	Bulk erase time (32k Bytes)	_	_	35		_
SID180	TDEVPROG	Total device program time	_	_	7.5	secs	_
SID182	FRET1	Flash retention, TA ≤ 55 °C, 100 K P/E cycles	20	_	_	years	_
SID182A	FRET2	Flash retention, TA ≤ 85 °C, 10 K P/E cycles	10	_	_		_
SID182A	FRET3	Flash retention, TA ≤ 105 °C, 10 K P/E cycles	3	_	_		_

Table 16. SWD Specifications

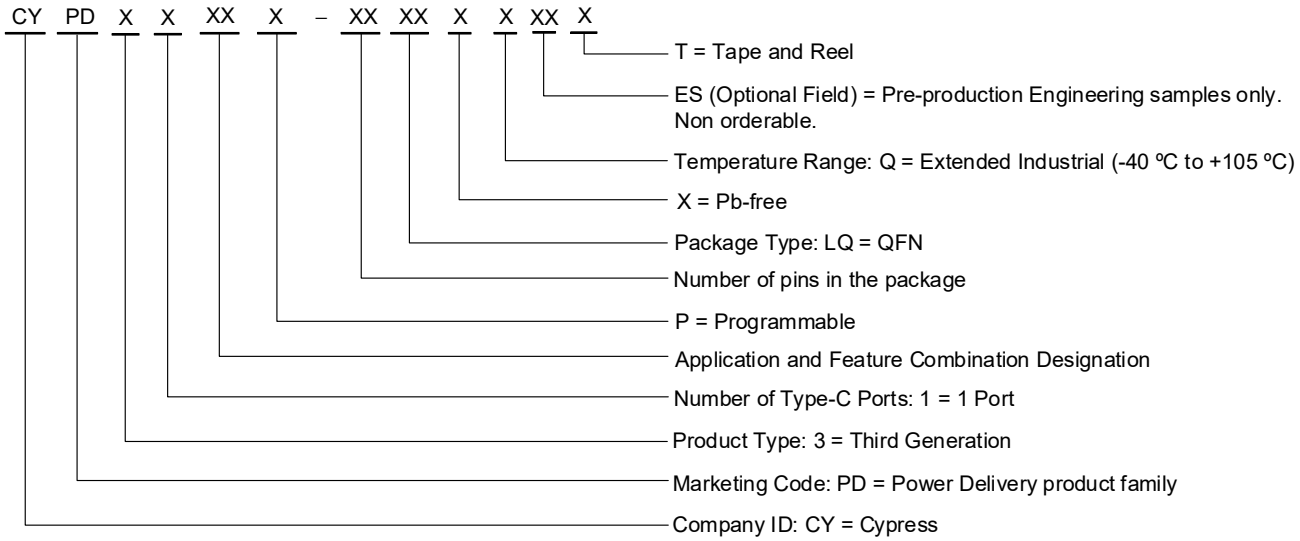
Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.SWD#1	F_swdclk1	3 V <= V_{DDD} <= 5.5 V	–	–	14	MHz	–
SID.SWD#2	T_swdi_setup	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID.SWD#3	T_swdi_hold	T = 1/f SWDCLK	0.25*T	–	–		–
SID.SWD#4	T_swdo_valid	T = 1/f SWDCLK	–	–	0.50*T		–
SID.SWD#5	T_swdo_hold	T = 1/f SWDCLK	1	–	–		–

Ordering Information

Table 17. CCG3PA-NFET Ordering Information

MPN	Application	Package Type	Si ID
CYPD3172-24LQXQ	Power Adapter based on Opto Coupler Feedback (Pre programmed)	24-Pin QFN	2B02
CYPD3172P-24LQXQ	Power Adapter based on Opto Coupler Feedback (Programmable)		2B03
CYPD3173-24LQXQ	Power Adapter based on Direct Feedback (Pre programmed)		2B04
CYPD3173P-24LQXQ	Power Adapter based on Direct Feedback (Programmable)		2B05

Ordering Code Definitions



Packaging

Table 18. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Extended Industrial	–40	25	105	°C
T_J	Operating junction temperature		–40	25	120	
T_{JA}	Package θ_{JA}	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC}		–	–	4.78	

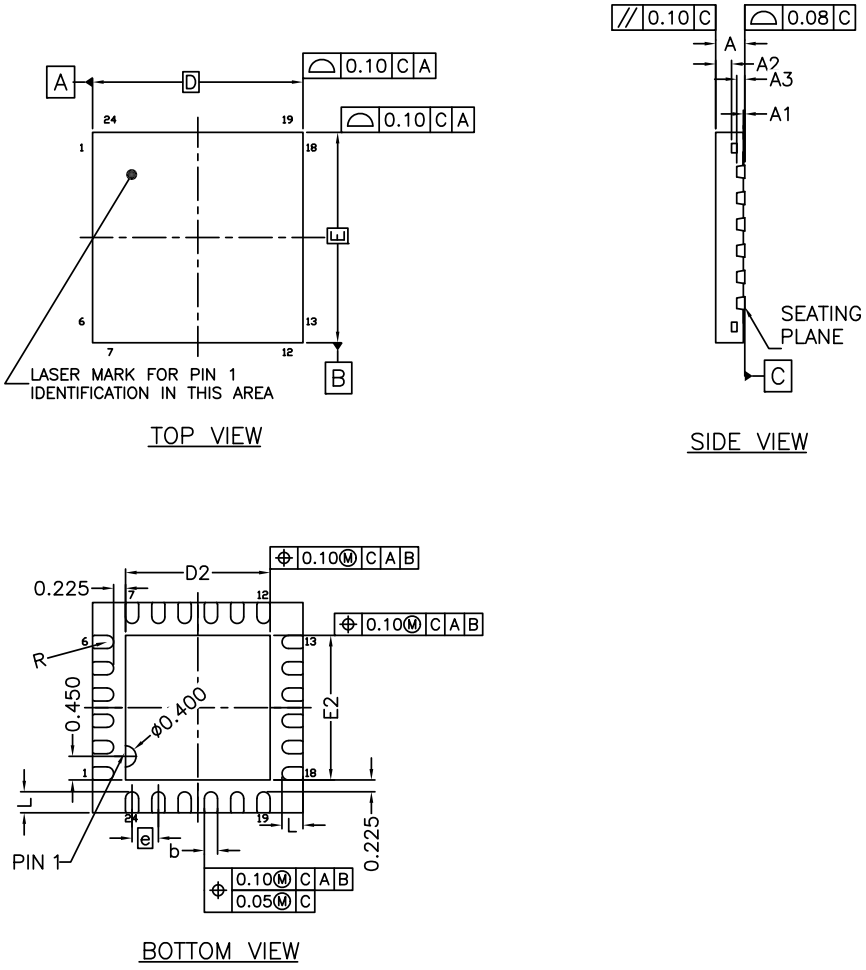
Table 19. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
24-pin QFN	260 °C	30 seconds

Table 20. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL 3

Figure 6. 24-pin QFN Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A_1	0.00	—	0.05
A_2	—	0.40	0.425
A_3	0.152 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D_2	2.65	2.75	2.85
E	4.00 BSC		
E_2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.

002-16934 *C

Acronyms

Table 21. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	constant current
CC	configuration channel
CV	constant voltage
BOD	Brown out Detect
BMC	biphase mark code
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CrCM	critical conduction mode
CS	current sense
DCM	discontinuous conduction mode
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LSCSA	low-side current sense amplifier
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt

Table 21. Acronyms Used in this Document *(continued)*

Acronym	Description
NMOS	N-type metal-oxide-semiconductor
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
OTP	over-temperature protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
PMOS	P-type metal-oxide-semiconductor
POR	power-on reset
PPS	programmable power supply
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SCP	short circuit protection
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SR	synchronous rectifier
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG5 pins used to connect to a USB port
UVP	undervoltage protection

Table 21. Acronyms Used in this Document *(continued)*

Acronym	Description
WDT	watchdog timer
USBIO	USB input/output, CCG5 pins used to connect to a USB port
XRES	external reset I/O pin
ZCD	zero crossing detect

Document Conventions

Units of Measure

Table 22. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Document Title: CCG3PA-NFET, USB Type-C Port Controller Document Number: 002-30172			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6890477	06/01/2020	Initial release.
*A	6960049	10/16/2020	Updated datasheet status from Advance to Final. Added Note [1] for USB PD 3.0 PPS Power Adapter in Applications. Updated text in OTP. Updated error amplifier constant voltage regulation from 21.5 V to 21 V in FB, EA_OUT, CC_COMP_GPIO2. Added text in Application Firmware Update over CC Interface (Programmable Version). Updated text in CCG3PA-NFET Programming and Bootloading. Updated Typ values and details/conditions for SID.PWR.15, SID.PWR.16, and SID.PWR#16_A in Table 3.

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