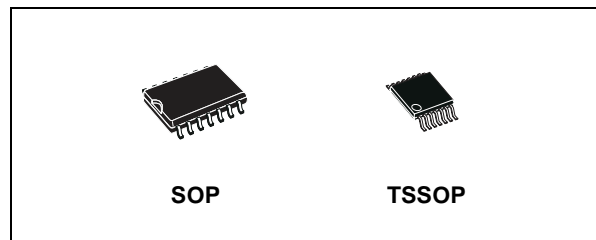




74LCX74

LOW VOLTAGE CMOS DUAL D-TYPE FLIP FLOP WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED :
 $f_{MAX} = 150 \text{ MHz (MAX.) at } V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA (MIN) at } V_{CC} = 3V$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2.0V \text{ to } 3.6V \text{ (1.5V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
 $HBM > 2000V \text{ (MIL STD 883 method 3015);}$
 $MM > 200V$



ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LCX74M	74LCX74MTR
TSSOP		74LCX74TTR

DESCRIPTION

The 74LCX74 is a low voltage CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

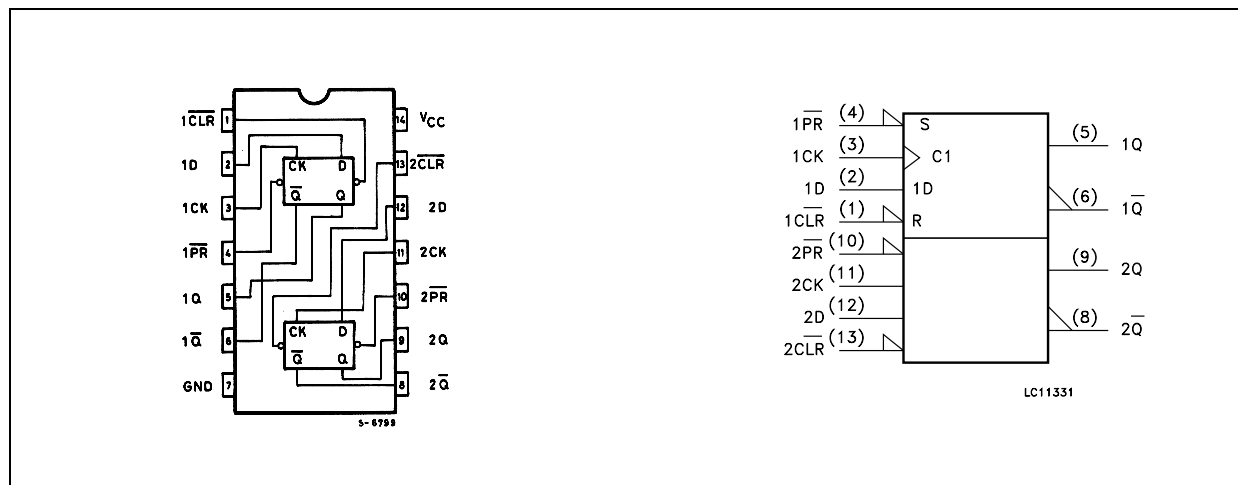
A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.

CLR and PR are independent of the clock and accomplished by a low setting on the appropriate input.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

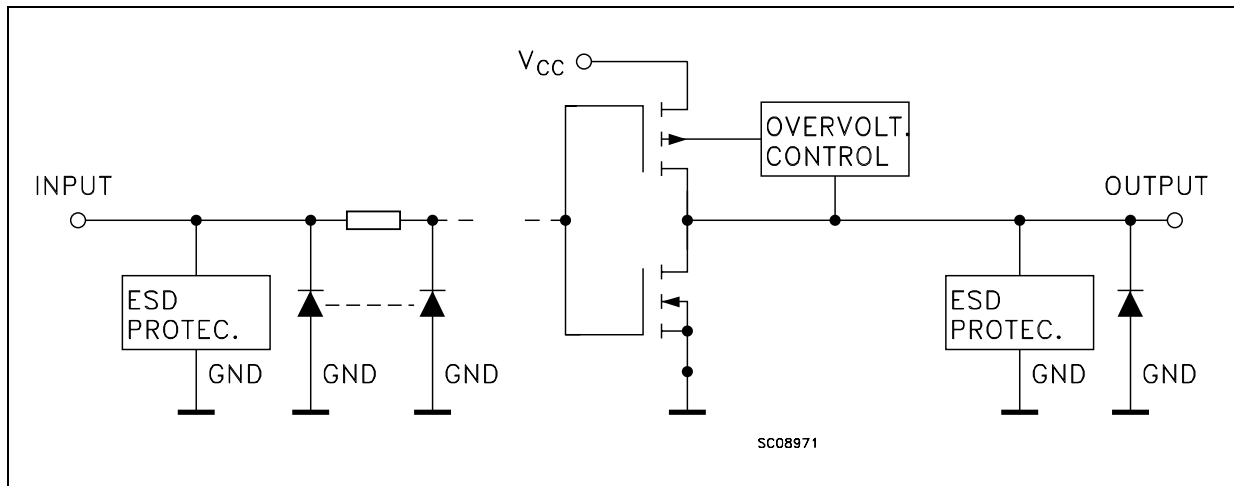
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



74LCX74

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	1CLR, 2CLR	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW to HIGH, Edge Triggered)
4, 10	1PR, 2PR	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	1Q, 2Q	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L		L	H	
H	H	H		H	L	
H	H	X		Q _n	$\overline{\text{Q}}_n$	NO CHANGE

X : Don't Care

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		V _{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
V _{IL}	Low Level Input Voltage					0.8		0.8
V _{OH}	High Level Output Voltage	2.7 to 3.6	I _O =-100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		2.7	I _O =-12 mA	2.2		2.2		
		3.0	I _O =-18 mA	2.4		2.4		
			I _O =-24 mA	2.2		2.2		
V _{OL}	Low Level Output Voltage	2.7 to 3.6	I _O =100 μA		0.2		0.2	V
		2.7	I _O =12 mA		0.4		0.4	
		3.0	I _O =16 mA		0.4		0.4	
			I _O =24 mA		0.55		0.55	
I _I	Input Leakage Current	2.7 to 3.6	V _I = 0 to 5.5V		± 5		± 5	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 5.5V		10		10	μA
I _{CC}	Quiescent Supply Current	2.7 to 3.6	V _I = V _{CC} or GND		10		10	μA
			V _I or V _O = 3.6 to 5.5V		± 10		± 10	
ΔI _{CC}	I _{CC} incr. per Input	2.7 to 3.6	V _{IH} = V _{CC} - 0.6V		500		500	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Level Quiet Output (note 1)	3.3	C _L = 50pF V _{IL} = 0V, V _{IH} = 3.3V		0.8		V
V _{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition				Value				Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time (CK to Q or Q̄)	2.7	50	500	2.5	1.5	8.0	1.5	9.2	ns
		3.0 to 3.6				1.5	7.0	1.5	8.0	
t _{PLH} t _{PHL}	Propagation Delay Time (PR or CLR to Q or Q̄)	2.7	50	500	2.5	1.5	8.0	1.5	9.2	ns
		3.0 to 3.6				1.5	7.0	1.5	8.0	
t _S	Setup Time, HIGH or LOW level D to CK	2.7	50	500	2.5	2.5		3.5		ns
		3.0 to 3.6				2.5		3.5		
t _H	Hold Time, HIGH or LOW level D to CK	2.7	50	500	2.5	1.5		1.5		ns
		3.0 to 3.6				1.5		1.5		
t _W	CK Pulse Width, HIGH or LOW PR or CLR Pulse Width, LOW	2.7	50	500	2.5	3.0		4.0		ns
		3.0 to 3.6				3.0		4.0		
t _{rec}	Recovery Time PR or CLR to CK	2.7	50	500	2.5	0		0		ns
		3.0 to 3.6				0		0		
f _{MAX}	Clock Pulse Frequency	2.7	50	500	2.5	150		150		MHz
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

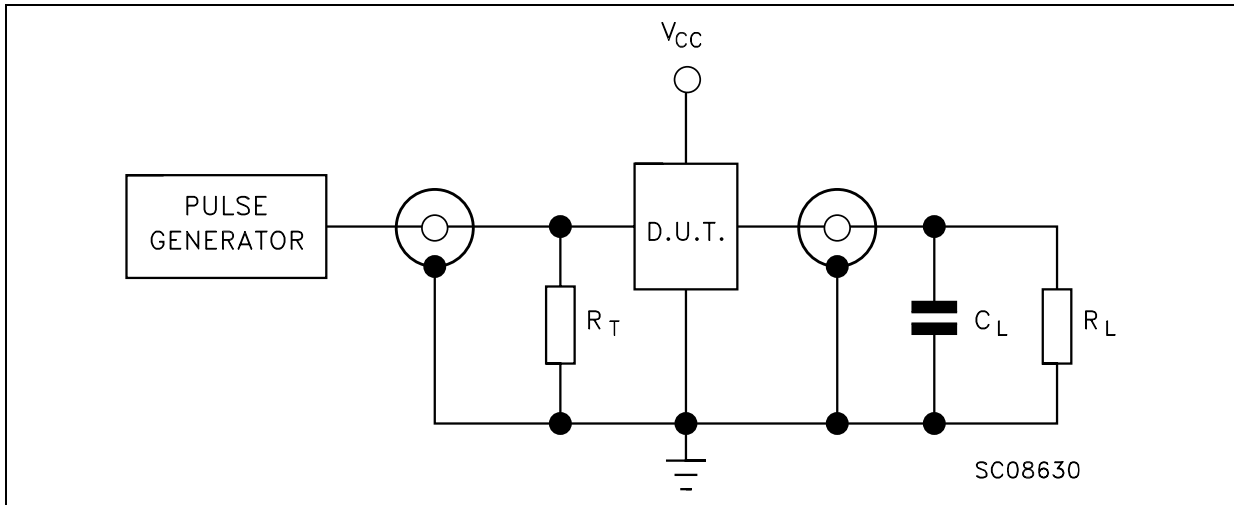
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance	3.3	V _{IN} = 0 to V _{CC}		6		pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10MHz V _{IN} = 0 or V _{CC}		40		pF

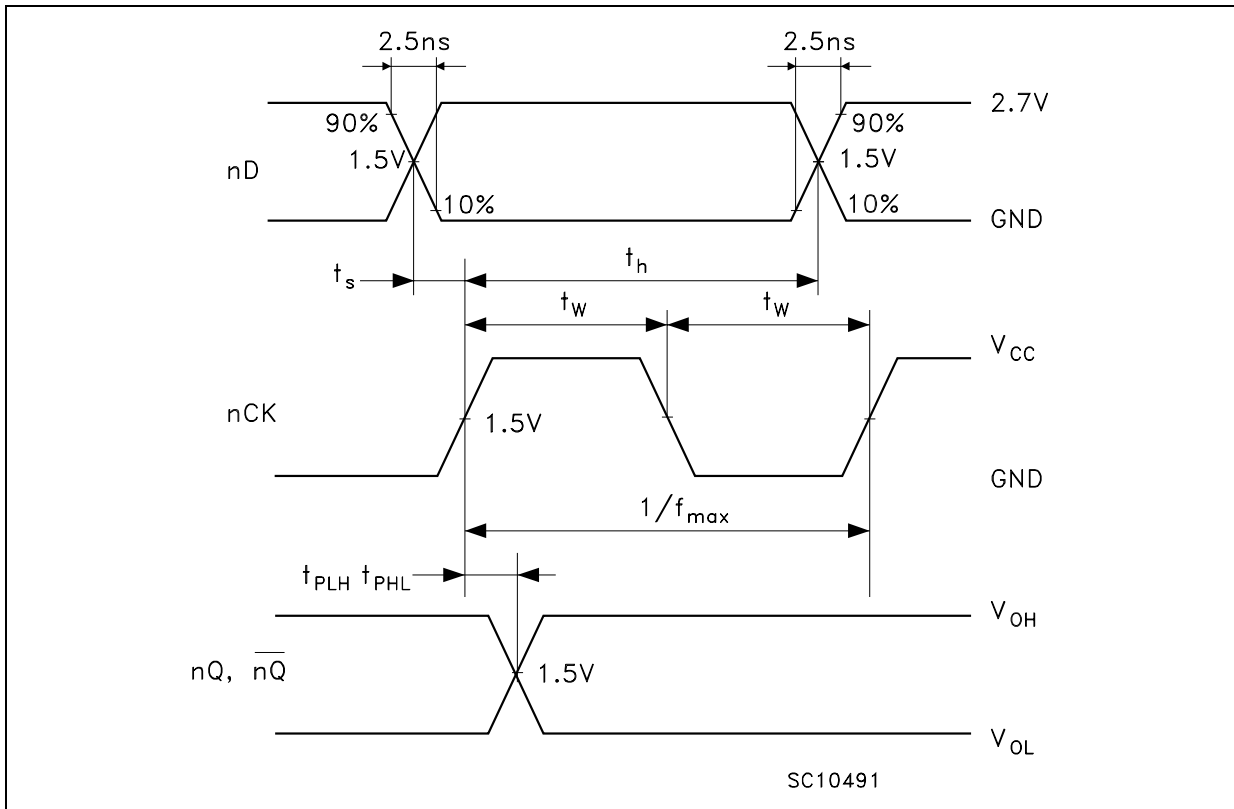
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per Flip-Flop)

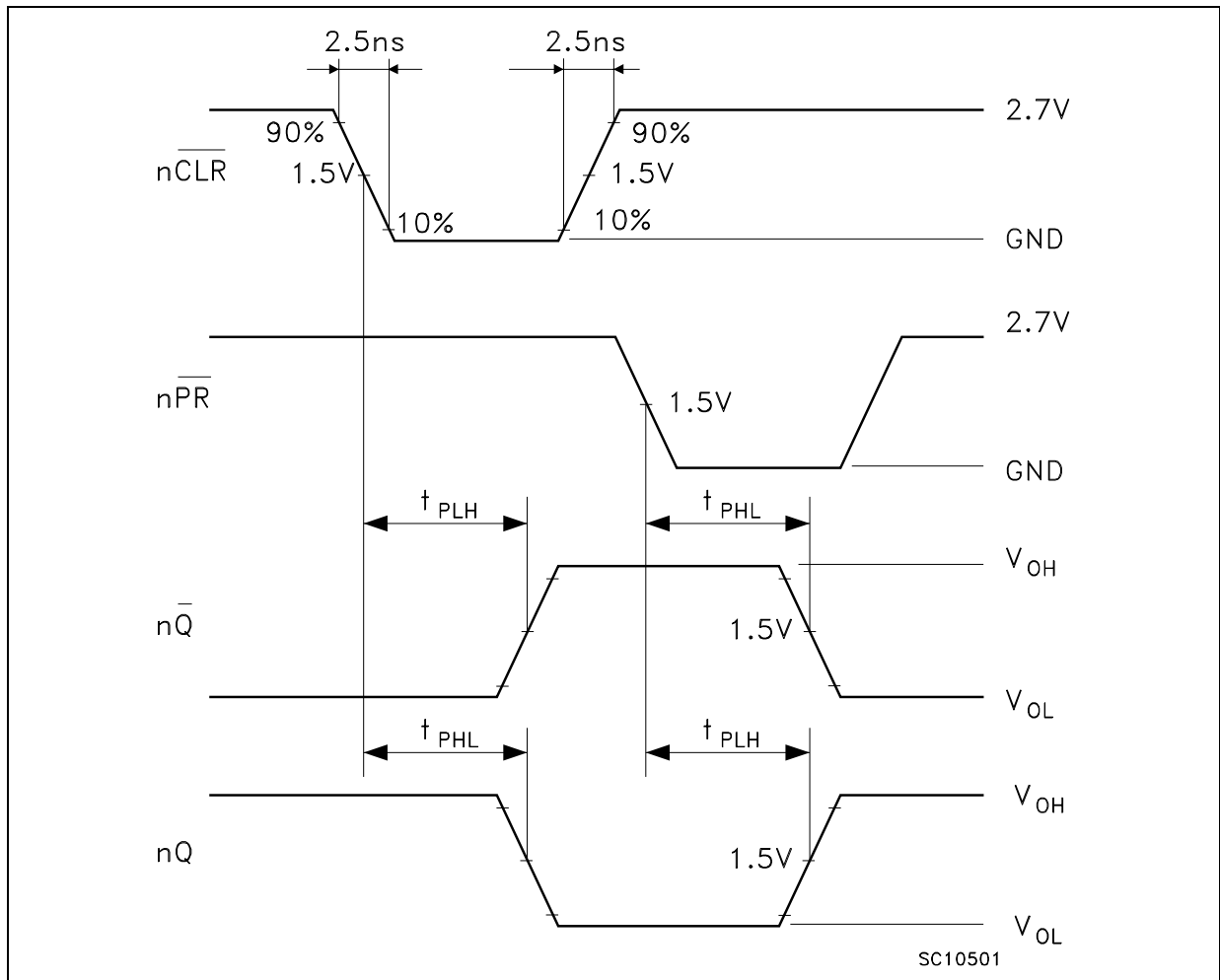
TEST CIRCUIT



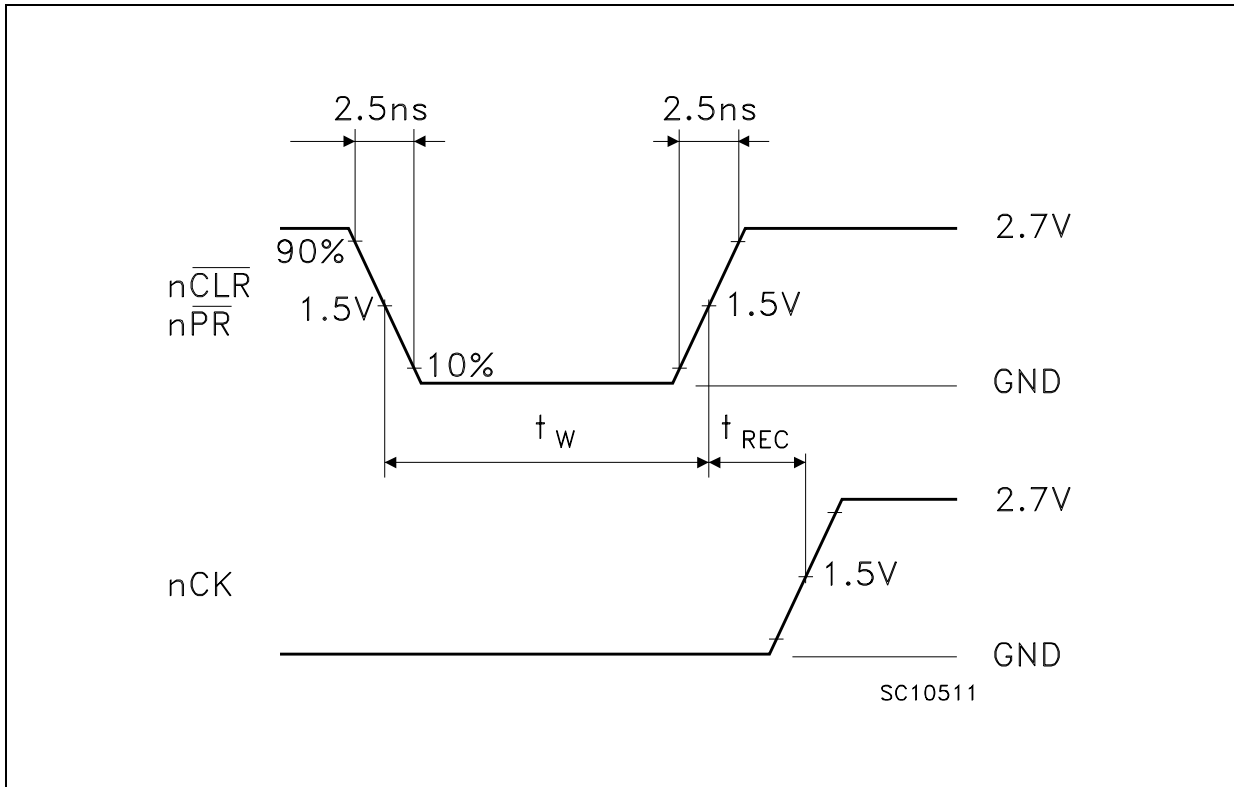
$C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAYS, SETUP AND HOLD TIMES ($f=1\text{MHz}$; 50% duty cycle)

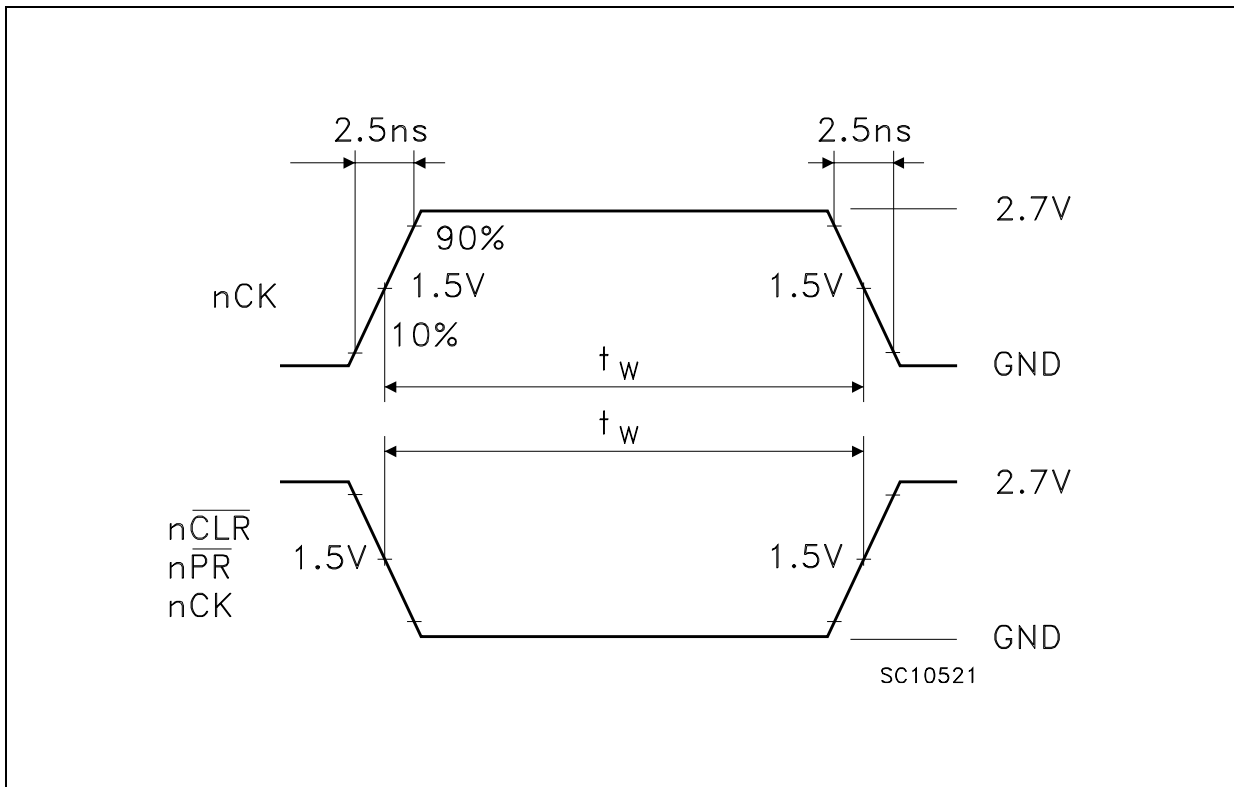


WAVEFORM 2 : PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 3 : RECOVERY TIMES (f=1MHz; 50% duty cycle)

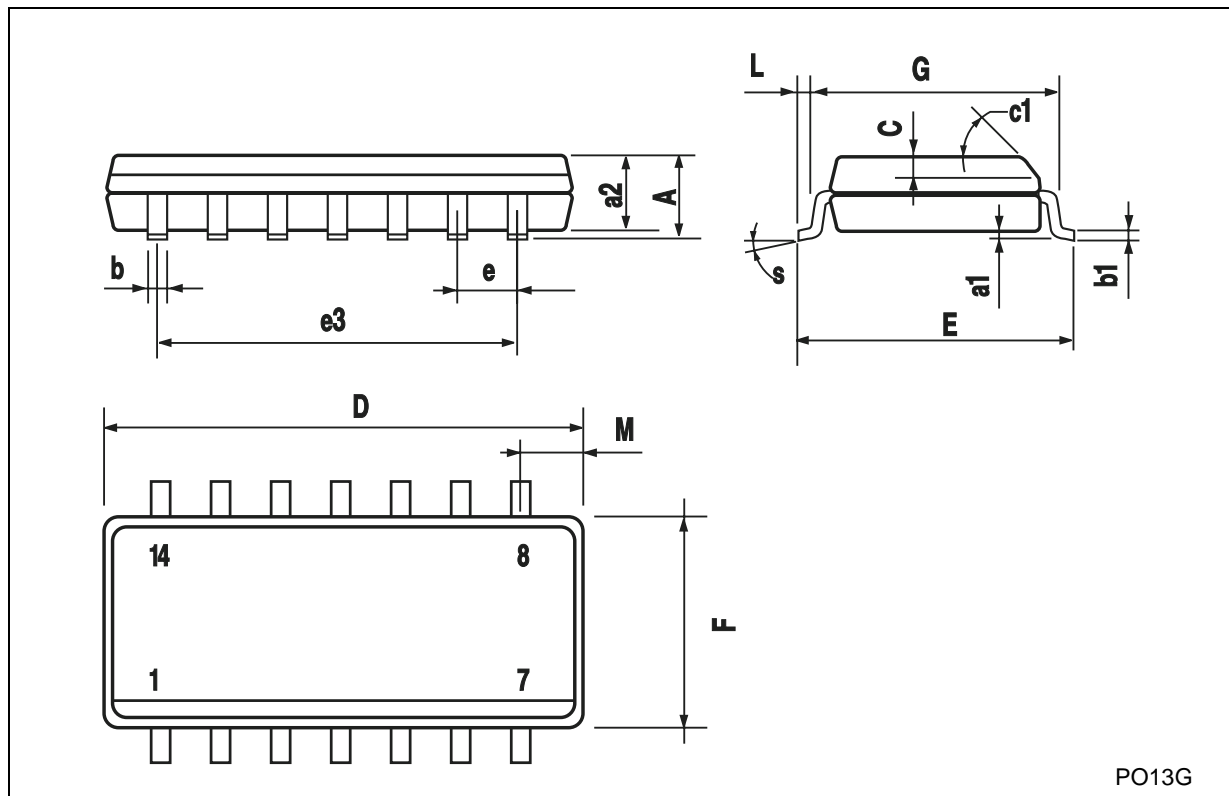


WAVEFORM 4 : PULSE WIDTH (f=1MHz; 50% duty cycle)



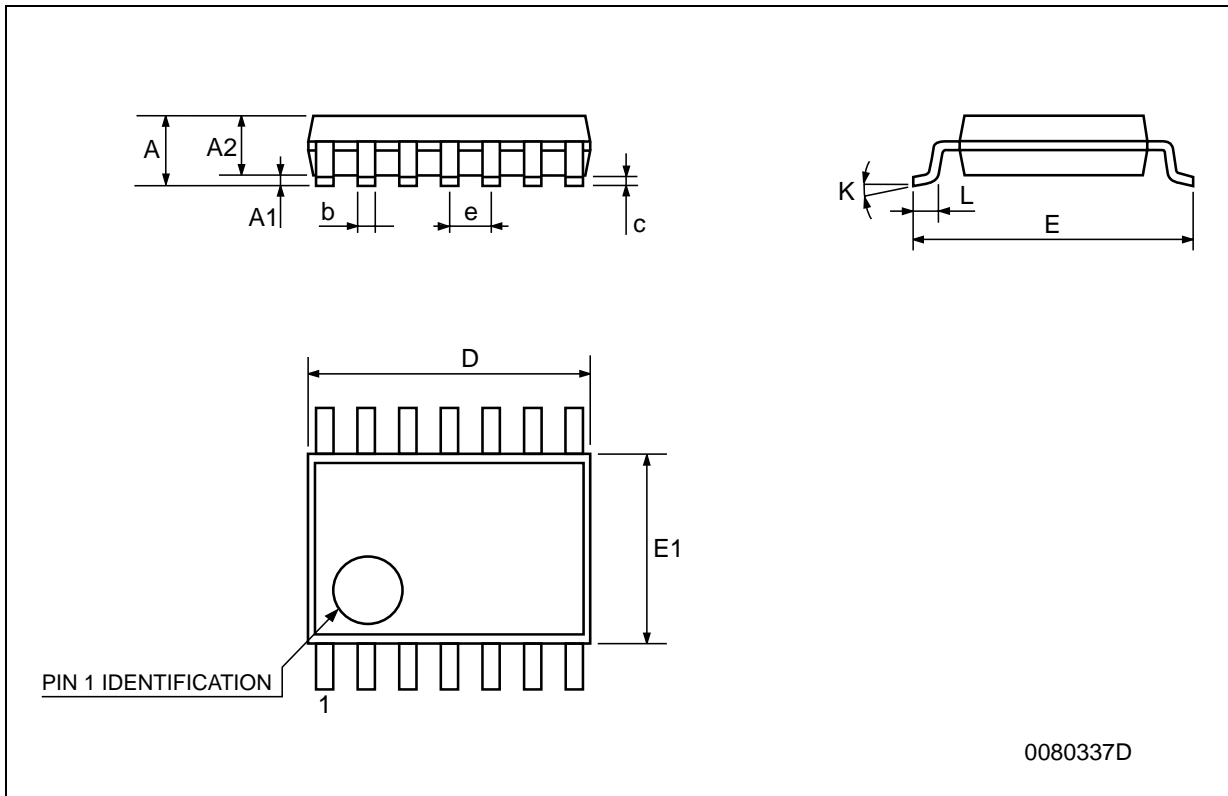
SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2000 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

