A product Line of
Diodes Incorporated

PI6C5912016-01

16 Output LVPECL Fanout Buffer

Features

- 16 Differential LVPECL outputs
- 2 Selectable reference inputs support either single-ended or differential
- Up to 2GHz output frequency
- Ultra low additive phase jitter: < 0.01 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Low skew between outputs
- Low delay from input to output
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFP-48 package

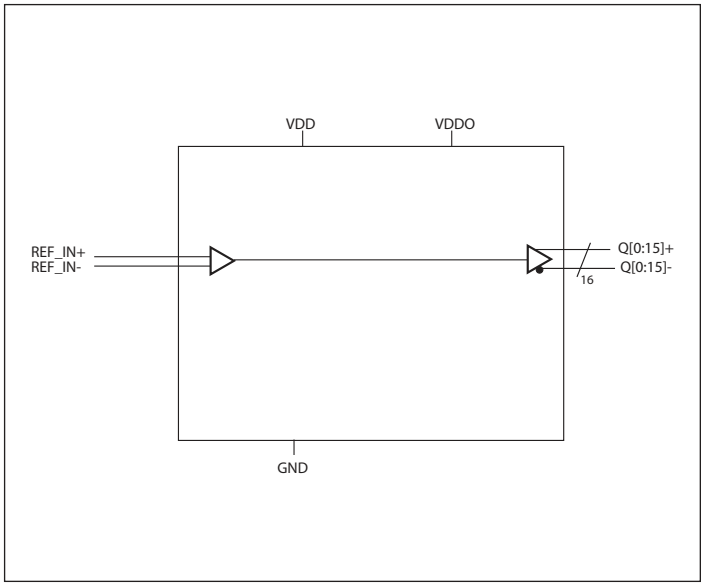
Description

The PI6C5912016-01 is a high performance LVPECL fanout buffer device which supports up to 2GHz frequency. This device is ideal for systems that need to distribute low jitter LVPECL clock signals to multiple destinations.

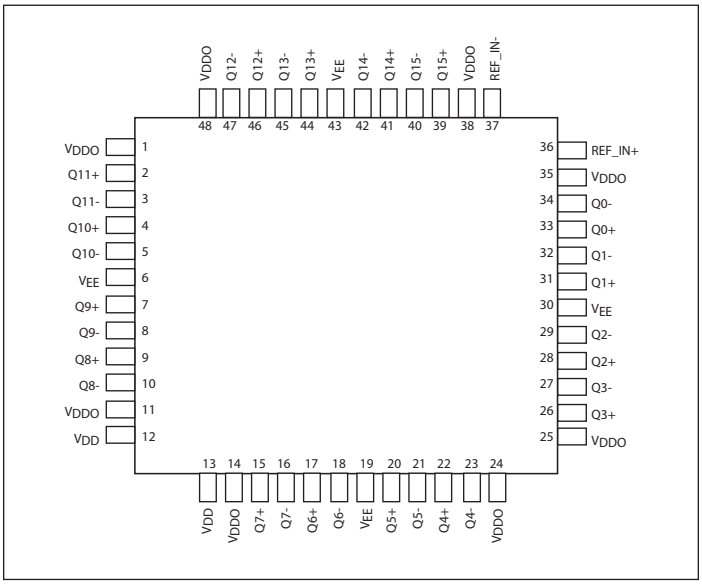
Applications

- Networking systems including switches and routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (48-Pin TQFP)



Pin Description

Pin #	Pin Name	Type	Description
1, 11, 14, 24, 25, 35, 38, 48	V_{DDO}	Power	Output power supply
2, 3	Q11+, Q11-	Output	LVPECL output pair 11.
4, 5	Q10+, Q10-	Output	LVPECL output pair 10.
6, 19, 30, 43	V_{EE}	Power	Negative power supply
7, 8	Q9+, Q9-	Output	LVPECL output pair 9.
9, 10	Q8+, Q8-	Output	LVPECL output pair 8.
12, 13	VDD	Power	Core power supply
15, 16	Q7+, Q7-	Output	LVPECL output pair 7.
17, 18	Q6+, Q6-	Output	LVPECL output pair 6.
20, 21	Q5+, Q5-	Output	LVPECL output pair 5.
22, 23	Q4+, Q4-	Output	LVPECL output pair 4.
26, 27	Q3+, Q3-	Output	LVPECL output pair 3.
28, 29	Q2+, Q2-	Output	LVPECL output pair 2.
31, 32	Q1+, Q1-	Output	LVPECL output pair 1.
33, 34	Q0+, Q0-	Output	LVPECL output pair 0.
36, 37	REF_IN+	Input	Reference input. Accepts Differential or Single Ended inputs
	REF_IN-		
39, 40	Q15+, Q15-	Output	LVPECL output pair 15.
41, 42	Q14+, Q14-	Output	LVPECL output pair 14.
44, 45	Q13+, Q13-	Output	LVPECL output pair 13.
46, 47	Q12+, Q12-	Output	LVPECL output pair 12.
Thermal Pad*	-	-	Thermal pad. Connect to ground.

*Package type dependent. Only certain packages have thermal pad

Function Table

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
C_{IN}	Input Capcitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_{PULLUP}	Input Pullup Resistor			50		kΩ

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential ($V_{DD,}$ V_{DDO})... -0.5 to +4.6V
Inputs (Referenced to GND) ..... -0.5 to V_{DD}+0.5V
Clock Output (Referenced to GND)..... -0.5 to V_{DD}+0.5V
Latch up.....200mA
ESD Protection (Input) .....2000 V min (HBM)
ESD Protection (Input) ..... 1000 V min (CDM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Supply Internal Current				125	mA
I_{DD}	Core Power Supply Current				30	
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter		Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			100	uA
I_{IL}	Input Low current	Input = GND	-100			uA
V_{IH}	Input high voltage				V_{DD}+0.3	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.1			V
V_{CM}	Common model input voltage		GND + 0.5		V_{DD}-0.85	V
ISO_{MUX}	MUX isolation			-89		dBc

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			50	uA
I_{IL}	Input Low current	Input = GND	-50			uA
V_{IH}	Input high voltage	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage	V_{DD}=2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=2.5V	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		V_{DDO}-1.4		V_{DDO}-0.9	V
V_{OL}	Output Low voltage	V_{DD}=2.5V	V_{DDO}-1.9		V_{DDO}-1.25	V
		V_{DD}=3.3V	V_{DDO}-2.2		V_{DDO}-1.25	V

AC Electrical Specifications – Differential Inputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Clock input frequency				2000	MHz
V_{INPP}	Differential Input peak to peak voltage	1.5GHz ≤ F_{IN} ≤ 2 GHz	0.2		1.5	V
		F_{IN} ≤ 1.5 GHz	0.1		1.5	V
ER	Input Edge Rate		1.5			V/ns

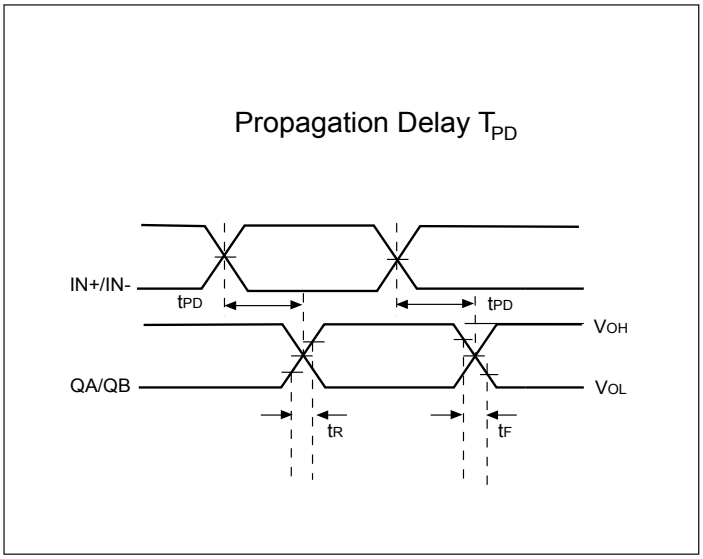
AC Electrical Specifications – LVCMOS Inputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Clock input frequency				200	MHz
V_{INPP}	Differential Input peak to peak voltage	1.5GHz ≤ F_{IN} ≤ 2 GHz	0.2		1.5	V
		F_{IN} ≤ 1.5 GHz	0.1		1.5	V
ER	Input Edge Rate		1.5			V/ns

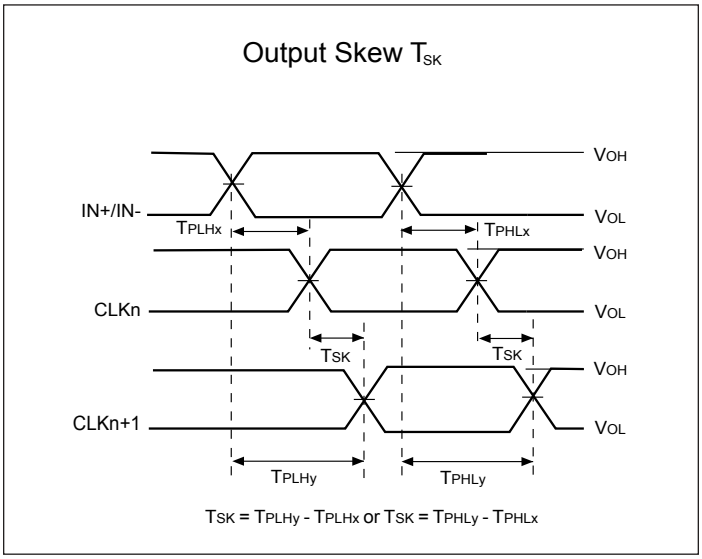
AC Electrical Specifications – LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL			2000	MHz
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle		48		52	%
V_{PP}	Output swing Single-ended	@1GHz to ≤2GHz	200		850	mV
		@ ≤1GHz	450		950	mV
T_j	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz		0.01	0.08	ps
		156.25MHz, 10kHz to 1MHz		0.01	0.08	ps
T_{SK}	Output Skew			13	30	ps
T_{PD}	Propagation Delay				750	ps
T_{OD}	Valid to HiZ				100	ns
T_{OE}	HiZ to valid				100	ns
$T_{P2P\ Skew}$	Part to Part Skew[1]		-50		50	ps
V_{REF_AC}	Input bias voltage	I_{AC} = 2mA	V_{DD}-1.6		V_{DD}-1.1	V

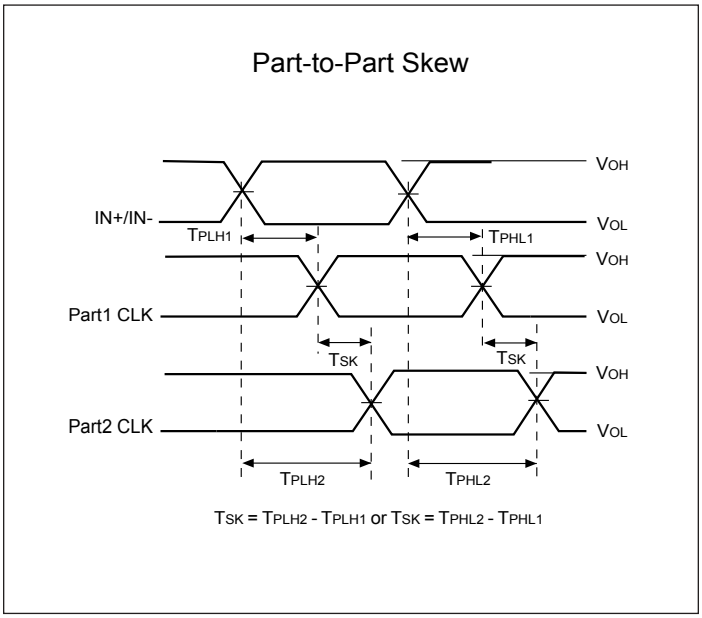
Propagation Delay



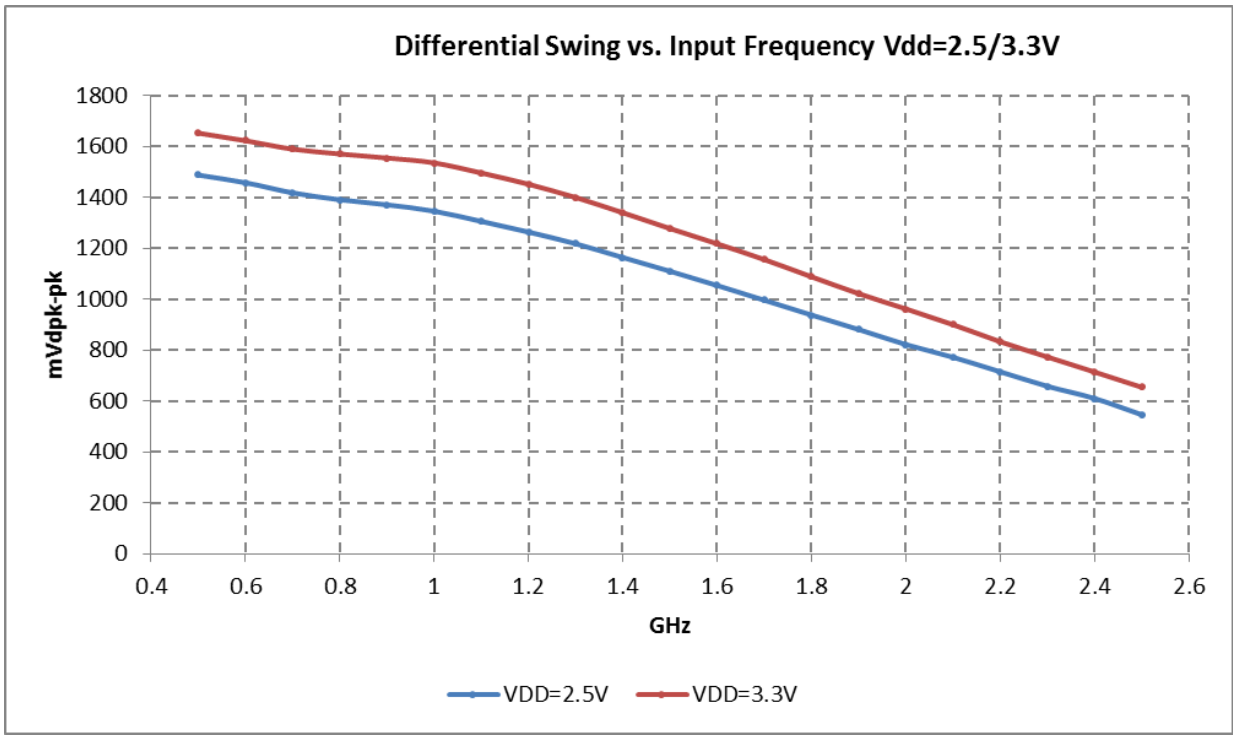
Output Skew



Part to Part Skew



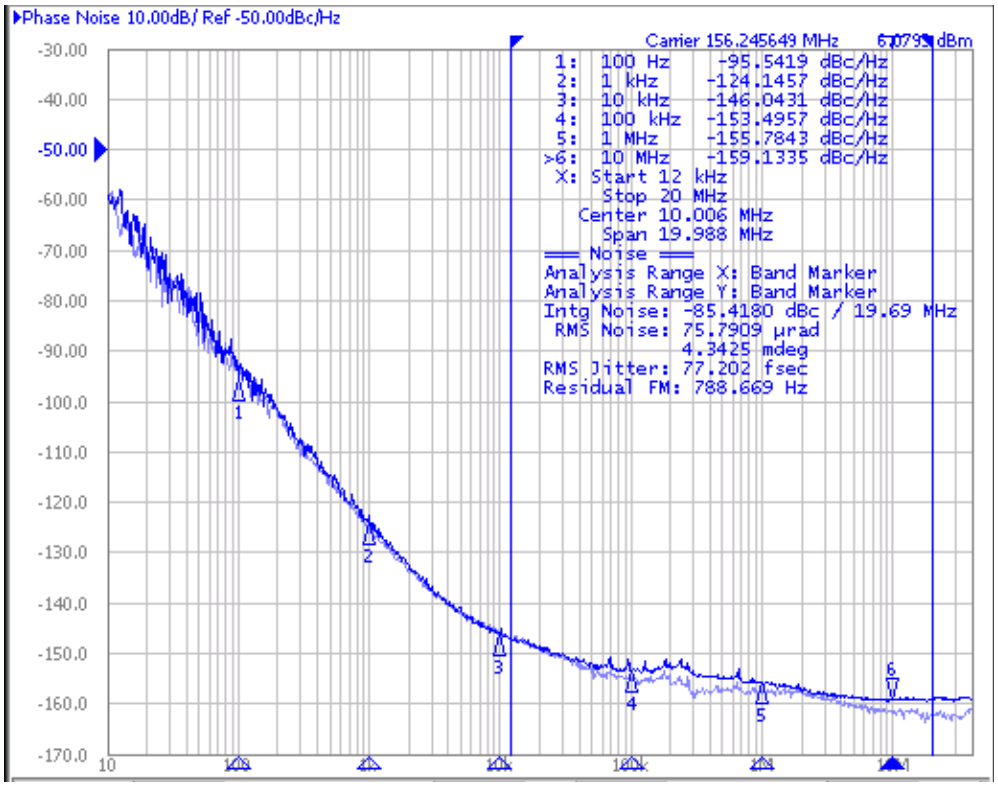
LVPECL Output Swing vs. Frequency



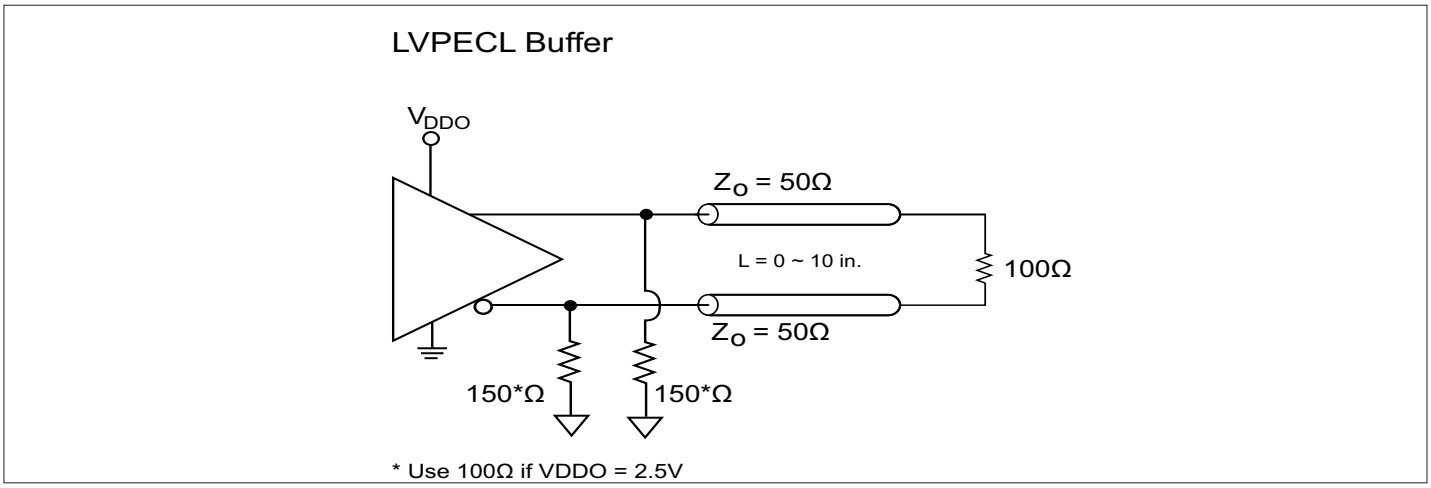
Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



Configuration Test Load Board Termination for LVPECL Outputs



Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

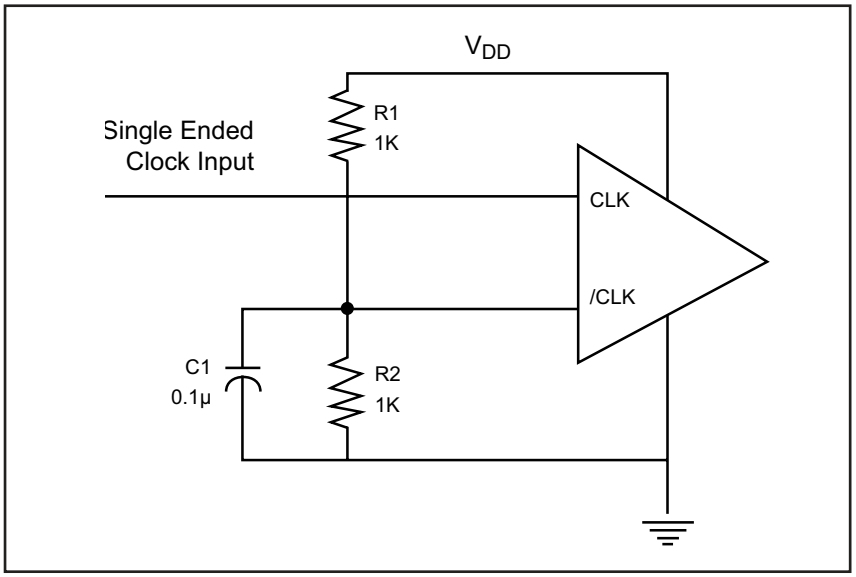
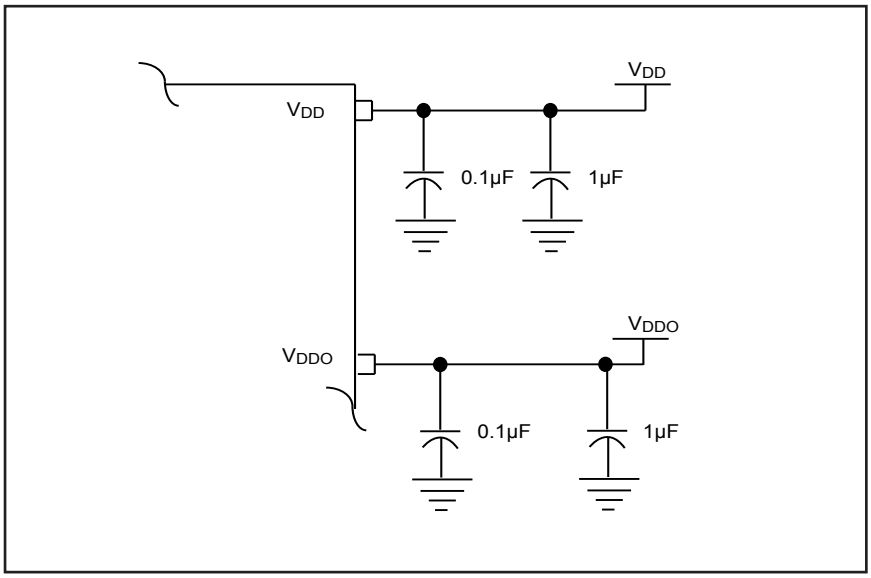


Figure 1. Single-ended input to Differential input device

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.



Thermal Information

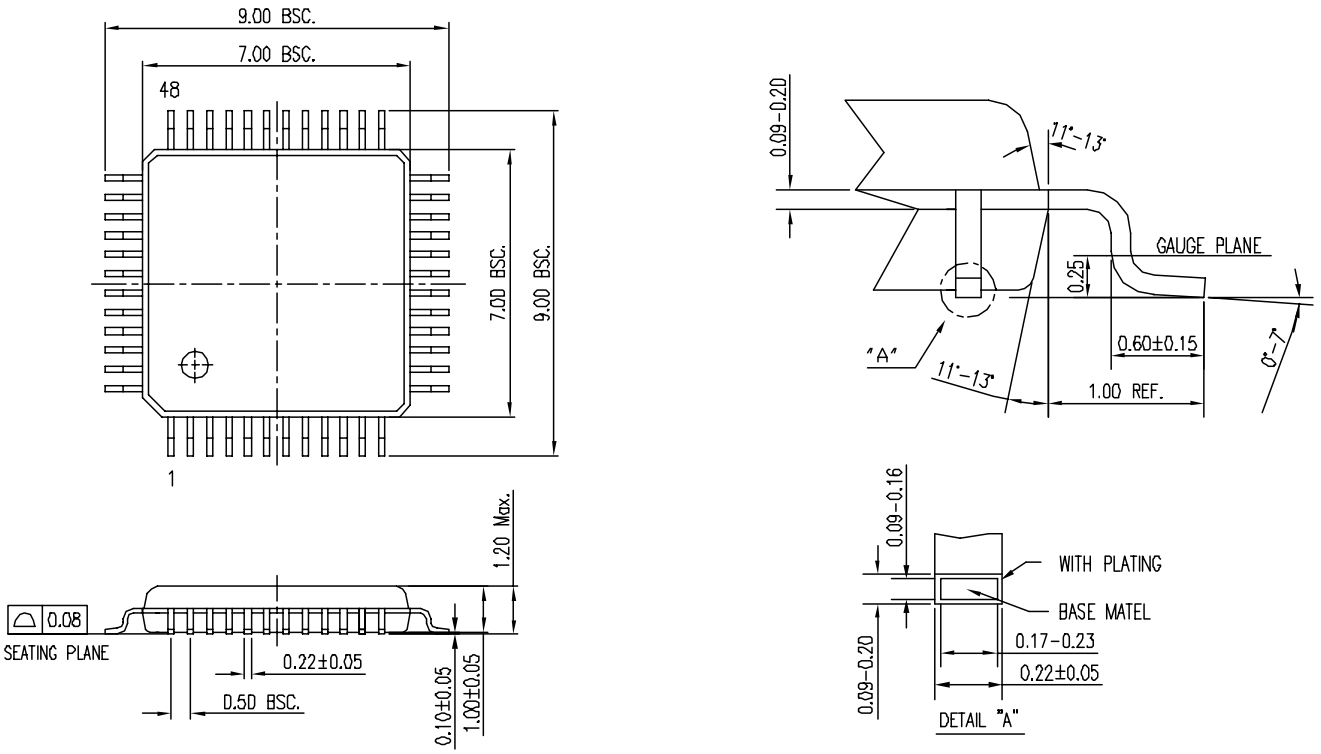
Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	56.6 °C/W
Θ_{JC}	Junction-to-case thermal resistance		12.8 °C/W

Part Marking

FA Package

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical: 48-TQFP (FA)



Notes:
1) All dimensions are in millimeters, Angles in Degrees
2) Ref JEDEC: MO-026D, variation ABC
3) Dimensions do not include mold protrusion

PERICOM Semiconductor Corporation — DATE: 02/16/06

DESCRIPTION: 48-pin Thin Quad Flat Package (TQFP)

PACKAGE CODE: FA48

DOCUMENT CONTROL #: PD-2056 — REVISION: - -

06-0182

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C5912016-01FAIEX	FA	48-pin, Thin Quad Flat Package (TQFP)	-40 °C to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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