

4720B/4720BX

256-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUT

DESCRIPTION — The 4720B/4720BX is a 256-Bit Random Access Memory with 3-State Outputs. It has a Data Input (D), eight Address inputs (A_0 - A_7), an active HIGH Write Enable Input (WE), an active LOW Chip Select Input (\overline{CS}), an active HIGH 3-State Output (Q) and an active LOW 3-State Output (\overline{Q}). Information on the Data Input (D) is written into the memory location selected by the Address Inputs (A_0 - A_7) when the Chip Select Input (\overline{CS}) is LOW and the Write Enable Input (WE) is HIGH. Under these conditions, the device is transparent, i.e., the data input is reflected at the True and Complementary Outputs (Q, \overline{Q}). Information is read from the memory location selected by the Address Inputs (A_0 - A_7) while the Chip Select (\overline{CS}) and the Write Enable (WE) Inputs are LOW. The Q Output is the information written into the memory, \overline{Q} is its complement. When the Chip Select Input (\overline{CS}) is HIGH, both outputs (Q, \overline{Q}) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The 4720B/4720BX offers fully static operation.

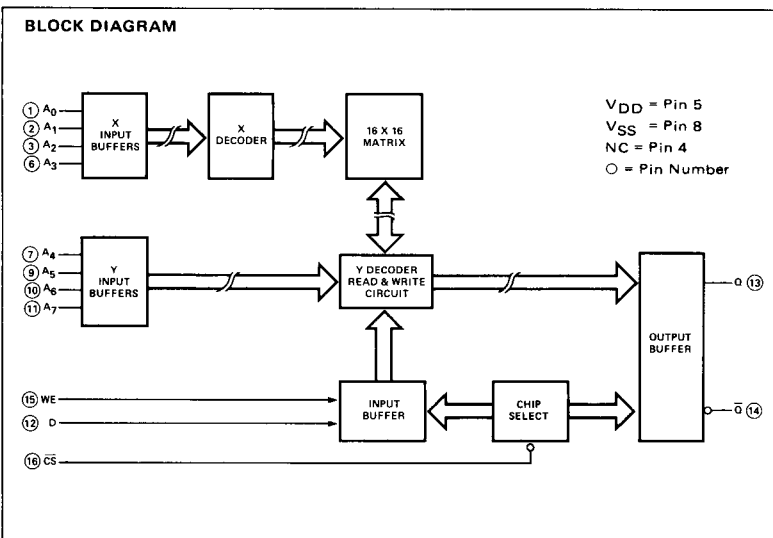
The 4720B is specified to operate over a power supply voltage range of 4.5 to 12.5 V. The 4720BX is specified to operate over a power supply voltage range of 3 to 15 V.

- 3-STATE OUTPUTS
- ORGANIZATION — 256 WORDS X 1-BIT
- ON-CHIP DECODING
- TRUE AND COMPLEMENT OUTPUTS AVAILABLE
- FULLY STATIC
- LOW POWER DISSIPATION
- HIGH SPEED
- TYPICAL HOLDING VOLTAGE OF 1.5 V

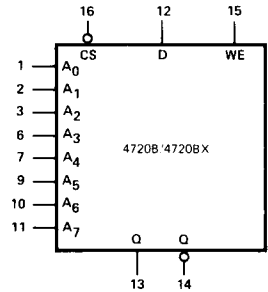
MODE SELECTION

| \overline{CS} | WE | Q | \overline{Q} | MODE |
|-----------------|----|--------------------------|--|---------|
| L | H | Data Written Into Memory | Complement of Data Written Into Memory | Write |
| L | L | Data Written Into Memory | Complement of Data Written Into Memory | Read |
| H | X | High Impedance | High Impedance | Inhibit |

BLOCK DIAGRAM

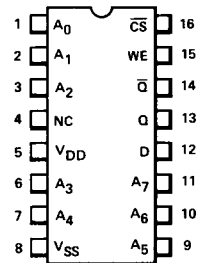


LOGIC SYMBOL



V_{DD} = Pin 5
 V_{SS} = Pin 8
 NC = Pin 4

**CONNECTION DIAGRAM
DIP (TOP VIEW)**



PIN NAMES

- \overline{CS} Chip Select Input (Active LOW)
- WE Write Enable Input
- D Data Input
- A_0 - A_7 Address Inputs
- Q 3-State Output (Active HIGH)
- \overline{Q} 3-State Output (Active LOW)

NOTE:

The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0\text{ V}$ (See Note 1)

| SYMBOL | PARAMETER | | LIMITS | | | | | | | | | UNITS | TEMP | TEST CONDITIONS |
|-----------|--------------------------------|----|-----------------------|-----|-----------|------------------------|-----|-----|------------------------|-----|-------------|---------------|------------------|--|
| | | | $V_{DD} = 5\text{ V}$ | | | $V_{DD} = 10\text{ V}$ | | | $V_{DD} = 15\text{ V}$ | | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| I_{OZH} | Output OFF Current, HIGH | XC | | | | | | | | | 1.6 12 | μA | MIN, 25°C MAX | Output Returned to V_{DD} , $\overline{CS} = V_{DD}$ |
| | | XM | | | | | | | | | 0.4 12 | | | |
| I_{OZL} | Output OFF Current, LOW | XC | | | | | | | | | -1.6 -12 | μA | MIN, 25°C MAX | Output Returned to V_{SS} , $\overline{CS} = V_{DD}$ |
| | | XM | | | | | | | | | -0.4 -12 | | | |
| I_{DD} | Quiescent Power Supply Current | XC | | | 20 150 | | | | | | 40 300 | μA | MIN, 25°C MAX | All inputs at 0 V or V_{DD} |
| | | XM | | | 5 150 | | | | | | 10 300 | | | |

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (See Note 2)

| SYMBOL | PARAMETER | | LIMITS | | | | | | | | | UNITS | TEST CONDITIONS |
|------------|---|--|-----------------------|-----|-----|------------------------|-----|-----|------------------------|-----|-----|-------|--|
| | | | $V_{DD} = 5\text{ V}$ | | | $V_{DD} = 10\text{ V}$ | | | $V_{DD} = 15\text{ V}$ | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| READ MODE | | | | | | | | | | | | | |
| t_{PLH} | Propagation Delay, Address to Output | | | 250 | 500 | | 95 | 190 | | 68 | 136 | ns | $(R_L = 1\text{ k}\Omega \text{ to } V_{SS})$ $(R_L = 1\text{ k}\Omega \text{ to } V_{DD})$ $(R_L = 1\text{ k}\Omega \text{ to } V_{SS})$ $(R_L = 1\text{ k}\Omega \text{ to } V_{DD})$ |
| t_{PHL} | Propagation Delay, Address to Output | | | 250 | 500 | | 95 | 190 | | 68 | 136 | | |
| t_{PZH} | Enable Time, \overline{CS} to Output | | | 30 | 60 | | 15 | 30 | | 11 | 22 | ns | |
| t_{PZL} | Enable Time, \overline{CS} to Output | | | 35 | 70 | | 17 | 34 | | 12 | 24 | ns | |
| t_{PHZ} | Disable Time, \overline{CS} to Output | | | 25 | 50 | | 15 | 30 | | 11 | 22 | ns | |
| t_{PLZ} | Disable Time, \overline{CS} to Output | | | 27 | 54 | | 16 | 32 | | 12 | 24 | ns | |
| t_{TLH} | Output Transition Time | | | 75 | 150 | | 35 | 70 | | 25 | 50 | ns | |
| t_{THL} | Output Transition Time | | | 75 | 150 | | 35 | 70 | | 25 | 50 | ns | |
| WRITE MODE | | | | | | | | | | | | | |
| t_{PLH} | Propagation Delay, WE to Output | | | 250 | 500 | | 100 | 200 | | 65 | 130 | ns | |
| t_{PHL} | Propagation Delay, WE to Output | | | 250 | 500 | | 100 | 200 | | 65 | 130 | | |
| t_{wWE} | Minimum WE Pulse Width | | 240 | 120 | | 110 | 55 | | 80 | 40 | ns | | |
| t_s | Set-Up Time, D to WE | | 80 | 40 | | 38 | 19 | | 28 | 14 | ns | | |
| t_h | Hold Time, D to WE | | 40 | 20 | | 22 | 11 | | 18 | 9 | ns | | |
| t_s | Set-Up Time, Address to WE | | 260 | 130 | | 130 | 65 | | 90 | 45 | ns | | |
| t_h | Hold Time, Address to WE | | 160 | 80 | | 80 | 40 | | 40 | 20 | ns | | |
| t_s | Set-Up Time, \overline{CS} to WE | | 60 | 30 | | 30 | 15 | | 20 | 10 | ns | | |
| t_h | Hold Time, \overline{CS} to WE | | 60 | 30 | | 30 | 15 | | 20 | 10 | ns | | |

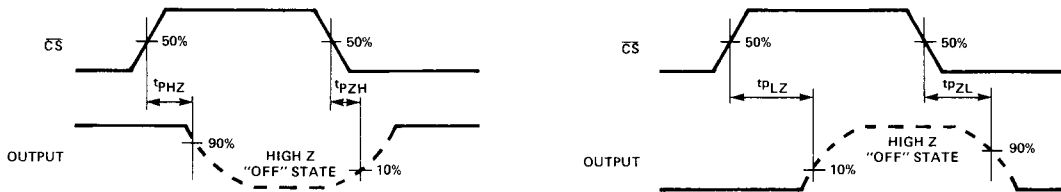
NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
- All set-up (t_s) and hold (t_h) times are measured with minimum write enable pulse width (t_{wWE}).



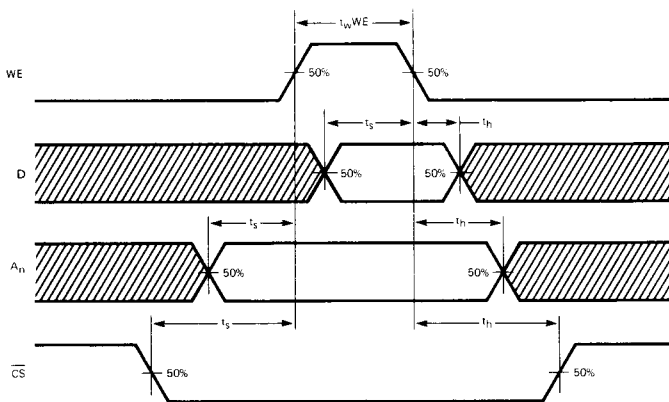
SWITCHING WAVEFORMS

READ MODE



CS TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



MINIMUM PULSE WIDTH FOR WE AND SET-UP AND HOLD TIMES, D TO WE, A_n TO WE, AND CS TO WE

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.