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NTE74LS107
Integrated Circuit
TTL – Dual J–K Negative Edge Triggered Flip–Flop with Clear

Description:

The NTE74LS107 contains two independent negative–edge–triggered flip–flops in a 14–Lead plastic DIP type package. The J and K inputs must be stable one setup prior to the high–to–low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{Q}$ output high.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2.0	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–0.4	mA
Low–Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	30	MHz
Pulse Duration CLK High	t_w	20	–	–	ns
$\overline{CLR}$ Low		25	–	–	ns
Setup Time before CLK↓ Data High or Low	t_{su}	20	–	–	ns
$\overline{CLR}$ Inactive		25	–	–	ns
Hold Time Data after CLK↓	t_h	20	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = -0.4mA	2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OL} = 4mA	–	0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OL} = 8mA	–	0.35	0.5	V
Input Current J or K	I_I	V_{CC} = MAX, V_I = 7V	–	–	0.1	mA
CLR			–	–	0.3	mA
CLK			–	–	0.4	mA
High Level Input Current J or K	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	20	μA
CLR			–	–	60	μA
CLK			–	–	80	μA
Low Level Input Current J or K	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−0.4	mA
CLK or CLR			–	–	−0.8	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	4	6	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. For certain devices where state commutation can be caused by shorting an output to GND, an equivalent test may be performed with V_O = 2.125V and the minimum and maximum limits reduced to one half of their stated values.

Note 5. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	t_{max}	R_L = 2kΩ, C_L = 15pF	30	45	–	MHz
Propagation Delay Time (From $\overline{CLR}$ or CLK Input to Q or $\overline{Q}$ Output)	t_{PLH}, t_{PHL}		–	15	20	ns

Truth Table:

Inputs				Outputs	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

Pin Connection Diagram