

Trench Gate IGBT

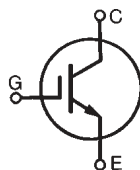
For PDP Applications

IXGP50N33TBM-A

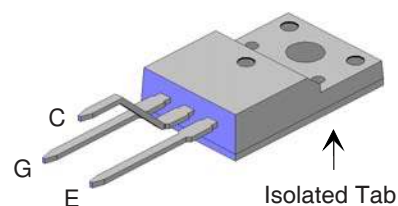
$$V_{CES} = 330V$$

$$I_{CP} = 200A$$

$$V_{CE(sat)} \leq 1.6V$$



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C}$ to 150°C	330	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$	30	A
I_{CP}	$T_J \leq 150^\circ\text{C}$, $t_p \leq 10\mu\text{s}$, duty cycle $\leq 1\%$	200	A
$I_{C(RMS)}$	Lead current limit	75	A
P_C	$T_C = 25^\circ\text{C}$	50	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6mm (0.062 in.) from case for 10s	300	$^\circ\text{C}$
T_{SOLD}	Plastic body for 10 seconds	260	$^\circ\text{C}$
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		2.5	g

**OVERMOLDED TO-220 W/ FORMED
LEAD (IXGP...M-A)**


G = Gate C = Collector
E = Emitter TAB = Isolated

Features

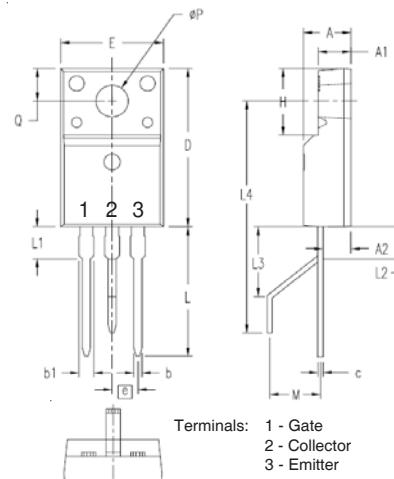
- Fast switching
- Plastic overmolded tab for electrical isolation
- Low $V_{CE(sat)}$
 - for minimum on-state conduction losses

Applications

- PDP Systems
- Capacitive load circuits
- Switching power supplies

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu\text{A}$, $V_{GE} = 0V$	330		V
$V_{GE(th)}$	$I_C = 250\mu\text{A}$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 330V$ $V_{GE} = 0V$ $T_J = 125^\circ\text{C}$			2 μA 125 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$V_{GE} = 15V$, $I_C = 25A$ $I_C = 50A$ $T_J = 125^\circ\text{C}$		1.37 1.35 1.71 1.76	V V V V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 25\text{A}, V_{CE} = 10\text{V}$, Note 1	25	42	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		1480	pF
C_{oes}			108	pF
C_{res}			15	pF
Q_g	$I_C = 25\text{A}, V_{GE} = 15\text{V}, V_{CE} = 0.5 \cdot V_{CES}$		42	nC
Q_{ge}			9	nC
Q_{gc}			12	nC
$t_{d(on)}$	Resistive load, $T_J = 25^\circ\text{C}$ $I_C = 25\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 240\text{V}, R_G = 15\Omega$		14	ns
t_{ri}			30	ns
$t_{d(off)}$			53	ns
t_{fi}			142	ns
$t_{d(on)}$	Resistive load, $T_J = 125^\circ\text{C}$ $I_C = 25\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 240\text{V}, R_G = 15\Omega$		13	ns
t_{ri}			32	ns
$t_{d(off)}$			74	ns
t_{fi}			270	ns
R_{thJC}				2.5 $^\circ\text{C/W}$

OVERMOLDED TO-220 W/ FORMED LEAD (IXGP...M-A)


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.016	.024	0.40	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.500	.523	12.70	13.30
L1	.119	.135	3.03	3.43
L2	.098	.138	2.50	3.50
L3	.256	.295	6.50	7.50
L4	.906	.945	23.00	24.00
M	.177	.216	4.50	5.50
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

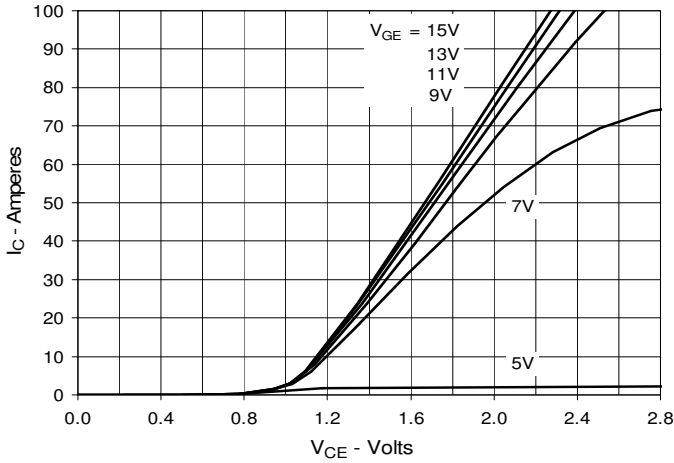
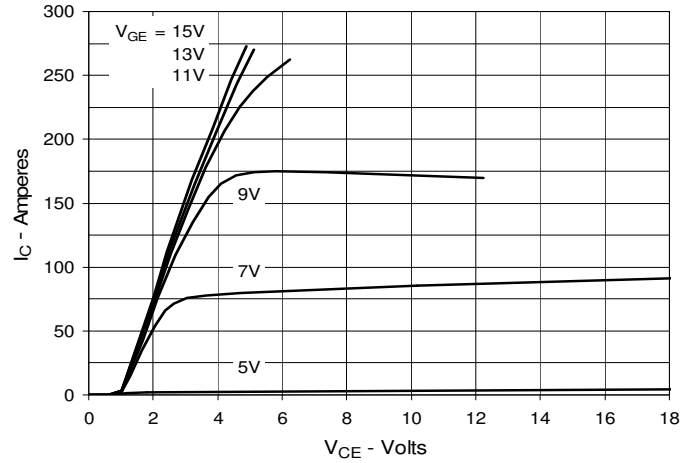
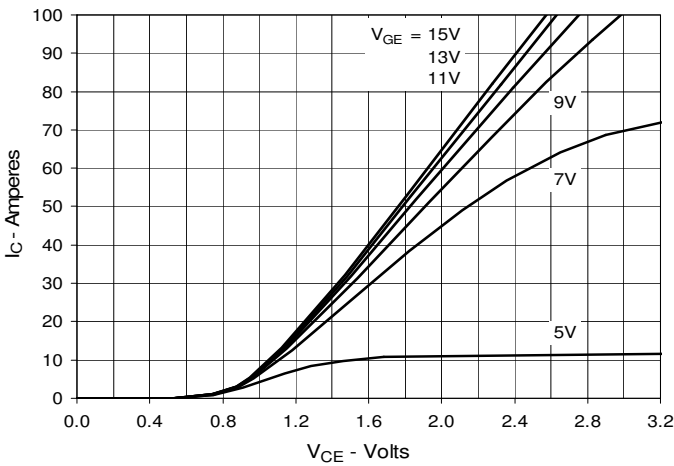
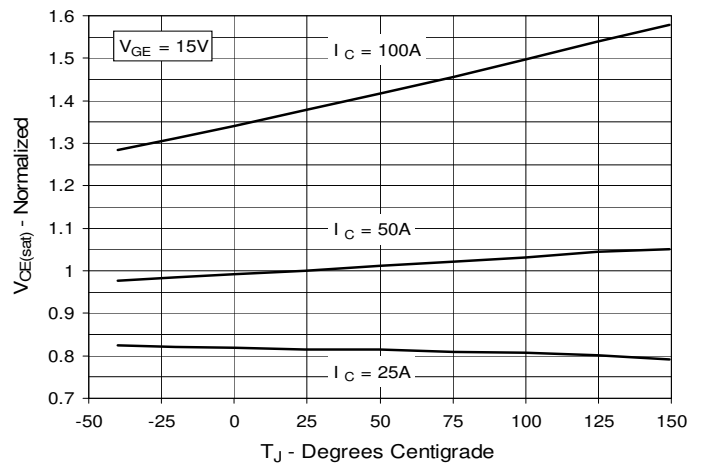
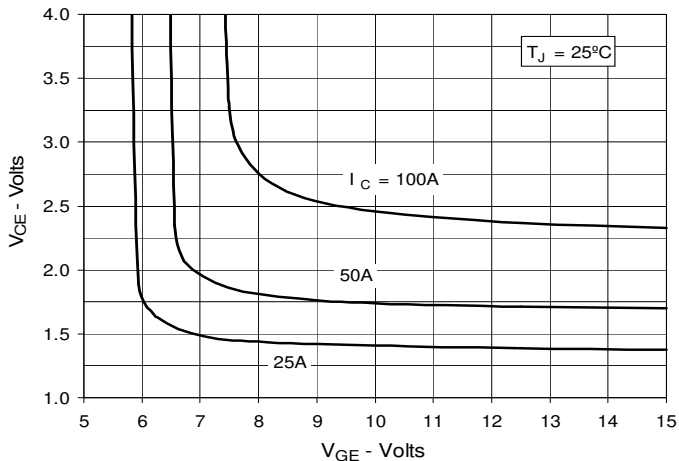
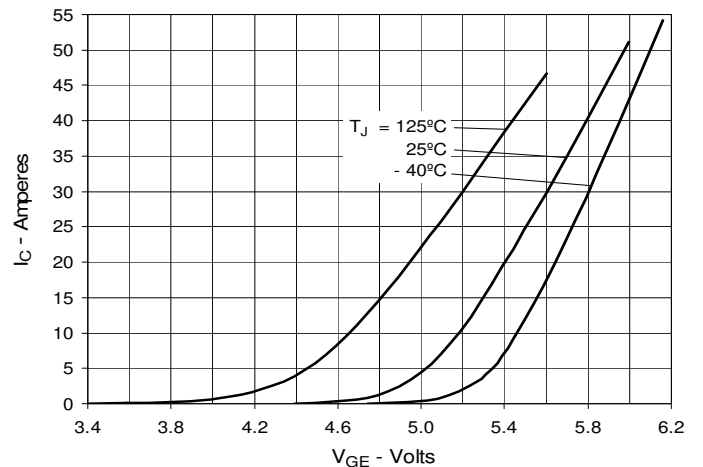
**Fig. 1. Output Characteristics
@ 25°C**

**Fig. 2. Extended Output Characteristics
@ 25°C**

**Fig. 3. Output Characteristics
@ 125°C**

**Fig. 4. Dependence of $V_{CE(sat)}$ on
Junction Temperature**

**Fig. 5. Collector-to-Emitter Voltage
vs. Gate-to-Emitter Voltage**

Fig. 6. Input Admittance


Fig. 7. Transconductance

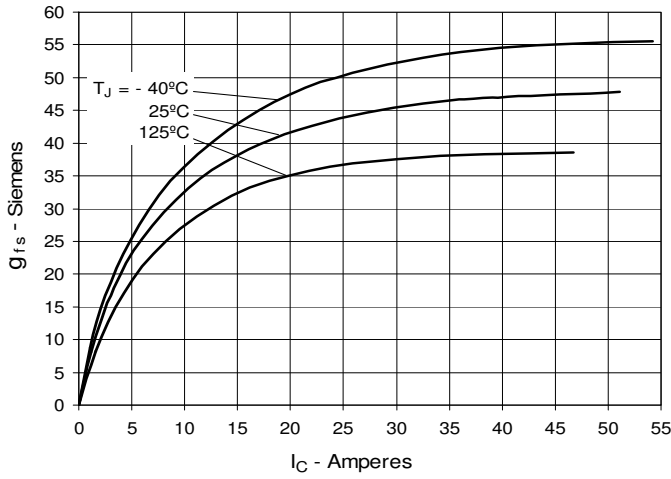


Fig. 8. Gate Charge

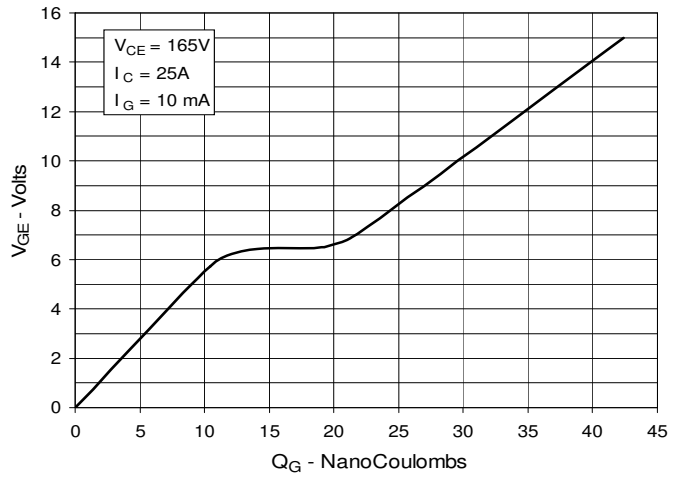


Fig. 9. Reverse-Bias Safe Operating Area

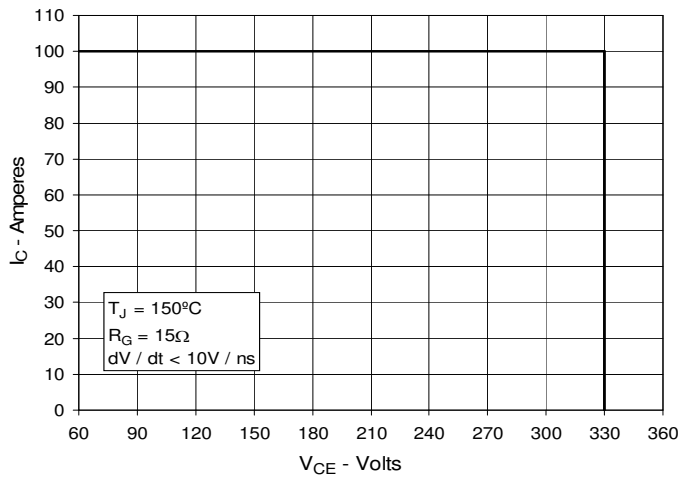


Fig. 10. Capacitance

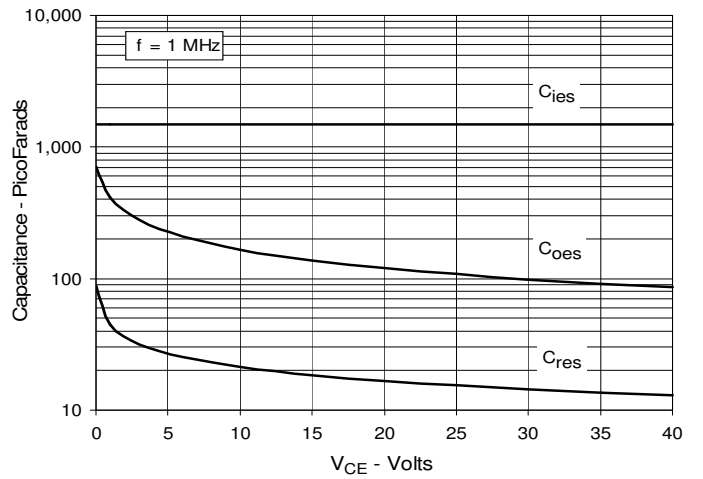


Fig. 11. Forward-Bias Safe Operating Area

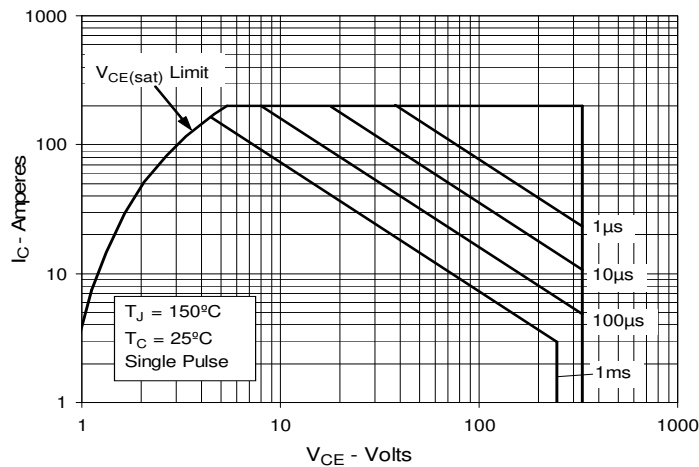


Fig. 12. Maximum Transient Thermal Impedance

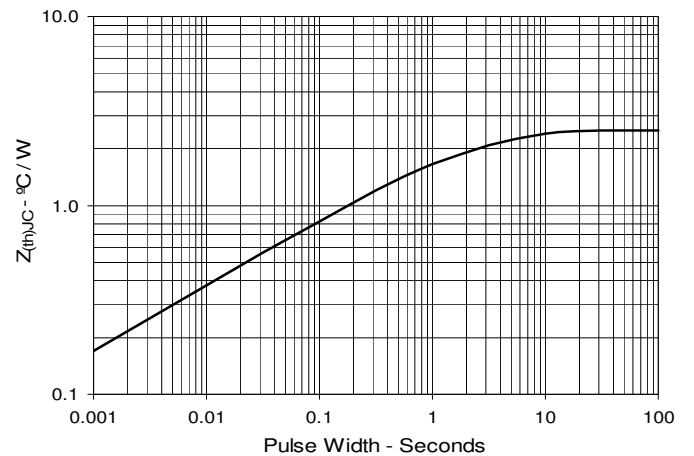
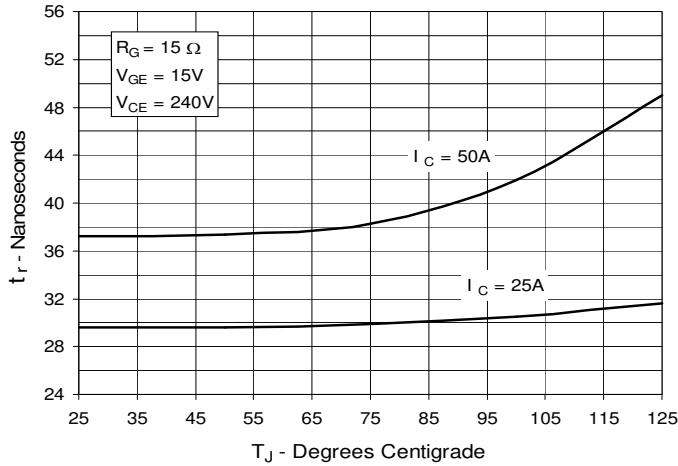
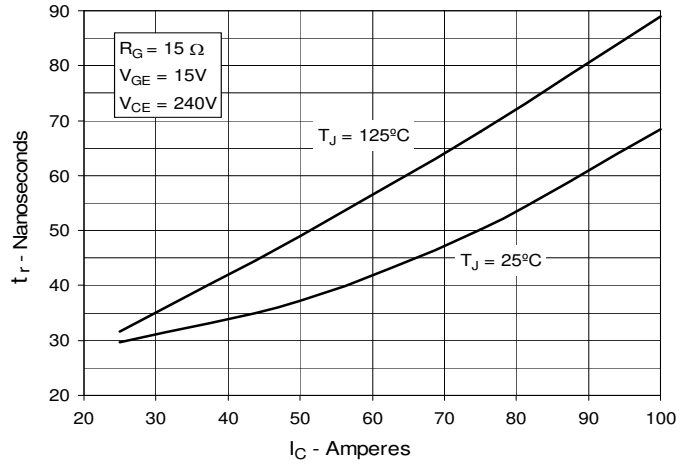
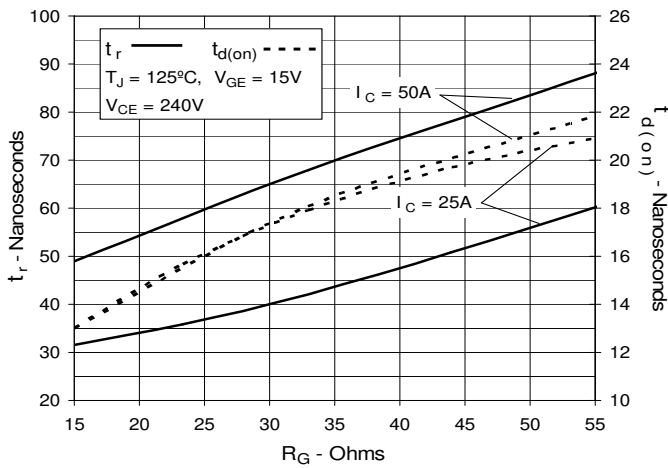
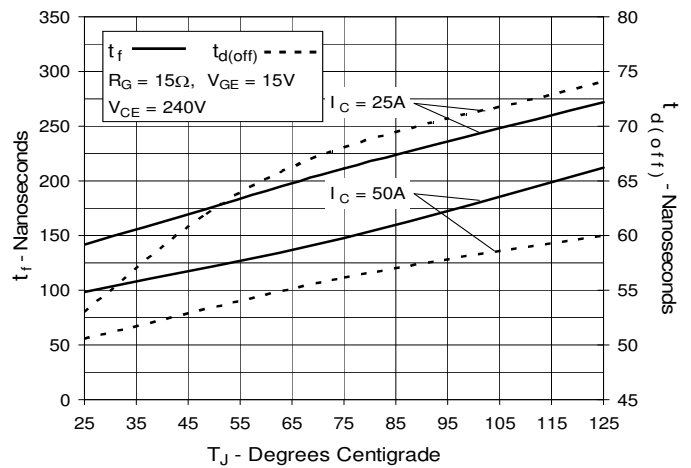
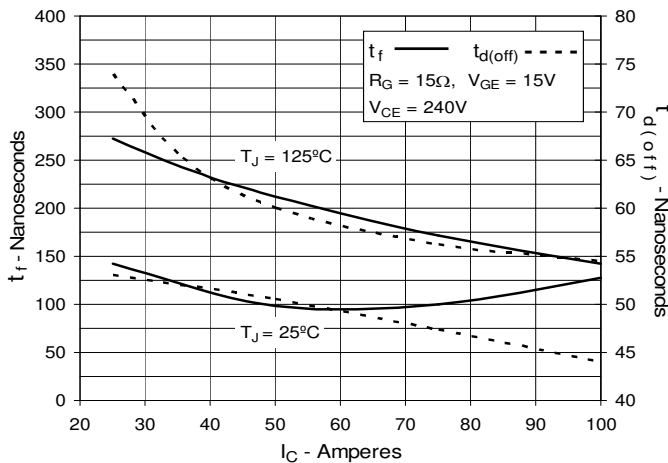


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance
