Spread Aware™, Frequency Multiplier and Zero Delay Buffer

Features

- **Spread Aware™—designed to work with SSFTG reference signals**
- **Two outputs**
- **Configuration options allow various multiplication of the reference frequency, refer to *Table 1* to determine the specific option which meets your multiplication needs**
- **Available in 8-pin SOIC package**

Key Specifications

Operating Voltage: .....3.3V ±5% or 5.0V ±10%

Operating Range: .....20 MHz < f_{OUT1} < 133 MHz

Absolute Jitter: ..... ±500 ps

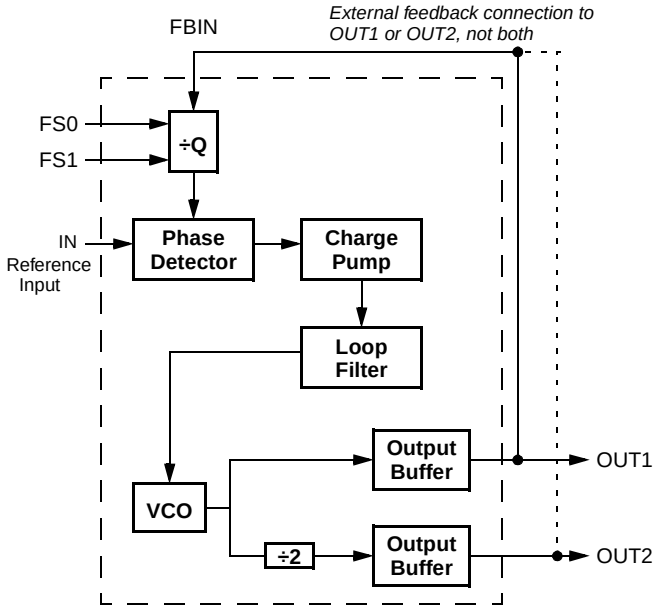
Output to Output Skew: ..... 250 ps

Propagation Delay: ..... ±350 ps
Propagation delay is affected by input rise time.

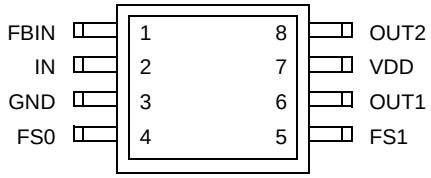
Table 1. Configuration Options

FBIN	FS0	FS1	OUT1	OUT2
OUT1	0	0	2 X REF	REF
OUT1	1	0	4 X REF	2 X REF
OUT1	0	1	REF	REF/2
OUT1	1	1	8 X REF	4 X REF
OUT2	0	0	4 X REF	2 X REF
OUT2	1	0	8 X REF	4 X REF
OUT2	0	1	2 X REF	REF
OUT2	1	1	16 X REF	8 X REF

Block Diagram



Pin Configuration



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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
IN	2	I	***Reference Input:*** The output signals will be synchronized to this signal.
FBIN	1	I	***Feedback Input:*** This input must be fed by one of the outputs (OUT1 or OUT2) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the REF signal input (IN).
OUT1	6	O	***Output 1:*** The frequency of the signal provided by this pin is determined by the feedback signal connected to FBIN, and the FS0:1 inputs (see *Table 1*).
OUT2	8	O	***Output 2:*** The frequency of the signal provided by this pin is one-half of the frequency of OUT1. See *Table 1*.
VDD	7	P	***Power Connections:*** Connect to 3.3V or 5V. This pin should be bypassed with a 0.1-μF decoupling capacitor. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	3	P	***Ground Connection:*** Connect all grounds to the common system ground plane.
FS0:1	4, 5	I	***Function Select Inputs:*** Tie to VDD (HIGH, 1) or GND (LOW, 0) as desired per *Table 1*.

Overview

The W170-01 is a two-output zero delay buffer and frequency multiplier. It provides an external feedback path allowing maximum flexibility when implementing the Zero Delay feature. This is explained further in the sections of this data sheet titled “How to Implement Zero Delay,” and “Inserting Other Devices in Feedback Path.”

The W170-01 is a pin-compatible upgrade of the Cypress W42C70-01. The W170-01 addresses some application dependent problems experienced by users of the older device. Most importantly, it addresses the tracking skew problem induced by a reference which has Spread Spectrum Timing enabled on it.

Spread Aware

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

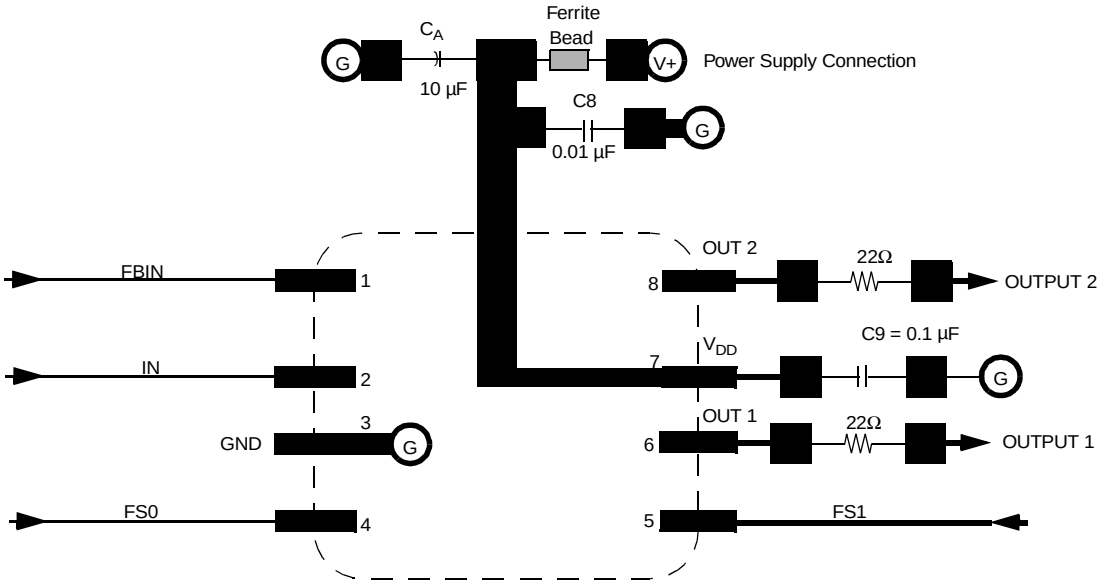


Figure 1. Schematic/Suggested Layout

How to Implement Zero Delay

Typically, zero delay buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation. The PLL on the ZDB will cause the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feed back and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals up to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) which is put into the feedback path.

Referring to *Figure 2*, if the traces between the ASIC/Buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device will be driven HIGH at the same time the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay in the ASIC/Buffer must be accounted for.

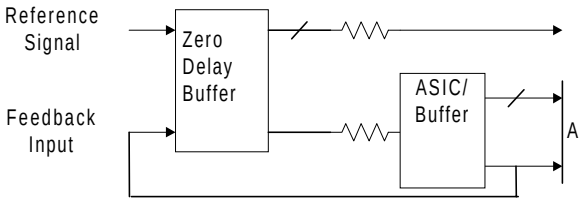


Figure 2. 6 Output Buffer in the Feedback Path

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: T_A =0°C to 70°C or –40° to 85°C, V_{DD} = 3.3V ±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Unloaded, 133 MHz		17	35	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 8 mA	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V	–40		5	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			5	µA

DC Electrical Characteristics: T_A =0°C to 70°C or –40° to 85°C, V_{DD} = 5V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Unloaded, 133 MHz		31	50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 8 mA	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V	-80		5	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			5	µA

AC Electrical Characteristics: T_A = 0°C to +70°C or –40° to 85°C, V_{DD} = 3.3V±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency[1]	OUT2 = REF				MHz
f_{OUT}	Output Frequency	OUT1	20		133	MHz
t_R	Output Rise Time	0.8V to 2.0V, 15-pF load			3.5	ns
t_F	Output Fall Time	2.0V to 0.8V, 15-pF load			2.5	ns
t_{ICLKR}	Input Clock Rise Time[2]				10	ns
t_{ICLKF}	Input Clock Fall Time[2]				10	ns
t_{PD}	FBIN to IN (Reference Input) Skew[3, 4]	Note 4			300	ps
t_D	Duty Cycle	Note 5	40	50	60	%
t_{LOCK}	PLL Lock Time	Power supply stable			1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle	Note 6			250	ps

AC Electrical Characteristics: T_A = 0°C to +70°C or –40° to 85°C, V_{DD} = 5V±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency[1]	OUT2 = REF				MHz
f_{OUT}	Output Frequency	OUT1	20		133	MHz
t_R	Output Rise Time	0.8V to 2.0V, 15-pF load			3.5	ns
t_F	Output Fall Time	2.0V to 0.8V, 15-pF load			2.5	ns
t_{ICLKR}	Input Clock Rise Time[2]				10	ns
t_{ICLKF}	Input Clock Fall Time[2]				10	ns
t_{PD}	FBIN to IN (Reference Input) Skew[3, 4]	Note 4			300	ps
t_D	Duty Cycle	Note 7, 8	40	50	60	%
t_{LOCK}	PLL Lock Time	Power supply stable			1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle	Note 6			200	ps

Notes:

1. Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration).
2. Longer input rise and fall time will degrade skew and jitter performance.
3. All AC specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
4. Skew is measured at 1.4V on rising edges.
5. Duty cycle is measured at 1.4V.
6. Jitter is measured on 133-MHz signal at 1.4V, low frequency jitter = 350 ps.
7. Duty cycle is measured at 1.4V, 120 MHz.
8. Duty cycle at 133 MHz is 35/65 worst case.

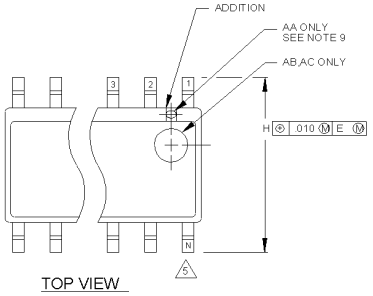
Ordering Information

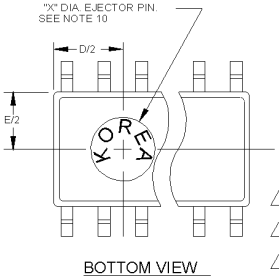
Ordering Code	Option	Package Name	Package Type	Temperature Grade
W170	-01	G	8-pin SOIC (150 mil)	Commerical (0^o to 70^o C) I = Industrail (–40^o to 85^oC)

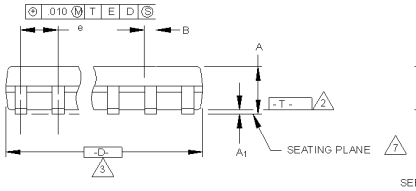
Document #: 38-00795-*A

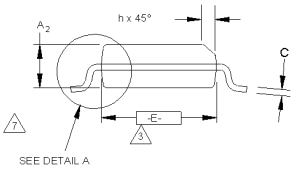
Package Diagram

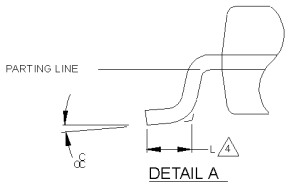
8-Pin Small Outlined Integrated Circuit (SOIC, 150 mil)











NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						