

Model 647H

Very Low Jitter HCSL Clock

Features

- High Speed Current Steering Logic [HCSL] Output
- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 500fs Typical
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 13.5MHz – 200MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-481



Part Dimensions:
7.0 x 5.0 x 1.65mm • 174.2mg

Applications

- PCI Express [PCIe]
- Data Storage Systems
- Ethernet Line Cards
- Serial ATA Express [SATAe]
- Intel Chipsets
- Network Servers
- Switches and Routers
- Set-Top Boxes/DVRs

Standard Frequencies

* See Page 8 for common frequencies.

Check with factory for availability of frequencies not listed.

Description

CTS Model 647H is a low cost, high performance clock oscillator supporting HCSL output. Employing the latest IC technology, M647H has excellent stability and low phase jitter performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging																					
647	H	XXX or XXXX	3	I	3	T																					
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Notes:

- 1) Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2) Check factory for availability. Stability codes 2 and 3 only.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V _{CC}	-	-0.3	-	4.0	V
Supply Voltage	V _{CC}	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current	I _{CC}	Maximum Load Maximum Current Value @ +3.3V	-	-	60	mA
Operating Temperature	T _A	-	-20 -40	+25	+70 +85	°C
Storage Temperature	T _{STG}	-	-50	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f ₀	-		13.5 - 200		MHz
Frequency Stability [Note 1]	Δf/f ₀	-		25, 30, 50 or 100		±ppm
Aging	Δf/f ₂₅	First Year @ +25°C, nominal V _{CC}	-5	±3	5	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCSL		-
Output Load	R _L	Terminated to ground	-	50	-	Ohms
Output Voltage Levels	V _{OH} V _{OL}	HCSL Load	-580 -150	-	850 150	mV
Output Duty Cycle	SYM	Differential Output, @ V _{CC} - 1.3V	45	-	55	%
Differential Output Voltage	V _{OD}	R _L = 50 Ohms to ground	0.4	-	-	Vp-p
Rise and Fall Time	T _R , T _F	@ 20%/80% Levels, R _L = 50 Ohms to ground	-	0.50	0.70	ns

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T _S	Application of V _{CC}	-	5	10	ms
Enable Function [Standby]						
Enable Input Voltage	V _{IH}	Pin 1 Logic '1', Output Enabled	0.7V _{CC}	-	-	V
Disable Input Voltage	V _{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.3V _{CC}	V
Disable Current	I _{IL}	Pin 1 Logic '0', Output Disabled	-	15	-	μA
Enable Time	T _{PLZ}	Pin 1 Logic '1', Output Enabled	-	-	2	ms
Phase Jitter, RMS	t _{jrms}	Bandwidth 12 kHz - 20 MHz	-	500	-	fs

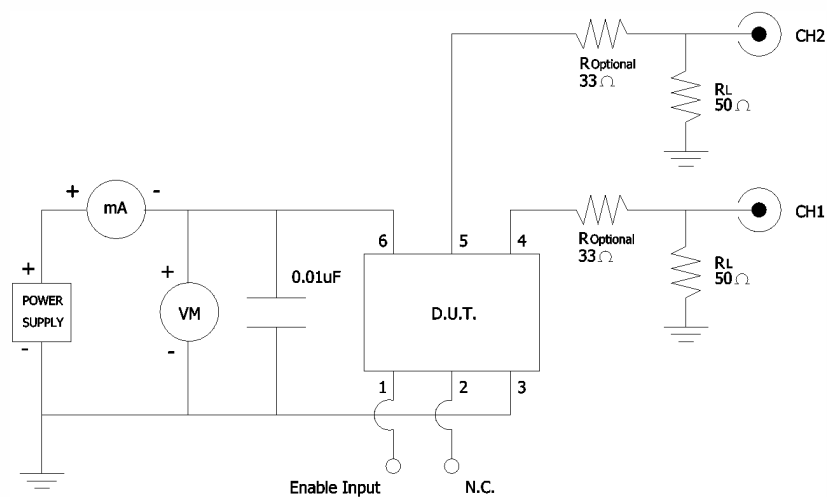
Electrical Specifications

Enable Truth Table

Pin 1	Pin 4 & Pin 5
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

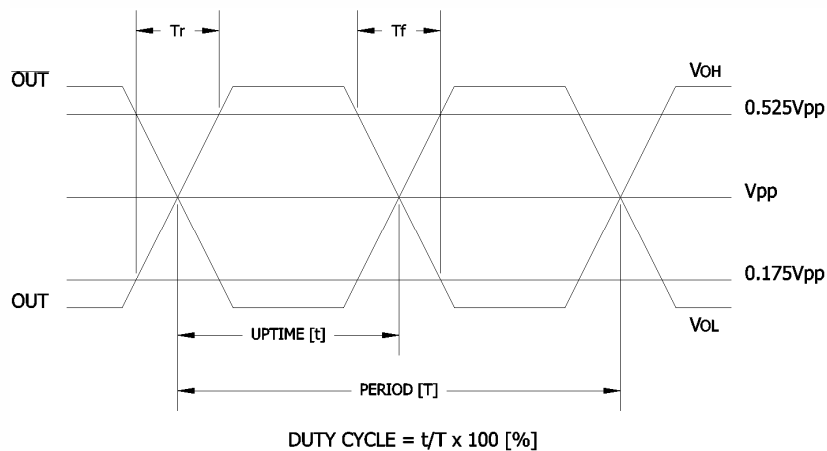
Test Circuit

HCSL



Output Waveform

HCSL

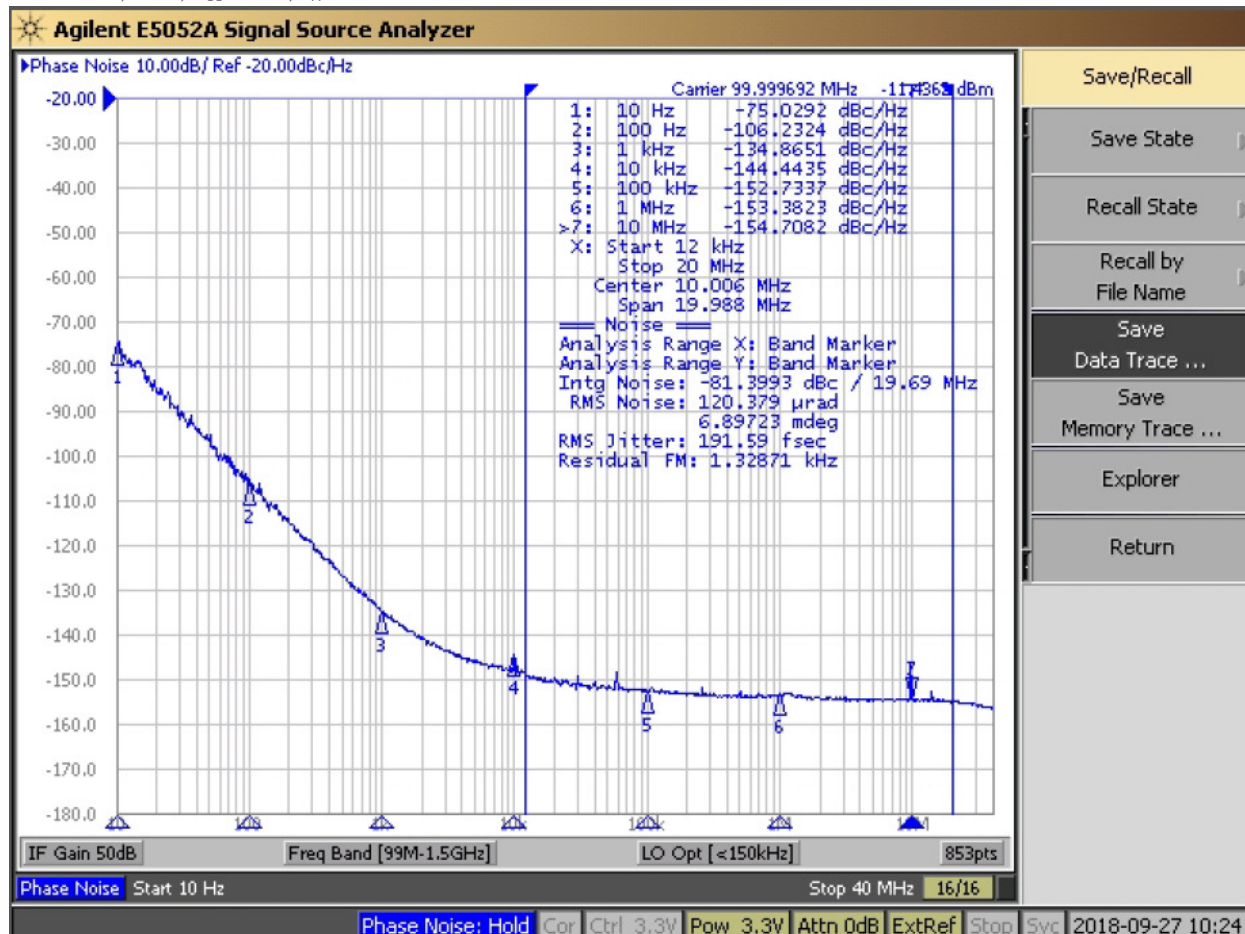


Electrical Specifications

Performance Data

Phase Noise [typical]

100.00MHz, HCSL, $V_{CC} = 3.3V$, $T_A = +25^\circ C$





Electrical Specifications

Performance Data

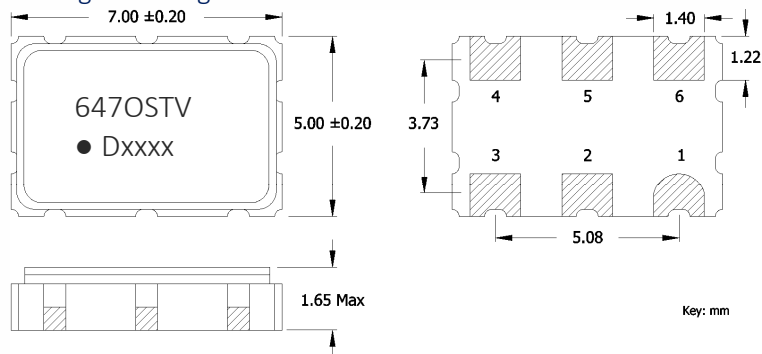
Phase Noise Tabulated

Typical, 100.00MHz, HCSL, $V_{CC} = 3.3V$, $T_A = +25^{\circ}C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
HCSL @ 100.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-75.9328	
		@ 100Hz	-106.9929	
		@ 1kHz	-135.1951	
		@ 10kHz	-144.2209	dBc/Hz
		@ 100kHz	-152.8159	
		@ 1MHz	-153.5793	
		@ 10MHz	-154.8219	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	188.2315	fs

Mechanical Specifications

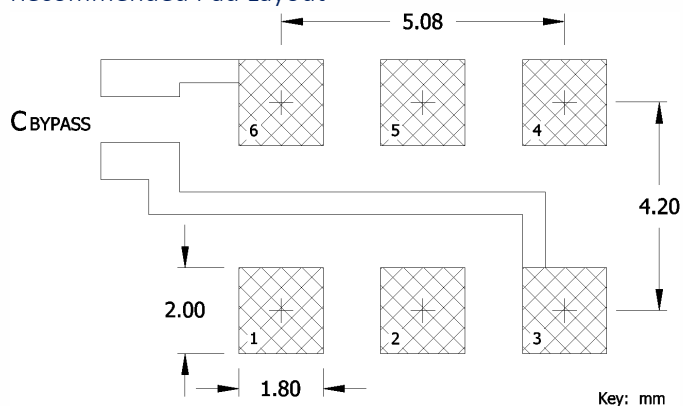
Package Drawing



Marking Information

1. O – Output Type; H = HCSL.
2. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
3. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
4. D – Date Code. See Table I for codes.
5. xxxx – Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater
[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Pin Assignments

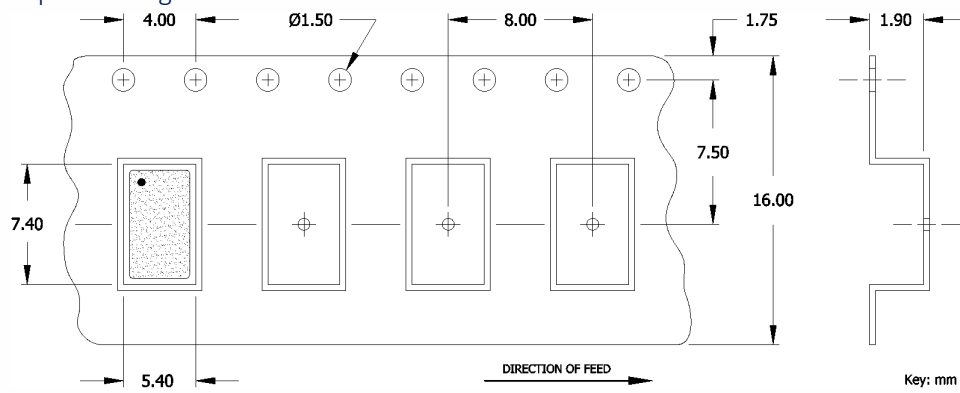
Pin	Symbol	Function
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	$\overline{\text{Output}}$	Complimentary RF Output
6	V _{CC}	Supply Voltage

Table I - Date Code, Beginning year 2021

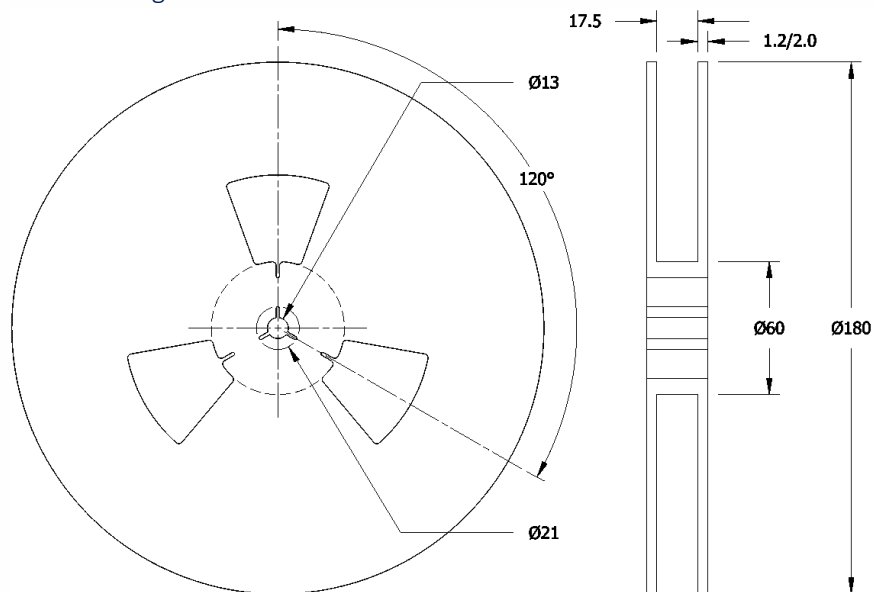
					MONTH											
					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
YEAR																
2021	2025	2029	2033	2037	A	B	C	D	E	F	G	H	J	K	L	M
2022	2026	2030	2034	2038	N	P	Q	R	S	T	U	V	W	X	Y	Z
2023	2027	2031	2035	2039	a	b	c	d	e	f	g	h	j	k	l	m
2024	2028	2032	2036	2040	n	p	q	r	s	t	u	v	w	x	y	z

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.



Addendum

Common Frequencies Available – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	250						
27.000000	270						
50.000000	500						
100.000000	1000						
106.250000	1062						
125.000000	1250						
155.520000	1555						
156.250000	1562						
