ON Semiconductor

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NTTD1P02R2

Power MOSFET
-1.45 Amps, -20 Volts

P−Channel Enhancement Mode
Dual Micro8™ Package

ON Semiconductor®

http://onsemi.com

−1.45 AMPERES
−20 VOLTS
160 mΩ @ V_{GS} = −4.5

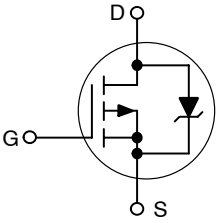
Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual Micro8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided
- Pb−Free Package is Available

Applications

- Power Management in Portable and Battery−Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

Dual P−Channel



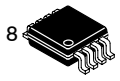
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−20	V
Gate−to−Source Voltage − Continuous	V_{GS}	±8.0	V
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 70°C Pulsed Drain Current (Note 3)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	250 0.50 −1.45 −1.15 −10	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 70°C Pulsed Drain Current (Note 3)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	125 1.0 −2.04 −1.64 −16	°C/W W A A A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −20 Vdc, V_{GS} = −4.5 Vdc, Peak I_L = −3.5 Apk, L = 5.6 mH, R_G = 25 Ω)	EAS	35	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

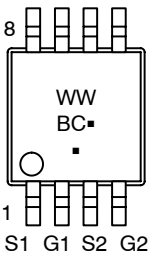
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR−4 or G−10 PCB, Steady State.
2. Mounted onto a 2" square FR−4 Board (1 in sq, 2 oz Cu 0.06″ thick single sided), Steady State.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

MARKING DIAGRAM & PIN ASSIGNMENT



Micro8
CASE 846A
STYLE 2



BC = Specific Device Code
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTD1P02R2	Micro8	4000/Tape & Reel
NTTD1P02R2G	Micro8 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 4)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	−20 –	– −12	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = −20 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = −20 Vdc, T_J = 125°C)		I_{DSS}	– –	– –	−1.0 −10	μAdc
Gate−Body Leakage Current (V_{GS} = −8 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	−100	nAdc
Gate−Body Leakage Current (V_{GS} = +8 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	−0.7 –	−0.95 2.3	−1.4 –	Vdc
Static Drain−to−Source On−State Resistance (V_{GS} = −4.5 Vdc, I_D = −1.45 Adc) (V_{GS} = −2.7 Vdc, I_D = −0.7 Adc) (V_{GS} = −2.5 Vdc, I_D = −0.7 Adc)		$R_{DS(on)}$	– – –	0.130 0.175 0.190	0.160 0.250 –	Ω
Forward Transconductance (V_{DS} = −10 Vdc, I_D = −0.7 Adc)		g_{FS}	–	2.5	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	265	–	pF
Output Capacitance		C_{oss}	–	100	–	
Reverse Transfer Capacitance		C_{rss}	–	60	–	
SWITCHING CHARACTERISTICS (Notes 5 & 6)						
Turn−On Delay Time	(V_{DD} = −16 Vdc, I_D = −1.45 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	10	–	ns
Rise Time		t_r	–	25	–	
Turn−Off Delay Time		$t_{d(off)}$	–	30	–	
Fall Time		t_f	–	25	–	
Turn−On Delay Time	(V_{DD} = −16 Vdc, I_D = −0.7 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	10	–	ns
Rise Time		t_r	–	20	–	
Turn−Off Delay Time		$t_{d(off)}$	–	30	–	
Fall Time		t_f	–	20	–	
Total Gate Charge	(V_{DS} = −16 Vdc, V_{GS} = −4.5 Vdc, I_D = −1.45 Adc)	Q_{tot}	–	5.0	10	nC
Gate−Source Charge		Q_{gs}	–	1.5	–	
Gate−Drain Charge		Q_{gd}	–	2.0	–	
BODY−DRAIN DIODE RATINGS (Note 5)						
Diode Forward On−Voltage	(I_S = −1.45 Adc, V_{GS} = 0 Vdc) (I_S = −1.45 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	– –	−0.91 −0.72	−1.1 –	Vdc
Reverse Recovery Time	(I_S = −1.45 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	–	25	–	ns
		t_a	–	13	–	
		t_b	–	12	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.015	–	μC

4. Handling precautions to protect against electrostatic discharge are mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

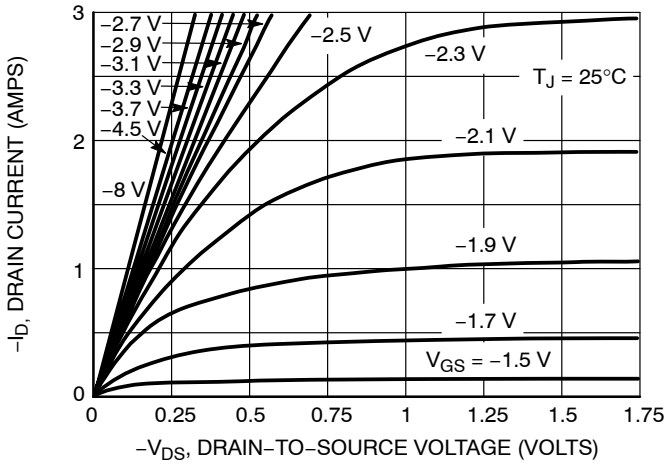


Figure 1. On−Region Characteristics

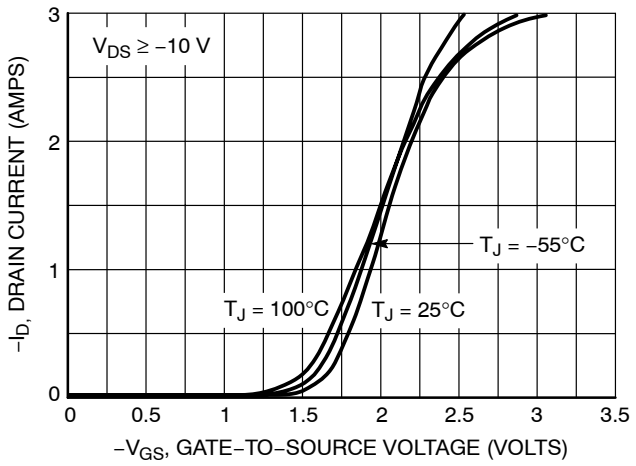


Figure 2. Transfer Characteristics

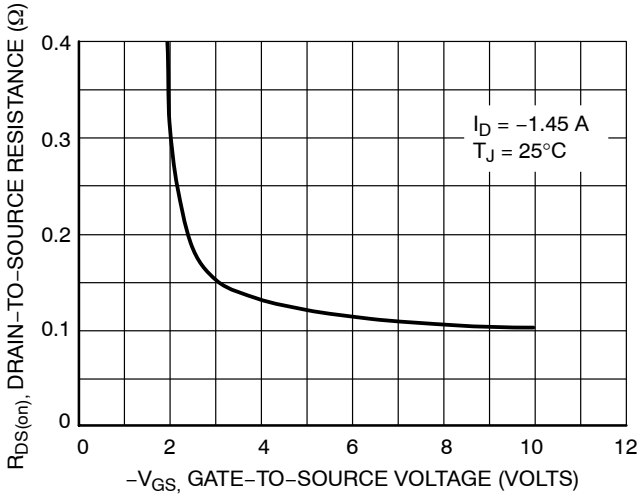


Figure 3. On−Resistance versus Gate−to−Source Voltage

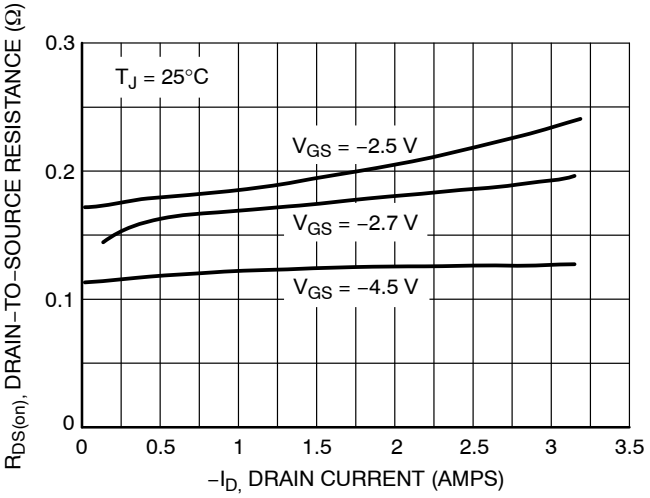


Figure 4. On−Resistance versus Drain Current and Gate Voltage

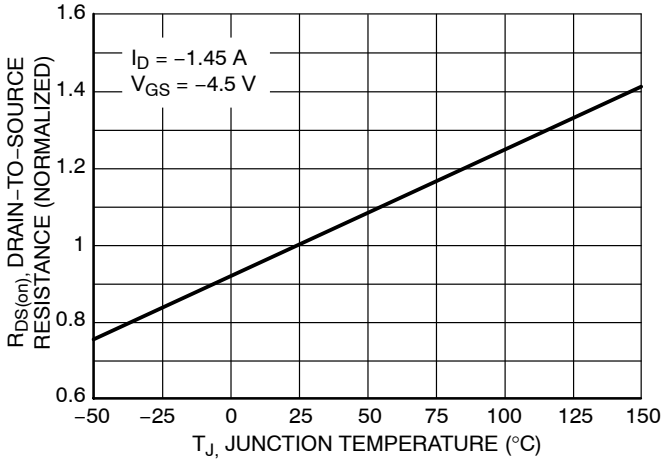


Figure 5. On−Resistance Variation with Temperature

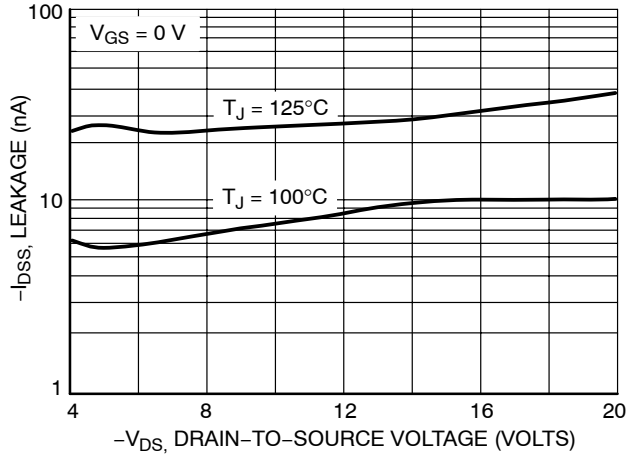


Figure 6. Drain−to−Source Leakage Current versus Voltage

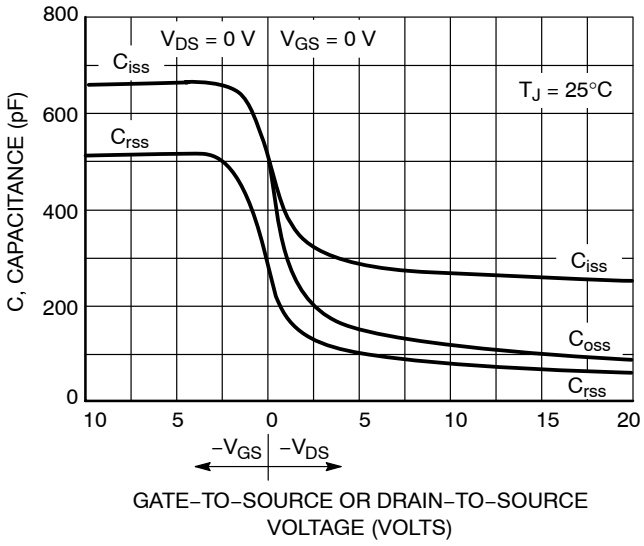


Figure 7. Capacitance Variation

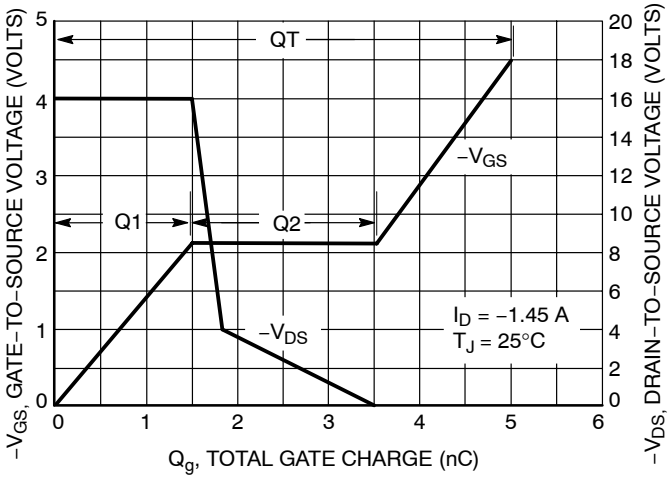


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

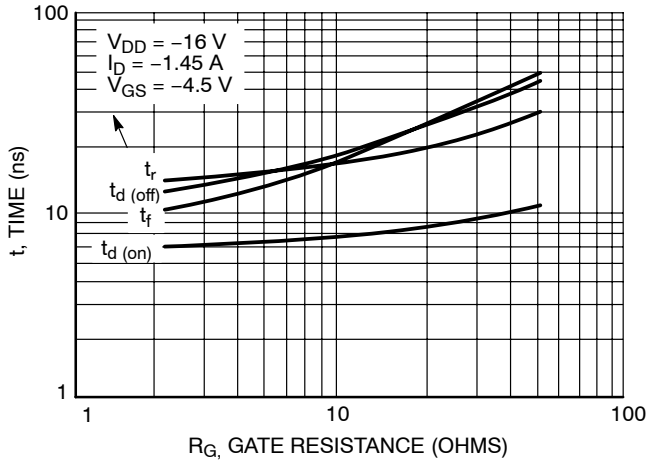


Figure 9. Resistive Switching Time Variation versus Gate Resistance

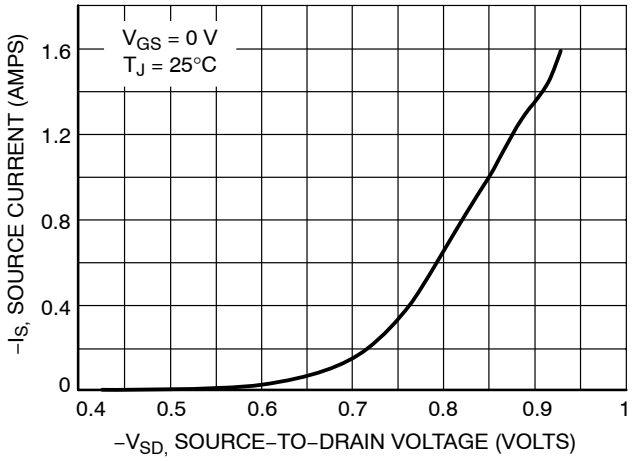


Figure 10. Diode Forward Voltage versus Current

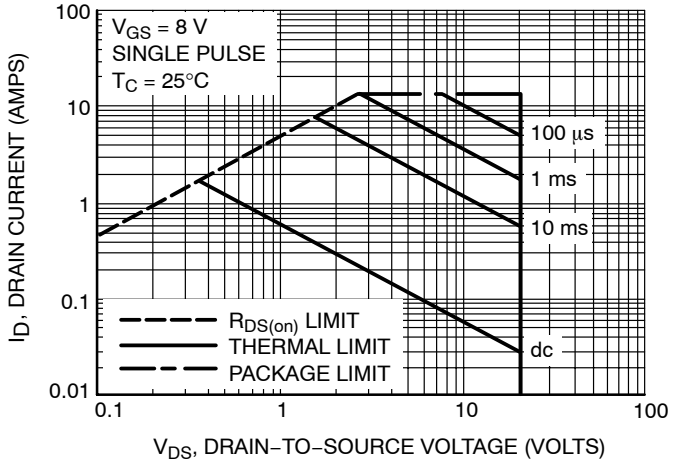


Figure 11. Maximum Rated Forward Biased Safe Operating Area

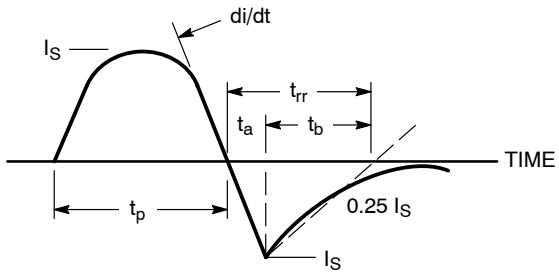


Figure 12. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

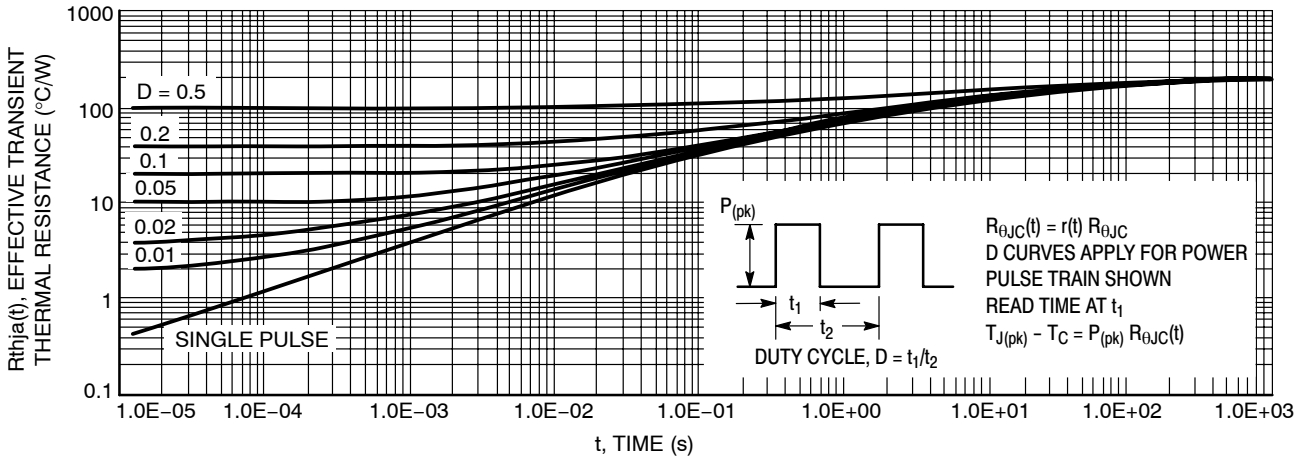
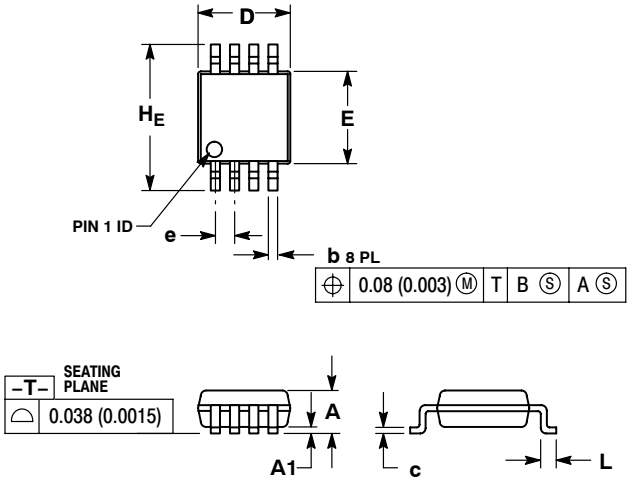


Figure 13. Thermal Response

NTTD1P02R2

PACKAGE DIMENSIONS

Micro8™
CASE 846A–02
ISSUE G

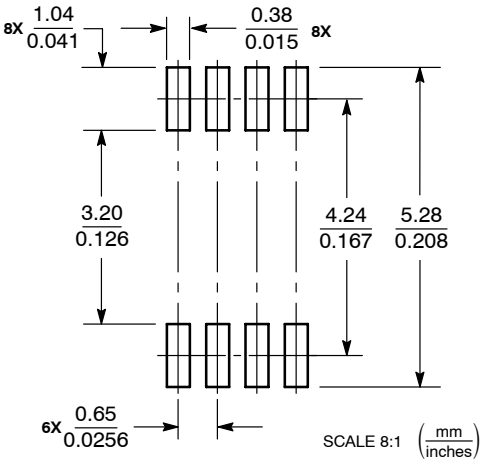


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A–01 OBSOLETE, NEW STANDARD 846A–02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	––	––	1.10	––	––	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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