



16×16-Bit CMOS Single Port Multiplier/Accumulator

ADSP-1110A

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit multiplier/accumulator integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-1110AS(X)/883B
-2	ADSP-1110AT(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28	28-Contact LCC

1.3 Absolute Maximum Ratings.

Supply Voltage	-0.3 V to 7 V
Input Voltage	-0.3 V to V_{DD}
Output Voltage	-0.3 V to V_{DD}
Operating Temperature Range (Ambient)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9, 10, 11	Test Condition ¹	Units
Digital Input High Voltage*	V _{IH}	-1, 2	2.0	2.2	2.2		V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8		V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	-1, 2	2.4	2.4	2.4		V _{DD} = min I _{OH} = -1 mA	V min
Digital Output Low Voltage*	V _{OL}	-1, 2	0.4	0.6	0.6		V _{DD} = min I _{OH} = +4 mA	V max
Digital Input High Current	I _{IH}	-1, 2	10	10	10		V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	-1, 2	10	10	10		V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage* Current Low	I _{OZL}	-1, 2	50	50	50		V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	-1, 2	50	50	50		V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	-1, 2	70	80	80		V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	-1, 2	35	40	40		V _{DD} = max All V _{IN} = 2.4 V	mA max
Clock Pulse Width	t _{PW}	-1, 2	15			15	Note 2	ns min
Input Control Hold Time	t _{CH}	-1, 2	5			6	Note 2	ns min
Input Data Setup Time	t _{DS}	-1, 2	15			15	Note 2	ns min
Clock Period*	t _{CLK}	-1	50			60	Note 2	ns min
		-2	42.5			50		
Input Control Setup Time	t _{CS}	-1	25			25	Note 2	ns min
		-2	20			20		
Input Data Hold Time*	t _{DH}	-1, 2	3			4	Note 2	ns min
Multiply/Accumulate Time*	t _{MAC}	-1	100			120	Note 2	ns max
		-2	85			100		
Control to Valid Output*	t _D	-1	30			30	Note 2	ns max
		-2	25			30		
Control to Valid Output* with Saturation	t _{DSAT}	-1	35			40	Note 2	ns max
		-2	32			35		
Output Driver Disable Time	t _{DIS}	-1, 2	25			25	Notes 2 and 3	ns max
Control to Overflow Flag*	t _O	-1	30			35	Note 2	ns max
		-2	25			30		
Control to Overflow Flag* W/SL	t _{LO}	-1	40			45	Note 2	ns max
		-2	35			45		

NOTES

*Indicates that a limit for this parameter has changed from REV. C.

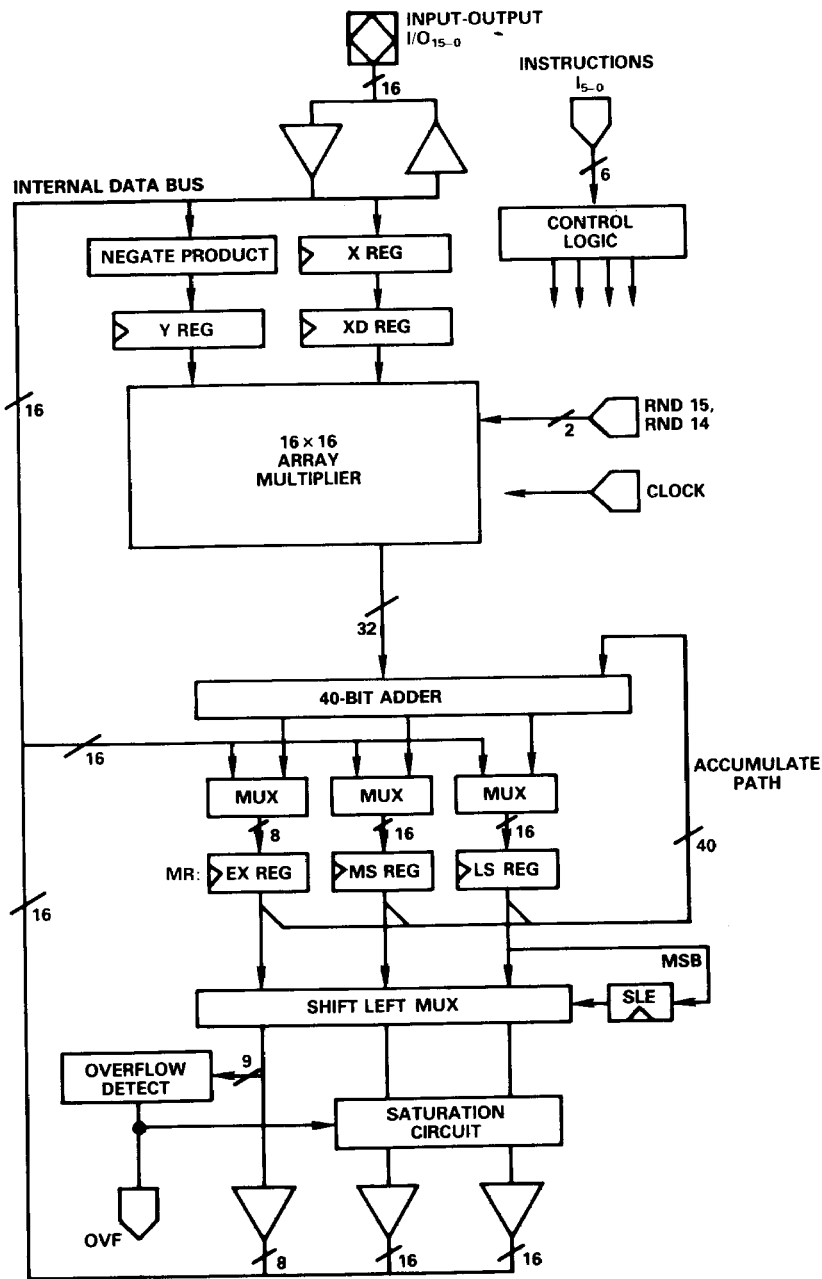
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	RND15	15	CLK
2	RND14	16	I ₃
3	I/O ₁₄	17	I ₄
4	I/O ₁₂	18	I ₅
5	I/O ₁₀	19	OVF
6	I/O ₈	20	I/O ₁
7	I/O ₆	21	I/O ₃
8	I/O ₄	22	I/O ₅
9	I/O ₂	23	I/O ₇
10	I/O ₀	24	I/O ₉
11	I ₀	25	I/O ₁₁
12	I ₁	26	I/O ₁₃
13	I ₂	27	I/O ₁₅
14	GND	28	V _{DD}

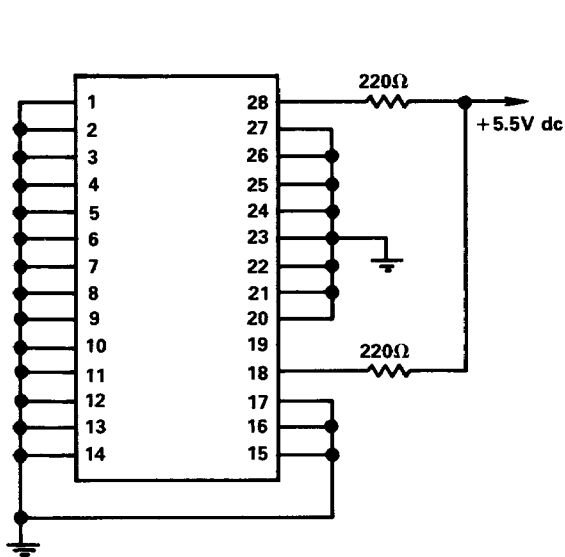
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

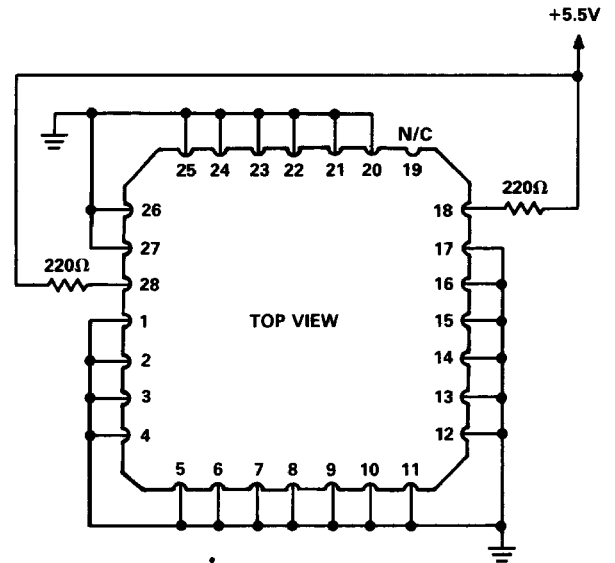
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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1110AD Life Test and Burn-In Circuit



ADSP-1110AE Life Test and Burn-In Circuit

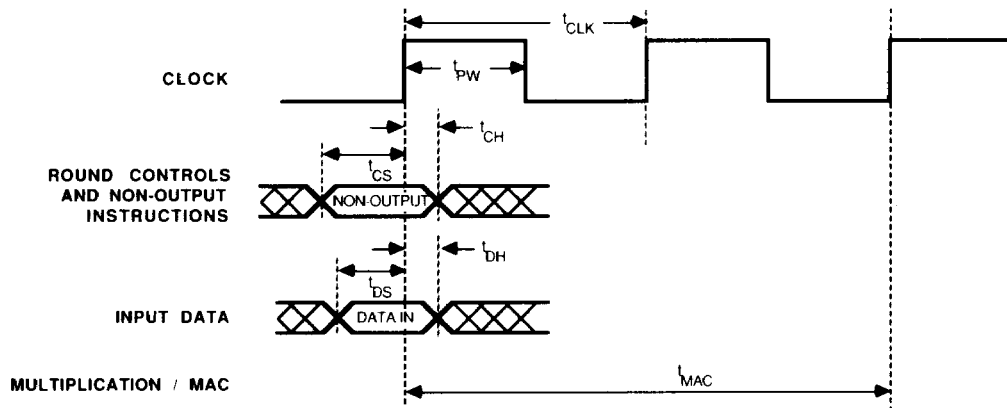


Figure 1. ADSP-1110A Timing: Clock (Synchronous) Operations All Non-Output Instructions

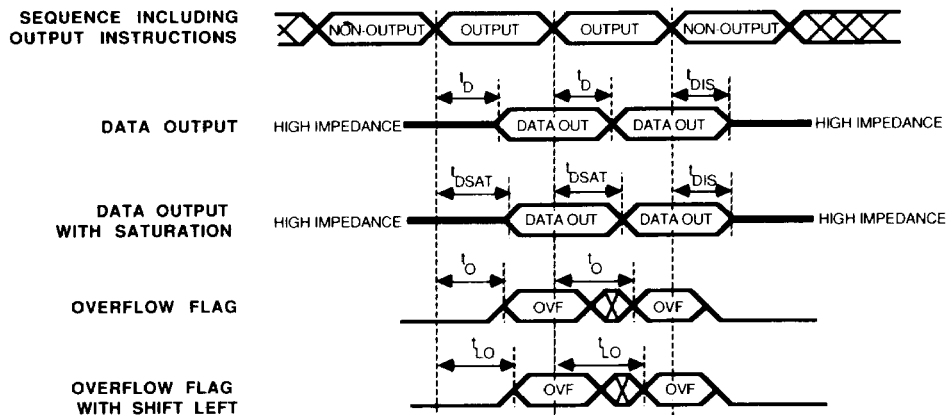


Figure 2. ADSP-1110A Timing: Unlocked (Asynchronous) Operations All Output Instructions

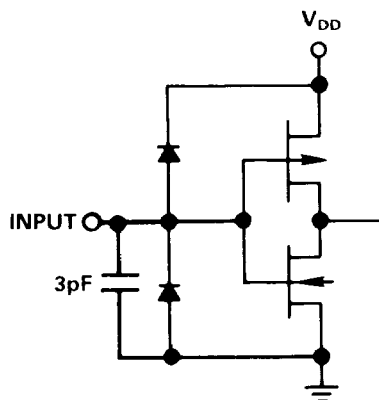


Figure 3. Equivalent Input Circuit

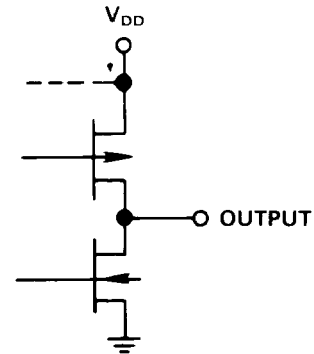


Figure 4. Equivalent Output Circuit

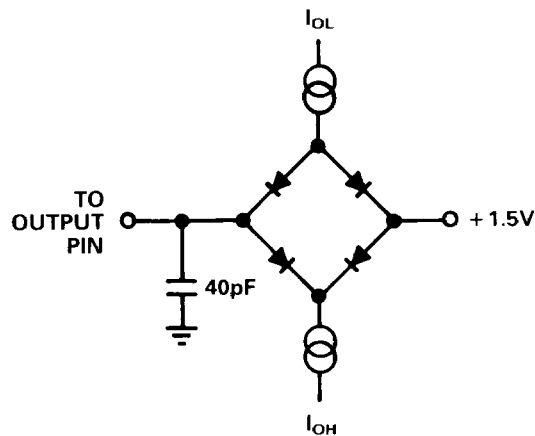


Figure 5. Normal Load Circuit for AC Measurements

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Instruction Group	Instruction	Microcode Instruction						Comments
		5	4	3	2	1	0	
Miscellaneous	NOP	0	0	0	0	X	X	No Operation
	CKMR	0	0	0	1	X	X	Clock MR
Input	X = BUS	0	0	1	0	X	X	
Preload	LS = BUS	0	1	0	0	0	0	
	MS = BUS	0	1	0	1	X	0	
	EX = BUS	0	1	0	0	1	0	
Transfer	LS = MS	0	1	0	0	0	1	Set SLE register
	MS = EX	0	1	0	1	0	1	
Sign Extend	EX = SIGN EXT MS	0	1	0	0	1	1	
	MS = SIG EXT LS	0	1	0	1	1	1	
Output	BUS = EX	0	0	1	1	0	1	All output instructions are asynchronous I5-I2: 0011 = EX 0110 = MS 0111 = LS I1-I0: 01 = to bus 00 = to bus shifted 10 = to bus shifted w/saturation 11 = to bus w/saturation
	BUS = EX (sl)	0	0	1	1	0	0	
	BUS = MS	0	1	1	0	0	1	
	BUS = MS (sl)	0	1	1	0	0	0	
	BUS = MS (sat)	0	1	1	0	1	1	
	BUS = MS (sl, sat)	0	1	1	0	1	0	
	BUS = LS	0	1	1	1	0	1	
	BUS = LS (sl)	0	1	1	1	0	0	
	BUS = LS (sat)	0	1	1	1	1	1	
	BUS = LS (sl, sat)	0	1	1	1	1	0	
Multi-Operation	Y = BUS; CKMR; X _{US} *Y _{US}	1	0	0	X	0	0	Require two cycles to complete. Other instructions can be executed on the second cycle. I5 = Multiply/MAC operation I4 = Y twos complement I3 = X twos complement I2 = Subtract previous result I1 = Add/subtract previous result from product I0 = Negate product
	Y = BUS; CKMR; -X _{US} *Y _{US}	1	0	0	X	0	1	
	Y = BUS; CKMR; X _{US} *Y _{US} +MR	1	0	0	0	1	0	
	Y = BUS; CKMR; -X _{US} *Y _{US} +MR	1	0	0	0	1	1	
	Y = BUS; CKMR; X _{US} *Y _{US} -MR	1	0	0	1	1	0	
	Y = BUS; CKMR; -X _{US} *Y _{US} -MR	1	0	0	1	1	1	
	Y = BUS; CKMR; X _{TC} *Y _{US}	1	0	1	X	0	0	
	Y = BUS; CKMR; -X _{TC} *Y _{US}	1	0	1	X	0	1	
	Y = BUS; CKMR; X _{TC} *Y _{US} +MR	1	0	1	0	1	0	
	Y = BUS; CKMR; -X _{TC} *Y _{US} +MR	1	0	1	0	1	1	
	Y = BUS; CKMR; X _{TC} *Y _{US} -MR	1	0	1	1	1	0	
	Y = BUS; CKMR; -X _{TC} *Y _{US} -MR	1	0	1	1	1	1	
	Y = BUS; CKMR; X _{US} *Y _{TC}	1	1	0	X	0	0	
	Y = BUS; CKMR; -X _{US} *Y _{TC}	1	1	0	X	0	1	
	Y = BUS; CKMR; X _{US} *Y _{TC} +MR	1	1	0	0	1	0	
	Y = BUS; CKMR; -X _{US} *Y _{TC} +MR	1	1	0	0	1	1	
	Y = BUS; CKMR; X _{US} *Y _{TC} -MR	1	1	0	1	1	0	
	Y = BUS; CKMR; -X _{US} *Y _{TC} -MR	1	1	0	1	1	1	
	Y = BUS; CKMR; X _{TC} *Y _{TC}	1	1	1	X	0	0	
	Y = BUS; CKMR; -X _{TC} *Y _{TC}	1	1	1	X	0	1	
	Y = BUS; CKMR; X _{TC} *Y _{TC} +MR	1	1	1	0	1	0	
	Y = BUS; CKMR; -X _{TC} *Y _{TC} +MR	1	1	1	0	1	1	
	Y = BUS; CKMR; X _{TC} *Y _{TC} -MR	1	1	1	1	1	0	
	Y = BUS; CKMR; -X _{TC} *Y _{TC} -MR	1	1	1	1	1	1	

Mnemonic Definitions

=	Assign right side to left.	sl	Shift left.
BUS	16-bit external data bus used for all I/O operations.	sat	Conditional on overflow, saturate the outputted value.
X	Input register for multiplier.	TC	Twos complement number.
Y	Input register for multiplier.	US	Unsigned magnitude number.
EX	8-bit extension register for accumulator.	SIGN	Sign bit (MSB) of specified register.
MS	16-bit most significant product register.	CKMR	Clock product into EX, MS and LS.
LS	16-bit least significant product register.	*	Multiply
MR	40-bit accumulator comprising EX, MS and LS.	X	Microcode instruction bit can be either a 0 or 1.

Table 2. ADSP-1110A Instruction Set