MOSFET – Power, N-Channel, Logic Level

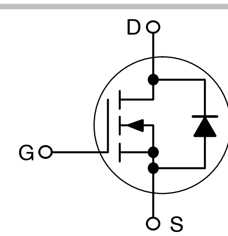
100 V, 25 A, 50 mΩ

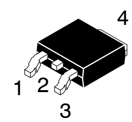
NVD6495NL

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	54 mΩ @ 4.5 V	25 A
	50 mΩ @ 10 V	





DPAK
CASE 369AA
STYLE 2

Features

- Low $R_{DS(on)}$
- 100% Avalanche Tested
- AEC−Q101 Qualified
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage − Continuous			V_{GS}	±20	V
Continuous Drain Current	Steady State	T_C = 25°C	I_D	25	A
		T_C = 100°C		18	
Power Dissipation	Steady State	T_C = 25°C	P_D	83	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	80	A
Operating and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	25	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, $I_{L(pk)}$ = 23 A, L = 0.3 mH, R_G = 25 Ω)			E_{AS}	79	mJ
Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds			T_L	260	°C

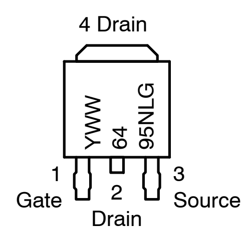
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case (Drain) − Steady State	$R_{\theta JC}$	1.8	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	49	

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

MARKING DIAGRAM & PIN ASSIGNMENT



6495NL	= Device Code
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = 250 μA, T_J = −40°C		100 92			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				115		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.8		mV/°C
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 10 A			44	54	mΩ
		V_{GS} = 10 V, I_D = 10 A			43	50	
Forward Transconductance	g_{FS}	V_{DS} = 5.0 V, I_D = 10 A			24		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1024		pF
Output Capacitance	C_{OSS}				156		
Reverse Transfer Capacitance	C_{RSS}				70		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 80 V, I_D = 23 A			20		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.1		
Gate−to−Source Charge	Q_{GS}				3.1		
Gate−to−Drain Charge	Q_{GD}				14		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 80 V, I_D = 23 A			35		nC
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DD} = 80 V, I_D = 23 A, R_G = 6.1 Ω			11		ns
Rise Time	t_r				91		
Turn−Off Delay Time	$t_{d(off)}$				40		
Fall Time	t_f				71		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 23 A	T_J = 25°C		0.87	1.2	V
			T_J = 125°C		0.74		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 23 A			64		ns
Charge Time	T_a				40		
Discharge Time	T_b				24		
Reverse Recovery Charge	Q_{RR}				152		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NVD6495NLT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

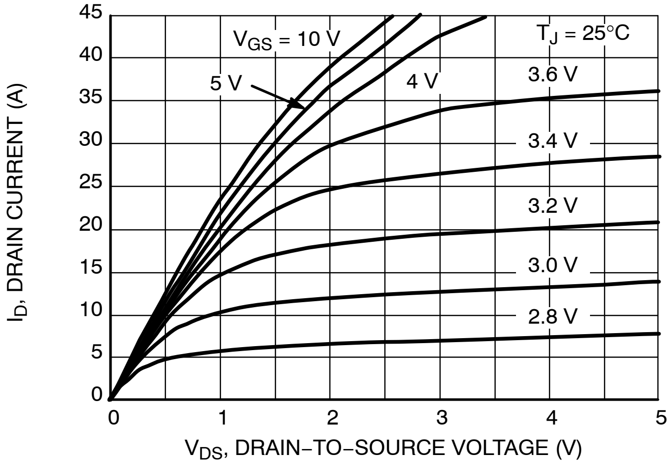


Figure 1. On−Region Characteristics

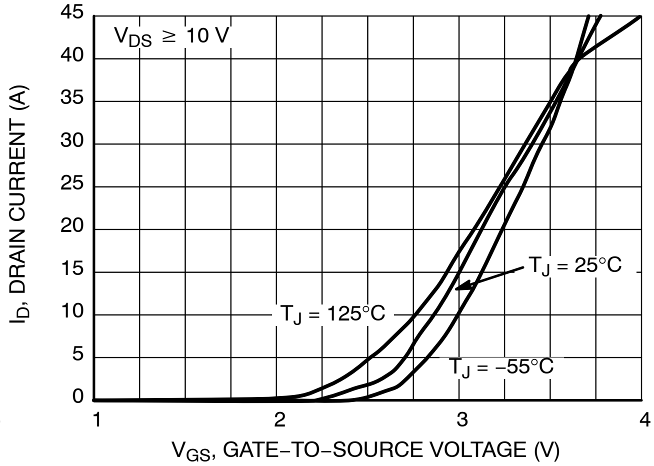


Figure 2. Transfer Characteristics

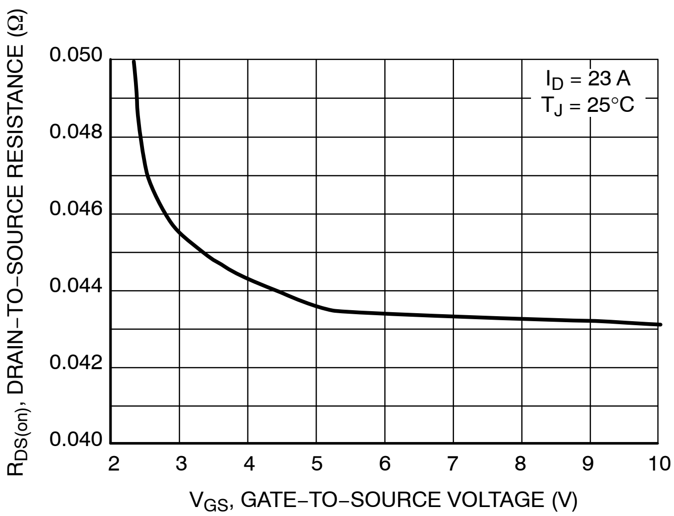


Figure 3. On−Region versus Gate Voltage

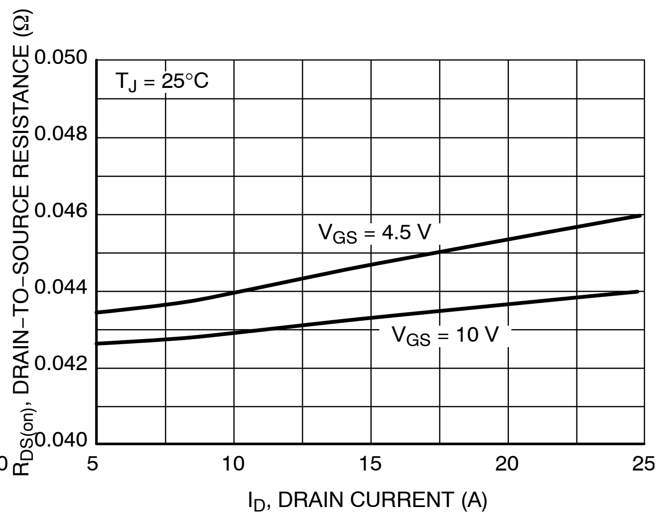


Figure 4. On−Resistance versus Drain Current and Gate Voltage

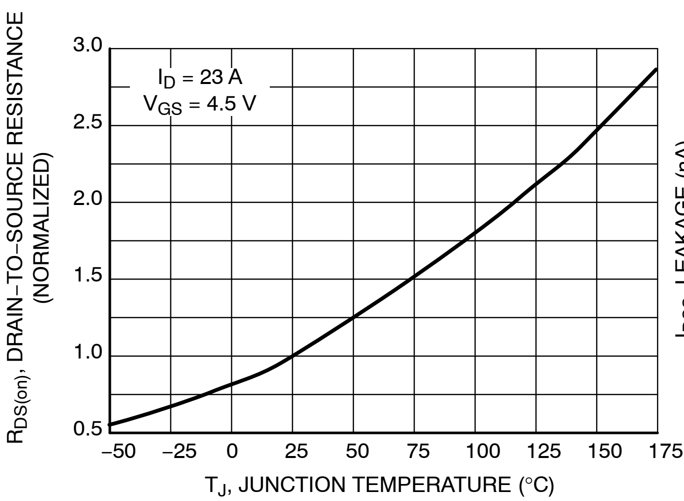


Figure 5. On−Resistance Variation with Temperature

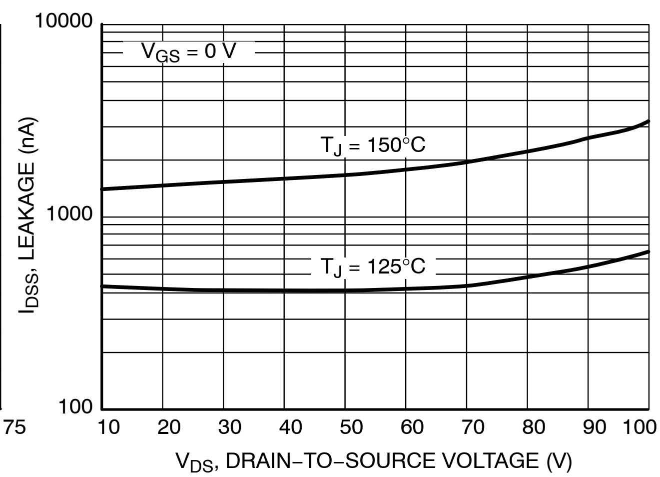


Figure 6. Drain−to−Source Leakage Current versus Voltage

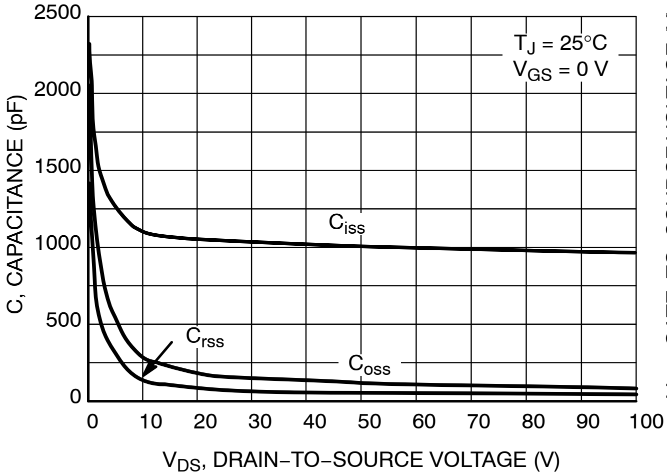


Figure 7. Capacitance Variation

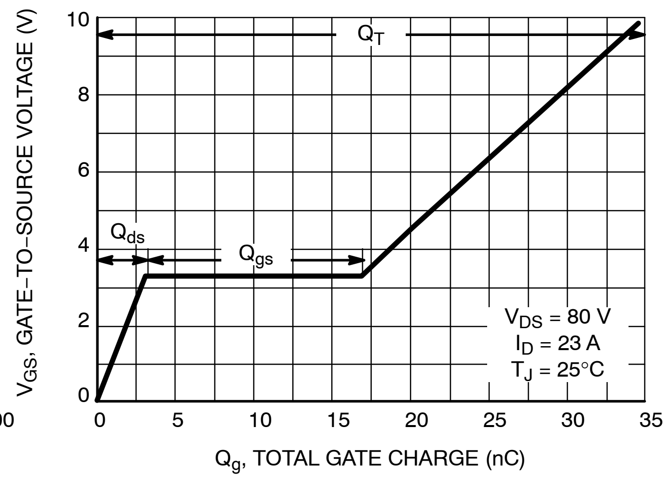


Figure 8. Gate−to−Source Voltage and Drain−to−Source Voltage versus Total Charge

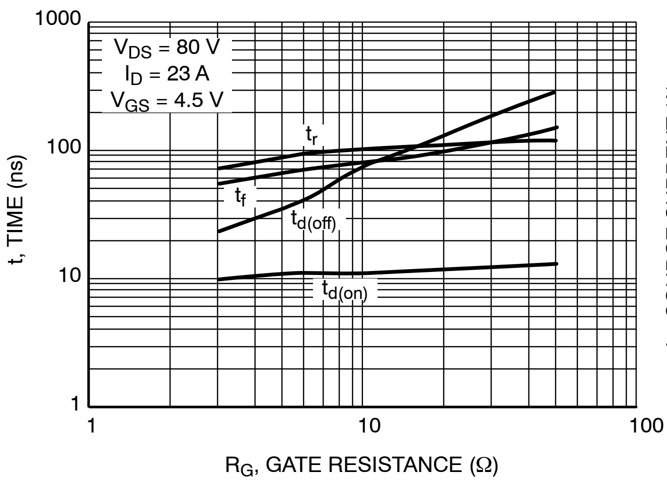


Figure 9. Resistive Switching Time Variation versus Gate Resistance

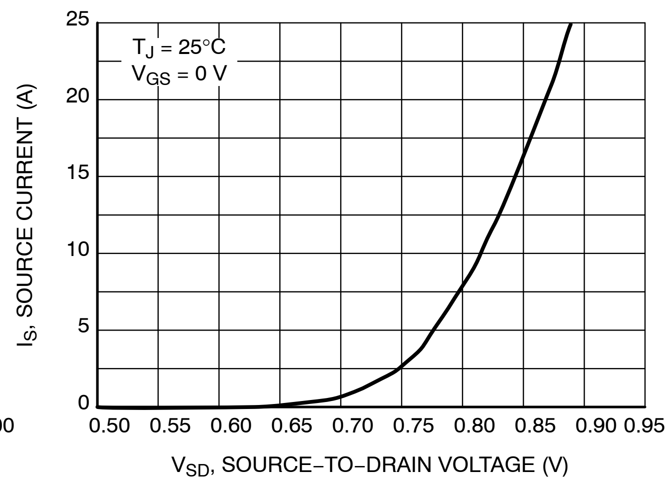


Figure 10. Diode Forward Voltage versus Current

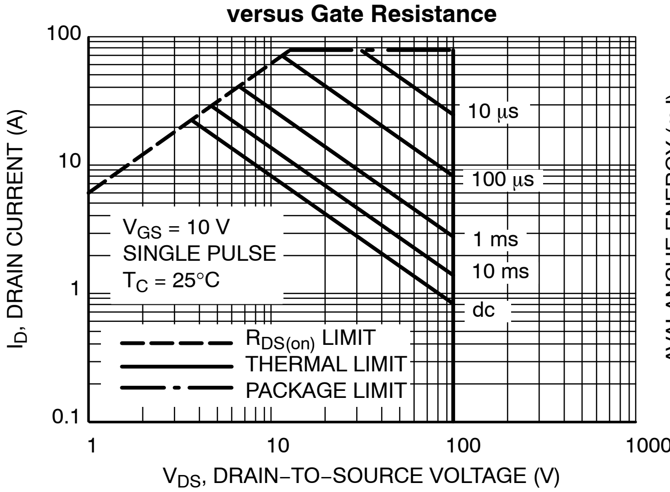


Figure 11. Maximum Rated Forward Biased Safe Operating Area

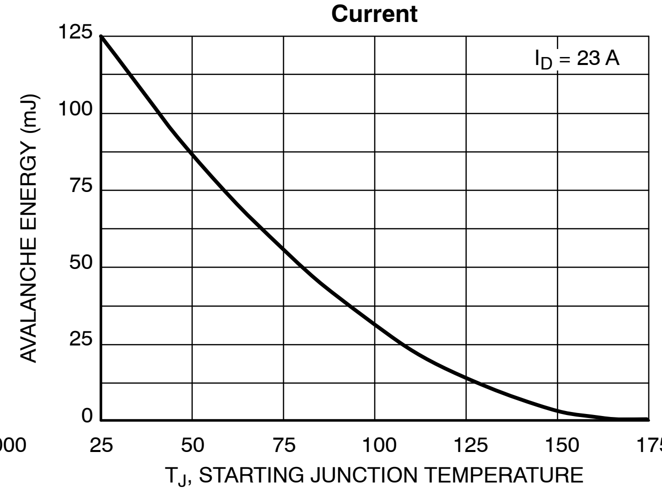


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

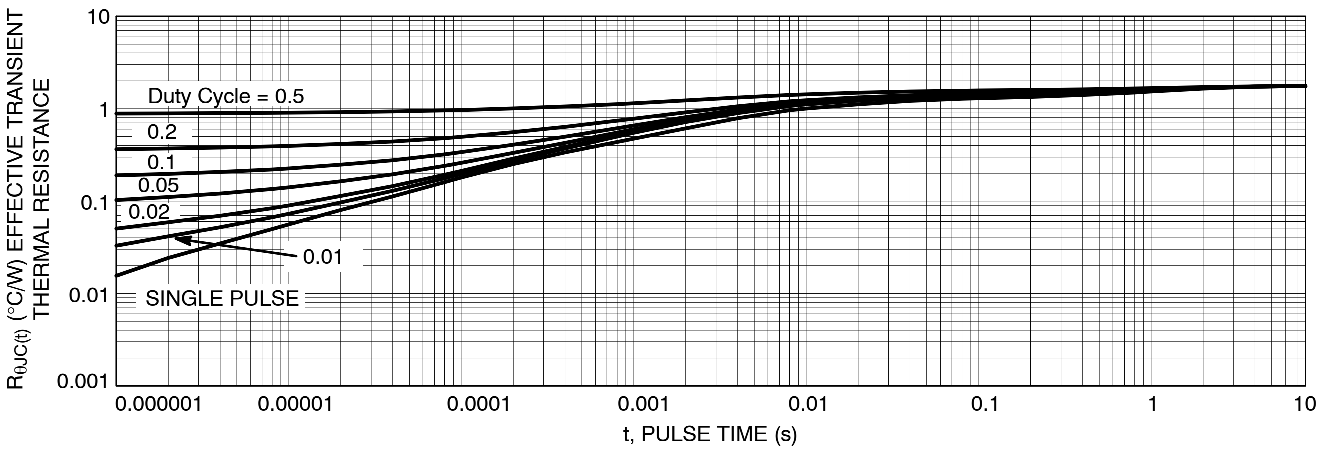
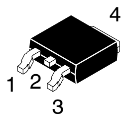


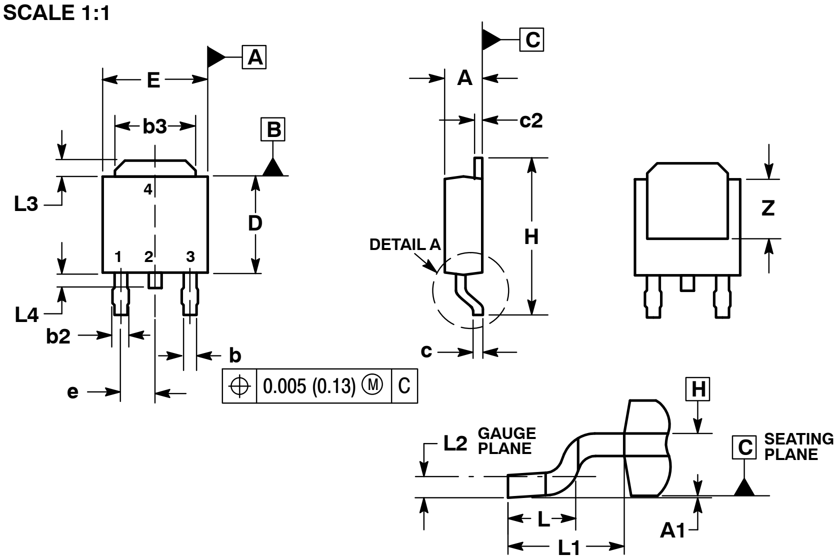
Figure 13. Thermal Response



SCALE 1:1

DPAK (SINGLE GUAGE)
CASE 369AA−01
ISSUE B

DATE 03 JUN 2010



DETAIL A
ROTATED 90° CW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

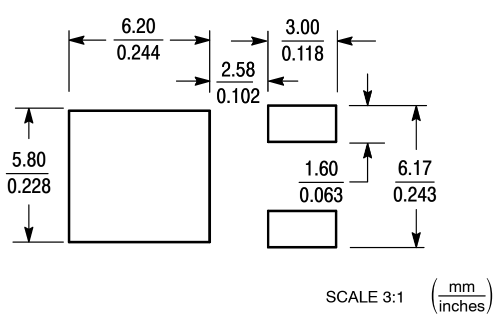
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

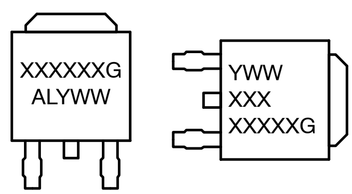
SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC   Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

DOCUMENT NUMBER:	98AON13126D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊