

# MT9V117PACSTCH-GEVB

## MT9V117 Evaluation Board User's Manual



ON Semiconductor®

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### EVAL BOARD USER'S MANUAL



Figure 1. MT9V117 Evaluation Board

#### Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 2X system. Test points and jumpers on the board provide access to clock, I/Os and other miscellaneous signals.

#### Features

- Clock Input
  - ◆ Default – 54 MHz crystal oscillator
  - ◆ Optional Demo 2X controlled MCIk
- Two Wire Serial Interface
  - ◆ Selectable base address
- Parallel Interface
- ROHS Compliant

#### Block Diagram

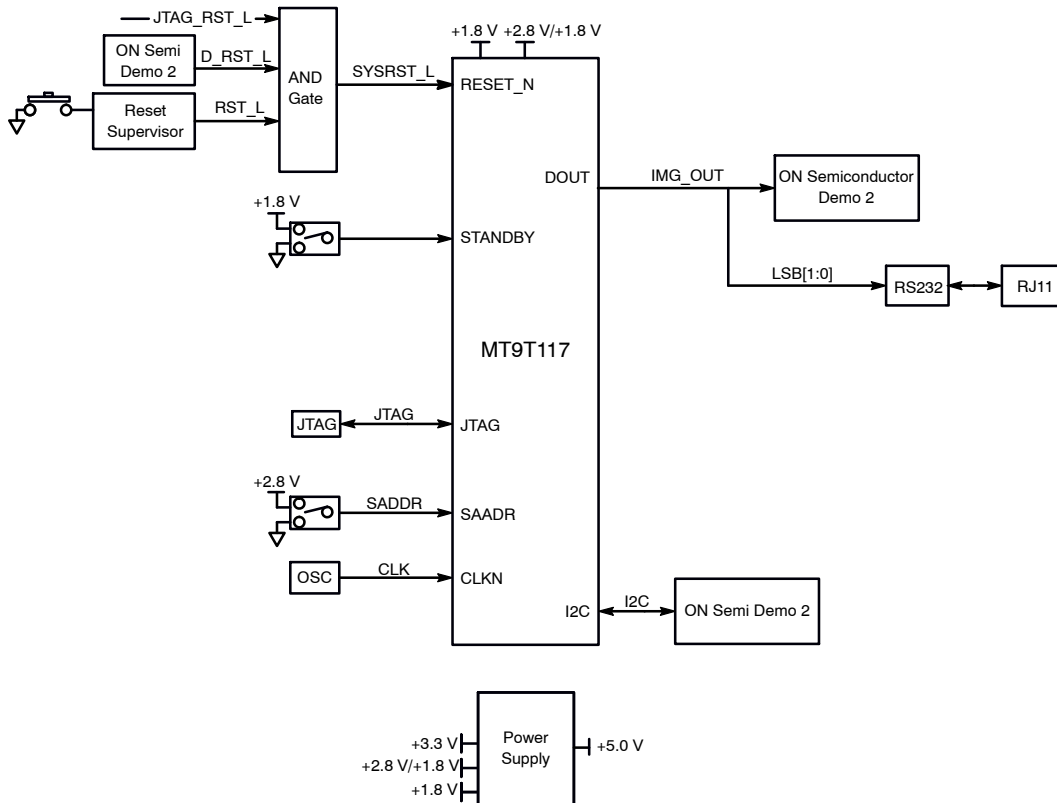


Figure 2. Block Diagram of MT9V117PACSTCH-GEVB

# MT9V117PACSTCH-GEVB

## Top View

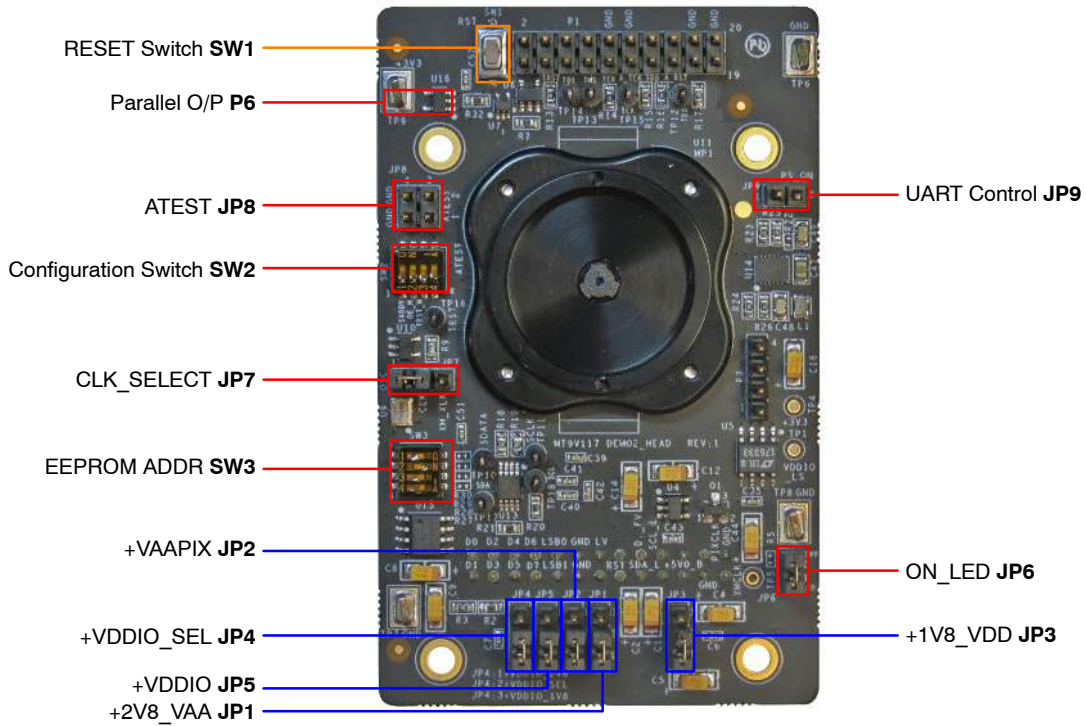


Figure 3. Top View of Evaluation Board – Default Jumpers

## Bottom View

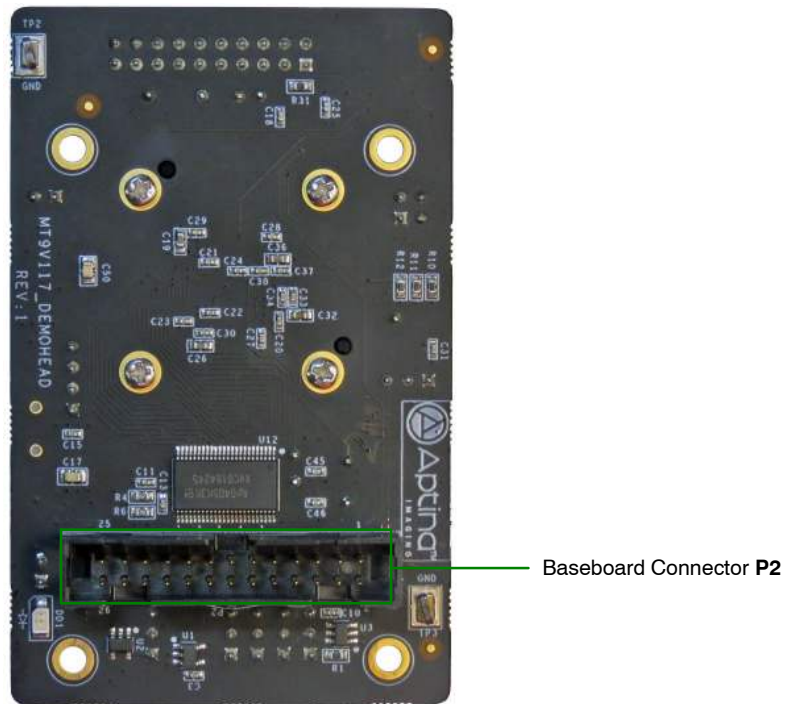
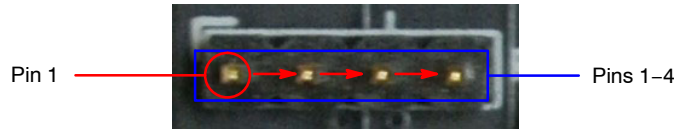


Figure 4. Bottom View of the Evaluation Board – Connector

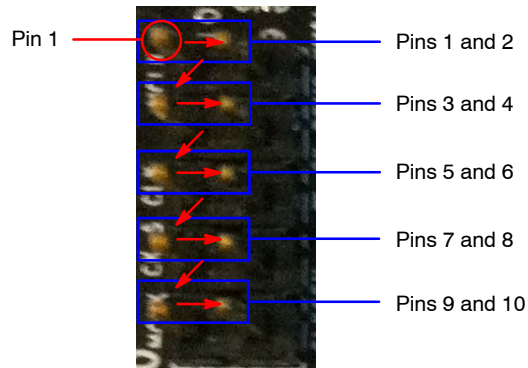
# MT9V117PACSTCH-GEVB

## Jumper Pin Locations

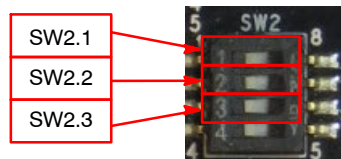
The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.



**Figure 5. Pin Locations for a Single Jumper.**  
Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right



**Figure 6. Pin Locations and Assignments of Grouped Jumpers.**  
Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture



**Figure 7. Switches of Configuration Switch SW2 in Their Default Positions.**  
SAADR (SW2.1), OE\_N (SW2.2), and TRST\_N (SW2.3) are All OFF by Default



**Figure 8. Address Switch Locations in their Default Positions.**  
The First Switch (ADR0) and the Second Switch (ADR1) of SW3 are Set to ON

## Jumper/Header Functions & Default Positions

**Table 1. JUMPERS AND HEADERS**

| Jumper/Header No. | Jumper/Header Name | Pins          | Description                                |
|-------------------|--------------------|---------------|--|
| JP1               | +2V8_VAA           | 1-2 (Default) | Connects to on-board +2V8_VAA power supply |
|                   |                    | 2-3           | External power supply connection           |
| JP2               | +VAAPIX            | 1-2 (Default) | Connects to on-board +VAAPIX power supply  |
|                   |                    | 2-3           | External power supply connection           |

## MT9V117PACSTCH-GEVB

**Table 1. JUMPERS AND HEADERS (continued)**

| Jumper/Header No. | Jumper/Header Name   | Pins                                  | Description  |
|-------------------|----------------------|---------------------------------------|--|
| JP3               | +1V8_VDD             | 1-2 (Default)                         | Connects to on-board +1V8_VDD power supply               |
|                   |                      | 2-3                                   | External power supply connection                         |
| JP4               | +VDDIO_SEL           | 1-2 (Default)                         | Sets +VDDIO to 2.8 V                                     |
|                   |                      | 2-3                                   | Sets +VDDIO to 1.8 V                                     |
| JP5               | +VDDIO               | 1-2 (Default)                         | Connection to on-board +VDDIO power supply               |
|                   |                      | 2-3                                   | External power supply connection                         |
| JP6               | ON_LED               | 1-2 (Default)                         | Connects LED to indicate power on                        |
| JP7               | CLK_SELECT           | 1-2 (Default)                         | Connects to on-board 54 MHz oscillator                   |
|                   |                      | 2-3                                   | Connects to XMCLK from Demo 2X board                     |
| JP8               | ATEST                | Open (Default)                        | For Debug/Test   |
| JP9               | UART Control         | Open (Default)                        | UART shutdown (Tri-State)                                |
|                   |                      | 1-2                                   | UART active  |
| SW1               | RESET                | N/A                                   | When pushed, 400 ms reset signal will be sent to MT9V117 |
| SW2               | Configuration Switch | SW2.1 ON (Default)                    | I <sup>2</sup> C address set to 0x90                     |
|                   |                      | SW2.1 OFF                             | I <sup>2</sup> C address set to 0xBA                     |
|                   |                      | SW2.2 ON (Default)                    | Normal Operation   |
|                   |                      | SW2.2 OFF                             | Tri-State Output   |
|                   |                      | SW2.3 ON (Default)                    | Normal Operation   |
|                   |                      | SW2.3 OFF                             | JTAG Mode  |
| SW3               | EEPROM ADDR          | A2 ON, A1 ON, A2 OFF, WP ON (Default) | EEPROM Address set to 0xA8                               |
|                   |                      | A0 OFF, A1 OFF, A2 OFF, WP ON         | EEPROM Address set to 0xAC                               |
|                   |                      | A0 ON, A1 OFF, A2 ON, WP ON           | EEPROM Address set to 0xA4                               |
|                   |                      | A0 ON, A1 ON, A2 ON, WP ON            | EEPROM Address set to 0xA0                               |

### Interfacing to ON Semiconductor Demo 2X Baseboard

The ON Semiconductor Demo 2X baseboard has a similar 26-pin connector which mates with P2 of the

headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

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