BLF7G27L-200PB

Power LDMOS transistor

AMPLEON

Rev. 3 — 1 September 2015

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 2600 MHz to 2700 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	2620 to 2690	1700	32	65	16.5	29	−30[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

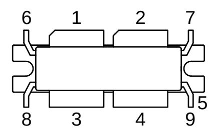
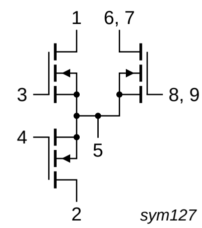
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2600 MHz to 2700 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
6, 7	sense drain		
8, 9	sense gate		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G27L-200PB	-	flanged LDMOST ceramic package; 2 mounting holes; 8 leads	SOT1110A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 65 W; V_{DS} = 32 V; I_{Dq} = 1700 mA	0.22	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.44 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 144 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	28	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.2 A	-	10.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.04 A	-	0.1	-	Ω
I_{Dq}	quiescent drain current	main transistor: V_{DS} = 32 V; sense transistor: I_{DS} = 31 mA, V_{DS} = 30.1 V	1530	1700	1870	mA

7. Test information

Remark: All testing performed in a class-AB production test circuit.

Table 7. Functional test information

Mode of operation: 2-carrier W-CDMA, PAR = 8.4 dB at 0.01 % probability on the CCDF, 3GPP test model 1; 1-64 DPCH; f_1 = 2622.5 MHz; f_2 = 2627.5 MHz; f_3 = 2682.5 MHz; f_4 = 2687.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 1700 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	65	-	W
G_p	power gain		14.8	16.5	17.7	dB
RL_{in}	input return loss		-	−15	−5	dB
η_D	drain efficiency		25.5	29	-	%
ACPR	adjacent channel power ratio		-	−30	−27	dBc

7.1 Ruggedness in class-AB operation

The BLF7G27L-200PB is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 1700 mA; P_L = 200 W (CW); f = 2600 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data half device; I_{Dq} = 850 mA; V_{DS} = 32 V.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)
2500	3.07 – j3.51	2.79 – j4.86
2600	4.51 – j12.51	2.61 – j4.49
2700	7.56 – j15.0	2.36 – j4.41

[1] Z_S and Z_L defined in Figure 1.

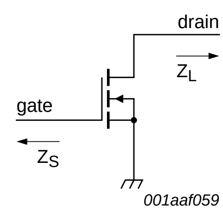
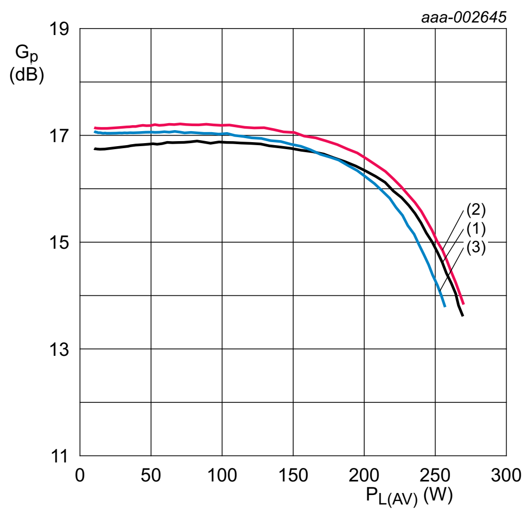


Fig 1. Definition of transistor impedance

7.3 1 Tone CW



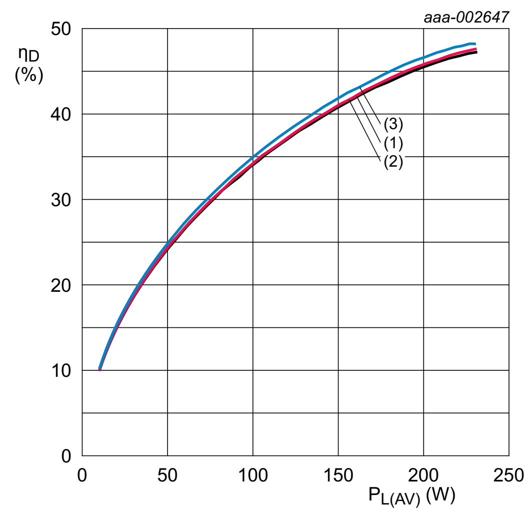
V_{DS} = 32 V; I_{Dq} = 1700 mA.

(1) f = 2600 MHz

(2) f = 2650 MHz

(3) f = 2700 MHz

Fig 2. Power gain as a function of average load power; typical values



V_{DS} = 32 V; I_{Dq} = 1700 mA.

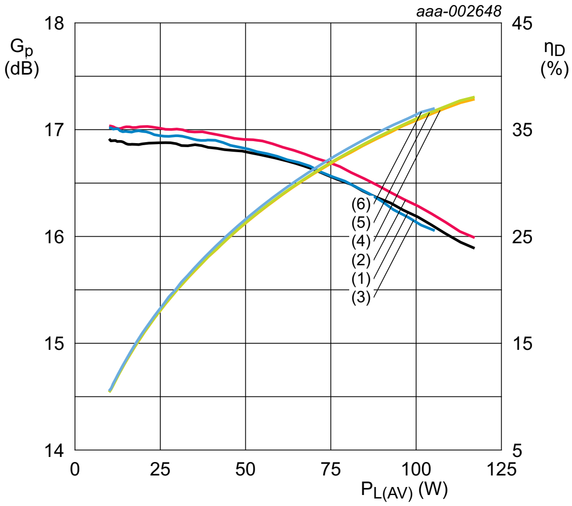
(1) f = 2600 MHz

(2) f = 2650 MHz

(3) f = 2700 MHz

Fig 3. Drain efficiency as a function of average load power; typical values

7.4 1-carrier W-CDMA



V_{DS} = 32 V; I_{Dq} = 1700 mA; PAR = 7.2 dB at 0.01 % probability on the CCDF.

(1) G_p; f = 2620 MHz

(2) G_p; f = 2650 MHz

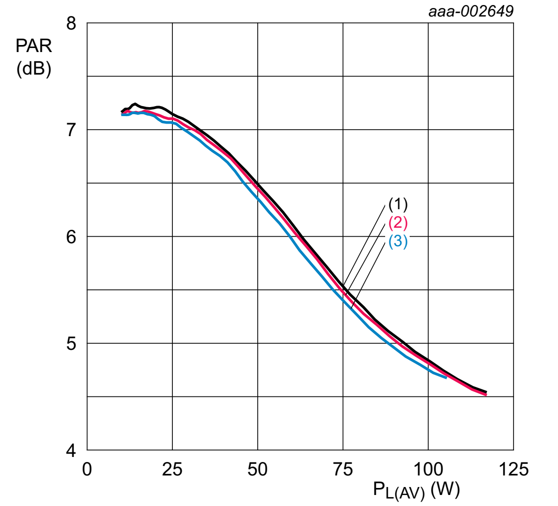
(3) G_p; f = 2690 MHz

(4) η_D; f = 2620 MHz

(5) η_D; f = 2650 MHz

(6) η_D; f = 2690 MHz

Fig 4. Power gain and drain efficiency as function of average load power; typical values



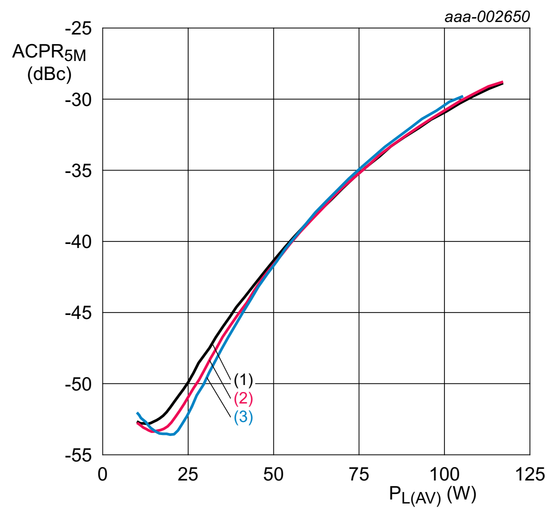
V_{DS} = 32 V; I_{Dq} = 1700 mA; PAR = 7.2 dB at 0.01 % probability on the CCDF.

(1) f = 2620 MHz

(2) f = 2650 MHz

(3) f = 2690 MHz

Fig 5. Peak-to-average power ratio as a function of peak power; typical values



V_{DS} = 32 V; I_{Dq} = 1700 mA; PAR = 7.2 dB at 0.01 % probability on the CCDF.

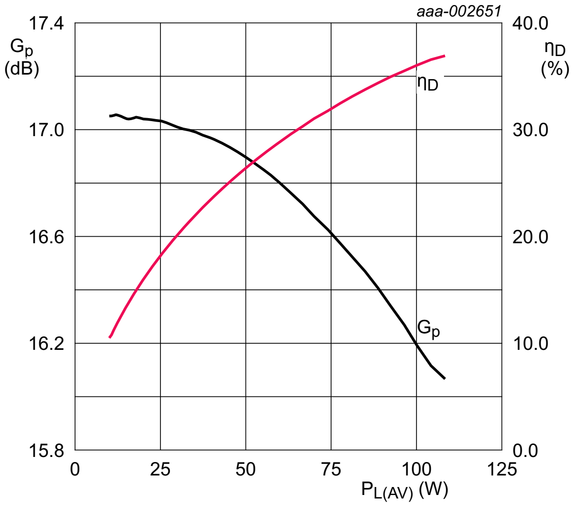
(1) f = 2620 MHz

(2) f = 2650 MHz

(3) f = 2690 MHz

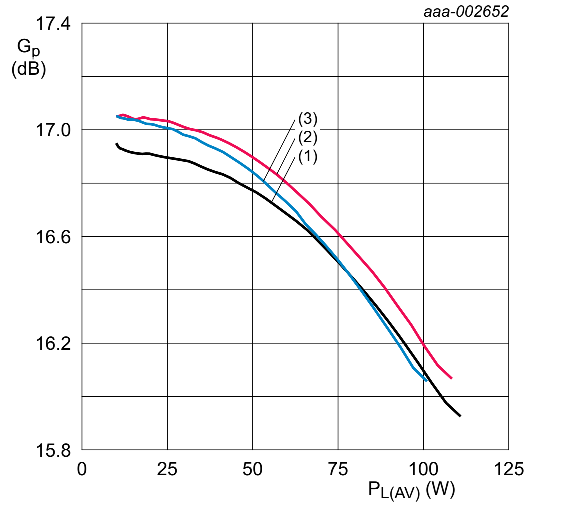
Fig 6. Adjacent power channel ratio (5 MHz) as a function of average load power; typical values

7.5 2-carrier W-CDMA



V_{DS} = 32 V; I_{Dq} = 1700 mA; f = 2650 MHz; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

Fig 7. Power gain and drain efficiency as function of average load power; typical values



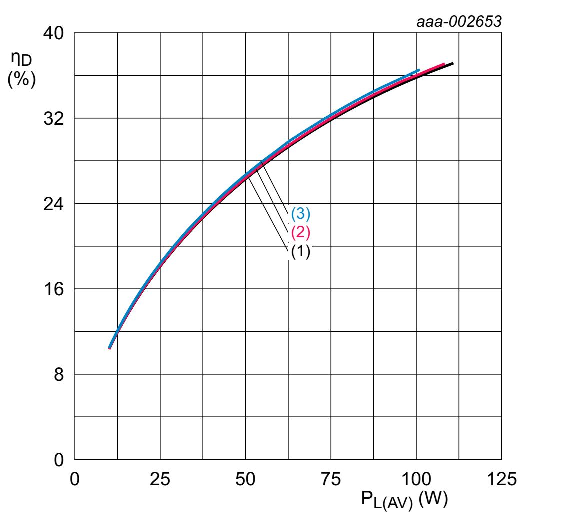
V_{DS} = 32 V; I_{Dq} = 1700 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

(1) f = 2620 MHz

(2) f = 2650 MHz

(3) f = 2690 MHz

Fig 8. Power gain as a function of average load power; typical values



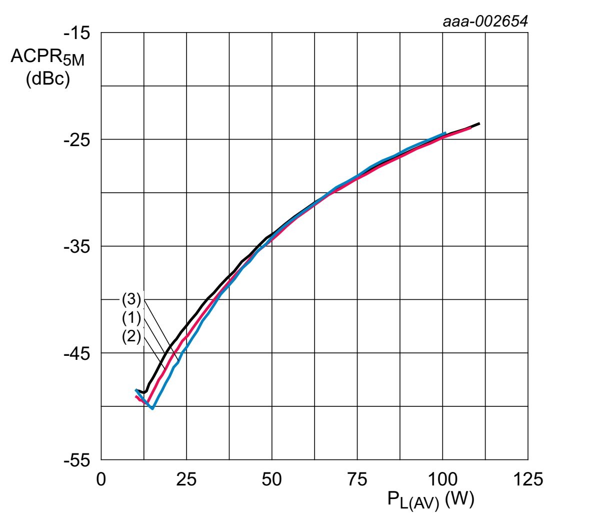
V_{DS} = 32 V; I_{Dq} = 1700 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

(1) f = 2620 MHz

(2) f = 2650 MHz

(3) f = 2690 MHz

Fig 9. Drain efficiency as a function of average load power; typical values



V_{DS} = 32 V; I_{Dq} = 1700 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

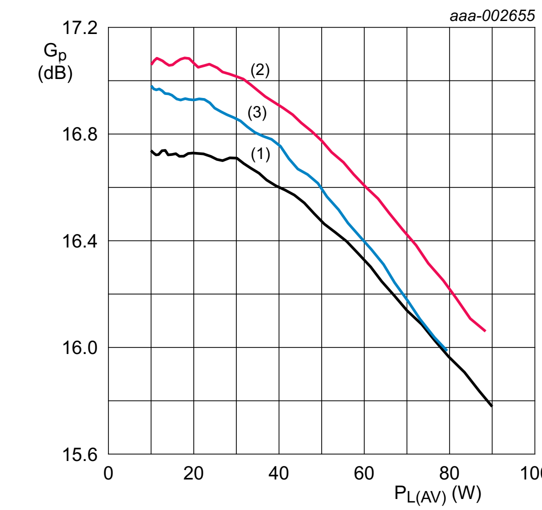
(1) f = 2620 MHz

(2) f = 2650 MHz

(3) f = 2690 MHz

Fig 10. Adjacent power channel ratio (5 MHz) as a function of average load power; typical values

7.6 IS-95



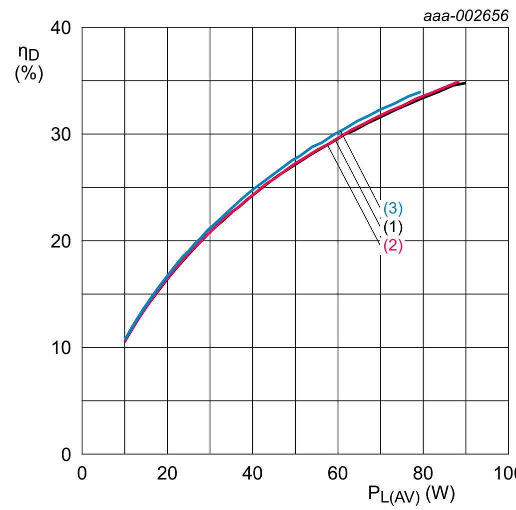
V_{DS} = 32 V; I_{Dq} = 1700 mA.

(1) f = 2600 MHz

(2) f = 2650 MHz

(3) f = 2700 MHz

Fig 11. Single carrier IS-95 power gain as a function of average output power; typical values



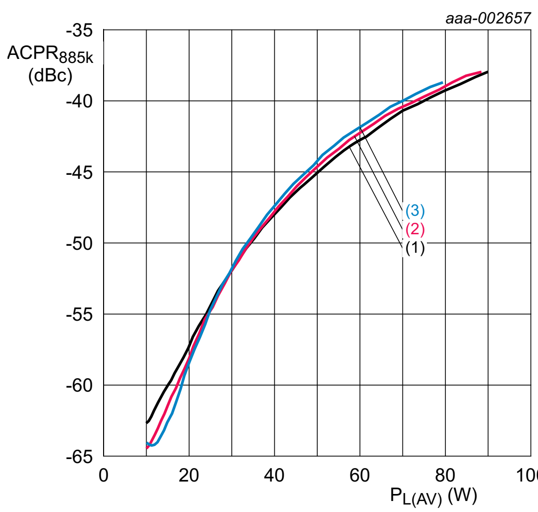
V_{DS} = 32 V; I_{Dq} = 1700 mA.

(1) f = 2600 MHz

(2) f = 2650 MHz

(3) f = 2700 MHz

Fig 12. Single carrier IS-95 drain efficiency as a function of average load power; typical values



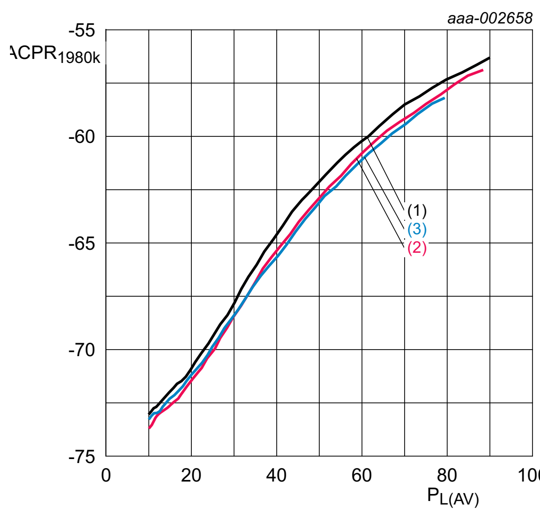
V_{DS} = 32 V; I_{Dq} = 1700 mA.

(1) f = 2600 MHz

(2) f = 2650 MHz

(3) f = 2700 MHz

Fig 13. Single carrier IS-95 ACPR at 885 kHz as a function of average output power; typical values



V_{DS} = 32 V; I_{Dq} = 1700 mA.

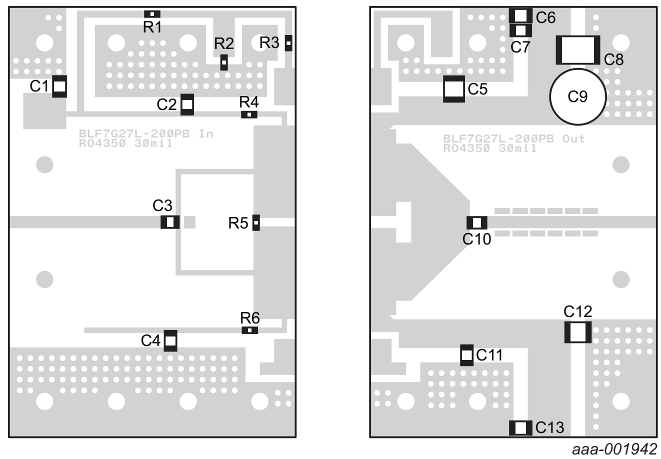
(1) f = 2600 MHz

(2) f = 2650 MHz

(3) f = 2700 MHz

Fig 14. Single carrier IS-95 at ACPR at 1980 kHz as a function of average output power; typical values

7.7 Test circuit



See Table 9 for list of components.

Fig 15. Component layout

Table 9. List of components

See Figure 15 for component layout.

The used PCB material is Rogers RO4350B with a thickness of 0.76 mm.

Component	Description	Value		Remarks
C1, C6, C13	multilayer ceramic chip capacitor	4.7 μF	[1]	Murata
C2, C4	multilayer ceramic chip capacitor	9.1 pF	[2]	ATC100B
C3	multilayer ceramic chip capacitor	22 pF	[3]	ATC100A
C5, C10, C11	multilayer ceramic chip capacitor	8.2 pF	[2]	ATC100B
C7	multilayer ceramic chip capacitor	470 nF	[4]	AVX
C8, C12	multilayer ceramic chip capacitor	10 μF	[5]	TDK
C9	electrolytic capacitor	470 μF		
R1	chip resistor	820 Ω	[6]	Philips 0603
R2	chip resistor	2K2 Ω	[6]	Philips 0603
R3	chip resistor	22 Ω	[6]	Philips 0603
R4, R6	chip resistor	10 Ω	[6]	Philips 0603
R5	chip resistor	33 Ω	[6]	Philips 0603

[1] Murata or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 100A or capacitor of same quality.

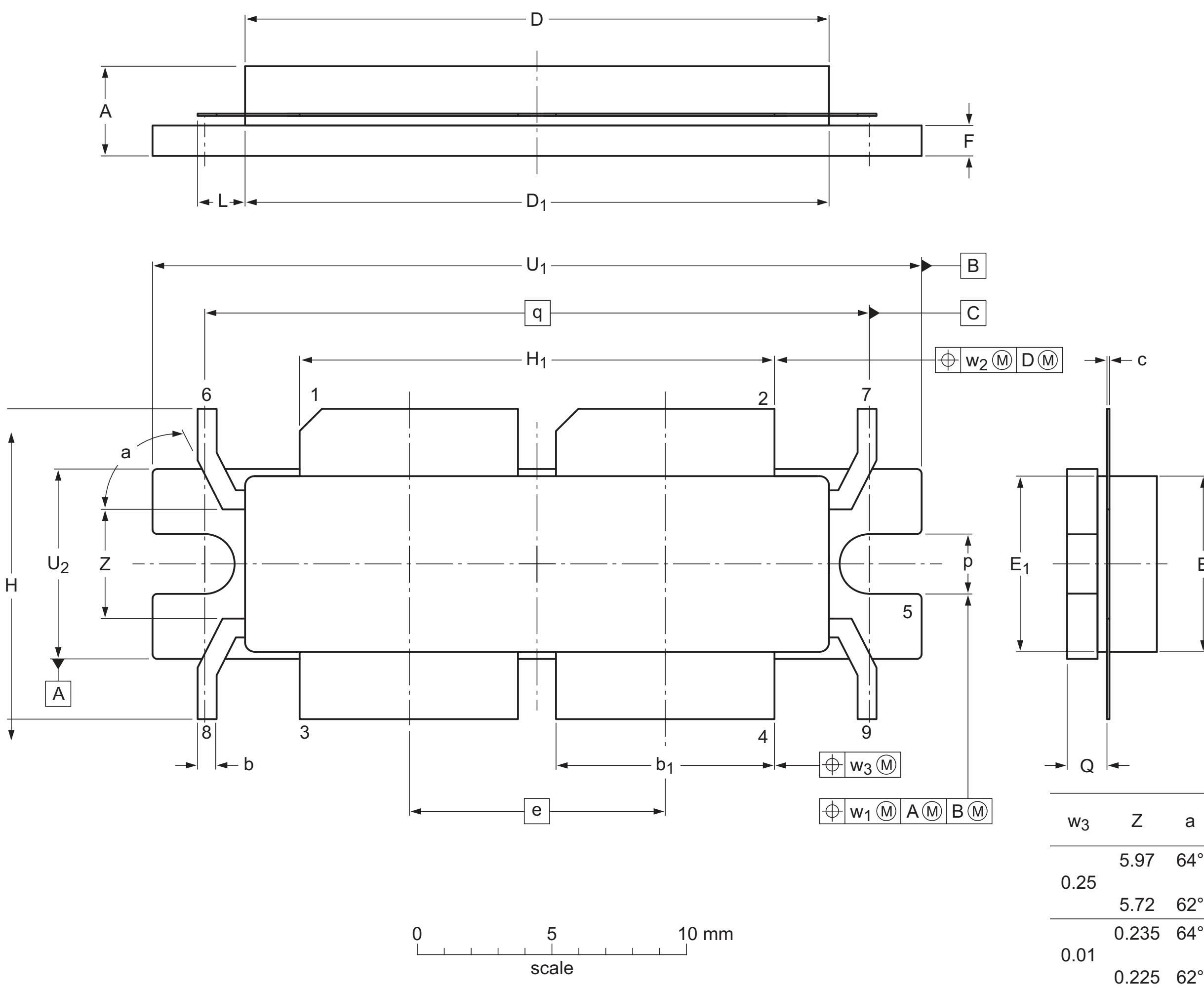
[4] AVX or capacitor of same quality.

[5] TDK or capacitor of same quality.

[6] Philips or resistor of same quality.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 8 leads **SOT1110A**



w_3	Z	a
0.25	5.97	64°
	5.72	62°
0.01	0.235	64°
	0.225	62°

Dimensions

Unit[1]		A	b	b_1	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q[2]	q	U_1	U_2	w_1	w_2
mm	max	5.36	1.14	11.81	0.18	31.55	31.52		9.50	9.53	1.75	17.12	25.53	2.67	3.30	2.26		41.28	10.29		
	nom							13.72									35.56			0.25	0.51
	min	3.99	0.89	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.41	3.05	2.01		41.02	10.03		
inches	max	0.211	0.045	0.465	0.007	1.242	1.241		0.374	0.375	0.069	0.674	1.005	0.105	0.13	0.089		1.625	0.405		
	nom							0.540									1.4			0.01	0.02
	min	0.157	0.035	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.095	0.12	0.079		1.615	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.
3. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

sot1110a_po

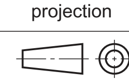
Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT1110A						~~10-02-02~~ 12-02-20

Fig 16. Package outline SOT1110A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G27L-200PB#3	20150901	Product data sheet	-	BLF7G27L-200PB v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF7G27L-200PB v.2	20120220	Product data sheet	-	BLF7G27L-200PB_27LS-200PB v.1
BLF7G27L-200PB_27LS-200PB v.1	20110405	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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