Intel® SM35 Express Chipset

Datasheet

January 2012

Revision 002

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Revision History

Revision	Version	Description	Revision Date
-001	1.0	• Initial release	April 2011
-002	2.0	• Updated Chapter 4	January 2012

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1 Read Me First

1.1 Abstract

The *Intel® SM35 Express Chipset Datasheet* describes the architecture, features, buffers, signal descriptions, register definition, power management, pin states, operating parameters, electrical, mechanical, and thermal specifications for the Platform Controller Hub (PCH).

The *Intel® SM35 Express Chipset Platform Controller Hub (PCH) Datasheet* is intended for use by hardware developers that are designing and manufacturing products using the Intel® SM35 Express Chipset PCH.

1.2 Reference Documents

Document	Document Number/ Location
Intel® Atom™ Processor Z6xx Series Datasheet For Intel® Atom™ Processor Z670 on 45-nm Process Technology	325310-001
Intel® Atom™ Processor Z6xx Series Specification Update for Intel® Atom™ Processor Z670 on 45-nm Process Technology	325309-001
Intel® SM35 Express Chipset Specification Update	325307-001
Universal Host Controller Interface, Revision 1.1 (UHCI)	ftp://download.intel.com/technology/usb/uhci11d.pdf
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Universal Serial Bus Specification (USB), Revision 2.0	http://www.usb.org/developers/docs
SDIO Specification	http://www.sdcard.org/developers/tech/sdio/sdio_spec/Simplified_SDIO_Card_Spec.pdf
SD Host Controller Specification	http://www.sdcard.org/developers/tech/host_controller/simple_spec/Simplified_SD_Host_Controller_Spec.pdf
I^2C Bus Specification	http://www.esacademy.com/faq/i2c/I2C_Bus_specification.pdf
Power Management IC (PMIC) Specification	Vendor Specific (Contact your PMIC vendor for the datasheet)

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2 Introduction

2.1 Overview

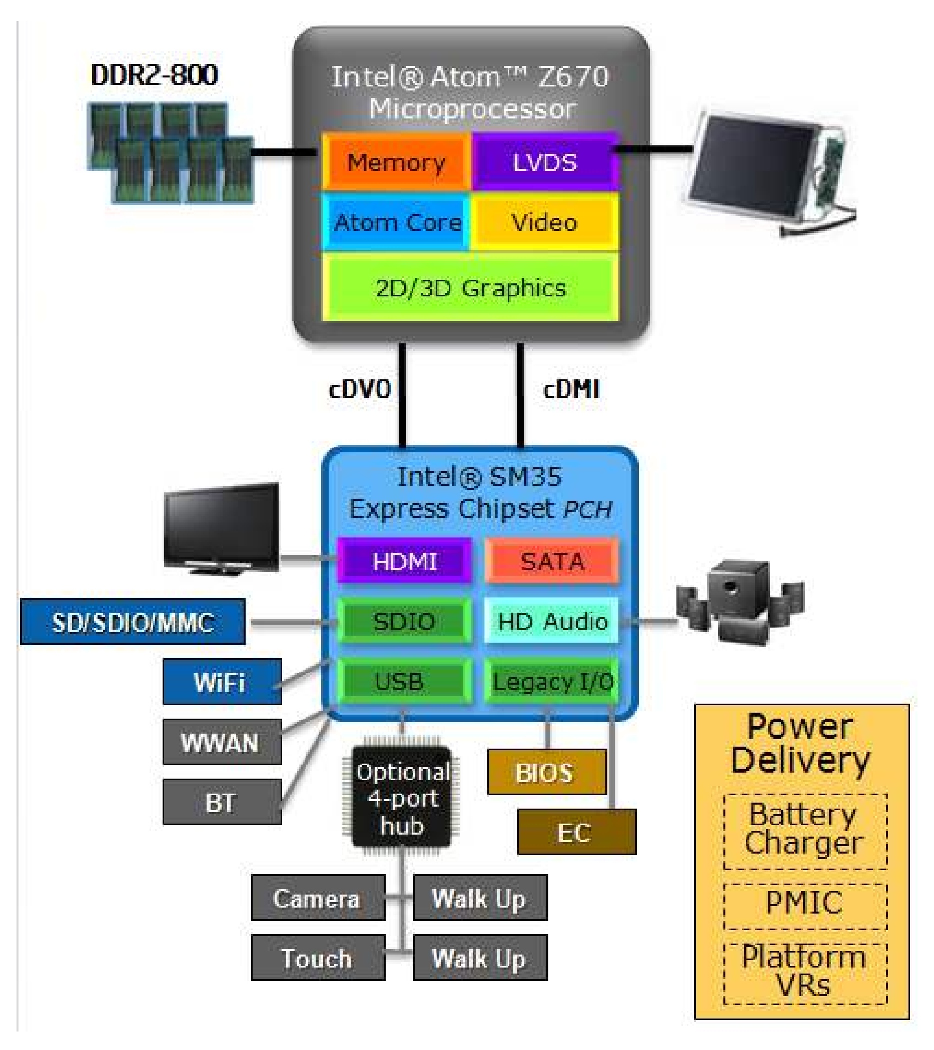
The Oak Trail platform consists of 3 chips:

- Intel® Atom™ Z670 Processor with Integrated Graphics and Memory Controller
- Intel® SM35 Express Chipset Platform Controller Hub (PCH)
- Power Management Integrated Circuit (PMIC)

Note: Throughout this document, the Intel® Atom™ Processor Z6xx Series is referred as the processor and Intel® SM35 Express Chipset is referred to as the PCH.

Below is a block diagram that describes the platform architecture.

Figure 2-1. Platform Block Diagram



The PCH is built around the AMBA protocol and OCP industry standard interfaces and interconnects. The Intel SM35 Express Chipset PCH is designed to leverage proven functional blocks from the System-on-Chip (SoC) ecosystem; thus, improving software stability and reducing time-to-market (TTM).

The PCH integrates accelerators and system control functions that are typically performed by the system CPU or programmable external components. This significantly reduces the system power for many applications and lowers the system cost and component count.

To protect personal data and play protected multimedia content, the PCH integrates a cryptographic engine. This engine performs high speed decryption of protected content and provides storage and management of cryptographic secret keys.

The PCH introduces several USB power saving features. In addition, PCH also allows the end device to reactivate the link when it needs attention. This significantly reduces platform power by eliminating USB polling in an otherwise idle system.

To reduce component count and board space the PCH integrates the system clock generation functions for the platform. The PCH also provides voltage control by means of the PMIC to optimize battery life. Additionally, it provides voltage and protocol conversion to drive a variety of external display standards.

2.2 PCH Feature Set

The major features of the PCH are:

- CMOS Direct Media Interface (cDMI)—Primary link between Processor and PCH
- CMOS Digital Video Out (cDVO)—Display Interface between Processor and PCH for driving external displays.
- Universal Serial Bus (USB) High Speed (HS)—In the box USB HS device interface
- One SD/SDIO/MMC interface
- One dedicated SDIO communication interface.
- Intel® HD Audio 1.0 Interface with two SDIs
- One HDMI 1.3a interface for external display
- Single ported AHCI 1.3 compliant SATA host controller with support for up to 3.0 Gbs (Gen2) transfer rate
- Three I2C interfaces to allow monitoring in-box environmental sensors and to control in-box components
- Two SPI master interfaces to interface with simple external devices (e.g., the touch screen controller or GPS device)
- Protocol/voltage level converters for external displays
- The system clock generator providing clocks for all components in the system except for the real-time clock.
- System Controller Unit (SCU)—Provides platform power management by use of PMIC and management system standby states
- Intel Legacy Block t(iLB) hat includes the following blocks
    - LPC
    - 8254
    - 8259
    - RTC
    - IOAPIC
- Support for ACPI 1.3 configuration and power managementSRAM—A 256-KB block of SRAM used for system boot code and other functions when system DRAM (connected to Processor) is unavailable.
    - This allows the processor to extend standby time and enhances battery life.
- DFx—Design for Test/Debug
    - Boundary Scan
    - JTAG access to System Controller Unit (SCU) to support power management and boot debug

The major features are outlined in the following sections:

2.2.1 cDMI

- Dual uni-directional interfaces between PCH and Processor
- cDMI operates at 400 MT/s in CMOS mode to reduce power consumption

2.2.2 cDVO

- Uni-directional display interfaces between PCH and Processor to drive external displays.
- cDMI operates at 800 MT/s in CMOS mode to reduce power consumption

2.2.3 USB

- Four (4), USB High Speed ports

2.2.4 SD/SDIO/MMC

- Two SDIO ports that support generic SD, SDIO or MMC device.
    - Supports for SD v2.0
    - SD and SDHC cards (Classes 2, 4, and 6)
    - Up to 200 Mb/s
    - Supports two operating voltages, 1.8 V or 3.3 V on Port 0
- Support SDIO v2.0: in the box SDIO connection
- One dedicated port (SDIO Port 2) for communication devices.

2.2.5 I^2C, and SPI Inputs and Outputs

I^2C, and SPI are described in this section. The other inputs and outputs are covered in their respective sections.

2.2.5.1 Inter-Integrated Circuit (I^2C) Controller

The PCH supports three instances of the I^2C controller. Both seven (7)-bit and 10-bit addressing modes are supported. These controllers operate in master mode only.

Modes of operation:

- Standard Speed Mode = 100 Kb/s
- Fast Mode = 400 Kb/s
- High Speed Mode = 3.4 Mb/s

2.2.5.2 Serial Peripheral Interface (SPI)

- The PCH implements two SPI master controllers
  - SPI1 contain four (4) chip select which are managed by the SCU.
  - SPI2: one chip select. This controller is exclusively accessed by the SCU and is used for controlling the PMIC.
- Default format - Motorola SPI
- Master configuration
- Receive FIFO buffer depth is 40
- Transmit FIFO buffer depth is 40

2.2.6 Integrated Clocking

The system clock generator provides timing for all components in the system except for the real-time clock.

The PCH is responsible for generating most of the peripheral and source clocks on the entire platform. It creates these clocks using a 25 MHz reference crystal, an integrated Pierce Oscillator, and three PLLs.

2.2.6.1 Output clocks

- BCLK: 100 MHz differential
- LPC Clock: 33 MHz

2.2.7 System Controller Unit (SCU)

The System Controller Unit is one of the first subsystems that is functional after reset. The SCU is ON all the time and is designed to use very little power. It is responsible for the following functionality:

- System boot including loading boot block code for IA
- Platform Level Configuration Block
- Implements sequencer logic for clock gating
- Implements Message Signaled Interrupts (MSI)—I/O APIC Emulation

- Handles interrupts and wakeup events
- Receive messages from Intel® Atom™ Z670 Processor
- Communication with Low Speed peripherals
- Eight (8) count-down timers that can generate periodic or single interrupts
- Implement Virtual RTC (copy of PMIC RTC).

2.2.8 Comprehensive Power Management

PCH is responsible for controlling the regulation of its own external power supplies and does so by communicating with the Power Management IC (PMIC), over a dedicated SPI interface.

The PCH will support a number power saving features. These are split into two categories—clock services and power domain delivery.

The following is a list of Platform Power Management features:

- Supports removal of external I/O voltages by means of communication with the PMIC over dedicated SPI interface
- SDIO insertion detection plus negotiated I/O voltage ranging from 3.3 to 1.8 volts
- Platform selectable I/O termination for low-speed interfaces
- GPIO I/O supports 3.3 volts
- Support Platform DDR Self-Refresh by means of an external pin (SRFWEN#) to save host processor power.

The PCH integrates enhanced features that dynamically adapts energy consumption according to application needs and performance requirements. Some of the features that the PCH adapts to control energy consumption and performance requirement are:

- Clock Gating
  - — Register-based, coarse-grain clock-gating for entire core subsystem
  - — Auto hardware clock gating for some clients and sub clients to reduce C0 dynamic
  - — Programmable clock speed ratios to reduce C0 dynamic power.

2.2.9 SRAM

The SRAM used in the PCH is essentially a single port (1RW), fully pipelined RAM with a throughput and latency of one (1) cycle. The total capacity is 256 Kb. It is divided into eight 32 Kb chunks (8 physical 32 Kb instances). The SRAM will be shared between multiple agents in the PCH, USB, and the System Controller.

The SRAM controller acts as the interface between the PCH Fabric and RAM. It provides secure access to RAM in addition to the protocol conversion between the Fabric and RAM.

2.2.10 HDMI Supported Video Resolution and Audio Frequencies

Table 2-1. HDMI Supported Video Resolution and Audio Frequency Combinations

Resolution	Stall Used	H Blank	Max 2 Channel Supported	Max >2 and <=8 Channels Supported
640x480p@60	32 (0x1000= 0x67)	160	96 KHz	None
720x576p@60	32 (0x1000= 0x67)	144	96 KHz	None
720x480p@60	32 (0x1000= 0x67)	138	96 KHz	None
800x600p@60	64 (0x1000=0x167)	256	192 KHz	48 KHz
720x576p@100	32 (0x1000= 0x67)	144	192 KHz	48 KHz
1440x480p@60	96 (0x1000=0x267)	276	192 KHz	48 KHz
1024x768p@60	128(0x1000=0x367)	320	192 KHz	96 KHz
1280x720p@60	160(0x1000=0x467)	370	192 KHz	192 KHz
1920x1080p@24	224 (0x1000=0x667)	830	192 KHz	176.4 KHz
1920x1080p@30	96 (0x1000=0x267)	280	192 KHz	88.2 KHz
1920x1080p@25	224(0x1000=0x667)	720	192 KHz	192 KHz
1280x720p@50	224(0x1000=0x667)	370	192 KHz	176.4 KHz
1360x768p@60	224(0x1000=0x667)	432	192 KHz	192 KHz
1440x900p@60	224(0x1000=0x667)	464	192 KHz	192 KHz
1280x960p@60	224(0x1000=0x667)	520	192 KHz	192 KHz

1. HDMI certification is being validated at 1080p @ 30 Hz with 75 Mhz doc clock. 1080p @ 60 Hz is not currently supported.
2. The resolution highlighted in RED, indicates that the audio channel and frequency supported for that particular resolution do not meet the spec requirements.

2.2.11 DFx Feature

The PCH supports the 1149.1 JTAG interface and the Boundary Scan specification on most of the input, output, and I/O signals.

Note: The details of the boundary scan capabilities are covered in the BSDL files.

2.3 External/Industry Standard Interfaces

The PCH adheres to the following external specifications:

- USB
- D/SDIO/MMC
- Serial ATA Specification Revision 2.6
- HDMI1.3a
- I2C
- SPI
- LPC
- Intel HD Audio

2.4 Terminology

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
AOAC	Always On, Always Connected
AC	Audio Codec
BGA	Ball Grid Array
Bluetooth, BT	Bluetooth is a local connectivity wireless protocol. Bluetooth supports the transport of unencoded voice signals (that is, wireless headsets). Bluetooth* basebands typically have a PCM audio interface for the unencoded voice data and a UART or USB for control, data, and compressed audio (using sub-band coding).
cDMI	CMOS Direct Media Interface
cDVO	CMOS Digital Video Out
CI/CSI	Camera Interface/Camera Sideband Interface
CSB	Camera Side Band signals
eMMC	Embedded MultiMedia Card
ESSP	Enhanced Synchronous Serial Port
FIPS	Federal Information Processing Standards
GPIO	General Purpose Input Output
GPS	Global Positioning Satellite
Host	This term is used synonymously with the processor.
JTAG	Joint Test Action Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling
MLC	Multiple Layer Cell
MMC	MultiMedia Card
MSI	Message Signaled Interrupt—MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
Multi-drop	Indicates that a line goes to several devices on a board. Multi-drop buses make use of multi-drop lines to provide a data transport between multiple devices. Output drivers of devices on a multi-drop line often tri-state to avoid bus contention.
OCP	Open Core Protocol
OCP-IP	Open Core Protocol International Partnership
PCH	Platform Controller Hub
PCM interface	Basic serial interface providing connectivity processors and audio sources/sinks. Data format commonly used is PCM though compounded variants are also used. The simplest PCM interface has lines for CLK, SYNC, TxDATA, and RxDATA though 6-wire PCM interfaces with rate-independent transmit and receive subsections are also used. Many variations in PCM interfaces exist (rising-edge clock versus falling-edge clock, positive polarity SYNC versus negative polarity SYNC, bit-length SYNC versus word-length SYNC.

Acronym	Description
PMIC SPI	Power Management Integrated Controller Serial Peripheral Interface
Pulse Code Modulation (PCM)	Standard technique of representing an audio stream using x bits sampled uniformly y times a second. Each sample captures the amplitude of the signal at that point in time. PCM samples are sent over serial buses between processors and audio codecs.
RO	Reset Out
SCU	System Controller Unit
SD	Secure Digital Memory Device
SDIO	Secure Digital I/O
SLC	Single Layer Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
Tristate	An output is tri-stated when it is not actively driven either high or low. Output drivers on a serial bus are often tri-stated to allow other devices to communicate on the same line. The electrical state of such line is determined by either the output of another driver on the same line (if being actively driven), by a pull-up/down resistor, or by a weak keeper
USB	Universal Serial Bus
UTMI	USB Transceiver Macrocell Interface
Voice codec	A voice codec typically contains one (or more ADCs) and one DAC tailored for voice-band operation (8 kHz, 16 kHz, and 26 kHz). The voice codec is a key device during a voice call.
WLAN	Wireless Local Area Network

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3 Signal Descriptions

3.1 Buffer Types and Descriptions

Below table describes various buffers used on the PCH. CMOS18, CMOS25 and CMOS33 buffer are based on the same CMOSXX buffer. The COMSXX buffer is capable to support 1.8 V, 2.5 V, and 3.3 V operation. The CMOS18, CMOS25, and CMOS33 represent the default configuration of the buffer set by the SCU Firmware.

Table 3-2. PCH I/O Buffer Characteristics

Type	Description
CMOS105	1.05 V CMOS buffers
CMOS18	CMOS buffers configured for 1.8 V operation
CMOS25	CMOS buffers configured for 2.5 V operation
CMOS33	CMOS buffers configured for 3.3 V operation
CMOSXX	CMOS buffers that can be configured for 3.3 V, 2.5 V, or 1.8 V operation
USB-HS	USB Hi-speed buffer type
A	Analog reference or output—May be used as a threshold voltage or for buffer compensation.

3.2 PCH Signal and Pin Descriptions

Each signal description table has the following headings:

- **Signal/Pin:** The name of the signal/pin that supports the interface.
- **Type:** The buffer direction. Buffer direction can be either Input (I), Output (O), or I/O (bi-directional).
- **Reset State:** Signal level while reset.
- **Description:** A brief explanation of the signal function.

3.2.1 cDMI Interface

Table 3-3. cDMI Interface Signals (Sheet 1 of 2)

Signal/Pin	Type	Reset State	Description
cDMI_TXD[7:0]	O	Z	cMOS DMI Transmit Data out to North Complex
cDMI_TXSP	O	Z	cMOS DMI Transmit Data Strobe Positive
cDMI_TXSN	O	Z	cMOS DMI Transmit Data Strobe Negative
cDMI_TXCHAR#	O	Z	cMOS DMI Transmit Control for command or data

Table 3-3. cDMI Interface Signals (Sheet 2 of 2)

Signal/ Pin	Type	Reset State	Description
cDMI_TXPWR#	O	Z	cMOS DMI Transmit Power Management This active low signal is used to gate-off input sense amps to save power in receiving chip. Signal must desasserted at least 2 clocks before sending data to the North complex.
cDMI_RXD[7:0]	I	Z	cMOS DMI Receive Data out to North Complex
cDMI_RXSP	I	Z	cMOS DMI Receive Data Strobe Positive
cDMI_RXSN	I	Z	cMOS DMI Receive Data Strobe Negative
cDMI_RXCHAR#	I	Z	cMOS DMI Receive Control for command or data
cDMI_RXPWR#	I	Z	cMOS DMI Receive Power Management control. This active low signal is used to gate-off PCH input sense amps to save power when asserted.
cDMI_CCOMP	A	N/A	cMOS Compensation
cDMI_GCOMP	A	N/A	GTL Compensation
CDMI_RX_CVREF	A	N/A	cMOS VREF for cDMI receiver
CDMI_RX_GVREF	A	N/A	GTL VREF for cDMI receivers

3.2.2 cDVO Interface

Table 3-4. cDMI Interface Signals

Signal/ Pin	Type	Reset State	Description
cDVO_RXD[5:0]	I	Z	cMOS Display Link Receive Data – 6 bits of data
cDVO_RXSP	I	Z	cMOS Display Link Receive Data Strobe Positive
cDVO_RXSN	I	Z	cMOS Display Link Receive Data Strobe Negative
cDVO_VBLNK	O	1	cMOS Display Link Vertical Blank
cDVO_STALL#	O	1	cMOS Display Link Receive Power Management. This active low signal is used to gate-off PCH input sense amps to save power when asserted.
cDVO_RXPWR#	I	Z	cMOS DVO Receive Power Management control. This active low signal is used to gate-off PCH input sense amps to save power when asserted.
CDVO_RX_CVREF	A	N/A	cMOS VREF for cDVO receiver
CDVO_RX_GVREF	A	N/A	GTL VREF for cDVO receivers

3.2.3 Host Power Management and Clock Interface

Table 3-5. Host Power Management and Clock Interface Signals

Signal/Pin	Type	Reset State	Description
CPU_PWRMODE[2:0]	O	000	**CPU PM:** Grey-code output to allow processor to transition properly on power-up.
CPU_HCLKSEL	I	Z	**CPU Clock Select:** Host Clock Frequency Select. 0= 100 MHz
HCLKP	O	X	**Positive Host Ref Clock:** 100 MHz – based on value of CPU_HCLKSEL -0.5% SSC at spread modulation of 32 KHz
HCLKN	O	X	**Negative Host Ref Clock:** 100 MHz - based on value of CPU_HCLKSEL -0.5% SSC at spread modulation of 32 KHz PCH will support a S/W option to not toggle this signal to save power.

3.2.4 High-Definition Multimedia Interface (HDMI) or Digital Visual Interface (DVI)

The High-Definition Multimedia Interface (HDMI) transmits digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. HDMI is a display interface connecting the PCH and display devices that utilizes transition minimized differential signaling (TMDS) to carry audio-visual information through the same HDMI cable. In addition, DVI is also supported by the PCH on the same channel.

Note: Refer to Table 2-1 for supported video and audio resolution combinations.

Table 3-6. HDMI Data Interface

Signal/Pin	Type	Reset State	Description
HDMI_DATA2P	O	X	Data 2 +
HDMI_DATA2N	O	X	Data 2 -
HDMI_DATA1P	O	X	Data 1 +
HDMI_DATA1N	O	X	Data 1 -
HDMI_DATA0P	O	X	Data 0 +
HDMI_DATA0N	O	X	Data 0 -
HDMI_CLKP	O	X	CLK +
HDMI_CLKN	O	X	CLK -

Table 3-7. HDMI Support Interface

Signal/Pin	Type	Reset State	Description
HDMI_COMP	A	N/A	HDMI_COMP:Tied to 3.3V rail via external resistor for input buffer compensation. Requires 50 ±1% ohm external resistor. Refer to Oak Trail Platform Design Guide for termination guideline.
HDMI_HPD	I	PD	Hot Plug Detect signal

3.2.5 I2C Interface

Table 3-8. I2C Control Interface

Signal/Pin	Type	Reset State	Description
I2C_0_SCK	I/O	PU	I2C Bus 0 Serial Clock
I2C_0_SDATA	I/O	PU	I2C Bus 0 Serial Data
I2C_1_SCK	I/O	PU	I2C Bus 1 Serial Clock; recommended for LVDS
I2C_1_SDATA	I/O	PU	I2C Bus 1 Serial Data; recommended for LVDS
I2C_2_SCK	I/O	PU	I2C Bus 2 Serial Clock; recommended for HDMI
I2C_2_SDATA	I/O	PU	I2C Bus 2 Serial Data; recommended for HDMI

3.2.6 USB Interface

Table 3-9. USB Interface Signals

Signal/Pin	Type	Reset State	Description
USB_DP[3:0]	I/O	Z	USB 2.0 Data Positive Data (D+): In USB 2.0 mode this is the positive differential data signal. In HSIC mode, this is simply a cMOS data signal which is strobe with HSIC_CLK both positive and negative edges.
USB_DN[3:0]	I/O	Z	USB 2.0 Data Negative (D-): In USB 2.0 mode, this is the negative differential data signal. In HSIC mode, this is the single-ended, cMOS source synchronous clock on which data is latched on both rising and falling edges in a DDR fashion.
USB_REFEXT	I A	N/A	Reference Resistor External: Used to set 200 µA IREF. Requires 6.04K ±1% external termination resistor. Refer to Oak Trail Platform Design Guide for guideline.

3.2.7 Storage Device Interface

The PCH supports 3 SDIO ports. 2 are dedicated SDIO ports and 1 is for com port only. The two generic ports are for SD or MMC storage cards. Port 0 has only 4 data bits and it can only support MMC cards. The one dedicated SDIO port supports SD or MMC cards. Communication module can be supported on this dedicated port.

The PCH supports two output supply voltages on Port 0 – 1.8 and 3.3 Volts – which are individually negotiated by each storage device. This implies that each Storage Device resides in its own power island.

Table 3-10.SD/MMC Port 0 Interface Signals

Signal/Pin	Type	Reset State	Description
SDIO_0_DATA[3:0]	I/O	Z	**SDIO Port 0 Data:** By default, after power-up, only SDIO_DATA[0] is used for data transfer. A wider data bus can be configured for data transfer. **MMC Port 0 Data:** These signals operate in push-pull mode. The MMC card includes internal pullups for all data lines. By default, after power-up, only MMC_DATA[0] is used for data transfer. A wider data bus can be configured for data transfer.
SDIO_0_CMD	I/O	PU	**SDIO Port 0 Command:** Used for card initialization and transfer of commands. **MMC Port 0 Command:** Used for card initialization and transfer of commands. It has two modes: open-drain for initialization, and push-pull for fast command transfer.
SDIO_0_CLK	O	PD	**SD Port 0 Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. Generated by the PCH, at a maximum frequency of 25 MHz. **MMC Port 0 Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. Generated by the PCH, at a maximum frequency of 52 MHz.
SDIO_0_WP	I	PU	**SD Port 0 Write Protect:** Active high when a card does not want to accept writes. **MMC Port 0 Write Protect:** Active high when a card is not accepting writes.
SDIO_0_CD#	I	Z	**SD Port 0 Card Detect:** Active low when a card is present. Floating (pulled high) when a card is not present. This signal is attached to the SDIO connector. **MMC Port 0 Card Detect:** Active low when a card is present. Floating (pulled high) when a card is not present. This signal is attached to the MMC connector.
SDIO_0_PD#	O	Z	**SD Port 0 Power Down:** Active low. Asserts when host controller needs to power down the port. Refer to Oak Trail Platform Design Guide for implementation guidelines.

Table 3-11.SD/MMC Port 1 Interface Signals

Signal/Pin	Type	Reset State	Description
SDIO_1_DATA[7:0]	I/O	Z	**SDIO Port 1 Data:** By default, after power-up, only SDIO_DATA[0] is used for data transfer. A wider data bus can be configured for data transfer. **MMC Port 1 Data:** These signals operate in push-pull mode. The MMC card includes internal pullups for all data lines. By default, after power-up, only MMC_DATA[0] is used for data transfer. A wider data bus can be configured for data transfer.
SDIO_1_CMD	I/O	Z	**SDIO Port 1 Command:** Used for card initialization and transfer of commands. **MMC Port 1 Command:** Used for card initialization and transfer of commands. It has two modes: open-drain for initialization, and push-pull for fast command transfer.
SDIO_1_CLK	O	Z	**SD Port 1 Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. Generated by the PCH, at a maximum frequency of 25 MHz. **MMC Port 1 Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. Generated by the PCH, at a maximum frequency of 52 MHz.
SDIO_1_WP	I	Z	**SD Port 1 Write Protect:** Active high when a card does not want to accept writes. **MMC Port 1 Write Protect:** Active high when a card is not accepting writes.
SDIO_1_CD#	I	Z	**SD Port 1 Card Detect:** Active low when a card is present. Floating (pulled high) when a card is not present. This signal is attached to the SDIO connector. **MMC Port 1 Card Detect:** Active low when a card is present. Floating (pulled high) when a card is not present. This signal is attached to the MMC connector.
SDIO_1_PD#	O	Z	**SD Port 1 Power Down:** Active low. Asserts when host controller needs to power down the port. Refer to Oak Trail Platform Design Guide for implementation guidelines.

3.2.8 COMM SDIO PORT

In addition to 4 USB ports PCH supports an SDIO port for connections to Comm's. This is a dedicated port and is not muxed with other pins.

Table 3-12. COMM SDIO Port Signals

Signal/Pin	Type	Reset State	Description
SDIO_2_DATA[3:0]	I/O	Z	**SDIO Port 2 Data:** Four bi-directional data signals.
SDIO_2_CMD	I/O	PU	**SDIO Port 2 CMD:** Bi-directional command response signal.
SDIO_2_CLK	O	PD	**SDIO Port 2 CLK:** Active high clock that is cMOS level and interfaces to internal communication ports.
SDIO_2_PD#	O	Z	**SD Port 2 Power Down:** Active low. Asserts when host controller needs to power down the port. Refer to Oak Trail Platform Design Guide for implementation guidelines.

3.2.9 Audio Interface

The Audio I/F is power off of PWRPAUDIO and will connect to PMIC at the platform level. Customers wishing to provide their own Audio CODED interface can drive this Power Island to 1.5 or 3.3-V interfaces.

Table 3-13. Intel HD Audio Interface Signals (Sheet 1 of 2)

Signal/Pin	Type	Reset State	Description
HDA_RST#	O	PD	Active low link reset signal. It is sourced from the controller and connects to all Codecs on the link.
HDA_SYNC	O	PD	This signal marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codecs on the link.
HDA_CLK	O	PD	**24 MHz clock**, sourced from the controller and connecting to all codecs on the link.
HDA_SDO	O	PD	**Serial Data Out:** one or more serial data output signal(s) driven by the Controller to all codecs on the link. Data is double pumped – i.e., the controller drives data onto SDO, and codecs sample data present on SDO with respect to every edge of HDA_CLK
HDA_SDI[1]	I	Z	**Serial Data In:** one or more point-to-point serial data input signals, each driven by only one codec. Data is single pumped; codecs drive SDI and the controller samples SDI with respect to the rising edge of HDA_CLK.

Table 3-13. Intel HD Audio Interface Signals (Sheet 2 of 2)

Signal/Pin	Type	Reset State	Description
HDA_SDI[0]	I	Z	**Serial Data In:** one or more point-to-point serial data input signals, each driven by only one codec. Data is single pumped; codecs drive SDI and the controller samples SDI with respect to the rising edge of HDA_CLK.
HDA_DOCKEN#	O	PD	**HD Audio Dock Enabler:** Enables dock codec
HDA_DOCKRST#	O	PD	**HD Audio Dock Reset:** Reset dock codec

3.2.10 Analog Clock and Analog Interface

Table 3-14. Analog Clock and Analog Interface Signals

Signal/Pin	Type	Power Well	Description
OSC_IN	I	VCCAHPLL	**Oscillator Input:** Provides input to Pierce oscillator from 25-MHz crystal. If this signal is used, OSC_OUT should be left floating.
OSC_OUT	I	VCCAHPLL	**Oscillator Output:** This is the output of Pierce oscillator and should be connected to the crystal.
VCC_HCLK_0P8	A	1.05V	Supply for the HCLKP & HCLKN main clock 0.8V
VCC_HCLK_3P3	A	3.3V	Supply for Host Clock Buffer
VCCA_DPLL	A	1.2V	1.2 V dedicated analog supply for display PLL
VCCA_HPLL	A	1.2V	Supply for 25-MHz oscillator ckt and the host PLL
VCCA_UPLL_1P2	A	1.2V	Dedicated Analog supply for USB PLL
VCCA_UPLL_2P5	A	2.5V	Dedicated Analog supply for USB PLL
VSSA_UPLL	A		Dedicated Analog ground for Host PLL
VSSA_HDMIBG	F		Display Bandgap VSS supply for HDMI

3.2.11 SATA Interface

SATA interface a high speed data link for devices like Disk drive. Up to 3.0 Gbs transfer speed is supported. These are dedicated pins – not muxed with other signals.

Table 3-15. SATA Interface Signals (Sheet 1 of 2)

Signal	Type	Reset State	Description
SATA_TXP	O	Z	High speed differential pair to transmit output
SATA_TXN	O	Z	High speed differential pair to transmit output
SATA_RXP	I	Z	High speed differential pair to transmit input

Table 3-15. SATA Interface Signals (Sheet 2 of 2)

Signal	Type	Reset State	Description
SATA_RXN	I	Z	High speed differential pair to transmit input
SATA_LED#	O	Z	LED for SATA Port
SATA_REXT	I	Z	191 ±1% ohm precision resistor to ground. During resistor turning, current is forced through the external register. Refer to Oak Trail Platform Design Guideline for termination guideline.

3.2.12 JTAG Interface

Table 3-16. JTAG Interface Signals

Signal	Type	Reset State	Description
TDO	O	Z	**JTAG Test Data Output:** Serial output for test instruction and data from the test logic.
TDI	I	PU	**JTAG Test Data Input:** This signal receives serial test instruction and data of test logic.
TMS	I	PU	**JTAG Test Mode Select:** Decoded by the TAP controller to control test operations.
TCK	I	PU	**JTAG Test Clock:** Clock for the test logic.
TRST#	I	PU	**JTAG Test Reset:** Asynchronous initialization of the TAP controller.

3.2.13 Reset Out Interface

Table 3-17. Reset Out Interface Signals

Signal/Pin	Type	Reset State	Description
RESET_OUT#	O	0	Copy of RESET_N pin. It is asserted at the same time as RESET_N is asserted; however, it its de-assertion is controlled by the SCU. RESET_OUT# trails Reset# driven to PCH from PMIC. This allows the SCU to complete reset and then have the rest of the platform components reset at a predefined time. This signal is 1.8 V and it will not be asserted in S3 transition.

3.2.14 PMIC Interface

Table 3-18.PMIC Interface Signals

Signal/Pin	Type	Reset State	Description
PWRGOOD	I	N/A	POWER GOOD: PMIC asserts this signal to indicate that all initial power rails to the PCH are valid. Assertion of PWRGOOD also means that VCCA_OSC has been valid for at least 30 µs. The PCH will remain off until this signal is asserted.
RESET#	I	N/A	Active Low Hard Reset for PCH: This signal is driven by the PMIC.
PMIC_INT	I	Z	PMIC Interrupt: Active high for PM reasons and powerup glitch avoidance reasons. Defaults to PMIC_INT. Attach this to IRQ9 on PMIC.
VR_COMP#	I	N/A	Voltage Regulator Complete: Indication from PMIC that requested voltage regulation request over SPI has completed.
EXIT_STDBY	O	PD	EXIT Standby: When asserted the PMIC should exit the AOAC Standby settings for regulating the platform supplies.
SLFREF#	O	PU	Memory Self-Refresh: Default to GPIO 58 – reserved for Memory Self-Refresh; Active low.
HRCOMP	I	N/A	HVIO Buffer RCOMP: Tie to a precision ±1% resistor to ground.Please refers to the Oak Trail Platform Design Guide for specific recommendation.

3.2.15 SPI Port 1 Interface

Table 3-19.SPI Port 1 Interface Signals

Signal	Type	Reset State	Description
SPI_1_CS[3:0]#	I/O	PU	SPI 1 Chip Select(s): active low; output from master A total of 4 slaves are supported on this SPI port.
SPI_1_SDO	I/O	PD	SPI Port 1 Serial Data Out: defaults to output.
SPI_1_SDI	I/O	PD	SPI Port 1 Serial Data In: defaults to input
SPI_1_CLK	I/O	PD	SPI Port 1 Clock: Serial Clock (output from master)

3.2.16 SPI Port 2 Interface

Table 3-20. SPI Port 2 Interface Signals

Signal	Type	Reset State	Description
SPI_2_CS#	I/O	PU	SPI 2 Chip Select(s): Active Low; reserved for additional PMIC load.
SPI_2_SDO	I/O	PD	SPI Port 2 Serial Data Out: defaults to output.
SPI_2_SDI	I/O	PD	SPI Port 2 Serial Data In: defaults to input.
SPI_2_CLK	I/O	PD	SPI Port 2 Clock: defaults to output.

Note: The SDI/SDO convention requires that SDO on the master be connected to SDI on the slave, and vice-versa.

3.2.17 iLB - Intel Legacy Block

3.2.17.1 LPC Interface

PCH LPC interface supports LPC Specification Rev1.1.

Table 3-21. LPC Interface Signals

Signal	Type	Reset State	Description
LPC_AD[3:0]	I/O	Z	Multiplexed Command, Address and Data
LPC_FRAME#	O	Z	Indicates start of LPC/FHW cycle
LPC_SERIRQ	I/O	Z	Serial Interrupt Request: conveys the serial interrupt protocol
LPC_CLKRUN	I/O	Z	Clock Run Control: interface for clock run protocol for disabling the clock
LPC_CLKOUT[2:0]	O	Z	Clock: Clocks driven by the WPT to LPC devices. LPC_CLKOUT[0] is routed back into the iLB to clock its internal logic.
LPC_RESET#	O	0	LPC Bus Reset

3.2.17.2 Miscellaneous Signals Interface

(Sheet 1 of 2)

Signal	Type	Reset State	Description
SPKR	O	Z	System Speaker: Connected to 8254 counter 2 output
MED_CLK	I	Z	Media Clock: Used for 8254 timers and HPET. Running at 14.31818 MHz. Supplied by an external clock chip.
RTC_CLK	I	Z	RTC Clock: The 32.768-KHz clock supplied by PMIC.
SLP_S3#	O	0	Indicates to EC system is going into S3
SLP_S4#	O	0	Indicates to EC system is going into S4
SLP_S5#	O	0	Indicates to EC system is going into S5

(Sheet 2 of 2)

Signal	Type	Reset State	Description
SMI#	I	Z	System management interrupt
GPE#	I	Z	General Purpose Event: Asserted by an external device (typically, the embedded controller) to log an event in the PCH's ACPI space, and generate SCI (if enabled).
A20GATE	I	Z	From the keyboard controller. Acts as alternative method to force the A20M_N signal active. Saves the external OR gate needed with various other chipsets.
VDDQ_PWRGOOD	I	0	Indicating to SCU that the external VDDQ supply—not directly controlled by it—is good.
RCBIN	I	Z	Additional interrupt; can be used to reset the Processor. Can be configured as a regular GPIO.
TP		N/A	**Test Point:** Signals not used on the platform. Route to exposed test point on the platform for measurement, test and debug purposes.
RSVD		N/A	**Reserved:** Signals not used on the platform. Route to exposed test point on the platform for measurement, test and debug purposes.
NC		N/A	**No Connect:** Signals not used on the platform. They can be left floating.
VSS_NCTF		N/A	**VSS Non Critical to Function:** Connect to VSS. NCTF pins may require special routing guidelines. Consult with Platform Design Guide for details.

3.3 Power Rails

3.3.1 Power Rail Type

This section defines the power state and power level options.

Table 3-22. Power Rail Types (Sheet 1 of 2)

Rail Type	Description
F	**Fixed:** Voltage level is fixed—based on I/O family.
AON	**Always ON:** The voltage level must always be on for the component to operate safely and reliably.
S	**Selectable:** Voltage can be selected at the platform level, that is, low-speed I/O support for 1.8, 2.5, and 3.3-Volt levels.
V	**Variable:** Variable supplies are negotiable supply levels, that is, SDIO specification supports dynamic voltage management and the PCH will support negotiated from 3.3 V to 1.8 V.

Table 3-22. Power Rail Types (Sheet 2 of 2)

Rail Type	Description
SbF	**Selectable but Fixed:** I/O family or segment supports multi-termination levels but the current POR platform will only used one "fixed" level. This reduces electrical validation required at component and platform level.
VbF	**Variable but Fixed:** I/O family or segment supports variable, multi-term level but the current POR platform will only use one "fixed" level. This reduces the logic and electrical validation required at component and platform level.
NCTF	**Non Critical To Function:** Non-Critical to Function (NCTF) signals have been designed into the package footprint to enhance the solder joint reliability of our products by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the die-to-package interface. It is expected that in some cases these sacrificial balls may crack partially or completely. However, this will have no impact to product performance or reliability.

3.3.2 Power Rail Descriptions

3.3.2.1 Core and I/O Power

This section describes the power signals and power states of each power signal.

Table 3-23. Core and I/O Power Signals (Sheet 1 of 2)

Signal	Type	Voltage Level	Description
VCC	F, AON	1.2 V	**1.2 V Core Supply:** Always on core supply.
VCC_2P5	F	2.5 V	**2.5 V Core supply:** For One-Time-Programmable (OTP) arrays
VCCA_DMIDVO	F	1.8 V	cDVO and cDMI RX supply
VCCP_DMIDVO	F	1.05 V	Output drivers for cDMI_DVO
VCC_HPM	F, AON	1.05 V	Output signals for Always-On PM signals including HCLK. Also includes JTAG I/F(s).
VCCA_HDMIBG	F	3.3 V	Display Bandgap supply for HDMI
VCC_HDMI_3P3	F	3.3 V	Used to power HDMI interface
VCCA_HDMI_1P8	F	1.8 V	Analog 1.8-V supply for HDMI **Note:** This power supply is for back up purpose only and it should not be connected on the platform.
VCCA_HDMI_1P2	F	1.2 V	Analog 1.2-V supply for HDMI
VCC_SATA_1P2	F	1.2 V	SATA PHY 1.2-V Supply
VCC_SATA_2P5	F	2.5 V	SATA PHY 2.5-V Supply
VCC_SDIO0	VbF	1.8/3.3 V	Reserved for SDIO Port 0 – dynamically negotiated from 3.3 V to 1.8 V based on plug-in device
VCC_SDIO1	F	3.3 V	Supplies SDIO Port 1 Interface
VCC_SDIO2	F	3.3 V	Supply for the SDIO Port 2 Comm's interface

Table 3-23.Core and I/O Power Signals (Sheet 2 of 2)

Signal	Type	Voltage Level	Description
VCCP_AUDIO	S	1.5/3.3 V	Power HD Audio interface; kept separate to allow vendor to add external customer owned CODEC if desired; supports 1.5 and 3.3 V.
VCCA_USB_3P3	F	3.3 V	Supplies USB analog front end interface. This rail needs to be powered if any of the ports needs to be active.
VCC_PMIC	SbF	1.8 V	Power signals to PMIC which is 1.8 V; Customers could use different voltage if desired.
VCCP_LEGACY	VbF	3.3 V	Powers for legacy interface
VCCP_SPI	VbF	3.3 V	Powers all signals on SPI interface
VCCA_DPLL	AON	1.2 V	1.2 V dedicated analog supply for display PLL
VCCA_HPLL	AON	1.2 V	Supply for 25MHz oscillator ckt and the host PLL
VCC_HCLK_0P8	F	1.05 V	Supply for the HCLKP & HCLKN main clock 0.8 V
VCC_HCLK_3P3	F	3.3 V	Supply for Host Clock Buffer
VCCA_UPLL_1P2	F	1.2 V	USB PLL supply
VCCA_UPLL_2P5	F	2.5 V	USB PLL supply
VCCP_MISC	F	3.3 V	Supply for Miscellaneous signals

3.3.2.2 PLL/Bandgap Power and Ground

Table 3-24.PLL/Bandgap Power and Ground Signals

Signal	Type	Signal Group	Description
VCCA_HPLL	F, AON	Host PM, Analog CLK	1.2-V analog supply for oscillator and host PLL
VCCA_DPLL	F, AON	Display PLL	1.2-V dedicated analog supply for display PLL
VSSA_HPLL		N/A	Host PLL VSS supply
VSSA_DPLL		N/A	Display PLL VSS supply
VCCA_UPLL_1P2	F	1.2 V	USB PLL supply
VCCA_UPLL_2P5	F	2.5 V	USB PLL VSS supply
VSSA_UPLL		N/A	USB PLL VSS supply

3.4 Serial I/O and GPIO

The PCH provides 62 highly-multiplexed General Purpose I/O (GPIO) pins for use in generating and capturing application-specific input and output signals. Each pin can be programmed as an output, an input, or as a bi-directional for certain alternate functions. Refer to Table 3-25 for the default GPIO usage.

When programmed as an input, a GPIO can also serve as an interrupt source. All GPIO pins are configured as inputs during the assertion of all resets, and they remain inputs until configured otherwise.

Table 3-25. GPIO Alternate Function Mapping (Sheet 1 of 2)

GPIO Pin	Pin Name	Alternate Function
0	GPIO0	PWRGOOD
1	GPIO1	RESET#
2	GPIO2	PMIC_INT
3	GPIO3	VR_COMP#
4	GPIO4	EXIT_STDBY
5	GPIO5	SPI_2_SS[0]
6	GPIO6	RTC_CLK
7	GPIO7	SPI_2_SDO
8	GPIO8	SPI_2_SDI
9	GPIO9	SPI_2_CLK
10	GPIO10	SPI_1_SS[0]
11	GPIO11	SPI_1_SS[1]
12	GPIO12	SPI_1_SS[2]
13	GPIO13	SPI_1_SS[3]
14	GPIO14	SPI_1_SDO
15	GPIO15	SPI_1_SDI
16	GPIO16	SPI_1_CLK
17	GPIO17	SMI#
18	GPIO18	GPE#
19	GPIO19	SATA_LED#
20	GPIO20	SLP_S3#
21	GPIO21	SLP_S4#
22	GPIO22	SLP_S5#
23	GPIO23	A20GATE
24	GPIO24	LPC_LAD[0]
25	GPIO25	LPC_LAD[1]
26	GPIO26	LPC_LAD[2]
27	GPIO27	LPC_LAD[3]
28	GPIO28	LPC_FRAME#
29	GPIO29	LPC_SERIRQ
30	GPIO30	LPC_CLKRUN
31	GPIO31	LPC_CLKOUT[0]

Table 3-25.GPIO Alternate Function Mapping (Sheet 2 of 2)

GPIO Pin	Pin Name	Alternate Function
32	GPIO32	LPC_CLKOUT[1]
33	GPIO33	LPC_CLKOUT[2]
34	GPIO34	GPIO34
35	GPIO35	GPIO35
36	GPIO36	GPIO36
37	GPIO37	MED_CLK
38	GPIO38	SPKR
39	GPIO39	LPC_RESET#
40	GPIO40	RCBIN
41	GPIO41	GPIO41
42	GPIO42	GPIO42
43	GPIO43	GPIO43
44	GPIO44	VDDQ_PWRGOOD
45	GPIO45	GPIO45
46	GPIO46	GPIO46
47	GPIO47	GPIO47
48	GPIO48	GPIO48
49	GPIO49	GPIO49
50	GPIO50	SYS_RESET#
51	GPIO51	GPIO51
52	GPIO52	I2C_2_SDA
53	GPIO53	I2C_2_SCL
54	GPIO54	I2C_1_SDA
55	GPIO55	I2C_1_SCL
56	GPIO56	I2C_0_SDA
57	GPIO57	I2C_0_SCL
58	GPIO58	SELREF#
59	GPIO59	GPIO59
60	GPIO60	GPIO60
61	GPIO61	GPIO61

NOTE: Only the shaded signals are available for general GPIO usage.

§ §

4 Electrical Specifications

4.1 PCH Power Net Characteristics

Table 4-26. Power Net Characteristics (Sheet 1 of 2)

Power Rail	Parameters	Input (V)	Tolerance (%)	Peak Sustained Current (ma)	Idle Current (µA)	S0	S3
VCC	1.2 V Core Supply: Always on, required for PCH power-on.	1.2	+5/-5	210		ON	ON
VCC_2P5	2.5 V Core Supply	2.5	+5/-5			ON	ON
VCCP_DMIDVO	1.05 V Supply for cDMI Output Drivers	1.05	+5/-5	174	14.7	ON	OFF
VCCA_DMIDVO	1.8 V Supply for cDMI Receivers	1.8	+5/-5	5	0	ON	ON
VCC_HPM	1.05 V Supply for Host PM and JTAG Signals	1.05	+5/-5	1	0.01	ON	OFF
VCC_HDMIBG	Display Bandgap supply for HDMI	3.3	+5/-5	3.62	0	ON	ON
VCC_HDMI_3P3	Used to power HDMI supply	3.3	+5/-5			ON	ON
VCCA_HDMI_1P8	Analog 1.8-V supply for HDMI	1.8	+5/-5			ON	ON
VCCA_HDMI_1P2	Analog 1.2-V supply for HDMI	1.2	+5/-5	13.8	5	ON	ON
VCC_SATA_1P2	SATA PHY 1.2-V Supply	1.2	+5/-5	20	250	ON	ON
VCC_SATA_2P5	SATA PHY 2.5-V Supply	2.5	+5/-5	20	430	ON	ON
VCC_SDIO0	SDIO/MMC Port 0 Supply: dynamically negotiated from 3.3 V to 1.8 V based on device type.	1.8	+5/-5			ON	ON
		3.3	+5/-5	7.5	0.03	ON	ON
VCC_SDIO1	SDIO Port 1 Supply: Typically 3.3 V	3.3	+5/-5	33	0.08	ON	ON
VCC_SDIO2	SDIO Port 2 Supply: Typically 3.3 V	3.3	+5/-5	5	0.03	ON	ON
VCCP_AUDIO	HD Audio Supply	1.5	+5/-5	7.5		ON	ON
		3.3	+5/-5	16.5		ON	ON
VCC_PMIC	Power signals to PMIC which is 1.8 V; Customers could use different voltage if desired.	1.8	+5/-5	1	0.01	ON	ON
VCCP_LEGACY	Powers for legacy interface	2.5	+5/-5			ON	ON
VCCP_SPI	Powers all signals on SPI interface	3.3	+5/-5	5	0.03	ON	ON

Table 4-26.Power Net Characteristics (Sheet 2 of 2)

Power Rail	Parameters	Input (V)	Tolerance (%)	Peak Sustained Current (ma)	Idle Current (µA) (Contin	S0	S3
VCCA_HPLL	Dedicated analog supply for oscillator and host PLL	1.2	+5/-5	10	0.01	ON	ON
VCCA_DPLL	Dedicated analog supply for display PLL	1.2	+5/-5	20	0.01	ON	ON
VCC_HCLK_0P8	Supply for Host Clock Driver.	1.05	+5/-5	4.1		ON	OFF
VCC_HCLK_3P3	3.3 V Supply for Host Clock PLL	3.3	+5/-5	1.2		ON	ON
VCCA_USB_3P3	3.3 V USB Supply	3.3	+5/-5	6	11	ON	ON
VCCA_UPLL_2P5	2.5 V USB PLL Supply	2.5	+5/-5	120	1.72	ON	ON
VCCA_UPLL_1P2	1.2 V USB PLL Supply	1.2	+5/-5	210		ON	ON
VCCP_MISC	Supply for Miscellaneous signals	3.3	+5/-5			ON	ON

4.2 PCH DC Characteristics

This section documents the DC characteristics of the following PCH signal groups and interfaces.

4.2.1 cDMI

Table 4-27.cDMI DC Characteristic

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
CMOS cDMI						
V_{OH}	Output High Voltage	0.9*PWR_DMIDVO	PWRDMIDVO	1.1*PWR_DMIDVO	V	
V_{IH}	Input High Voltage	1/2*PWR_DMIDVO + 0.1	PWRDMIDVO	PWR_DMIDVO+0.1	V	
V_{IL}	Input Low Voltage	-0.1	0	1/2*PWR_DMIDVO - 0.1	V	
V_{OL}	Output Low Voltage	0	0	0.1*PWR_DMIDVO		
I_{LEAK}	Input Leakage Current			10	µA	
C_{IN}	Input Capacitance	-	1.5	-	pF	

4.2.2 MMC

Table 4-28.MMC Power Supply—High Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VDD	Supply voltage	2.7	3.6	V	
VSS	Supply voltage	-0.5	0.5	V	

Table 4-29.MMC Power Supply—Dual Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VDDL	Supply voltage (low voltage range)	1.7	1.95	V	1.95–2.7 volts is not supported
VDDH	Supply voltage (high voltage range)	2.7	3.6	V	
VSS	Supply voltage	-0.5	0.5	V	

Table 4-30.MMC Power Supply—High Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VCC	Supply voltage (NAND)	2.7	3.6	V	
		1.7	1.95	V	
VCCQ	Supply voltage (I/O)	-0.5	0.5	V	
		1.7	1.95	V	

4.2.2.1 MMC Bus Signal Line Load

The total capacitance CL of each line of the MultiMediaCard bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself, and the capacitance CCARD of the card connected to this line,

CL = CHOST+CBUS+CCARD

and requiring the sum of the host and bus capacitances not to exceed 20 pF.

Table 4-31.MMC Capacitance (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
RCMD	Pull-up resistance for CMD	4.7		100	kohm	To prevent bus floating
RDAT		50		100	kohm	To prevent bus floating
RINT	Internal pull-up resistance DAT1-DAT7	50		150	kohm	To prevent unconnected lines floating
CL	Bus signal line capacitance			30	pF	Single card

Table 4-31. MMC Capacitance (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
CMICRO	Single card capacitance	1.7		1.95	pF	For MMCmicro
CMOBILE				30		For MMCmobile and MMCplus
CBGA			7	12		For BGA
	Maximum signal line capacitance			16	nH	fpp ≤ 52 MHz

4.2.2.2 MMC Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any VDD of the allowed voltage range.

Table 4-32. MMC Push-Pull Mode Bus Signal Level—High Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Units	Notes
VOH	Output High Voltage	0.75*VDD		V	IOH=−100 µA VDD minimum
VOL	Output Low Voltage		0.125*VDD	V	IOL = 100 µA VDD minimum
VIH	Input High Voltage	0.625*VDD	VDD+0.3	V	
VIL	Input Low Voltage	VSS−0.3	0.25*VDD	V	

The definition of the I/O signal levels for the Dual voltage MultiMediaCard changes as a function of VDD.

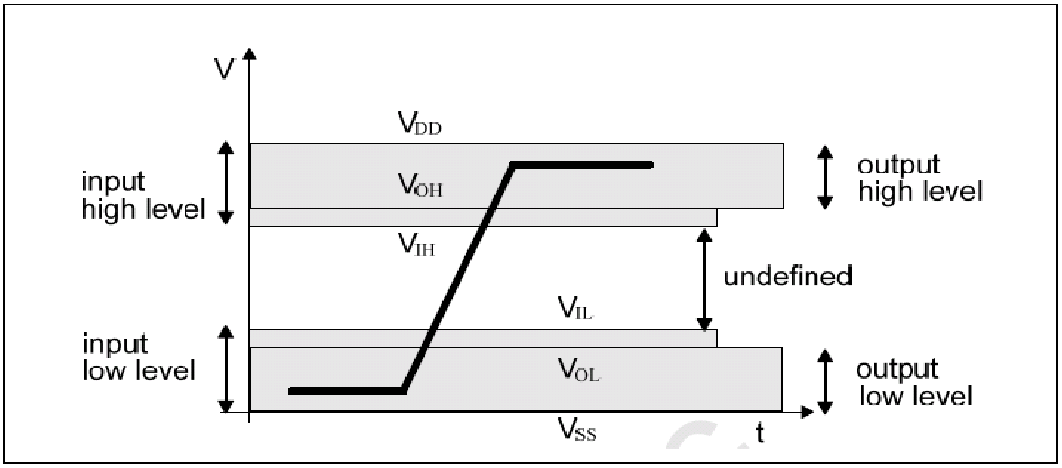
- 2.7 V – 3.6 V: Identical to the High Voltage MultiMediaCard
- 1.95 V – 2.7 V: Undefined. The card is not operating at this voltage range
- 1.70 V – 1.95 V: Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Wide Range" as defined in Table 4-33.

Table 4-33. MMC Push-Pull Mode Bus Signal Level—Dual Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Units	Notes
VOH	Output High Voltage	VDD−0.2		V	IOH = −100 µA VDD minimum
VOL	Output Low Voltage		0.2	V	IOL = 100 µA VDD minimum
VIH	Input High Voltage	0.7*VDD	VDD+0.3	V	
VIL	Input Low Voltage	VSS−0.3	0.3*VDD	V	

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 4-2. MMC Bus Signal Levels



4.2.3 SD/SDIO

Table 4-34. SD/SDIO Threshold Level for High Voltage Range and General Parameters

Symbol	Parameter	Minimum	Maximum	Units	Notes
VDD	Supply Voltage				
		2.7	3.6	V	3.3 V input
VOH	Output High Voltage	0.75*VDD		V	IOH=−100 µA VDD minimum
VOL	Output Low Voltage		0.125*VDD	V	IOL=100 µA VDD minimum
VIH	Input High Voltage	0.625*VDD	VDD+0.3	V	
VIL	Input Low Voltage	VSS−0.3	0.25*VDD	V	
	Power Up Time		250	ms	From 0 V to VDD minimum
	Peak voltage on all lines	-0.3	VDD + 0.3	V	
	Input Leakage Current	-10	10	uA	
	Output Leakage Current	-10	10	uA	

4.2.3.1 SD/SDIO/MMC Current Consumption

The current consumption is measured by averaging over one second.

- Before first command: Maximum current is 15 mA
- During initialization: Maximum current is 100 mA
- Operation in Default Mode: Maximum current is 100 mA
- Operation in High Speed Mode: Maximum current is 200 mA

- Operation with other functions: Maximum current is 500 mA.

4.2.3.2 SD/SDIO Bus Signal Line Load

The total capacitance of the SD Memory Card bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS, and the capacitance CCARD of each card connected to this line:

Total bus capacitance = CHOST + CBUS + N CCARD

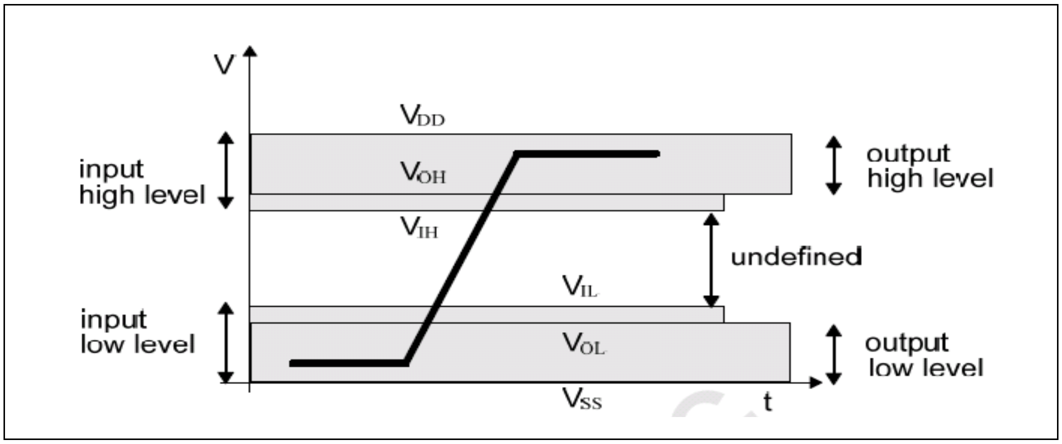
Where N is the number of connected cards.

Table 4-35.SD/SDIO Bus Signal Line Load

Symbol	Parameter	Minimum	Maximum	Units	Notes	Figure
RCMD RDAT	Pull-up resistance	10	100	kΩ	To prevent bus floating	
CL	Total bus capacitance for each signal line		40	pF	One card CHOST+CBUS shall not exceed 30 pF	
CCARD	Capacitance of the card for each signal pin		10	pF		
	Maximum signal line inductance		16	nH	fPP ≤ 20 MHz	
RDAT3	Pull-up resistance inside card (pin1)	10	90	kΩ	May be used for card detection	

4.2.3.3 SD/SDIO Bus Signal Levels

Figure 4-3. Timing Diagram Data Input/Output Referenced to Clock (Default)



4.2.4 I²C

This applies to PWR_KBDMISC = 3.3 V

Where VDD = PWR_KBDMISC

or

This applies to PWR_CSB and PWR_KBDMISC = 1.8 V

VDD = PWR_CSB or PWR_KBDMISC

Table 4-36. I²C—SDA and SCL I/O Stages for F/S-Mode Devices

Symbol	Parameter	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
V_{IL}	LOW level input voltage: VDD-related input levels	- 0.5	0.3 V_{DD}	- 0.5	0.3* V_{DD} (1)	V
V_{IH}	HIGH level input voltage: VDD-related input levels	0.7 V_{DD}	(2)	0.7 V_{DD}(1)	(2)	V
V_{IH}	HIGH level input voltage: VDD-related input levels					
V_{hys}	Hysteresis of Schmidt trigger inputs: VDD > 2 V VDD < 2 V	n/a n/a	n/a n/a	0.05 V_{DD} 0.1 V_{DD}	– –	V V
V_{OL}^{1} V_{OL3}	LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2 V VDD < 2 V	0 n/a	0.4 n/a	0 0	0.4 0.2V_{DD}	V V
t_{of}	Output fall time from VIHmin to VILmax with a bus capacitance from 10 – 400 pF	–	250(4)	20 + 0.1C_b(3)	250(4)	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	n/a	n/a	0	50	ns
I_i	Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDDmax	-10	10	-10(5)	10(5)	µA
C_i	Capacitance for each I/O pin	–	10	–	10	pF

NOTES:
1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the VDD voltage to which the pull-up resistors Rp are connected.
2. Maximum VIH = VDDmax + 0.5 V.
3. C_b = capacitance of one bus line in pF.
4. I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

4.2.5 SPI

Table 4-37.SPI Master Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
SPI						
PWR_SPI	Supply Voltage	1.57	1.8	1.98	V	
		2.92	3.3	3.63		
VIL	Input Low Voltage			PWR_SPI*0.30	V	
VIH	Input High Voltage	PWR_SPI*0.70			V	
VOL	Output Low Voltage			0.1	V	
VOH	Output High Voltage	PWR_SPI-0.1			V	
IOL	Output Low Current			3.5	mA	
ILEAK	Input Leakage Current			1.4	µA	
CIN	Input Capacitance	2.0		3.4	pF	

Table 4-38.SPI Slave Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
SPI						
VDD	Supply Voltage	1.57	1.8	1.98	V	
VIL	Input Low Voltage			.54	V	
VIH	Input High Voltage	1.26			V	
VOL	Output Low Voltage			.1	V	
VOH	Output High Voltage	1.7			V	
IOL	Output Low Current			3.5	mA	
ILEAK	Input Leakage Current			1.4	µA	
CIN	Input Capacitance	2.0		3.4	pF	

4.2.6 USB

Table 4-39. USB Low/ Full Speed DC Input Characteristics

Symbol	Parameter	Min.	Max.	Unit	Notes
Input					
V_{DI}	Differential Input Sensitivity	0.2		V	1, 3
V_{CM}	Differential Common Mode Range	0.8	2.5	V	2, 3
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	3
Output					
Vol	Low	0	0.3v	V	
VOH	High (Driven)	2.8	3.6	V	
VOSE1	SE1	0.8		V	
VCRS	Output Signal Crossover Voltage	1.3	2.0	V	

NOTES:
1. V_{DI} = |D+ – D-|
2. Includes VDI range.
3. Applies to Low-Speed/High-Speed USB.

Table 4-40. USB High Speed DC Input Characteristics

Symbol	Parameter	Min.	Max.	Unit	Notes
Input					
V_{HSSQ}	HS Squelch Detection Threshold	100	150	mV	Note 1
V_{HSDSC}	HS Disconnect Detection Threshold	525	625	mV	Note 1
V_{HSCM}	HS Data Signaling Common Mode Voltage Range	–50	500	mV	Note 1
Output					
V_{HSOI}	High-speed idle level	-10	10	mV	
V_{HSOH}	High-speed data signaling high	260	440	mV	
V_{HSOL}	High-speed data signaling low	-10	10	mV	
V_{CHIRPJ}	Chirp J level (differential voltage)	700	1100	mV	
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-500	mV	

NOTES:
1. Applies to USB_D{P/N}[2:0] that support USB High Speed only.

4.3 PCH Power Sequencing Timing

Please refers to the Power Management Integrated Circuit (PMIC) Specification for power-on sequencing timing.

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5 Thermal Management

5.1 Thermal Management Acronyms

Table 5-41.Thermal Management—Acronyms

Acronym	Description
Ψ_{jt}	Characterization—Juntion-to-top
Θ_{ja}	Thermal Resistance—Junction-to-ambient
T_j	Die Junction Operating Temperature

5.2 Absolute Maximum PCH Temperature Conditions

Table 5-43 lists the PCH maximum environmental stress ratings. Functional operating parameters at the absolute maximum and minimum is neither implied nor ensured.

The voltage on a specific pin shall be denoted as “V” followed by the subscripted name of that pin.

Caution: At conditions outside functional operation limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits. If the component is exposed to conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded. Although the device contains protective circuitry to resist damage from electro-static discharge, precautions should always be taken to avoid high static voltages or electric fields.

5.3 Absolute Maximum PCH DC Operating Conditions

The maximum DC ratings for the PCH are described in table below.

Table 5-42.PCH Absolute Maximum DC Ratings (Sheet 1 of 2)

Symbol	Absolute Minimum (V)	Absolute Maximum (V)	Note
VCC	-0.3	1.32	
VCC_2P5	-0.3	2.75	
VCC_HCLK_0P8	-0.3	1.15	

Table 5-42.PCH Absolute Maximum DC Ratings (Sheet 2 of 2)

Symbol	Absolute Minimum (V)	Absolute Maximum (V)	Note
VCC_HCLK_3P3	-0.3	3.63	
VCCP_DMIDVO	-0.3	1.15	
VCCA_DMIDVO	-0.3	1.98	
VCCA_USB_3P3	-0.3	3.63	
VCCA_UPLL_2P5	-0.3	2.75	
VCCA_UPLL_1P2	-0.3	1.32	
VCC_SDIO0	-0.3	3.63	
VCC_SDIO1	-0.3	3.63	
VCC_SDIO2	-0.3	3.63	
VCC_PMIC	-0.3	1.98	
VCCP_LEGACY	-0.3	3.63	
VCC_SPI	-0.3	3.63	
VCCA_HPLL	-0.3	1.32	
VCCA_DPLL	-0.3	1.32	
VCCA_HDMI_1P2	-0.3	1.32	
VCCA_HDMI_1P8	-0.3	1.98	
VCC_HDMI_3P3	-0.3	3.63	
VCC_HDMIBG	-0.3	3.63	
VCCP_MISC	-0.3	3.63	
VCC_SATA_1P2	-0.3	1.32	
VCC_SATA_2P5	-0.3	2.75	
VCCP_AUDIO	-0.3	1.65/3.63	
VCCP_HPM	-0.3	1.15	

5.4 PCH Thermal Characteristics

Table 5-43.PCH Absolute Maximum Temperature Storage Ratings

Parameter	Description/ Signal Names	Minimum	Maximum	Unit
$T_{\text{storage (mounted)}}$ $T_{\text{storage (un-mounted)}}$	Storage Temperature Storage Temperature	-40 -25	85 85	ºC

The thermal resistance of the package is provided in Table 5-44. Package thermal resistance is the measure of the package's heat dissipation capability from die active surface (junction) to a specified reference point (case, board, ambient, and so forth).

Table 5-44. Thermal Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Ψ_{jt}	Characterization Junction-to-top		3.0		ºC/ Watt	1
Θ_{ja}	Thermal Resistance Junction-to-ambient		32		ºC/ Watt	1
T_j	Die Junction Operating Temperature	-25		90	ºC	2, 3

NOTES:
1. Functionality is not ensured for parts that exceed T_j temperature above 90º C. T_j is measured at the top center of the package. Full performance may be affected if the on-die thermal sensor is enabled.
2. Possible damage to the system controller hub may occur if the PCH storage temperature exceeds $T_{storage}$ (mounted) or $T_{storage}$ (un-mounted). Intel does not ensure functionality for parts that have exceeded storage temperatures due to specification violation.
3. Storage temperature is applicable to storage conditions only. In this scenario, the device must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not effect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging.
4. In addition to this storage temperature specification, compliance to the latest IPC/JEDEC J-STD-033B.1 joint industry standard is required for all Surface Mount Devices (SMDs). This document governs handling, packing, shipping and use of moisture/reflow sensitive SMDs.

5.5 PCH Power Specifications

Table 5-45. Thermal Design Power

Symbol	Parameter	Value	Units	Notes
TDP	Thermal Design Power (under nominal voltages)	0.75	W	

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6 Pin States Definition

6.1 Integrated Pull-Up and Pull-Down Signals

Table 6-46. Default Integrated Pull-Up and Pull-Down Signals (Sheet 1 of 2)

Signal/Pin	Resistor	Nominal	Tolerance	Pull Up Rail	Notes
SDIO Port 2					
SDIO_2_CMD	Pull-up	75 k Ω	±30%	VCC_SDIO2	
SDIO_2_CLK	Pull-down	75 k Ω		n/a	
CPU					
CPU_HCLKSEL	disable	n/a		VCC_HPM	
CPU_PWRMODE[2:0]	n/a	n/a	n/a	n/a	Actively driven
JTAG Interface					
TEST	Pull-down	75 k Ω	±30%	n/a	
TDO	disable	n/a		n/a	Pull-up on platform
TDI	Pull-up	75 k Ω	±30%	VCC_HPM	
TMS	Pull-up	75 k Ω	±30%	VCC_HPM	
TCK	Pull-up	75 k Ω	±30%	VCC_HPM	
TRST#	Pull-up	75 k Ω	±30%	VCC_HPM	
USB					
USB_DP[3:0], USB_DN[3:0]	Pull-down	15 k Ω	±20%	n/a	
PMIC/SPI2					
PWRGOOD	n/a	n/a			
RESET#	disable	n/a			
PMIC_INT	disable	n/a			
VR_COMP#	n/a	n/a			
EXIT_STDBY	Pull-down	75 kΩ	±30%		
SPI_2_CS#	Pull-up	75 kΩ	±30%	VCC_PMIC	
SPI_2_SDO	Pull-down	75 kΩ	±30%	VCC_PMIC	
SPI_2_SDI	disable	n/a		VCC_PMIC	
SPI_2_CLK	Pull-down	75 kΩ	±30%	VCC_PMIC	
SPI1					
SPI_1_CS[3:0]#	Pull-up	75 kΩ	±30%	VCC_SPI	
SPI_1_SDO	Pull-down	75 kΩ	±30%		
SPI_1_SDI	Pull-down	75 kΩ	±30%		

Table 6-46. Default Integrated Pull-Up and Pull-Down Signals (Sheet 2 of 2)

Signal/Pin	Resistor	Nominal	Tolerance	Pull Up Rail	Notes
SPI_1_CLK	Pull-down	75 kΩ	±30%		
I2C					
I2C_2_SDATA	disable	n/a	±30%	VCCP_MISC	
I2C_2_SCK	disable	n/a	±30%	VCCP_MISC	
I2C_1_SDATA	disable	n/a	±30%	VCCP_MISC	
I2C_1_SCK	disable	n/a	±30%	VCCP_MISC	
I2C_0_SDATA	disable	n/a	±30%	VCCP_MISC	
I2C_0_SCK	disable	n/a	±30%	VCCP_MISC	
Spare GPIOs					
GPIO[18:17]	Pull-up	75 kΩ		VCCP_LEGACY	
GPIO[19]	disable	n/a		VCCP_LEGACY	
GPIO[22:20]	Pull-down	75 kΩ		VCCP_LEGACY	
GPIO[23]	disable	n/a		VCCP_LEGACY	
GPIO[36:34]	disable	n/a		VCCP_MISC	
GPIO[43:41]	disable	n/a		VCCP_MISC	
GPIO[51:45]	disable	n/a		VCCP_MISC	
GPIO[61:59]	disable	n/a		VCCP_MISC	

Note: The default Intel® SM35 Express Chipset integrated pull-up and pull-down signals are based on configuration registers.

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7 Mechanical and Package Specification

7.1 PCH Mechanical and Package Acronyms

Table 7-47. Mechanical and Package—Acronyms

Acronym	Description
BGA	Ball Grid Array
BO	Ball Out
DO	Die Outline
PL	Pin List

7.2 PCH Ballout Pin Information

Table 7-48 lists the PCH ballout information arranged alphabetically by signal name. Table 7-49 lists the ballout arranged numerically by pin number.

Table 7-48. PCH Ballout (Sort by Pin Name) (Sheet 1 of 14)

Pin Name	Pin #
A20GATE	F1
CDMI_COMP	F10
CDMI_RX_CVREF	G10
CDMI_RX_GVREF	H12
CDMI_RXCHAR#	H13
CDMI_RXD0	F12
CDMI_RXD1	B7
CDMI_RXD2	D9
CDMI_RXD3	A8
CDMI_RXD4	B9
CDMI_RXD5	G12
CDMI_RXD6	E10
CDMI_RXD7	A10
CDMI_RXPWR#	B11
CDMI_RXSN	E8
CDMI_RXSP	A6
CDMI_TXCHAR#	A16
CDMI_TXD0	D11
CDMI_TXD1	A12

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 2 of 14)

Pin Name	Pin #
CDMI_TXD2	F14
CDMI_TXD3	E12
CDMI_TXD4	B13
CDMI_TXD5	G14
CDMI_TXD6	A14
CDMI_TXD7	D13
CDMI_TXPWR#	F16
CDMI_TXSN	B15
CDMI_TXSP	E14
CDVO_RX_CVREF	G18
CDVO_RX_GVREF	H16
CDVO_RXD[0]	D17
CDVO_RXD[1]	G16
CDVO_RXD[2]	E18
CDVO_RXD[3]	B19
CDVO_RXD[4]	A18
CDVO_RXD[5]	F18
CDVO_RXPWR#	D19
CDVO_RXSN	B17
CDVO_RXSP	E16
CDVO_STALL#	H15
CDVO_VBLNK	D15
CPU_HCLKSEL	E21
CPU_PWRMODE[0]	E22
CPU_PWRMODE[1]	A22
CPU_PWRMODE[2]	B23
EXIT_STDBY	M1
GPE#	H1
GPIO34	V3
GPIO35	V5
GPIO36	T8
GPIO41	AC4
GPIO42	AC2
GPIO43	Y7
GPIO44	AC7
GPIO45	AD5
GPIO46	AA8
GPIO47	AE4

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 3 of 14)

Pin Name	Pin #
GPIO48	AB6
GPIO49	AC6
GPIO50	Y8
GPIO51	AD4
GPIO59	T3
GPIO60	T1
GPIO61	P1
HCLKN	E7
HCLKP	E6
HDA_CLK	AF23
HDA_DOCKEN#	AG22
HDA_DOCKRST#	AE22
HDA_RST#	Y21
HDA_SDI[0]	AC22
HDA_SDI[1]	AB20
HDA_SDO	AB22
HDA_SYNC	AA20
HDMI_CLKN	AG12
HDMI_CLKP	AE12
HDMI_COMP	AB12
HDMI_DATA0N	AA12
HDMI_DATA0P	Y12
HDMI_DATA1N	AB14
HDMI_DATA1P	AB13
HDMI_DATA2N	AC14
HDMI_DATA2P	AC13
HDMI_HPD	AC16
HRCOMP	K3
I2C_0_SCLK	T6
I2C_0_SDATA	T5
I2C_1_SCLK	AC5
I2C_1_SDATA	AB5
I2C_2_SCLK	P3
I2C_2_SDATA	P5
LPC_CLKOUT[0]	V7
LPC_CLKOUT[1]	V6
LPC_CLKOUT[2]	Y1
LPC_CLKRUN	Y3

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 4 of 14)

Pin Name	Pin #
LPC_FRAME#	AA2
LPC_LAD[0]	V8
LPC_LAD[1]	AB3
LPC_LAD[2]	AB1
LPC_LAD[3]	Y6
LPC_RESET#	T7
LPC_SERIRQ	Y5
MED_CLK	V1
NC	A27
NC	AE8
NC	AF7
NC	AG1
NC	AG8
OSC_IN	G8
OSC_OUT	F7
PMIC_INT	P8
PWRGOOD	P6
RCBIN	AB4
RESET#	P7
RESET_OUT#	L2
RSVD	AB16
RSVD	Y25
RSVD	Y22
RSVD	V25
RTC_CLK	M5
SATA_LED#	K5
SATA_REXT	AE10
SATA_RXN	AG10
SATA_RXP	AF9
SATA_TXN	AF5
SATA_TXP	AG6
SDIO_0_CD#	Y23
SDIO_0_CLK	W24
SDIO_0_CMD	W26
SDIO_0_DATA[0]	T23
SDIO_0_DATA[1]	T22
SDIO_0_DATA[2]	V27
SDIO_0_DATA[3]	U26

Table 7-48. PCH Ballout (Sort by Pin Name) (Sheet 5 of 14)

Pin Name	Pin #
SDIO_0_PD#	V24
SDIO_0_WP	V22
SDIO_1_CD#	F23
SDIO_1_CLK	D24
SDIO_1_CMD	D23
SDIO_1_DATA[0]	C24
SDIO_1_DATA[1]	H20
SDIO_1_DATA[2]	H21
SDIO_1_DATA[3]	H22
SDIO_1_DATA[4]	G22
SDIO_1_DATA[5]	G23
SDIO_1_DATA[6]	F24
SDIO_1_DATA[7]	D25
SDIO_1_PD#	Y27
SDIO_1_WP	G20
SDIO_2_CLK	T25
SDIO_2_CMD	R26
SDIO_2_DATA[0]	P25
SDIO_2_DATA[1]	P23
SDIO_2_DATA[2]	P27
SDIO_2_DATA[3]	T27
SDIO_2_PD#	V23
SLFREF#	K1
SLP_S3#	K6
SLP_S4#	H5
SLP_S5#	K7
SMI#	H3
SPI_1_CLK	F5
SPI_1_CS[0]#	E2
SPI_1_CS[1]#	H6
SPI_1_CS[2]#	F2
SPI_1_CS[3]#	K8
SPI_1_SDI	H7
SPI_1_SDO	F4
SPI_2_CLK	M7
SPI_2_CS#	M3
SPI_2_SDI	M8
SPI_2_SDO	M6

Table 7-48. PCH Ballout (Sort by Pin Name) (Sheet 6 of 14)

Pin Name	Pin #
SPKR	U2
TCK	H18
TDI	D21
TDO	H19
TMS	A20
TP	D4
TP	B1
TP	B5
TP	B21
TP	D1
TP	E26
TP	F25
TP	F27
TP	G26
TP	H25
TP	H27
TP	J26
TP	K22
TP	K23
TP	K25
TP	K27
TP	L26
TP	M21
TP	M22
TP	M23
TP	M25
TP	M27
TP	N26
TP	P20
TP	P21
TP	P22
TP	R20
TP	Y16
TP	AA16
TP	AA18
TP	AA23
TP	AB17
TP	AB18

Table 7-48. PCH Ballout (Sort by Pin Name) (Sheet 7 of 14)

Pin Name	Pin #
TP	AB19
TP	AC17
TP	AC18
TP	AC20
TP	AE14
TP	AE16
TP	AE18
TP	AE20
TP	AF19
TP	AF22
TP	AG2
TP	AG4
TP	AG14
TP	AG16
TP	AG18
TP	AG20
TRST#	E20
USB_DN[0]	AB25
USB_DN[1]	AC24
USB_DN[2]	AD24
USB_DN[3]	AB27
USB_DP[0]	AC26
USB_DP[1]	AD25
USB_DP[2]	AE24
USB_DP[3]	AA26
USB_REFEXT	AB24
VCC	P14
VCC	R12
VCC	R15
VCC	V13
VCC	V15
VCC_2P5	L12
VCC_HCLK_0P8	D3
VCC_HCLK_3P3	D5
VCC_HDMI_3P3	Y10
VCC_HDMI_3P3	AA10
VCC_HPM	K18
VCC_PMIC	N9

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 8 of 14)

Pin Name	Pin #
VCC_SATA_1P2	AB10
VCC_SATA_2P5	AC10
VCC_SDIO0	R17
VCC_SDIO0	R18
VCC_SDIO0	T20
VCC_SDIO0	T21
VCC_SDIO1	K20
VCC_SDIO1	K21
VCC_SDIO1	L17
VCC_SDIO1	L19
VCC_SDIO2	P18
VCC_SPI	L10
VCCA_DMIDVO	K10
VCCA_DPLL	AE6
VCCA_HDMIBG	AB11
VCCA_HDMI_1P2	Y14
VCCA_HDMI_1P8	AA14
VCCA_HPLL	H8
VCCA_UPLL_1P2	Y18
VCCA_UPLL_2P5	U18
VCCA_UPLL_2P5	U20
VCCA_USB_3P3	Y20
VCCP_AUDIO	V20
VCCP_DMIDVO	J2
VCCP_DMIDVO	J4
VCCP_DMIDVO	J11
VCCP_DMIDVO	J14
VCCP_DMIDVO	K12
VCCP_DMIDVO	K15
VCCP_DMIDVO	K16
VCCP_LEGACY	L9
VCCP_MISC	R10
VCCP_MISC	V10
VCCP_MISC	U10
VR_COMP#	N2
VSS	C4
VSS	L11
VSS	C6

Table 7-48. PCH Ballout (Sort by Pin Name) (Sheet 9 of 14)

Pin Name	Pin #
VSS	C8
VSS	C10
VSS	C12
VSS	C14
VSS	C16
VSS	C18
VSS	C20
VSS	C22
VSS	D7
VSS	E4
VSS	E5
VSS	E9
VSS	E11
VSS	E13
VSS	E15
VSS	E17
VSS	E19
VSS	E23
VSS	E24
VSS	F6
VSS	F8
VSS	F9
VSS	F11
VSS	F13
VSS	F15
VSS	F17
VSS	F19
VSS	F20
VSS	F21
VSS	F22
VSS	G2
VSS	G4
VSS	G5
VSS	G6
VSS	G9
VSS	G11
VSS	G13
VSS	G15

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 10 of 14)

Pin Name	Pin #
VSS	G17
VSS	G19
VSS	G24
VSS	H9
VSS	H11
VSS	H14
VSS	H17
VSS	H23
VSS	J5
VSS	J6
VSS	J7
VSS	J8
VSS	J12
VSS	J16
VSS	J17
VSS	J20
VSS	J21
VSS	J22
VSS	J23
VSS	J24
VSS	K13
VSS	L4
VSS	L5
VSS	L6
VSS	L7
VSS	L8
VSS	L13
VSS	L14
VSS	L15
VSS	L16
VSS	L18
VSS	L20
VSS	L21
VSS	L22
VSS	L23
VSS	L24
VSS	M20
VSS	N4

Table 7-48. PCH Ballout (Sort by Pin Name) (Sheet 11 of 14)

Pin Name	Pin #
VSS	N5
VSS	N6
VSS	N7
VSS	N8
VSS	N10
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N15
VSS	N16
VSS	N17
VSS	N18
VSS	N19
VSS	N20
VSS	N21
VSS	N22
VSS	N23
VSS	N24
VSS	P11
VSS	P12
VSS	P16
VSS	R2
VSS	R4
VSS	R5
VSS	R6
VSS	R7
VSS	R8
VSS	R13
VSS	R21
VSS	R22
VSS	R23
VSS	R24
VSS	T11
VSS	T13
VSS	T15
VSS	T17
VSS	T19

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 12 of 14)

Pin Name	Pin #
VSS	U4
VSS	U5
VSS	U6
VSS	U7
VSS	U8
VSS	U12
VSS	U14
VSS	U16
VSS	U21
VSS	U22
VSS	U23
VSS	U24
VSS	U25
VSS	V11
VSS	V12
VSS	V14
VSS	V16
VSS	V17
VSS	V18
VSS	V19
VSS	V21
VSS	W2
VSS	W4
VSS	W6
VSS	W7
VSS	W8
VSS	W20
VSS	W21
VSS	W22
VSS	W23
VSS	Y9
VSS	Y11
VSS	Y13
VSS	Y15
VSS	Y17
VSS	Y19
VSS	AA4
VSS	AA5

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 13 of 14)

Pin Name	Pin #
VSS	AA6
VSS	AA9
VSS	AA11
VSS	AA13
VSS	AA15
VSS	AA17
VSS	AA19
VSS	AA22
VSS	AA24
VSS	AB7
VSS	AB9
VSS	AB15
VSS	AB21
VSS	AC8
VSS	AC9
VSS	AC12
VSS	AC15
VSS	AC19
VSS	AC21
VSS	AC23
VSS	AD3
VSS	AD7
VSS	AD9
VSS	AD11
VSS	AD13
VSS	AD15
VSS	AD17
VSS	AD19
VSS	AD21
VSS	AD23
VSS	AF11
VSS	AF13
VSS	AF15
VSS	AF17
VSS_NCTF	B27
VSS_NCTF	AD1
VSS_NCTF	AF27
VSS_NCTF	AD27

Table 7-48.PCH Ballout (Sort by Pin Name) (Sheet 14 of 14)

Pin Name	Pin #
VSS_NCTF	AG26
VSS_NCTF	AF26
VSS_NCTF	B26
VSS_NCTF	AG25
VSS_NCTF	A26
VSS_NCTF	A24
VSS_NCTF	A4
VSS_NCTF	AF2
VSS_NCTF	B2
VSS_NCTF	A2
VSS_NCTF	AF1
VSS_NCTF	AG27
VSS_NCTF	D27
VSSA_DPLL	AB8
VSSA_HDMIBG	AC11
VSSA_HPLL	H10
VSSA_UPLL	AB23

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 1 of 14)

Pin #	Pin Name
A10	CDMI_RXD[7]
A12	CDMI_TXD[1]
A14	CDMI_TXD[6]
A16	CDMI_TXCHAR#
A18	CDVO_RXD[4]
A2	VSS_NCTF
A20	TMS
A22	CPU_PWRMODE[1]
A24	VSS_NCTF
A26	VSS_NCTF
A27	NC
A4	VSS_NCTF
A6	CDMI_RXSP
A8	CDMI_RXD[3]
AA10	VCC_HDMI_3P3
AA11	VSS
AA12	HDMI_DATA0N

Table 7-49. PCH Ballout (Sort by Pin Number) (Sheet 2 of 14)

Pin #	Pin Name
AA13	VSS
AA14	VCCA_HDMI_1P8
AA15	VSS
AA16	TP
AA17	VSS
AA18	TP
AA19	VSS
AA2	LPC_FRAME#
AA20	HDA_SYNC
AA22	VSS
AA23	TP
AA24	VSS
AA26	USB_DP[3]
AA4	VSS
AA5	VSS
AA6	VSS
AA8	GPIO46
AA9	VSS
AB1	LPC_LAD[2]
AB10	VCC_SATA_1P2
AB11	VCCA_HDMIBG
AB12	HDMI_COMP
AB13	HDMI_DATA1P
AB14	HDMI_DATA1N
AB15	VSS
AB16	RSVD
AB17	TP
AB18	TP
AB19	TP
AB20	HDA_SDI[1]
AB21	VSS
AB22	HDA_SDO
AB23	VSSA_UPLL
AB24	USB_REFEXT
AB25	USB_DN[0]
AB27	USB_DN[3]
AB3	LPC_LAD[1]
AB4	RCBIN

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 3 of 14)

Pin #	Pin Name
AB5	I2C_1_SDATA
AB6	GPIO48
AB7	VSS
AB8	VSSA_DPLL
AB9	VSS
AC10	VCC_SATA_2P5
AC11	VSSA_HDMIBG
AC12	VSS
AC13	HDMI_DATA2P
AC14	HDMI_DATA2N
AC15	VSS
AC16	HDMI_HPD
AC17	TP
AC18	TP
AC19	VSS
AC2	GPIO42
AC20	TP
AC21	VSS
AC22	HDA_SDI[0]
AC23	VSS
AC24	USB_DN[1]
AC26	USB_DP[0]
AC4	GPIO41
AC5	I2C_1_SCLK
AC6	GPIO49
AC7	GPIO44
AC8	VSS
AC9	VSS
AD1	VSS_NCTF
AD11	VSS
AD13	VSS
AD15	VSS
AD17	VSS
AD19	VSS
AD21	VSS
AD23	VSS
AD24	USB_DN[2]
AD25	USB_DP[1]

Table 7-49. PCH Ballout (Sort by Pin Number) (Sheet 4 of 14)

Pin #	Pin Name
AD27	VSS_NCTF
AD3	VSS
AD4	GPIO51
AD5	GPIO45
AD7	VSS
AD9	VSS
AE10	SATA_REXT
AE12	HDMI_CLKP
AE14	TP
AE16	TP
AE18	TP
AE20	TP
AE22	HDA_DOCKRST#
AE24	USB_DP[2]
AE4	GPIO47
AE6	VCCA_DPLL
AE8	NC
AF1	VSS_NCTF
AF11	VSS
AF13	VSS
AF15	VSS
AF17	VSS
AF19	TP
AF2	VSS_NCTF
AF22	TP
AF23	HDA_CLK
AF26	VSS_NCTF
AF27	VSS_NCTF
AF5	SATA_TXN
AF7	NC
AF9	SATA_RXP
AG1	NC
AG10	SATA_RXN
AG12	HDMI_CLKN
AG14	TP
AG16	TP
AG18	TP
AG2	TP

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 5 of 14)

Pin #	Pin Name
AG20	TP
AG22	HDA_DOCKEN#
AG25	VSS_NCTF
AG26	VSS_NCTF
AG27	VSS_NCTF
AG4	TP
AG6	SATA_TXP
AG8	NC
B1	TP
B11	CDMI_RXPWR#
B13	CDMI_TXD[4]
B15	CDMI_TXSN
B17	CDVO_RXSN
B19	CDVO_RXD[3]
B2	VSS_NCTF
B21	TP
B23	CPU_PWRMODE[2]
B26	VSS_NCTF
B27	VSS_NCTF
B5	TP
B7	CDMI_RXD[1]
B9	CDMI_RXD[4]
C10	VSS
C12	VSS
C14	VSS
C16	VSS
C18	VSS
C20	VSS
C22	VSS
C24	SDIO_1_DATA0
C4	VSS
C6	VSS
C8	VSS
D1	TP
D11	CDMI_TXD[0]
D13	CDMI_TXD[7]
D15	CDVO_VBLNK
D17	CDVO_RXD[0]

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 6 of 14)

Pin #	Pin Name
D19	CDVO_RXPWR#
D21	TDI
D23	SDIO_1_CMD
D24	SDIO_1_CLK
D25	SDIO_1_DATA7
D27	VSS_NCTF
D3	VCC_HCLK_0P8
D4	RSVD
D5	VCC_HCLK_3P3
D7	VSS
D9	CDMI_RXD[2]
E10	CDMI_RXD[6]
E11	VSS
E12	CDMI_TXD[3]
E13	VSS
E14	CDMI_TXSP
E15	VSS
E16	CDVO_RXSP
E17	VSS
E18	CDVO_RXD[2]
E19	VSS
E2	SPI_1_CS[0]#
E20	TRST#
E21	CPU_HCLKSEL
E22	CPU_PWRMODE[0]
E23	VSS
E24	VSS
E26	TP
E4	VSS
E5	VSS
E6	HCLKP
E7	HCLKN
E8	CDMI_RXSN
E9	VSS
F1	A20GATE
F10	CDMI_COMP
F11	VSS
F12	CDMI_RXD[0]

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 7 of 14)

Pin #	Pin Name
F13	VSS
F14	CDMI_TXD[2]
F15	VSS
F16	CDMI_TXPWR#
F17	VSS
F18	CDVO_RXD[5]
F19	VSS
F2	SPI_1_CS[2]#
F20	VSS
F21	VSS
F22	VSS
F23	SDIO_1_CD#
F24	SDIO_1_DATA6
F25	TP
F27	TP
F4	SPI_1_SDO
F5	SPI_1_CLK
F6	VSS
F7	OSC_OUT
F8	VSS
F9	VSS
G10	CDMI_RX_CVREF
G11	VSS
G12	CDMI_RXD[5]
G13	VSS
G14	CDMI_TXD[5]
G15	VSS
G16	CDVO_RXD[1]
G17	VSS
G18	CDVO_RX_CVREF
G19	VSS
G2	VSS
G20	SDIO_1_WP
G22	SDIO_1_DATA4
G23	SDIO_1_DATA5
G24	VSS
G26	TP
G4	VSS

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 8 of 14)

Pin #	Pin Name
G5	VSS
G6	VSS
G8	OSC_IN
G9	VSS
H1	GPE#
H10	VSSA_HPLL
H11	VSS
H12	CDMI_RX_GVREF
H13	CDMI_RXCHAR#
H14	VSS
H15	CDVO_STALL#
H16	CDVO_RX_GVREF
H17	VSS
H18	TCK
H19	TDO
H20	SDIO_1_DATA1
H21	SDIO_1_DATA2
H22	SDIO_1_DATA3
H23	VSS
H25	TP
H27	TP
H3	SMI#
H5	SLP_S4#
H6	SPI_1_CS[1]#
H7	SPI_1_SDI
H8	VCCA_HPLL
H9	VSS
J11	VCCP_DMIDVO
J12	VSS
J14	VCCP_DMIDVO
J16	VSS
J17	VSS
J2	VCCP_DMIDVO
J20	VSS
J21	VSS
J22	VSS
J23	VSS
J24	VSS

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 9 of 14)

Pin #	Pin Name
J26	TP
J4	VCCP_DMIDVO
J5	VSS
J6	VSS
J7	VSS
J8	VSS
K1	SLFREF#
K10	VCCA_DMIDVO
K12	VCCP_DMIDVO
K13	VSS
K15	VCCP_DMIDVO
K16	VCCP_DMIDVO
K18	VCC_HPM
K20	VCC_SDIO1
K21	VCC_SDIO1
K22	TP
K23	TP
K25	TP
K27	TP
K3	HRCOMP
K5	SATA_LED#
K6	SLP_S3#
K7	SLP_S5#
K8	SPI_1_CS[3]#
L10	VCC_SPI
L11	VSS
L12	VCC_2P5
L13	VSS
L14	VSS
L15	VSS
L16	VSS
L17	VCC_SDIO1
L18	VSS
L19	VCC_SDIO1
L2	RESET_OUT#
L20	VSS
L21	VSS
L22	VSS

Table 7-49. PCH Ballout (Sort by Pin Number) (Sheet 10 of 14)

Pin #	Pin Name
L23	VSS
L24	VSS
L26	TP
L4	VSS
L5	VSS
L6	VSS
L7	VSS
L8	VSS
L9	VCCP_LEGACY
M1	EXIT_STDBY
M20	VSS
M21	TP
M22	TP
M23	TP
M25	TP
M27	TP
M3	SPI_2_CS#
M5	RTC_CLK
M6	SPI_2_SDO
M7	SPI_2_CLK
M8	SPI_2_SDI
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
N17	VSS
N18	VSS
N19	VSS
N2	VR_COMP#
N20	VSS
N21	VSS
N22	VSS
N23	VSS
N24	VSS
N26	TP

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 11 of 14)

Pin #	Pin Name
N4	VSS
N5	VSS
N6	VSS
N7	VSS
N8	VSS
N9	VCC_PMIC
P1	GPIO61
P11	VSS
P12	VSS
P14	VCC
P16	VSS
P18	VCC_SDIO2
P20	TP
P21	TP
P22	TP
P23	SDIO_2_DATA[1]
P25	SDIO_2_DATA[0]
P27	SDIO_2_DATA[2]
P3	I2C_2_SCLK
P5	I2C_2_SDATA
P6	PWRGOOD
P7	RESET#
P8	PMIC_INT
R10	VCCP_MISC
R12	VCC
R13	VSS
R15	VCC
R17	VCC_SDIO0
R18	VCC_SDIO0
R2	VSS
R20	TP
R21	VSS
R22	VSS
R23	VSS
R24	VSS
R26	SDIO_2_CMD
R4	VSS
R5	VSS

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 12 of 14)

Pin #	Pin Name
R6	VSS
R7	VSS
R8	VSS
T1	GPIO60
T11	VSS
T13	VSS
T15	VSS
T17	VSS
T19	VSS
T20	VCC_SDIO0
T21	VCC_SDIO0
T22	SDIO_0_DATA[1]
T23	SDIO_0_DATA[0]
T25	SDIO_2_CLK
T27	SDIO_2_DATA[3]
T3	GPIO59
T5	I2C_0_SDATA
T6	I2C_0_SCLK
T7	LPC_RESET#
T8	GPIO36
U10	VCCP_MISC
U12	VSS
U14	VSS
U16	VSS
U18	VCCA_UPLL_2P5
U2	SPKR
U20	VCCA_UPLL_2P5
U21	VSS
U22	VSS
U23	VSS
U24	VSS
U25	VSS
U26	SDIO_0_DATA[3]
U4	VSS
U5	VSS
U6	VSS
U7	VSS
U8	VSS

Table 7-49.PCH Ballout (Sort by Pin Number) (Sheet 13 of 14)

Pin #	Pin Name
V1	MED_CLK
V10	VCCP_MISC
V11	VSS
V12	VSS
V13	VCC
V14	VSS
V15	VCC
V16	VSS
V17	VSS
V18	VSS
V19	VSS
V20	VCCP_AUDIO
V21	VSS
V22	SDIO_0_WP
V23	SDIO_2_PD#
V24	SDIO_0_PD#
V25	RSVD
V27	SDIO_0_DATA[2]
V3	GPIO34
V5	GPIO35
V6	LPC_CLKOUT[1]
V7	LPC_CLKOUT[0]
V8	LPC_LAD[0]
W2	VSS
W20	VSS
W21	VSS
W22	VSS
W23	VSS
W24	SDIO_0_CLK
W26	SDIO_0_CMD
W4	VSS
W5	VSS
W6	VSS
W7	VSS
W8	VSS
Y1	LPC_CLKOUT[2]
Y10	VCC_HDMI_3P3
Y11	VSS

Table 7-49. PCH Ballout (Sort by Pin Number) (Sheet 14 of 14)

Pin #	Pin Name
Y12	HDMI_DATA0P
Y13	VSS
Y14	VCCA_HDMI_1P2
Y15	VSS
Y16	TP
Y17	VSS
Y18	VCCA_UPLL_1P2
Y19	VSS
Y20	VCCA_USB_3P3
Y21	HDA_RST#
Y22	RSVD
Y23	SDIO_0_CD#
Y25	RSVD
Y27	SDIO_1_PD#
Y3	LPC_CLKRUN
Y5	LPC_SERIRQ
Y6	LPC_LAD[3]
Y7	GPIO43
Y8	GPIO50
Y9	VSS

7.3 PCH Package Specifications

The PCH comes in a Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 493 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters. Key package attributes are listed below:

Dimensions:

- Package parameters: 14 mm x 14 mm

- Height 1.3 mm (maximum)
- Ball Count: 493
- Land metal diameter: See following Diagrams
- Solder resist opening: See following Diagrams

7.4 PCH Package Diagrams

Figure 7-4. PCH (Top View)

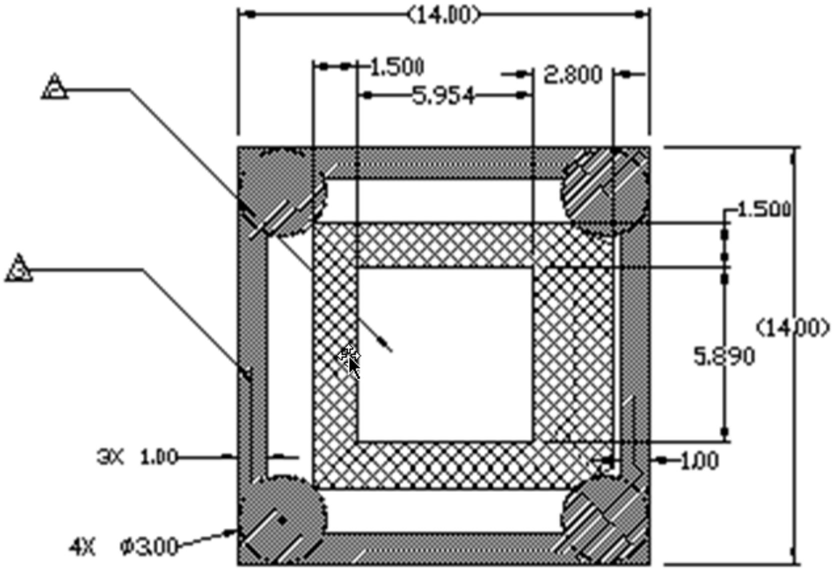


Figure 7-5. PCH (Bottom View)

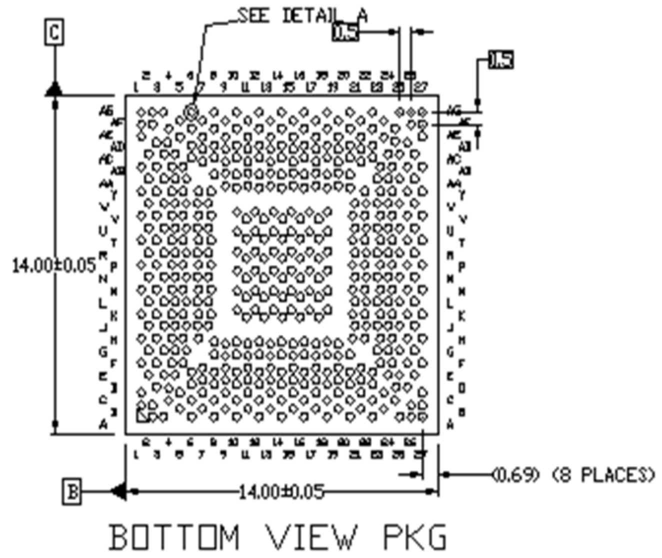
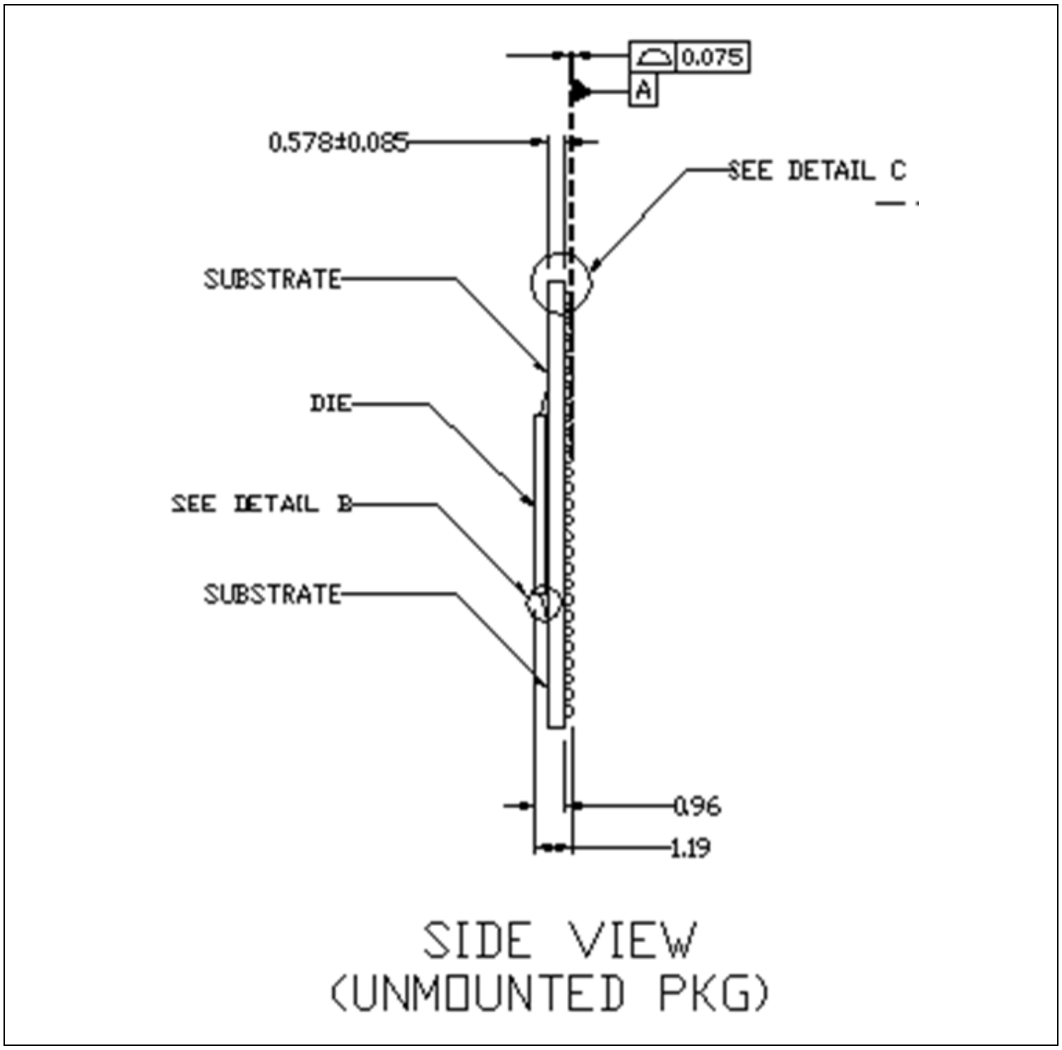


Figure 7-6. PCH (Side View, Unmounted)



NOTE:The maximum outgoing package coplanarity cannot exceed 8 mils.

Figure 7-7. PCH Package (Solder Ball Detail)

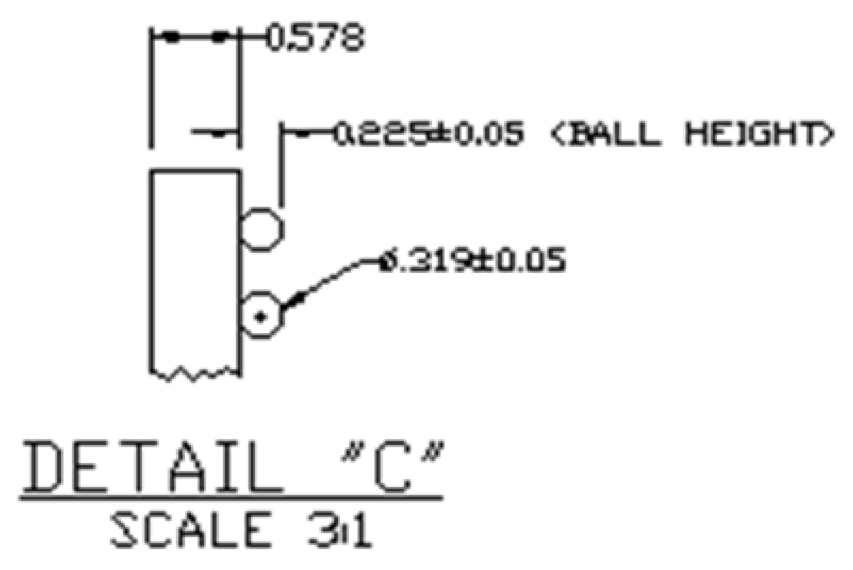


Figure 7-8. PCH Package (Underfill Detail)

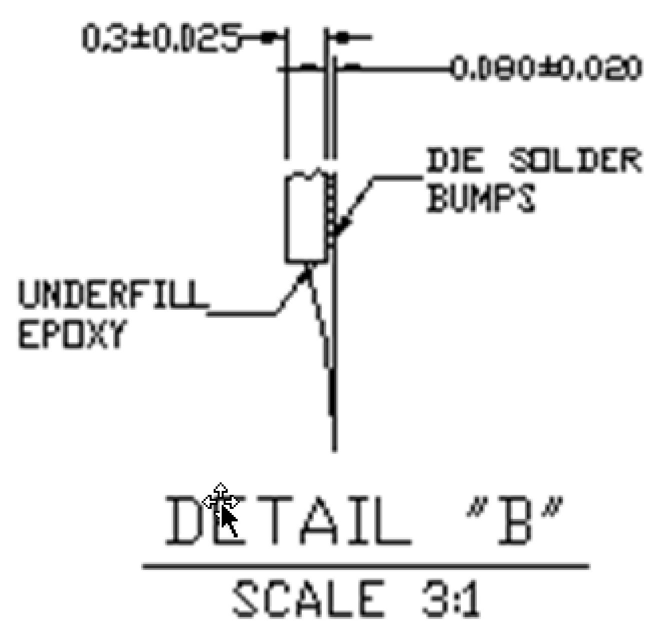
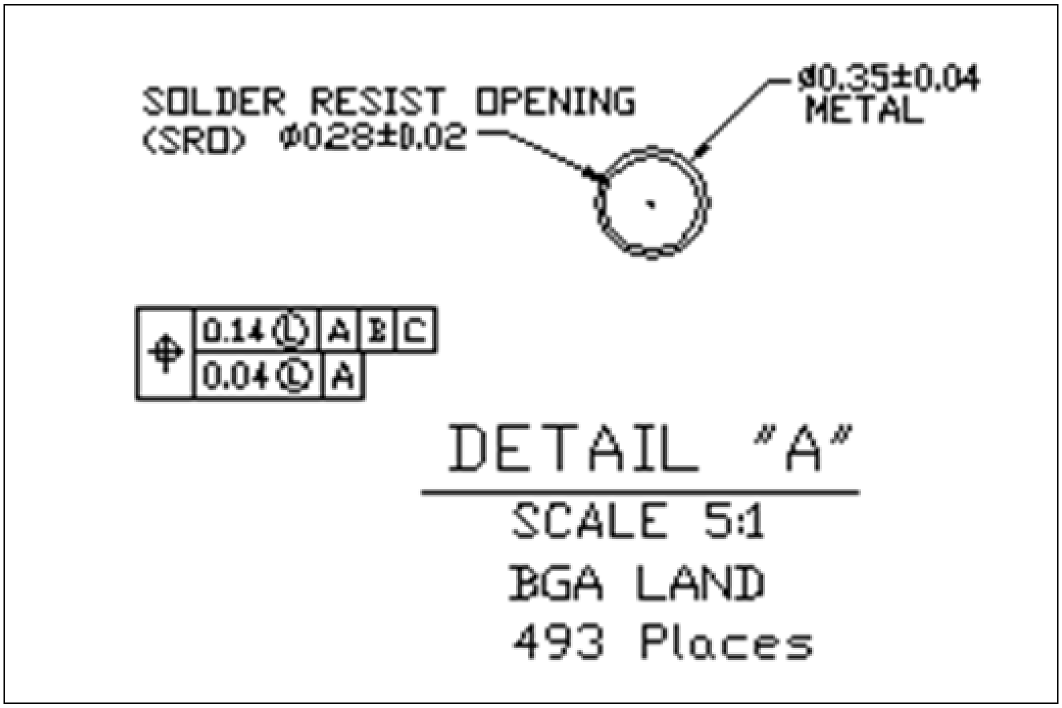


Figure 7-9. PCH Package (Solder Resist Opening)



7.5 PCH Ballout Definition and Signal Locations

Table 7-50.PCH Ball Map—Signal Locations (1–6)

	6	5	4	3	2	1	
AG	SATA_TXP		TP		TP	NC	AG
AF		SATA_TXN			VSS_NCTF	VSS_NCTF	AF
AE	VCCA_DPLL		GPIO47				AE
AD		GPIO45	GPIO51	VSS		VSS_NCTF	AD
AC	GPIO49	I2C_1_SCLK	GPIO41		GPIO42		AC
AB	GPIO48	I2C_1_SDATA	RCBIN	LPC_LAD[1]		LPC_LAD[2]	AB
AA	VSS	VSS	VSS		LPC_FRAME#		AA
Y	LPC_LAD[3]	LPC_SERIRQ		LPC_CLKRUN		LPC_CLKOUT[2]	Y
W	VSS	VSS	VSS		VSS		W
V	LPC_CLKOUT[1]	GPIO35		GPIO34		MED_CLK	V
U	VSS	VSS	VSS		SPKR		U
T	I2C_0_SCLK	I2C_0_SDATA		GPIO59		GPIO60	T
R	VSS	VSS	VSS		VSS		R
P	PWRGOOD	I2C_2_SDATA		I2C_2_SCLK		GPIO61	P
N	VSS	VSS	VSS		VR_COMP#		N
M	SPI_2_SDO	RTC_CLK		SPI_2_CS#		EXIT_STDBY	M
L	VSS	VSS	VSS		RESET_OUT#		L
K	SLP_S3#	SATA_LED#		HRCOMP		SLFREF#	K
J	VSS	VSS	VCCP_DMIDVO		VCCP_DMIDVO		J
H	SPI_1_CS[1]#	SLP_S4#		SMI#		GPE#	H
G	VSS	VSS	VSS		VSS		G
F	VSS	SPI_1_CLK	SPI_1_SDO		SPI_1_CS[2]#	A20GATE	F
E	HCLKP	VSS	VSS		SPI_1_CS[0]#		E
D		VCC_HCLK_3P3	TP	VCC_HCLK_0P8		TP	D
C	VSS		VSS				C
B		TP			VSS_NCTF	TP	B
A	CDMI_RXSP		VSS_NCTF		VSS_NCTF		A
	6	5	4	3	2	1	

Table 7-51.PCH Ball Map—Signal Locations (7-13)

	13	12	11	10	9	8	7	
AG		HDMI_CLKN		SATA_RXN		NC		AG
AF	VSS		VSS		SATA_RXP		NC	AF
AE		HDMI_CLKP		SATA_REXT		NC		AE
AD	VSS		VSS		VSS		VSS	AD
AC	HDMI_DATA2P	VSS	VSSA_HDMIBG	VCC_SATA_2P5	VSS	VSS	GPIO44	AC
AB	HDMI_DATA1P	HDMI_COMP	VCCA_HDMIBG	VCC_SATA_1P2	VSS	VSSA_DPLL	VSS	AB
AA	VSS	HDMI_DATA0N	VSS	VCC_HDMI_3P3	VSS	GPIO46		AA
Y	VSS	HDMI_DATA0P	VSS	VCC_HDMI_3P3	VSS	GPIO50	GPIO43	Y
W						VSS	VSS	W
V	VCC	VSS	VSS	VCCP_MISC		LPC_LAD[0]	LPC_CLKOUT[0]	V
U		VSS		VCCP_MISC		VSS	VSS	U
T	VSS		VSS			GPIO36	LPC_RESET#	T
R	VSS	VCC		VCCP_MISC		VSS	VSS	R
P		VSS	VSS			PMIC_INT	RESET#	P
N	VSS	VSS	VSS	VSS	VCC_PMIC	VSS	VSS	N
M						SPI_2_SDI	SPI_2_CLK	M
L	VSS	VCC_2P5	VSS	VCC_SPI	VCCP_LEGACY	VSS	VSS	L
K	VSS	VCCP_DMIDVO		VCCA_DMIDVO		SPI_1_CS[3]#	SLP_S5#	K
J		VSS	VCCP_DMIDVO			VSS	VSS	J
H	CDMI_RXCHAR#	CDMI_RX_GVREF	VSS	VSSA_HPLL	VSS	VCCA_HPLL	SPI_1_SDI	H
G	VSS	CDMI_RXD5	VSS	CDMI_RX_CVREF	VSS	OSC_IN		G
F	VSS	CDMI_RXD0	VSS	CDMI_COMP	VSS	VSS	OSC_OUT	F
E	VSS	CDMI_TXD3	VSS	CDMI_RXD6	VSS	CDMI_RXSN	HCLKN	E
D	CDMI_TXD7		CDMI_TXD0		CDMI_RXD2		VSS	D
C		VSS		VSS		VSS		C
B	CDMI_TXD4		CDMI_RXPWR#		CDMI_RXD4		CDMI_RXD1	B
A		CDMI_TXD1		CDMI_RXD7		CDMI_RXD3		A
	13	12	11	10	9	8	7	

Table 7-52.PCH Ball Map—Signal Locations (14–20)

	20	19	18	17	16	15	14	
AG	TP		TP		TP		TP	AG
AF		TP		VSS		VSS		AF
AE	TP		TP		TP		TP	AE
AD		VSS		VSS		VSS		AD
AC	TP	VSS	TP	TP	HDMI_HPD	VSS	HDMI_DATA2N	AC
AB	HDA_SDI[1]	TP	TP	TP	RSVD	VSS	HDMI_DATA1N	AB
AA	HDA_SYNC	VSS	TP	VSS	TP	VSS	VCCA_HDMI_1P8	AA
Y	VCCA_USB_3P3	VSS	VCCA_UPLL_1P2	VSS	TP	VSS	VCCA_HDMI_1P2	Y
W	VSS							W
V	VCCP_AUDIO	VSS	VSS	VSS	VSS	VCC	VSS	V
U	VCCA_UPLL_2P5		VCCA_UPLL_2P5		VSS		VSS	U
T	VCC_SDIO0	VSS		VSS		VSS		T
R	TP		VCC_SDIO0	VCC_SDIO0		VCC		R
P	TP		VCC_SDIO2		VSS		VCC	P
N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	N
M	VSS							M
L	VSS	VCC_SDIO1	VSS	VCC_SDIO1	VSS	VSS	VSS	L
K	VCC_SDIO1		VCC_HPM		VCCP_DMIDVO	VCCP_DMIDVO		K
J	VSS			VSS	VSS		VCCP_DMIDVO	J
H	SDIO_1_DATA[1]	TDO	TCK	VSS	CDVO_RX_GVREF	CDVO_STALL#	VSS	H
G	SDIO_1_WP	VSS	CDVO_RX_CVREF	VSS	CDVO_RXD[1]	VSS	CDMI_TXD5	G
F	VSS	VSS	CDVO_RXD[5]	VSS	CDMI_TXPWR#	VSS	CDMI_TXD2	F
E	TRST#	VSS	CDVO_RXD[2]	VSS	CDVO_RXSP	VSS	CDMI_TXSP	E
D		CDVO_RXPWR#		CDVO_RXD[0]		CDVO_VBLNK		D
C	VSS		VSS		VSS		VSS	C
B		CDVO_RXD[3]		CDVO_RXSN		CDMI_TXSN		B
A	TMS		CDVO_RXD[4]		CDMI_TXCHAR#		CDMI_TXD6	A
	20	19	18	17	16	15	14	

Table 7-53.PCH Ball Map—Signal Locations (21–27)

	27	26	25	24	23	22	21	
AG	VSS_NCTF	VSS_NCTF	VSS_NCTF			HDA_DOCKEN#		AG
AF	VSS_NCTF	VSS_NCTF			HDA_CLK	TP		AF
AE				USB_DP[2]		HDA_DOCKRST#		AE
AD	VSS_NCTF		USB_DP[1]	USB_DN[2]	VSS		VSS	AD
AC		USB_DP[0]		USB_DN[1]	VSS	HDA_SDI[0]	VSS	AC
AB	USB_DN[3]		USB_DN[0]	USB_REFEXT	VSSA_UPLL	HDA_SDO	VSS	AB
AA		USB_DP[3]		VSS	TP	VSS		AA
Y	SDIO_1_CD#		RSVD		SDIO_0_CD#	RSVD	HDA_RST#	Y
W		SDIO_0_CMD		SDIO_0_CLK	VSS	VSS	VSS	W
V	SDIO_0_DATA[2]		RSVD	SDIO_0_PD#	SDIO_2_PD#	SDIO_0_WP	VSS	V
U		SDIO_0_DATA[3]	VSS	VSS	VSS	VSS	VSS	U
T	SDIO_2_DATA[3]		SDIO_2_CLK		SDIO_0_DATA[0]	SDIO_0_DATA[1]	VCC_SDIO0	T
R		SDIO_2_CMD		VSS	VSS	VSS	VSS	R
P	SDIO_2_DATA[2]		SDIO_2_DATA[0]		SDIO_2_DATA[1]	TP	TP	P
N		TP		VSS	VSS	VSS	VSS	N
M	TP		TP		TP	TP	TP	M
L		TP		VSS	VSS	VSS	VSS	L
K	TP		TP		TP	TP	VCC_SDIO1	K
J		TP		VSS	VSS	VSS	VSS	J
H	TP		TP		VSS	SDIO_1_DATA[3]	SDIO_1_DATA[2]	H
G		TP		VSS	SDIO_1_DATA[5]	SDIO_1_DATA[4]		G
F	TP		TP	SDIO_1_DATA[6]	SDIO_1_CD#	VSS	VSS	F
E		TP		VSS	VSS	CPU_PWRMODE[0]	CPU_HCLKSEL	E
D	VSS_NCTF		SDIO_1_DATA[7]	SDIO_1_CLK	SDIO_1_CMD		TDI	D
C				SDIO_1_DATA[0]		VSS		C
B	VSS_NCTF	VSS_NCTF			CPU_PWRMODE[2]		TP	B
A	NC	VSS_NCTF		VSS_NCTF		CPU_PWRMODE[1]		A
	27	26	25	24	23	22	21	

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