FAIRCHILD SEMICONDUCTOR®

March 2008

FST3245 — 8-Bit Bus Switch

Features

- 4Ω Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low I_{CC}
- Zero Bounce in Flow-through Mode
- Control Inputs Compatible with TTL Level

Description

The FST3245 switch provides eight-bits of high-speed CMOS TTL-compatible bus switching in a standard ’245 pin-out. The low on resistance allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as an eight-bit switch. When /OE is LOW, the switch is ON and port A is connected to port B. When /OE is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FST3245WMX	-40 to +85°C	20-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300-inch Wide	Tape and Reel
FST3245QSC	-40 to +85°C	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide	Tube
FST3245QSCX	-40 to +85°C	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide	Tape and Reel
FST3245MTC	-40 to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tube
FST3245MTCX	-40 to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

The Fairchild switch family derives from and embodies Fairchild’s proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

Logic Diagram

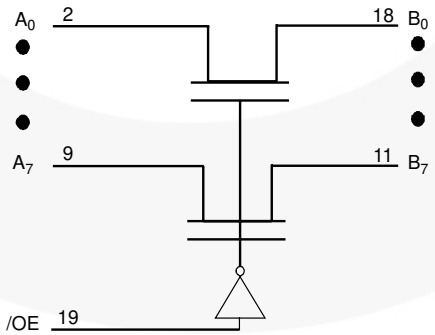


Figure 1. Logic Diagram

Pin Configuration

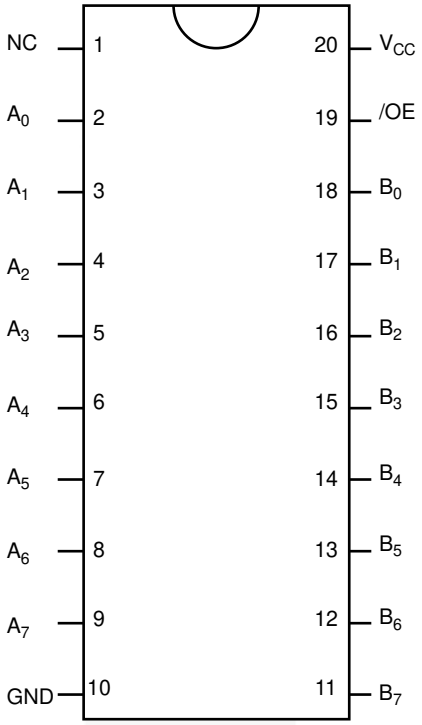


Figure 2. Pin Configuration

Pin Descriptions

Pin #	Pin Names	Description
1	NC	No Connnect
19	/OE	Bus Switch Enable
2,3,4,5,6,7,8,9	A_0,A_1,A_2,A_3,A_4,A_5,A_6,A_7	Bus A
10	GND	Ground
11,12,13,14,15,16,17,18	B_7,B_6,B_5,B_4,B_3,B_2,B_1,B_0	Bus B
20	V_{CC}	Supply Voltage

Truth Table

Input /OE	Function
LOW	Connect
HIGH	Disconnect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	7.0	V
V_S	DC Switch Voltage	-0.5	7.0	V
V_{IN}	DC Input Voltage[1]	-0.5	7.0	V
I_{IK}	DC Input Diode Current, $V_{IN} < 0V$		-50	mA
I_{OUT}	DC Output Sink Current		128	mA
I_{CC} / I_{GND}	DC V_{CC} / GND Current		±100	mA
T_{STG}	Storage Temperature Range	-65	+150	°C

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Power Supply Operating		4.0	5.5	V
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
t_r, t_f	Input Rise and Fall Time	Switch Control Input[2]	0	5	ns/V
		Switch I/O	0	DC	
T_A	Operating Temperature, Free Air		-40	+85	°C

Note:

2. Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Typical values are at V_{CC} = 5.0V and T_A = 25°C.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=-40 to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN} = -18mA	4.5			-1.2	V
V_{IH}	High-Level Input Voltage		4.0 to 5.5	2.0			V
V_{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	5.5			±1.0	µA
I_{OZ}	Off-state Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	µA
R_{ON}	Switch On Resistance(3)	V_{IN} = 0V, I_{IN} = 64mA	4.5		4	7	Ω
		V_{IN} = 0V, I_{IN} = 30mA	4.5		4	7	
		V_{IN} = 2.4V, I_{IN} = 15mA	4.5		8	15	
		V_{IN} = 2.4V, I_{IN} = 15mA	4.0		11	20	
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0	5.5			3	µA
ΔI_{CC}	Increase in I_{CC} per Input	One Input at 3.4V, Other Inputs at V_{CC} or GND	5.5			2.5	mA

Note:

3. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.

AC Electrical Characteristics

T_A = -40 to +85°C, C_L = 50pF, and R_U = R_D = 500Ω.

Symbol	Parameter	Conditions	V_{CC} = 4.5 – 5.5V		V_{CC} = 4.0V		Units	Figure
			Min.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay Bus-to-Bus(4)	V_{IN} = Open		0.25		0.25	ns	Figure 3 Figure 4
t_{PZH} ,t_{PZL}	Output Enable Time	V_{IN} = 7V for t_{PZL} V_{IN} = Open for t_{PZH}	1.5	5.9		6.4	ns	Figure 3 Figure 4
t_{PHZ}, t_{PLZ}	Output Disable Time	V_{IN} = 7V for t_{PLZ} V_{IN} = Open for t_{PHZ}	1.5	6.0		5.7	ns	Figure 3 Figure 4

Note:

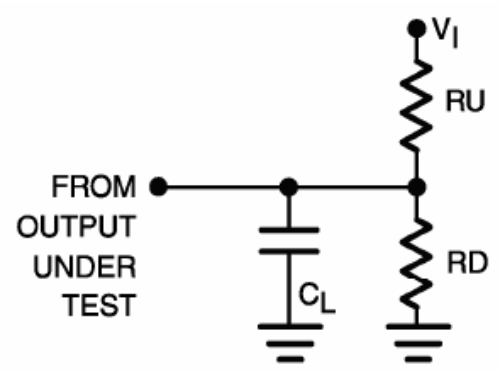
4. This parameter is guaranteed by design, but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance).

Capacitance

T_A = +25°C, f = 1MHz. Capacitance is characterized, but not tested.

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Control Pin Input Capacitance	V_{CC} = 5.0V	3	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC}, /OE = 5.0V	5	pF

AC Loadings and Waveforms



Notes: Input driven by 50Ω source terminated in 50Ω.
C_L includes load and stray capacitance.
Input PRR = 1.0MHz, t_w = 500ns.

Figure 3. AC Test Circuit

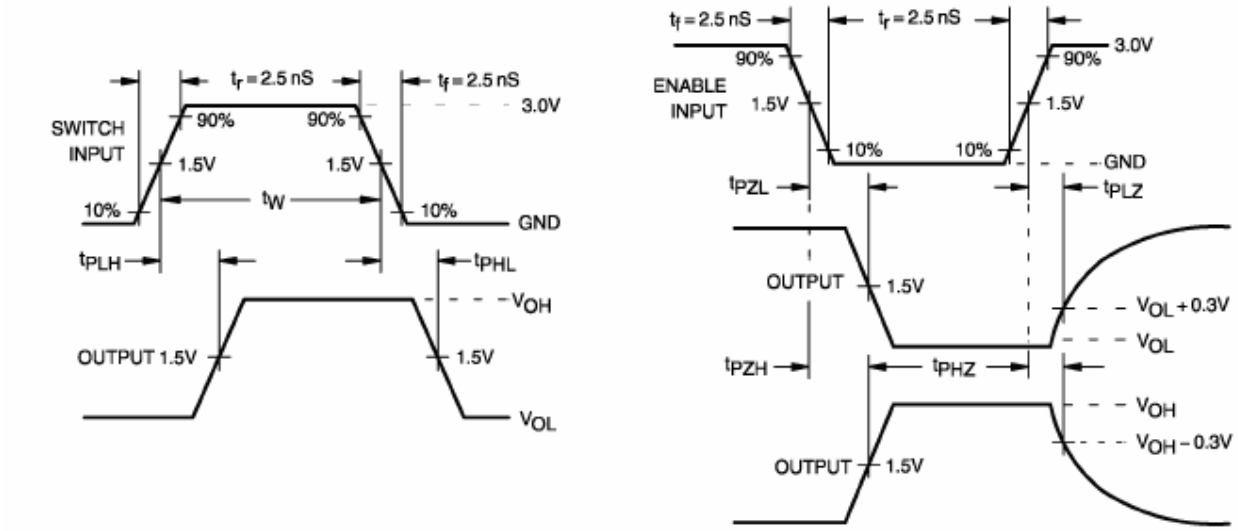


Figure 4. AC Waveforms

Physical Dimensions

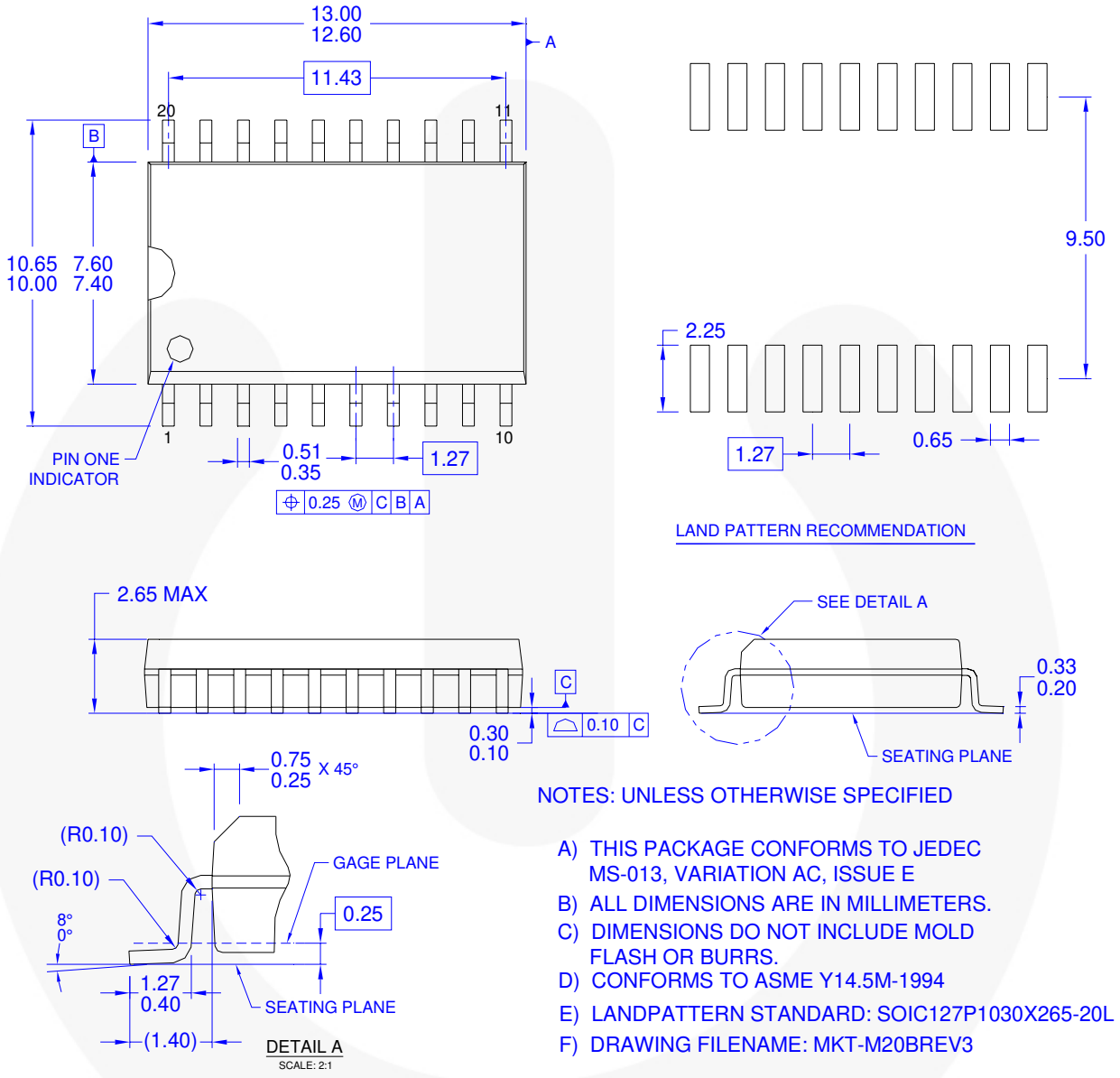


Figure 5. 20-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300-inch Wide

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Physical Dimensions

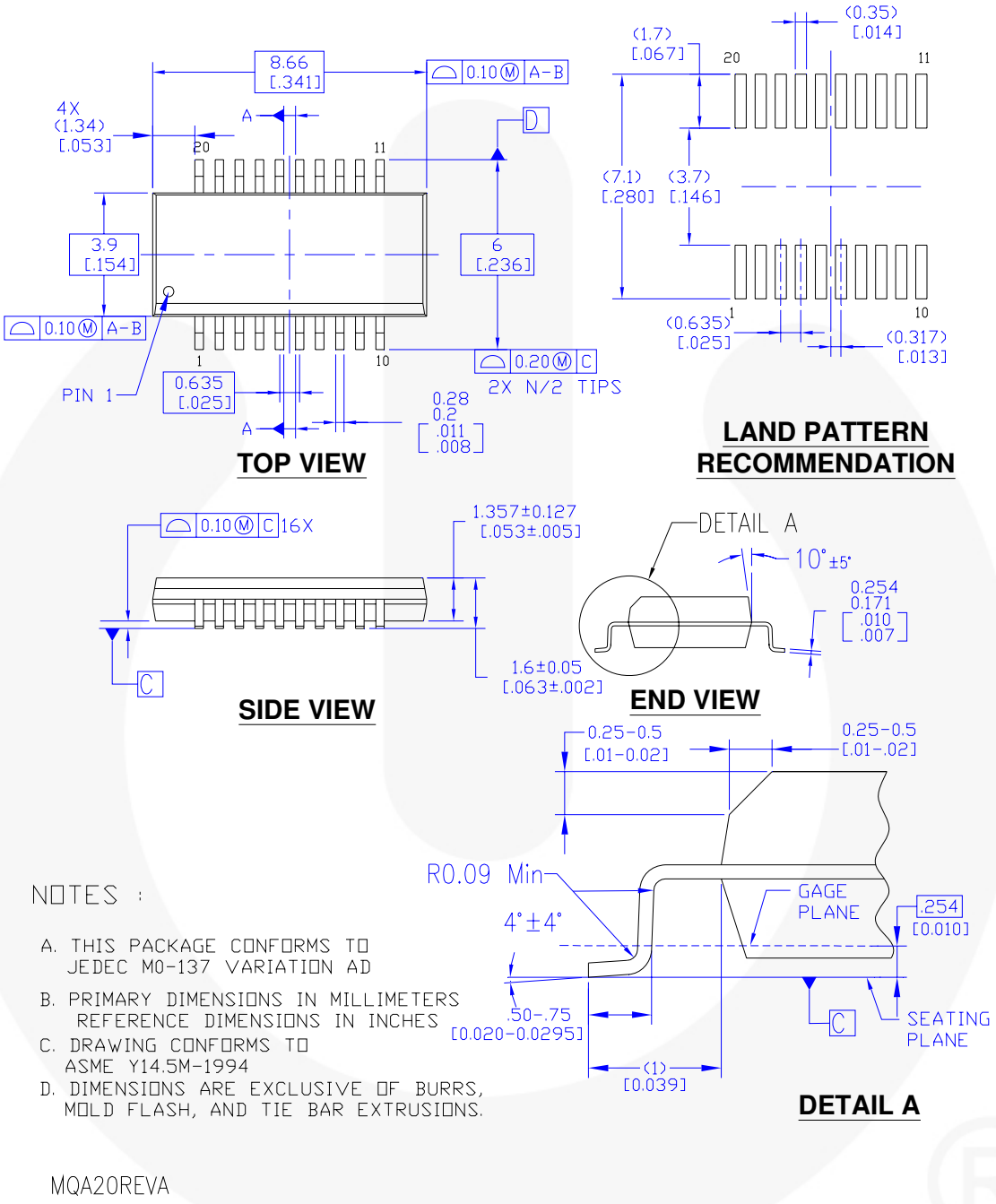

Figure 6. 20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide

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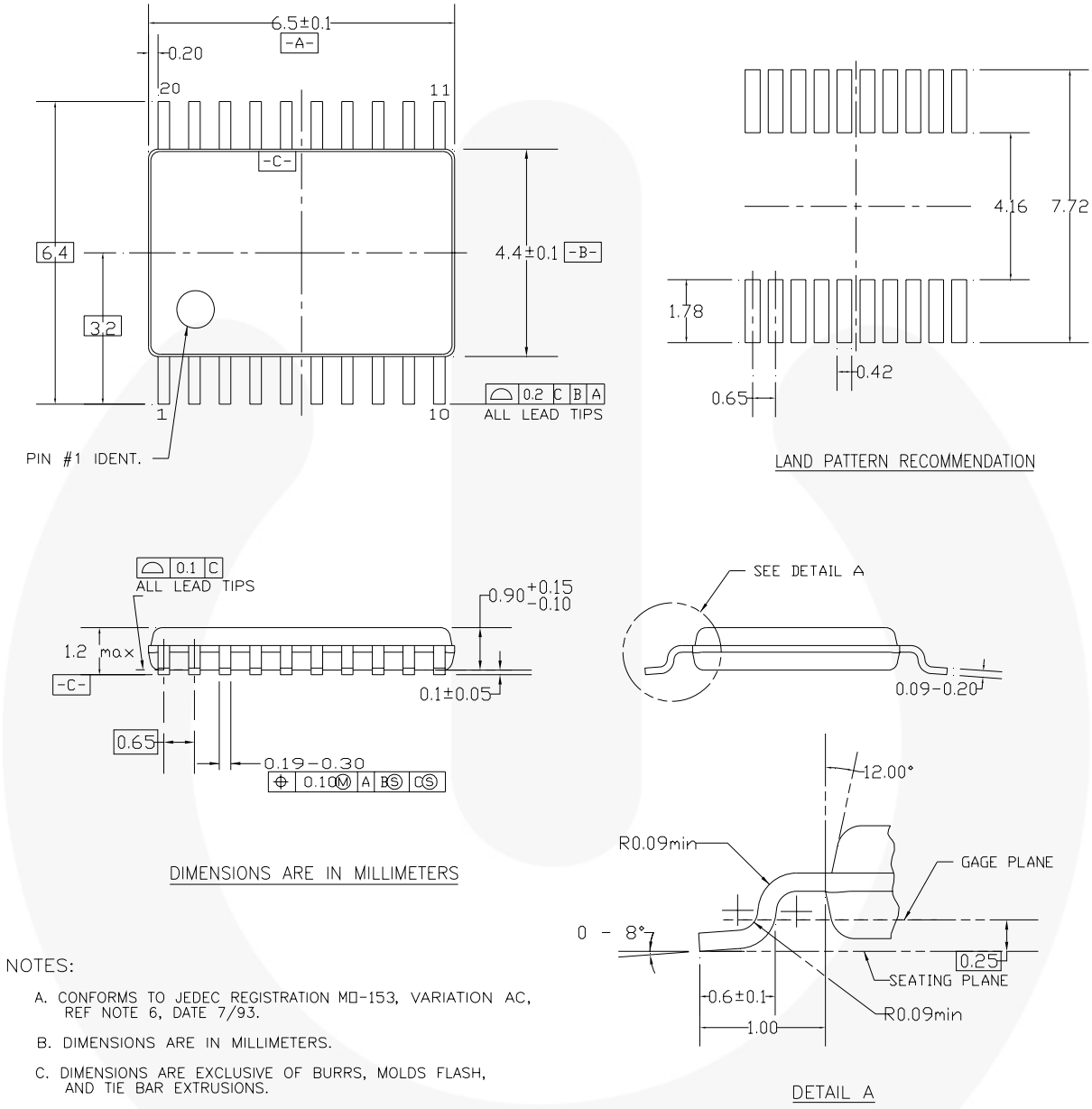
Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 7. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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