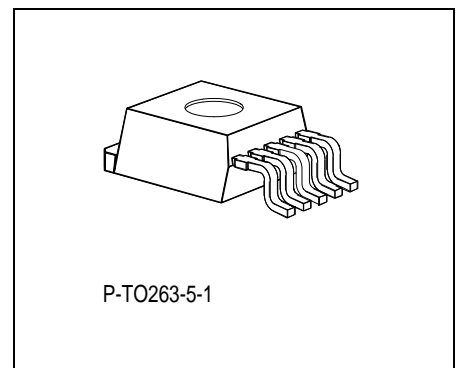
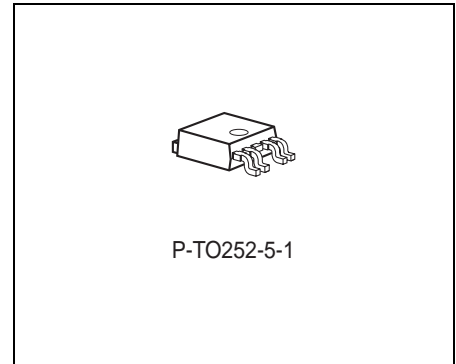


### Features

- Output voltage 5 V  $\pm$ 2%
- Ultra low current consumption: typ. 20  $\mu$ A
- 300 mA current capability
- Reset Feature
- Very low-drop voltage
- Short-circuit-proof
- Suitable for use in automotive electronics

### Functional Description

The TLE 7270 is a monolithic integrated low-drop voltage regulator which can supply loads up to 300 mA. An input voltage up to 42 V is regulated to  $V_{Q,nom} = 5.0$  V with a precision of  $\pm$ 2%. Due to its integrated reset circuitry featuring a 2-step adjustable power on timing and output voltage monitoring the IC is well suited as  $\mu$ -controller supply. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions. Of course the TLE 7270 can be used also in all other applications, where a stabilized 5 V voltage is required. Due to its ultra low current consumption the TLE 7270 is dedicated for use in applications permanently connected to  $V_{BAT}$ . An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage. For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7270. A mV-range output noise on the TLE 7270 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.



Type	Ordering Code	Package
TLE 7270 D	Q67006-A9670	P-TO252-5-1
TLE 7270 G	Q67006-A9726	P-TO263-5-1

### Reset

The Reset pin informs e.g. the microcontroller in case the output voltage has fallen below the lower threshold  $V_{RT}$  of typ. 4.65 V. The hysteresis is typically 100mV. Connecting the regulator to a battery voltage at first the reset signal remains LOW. When the output voltage has reached the reset threshold  $V_{RT}$  the reset output RO remains still LOW for the reset delay time  $t_{rd}$  adjustable in 2 steps via the DT Pin. Afterwards the reset output turns HIGH.

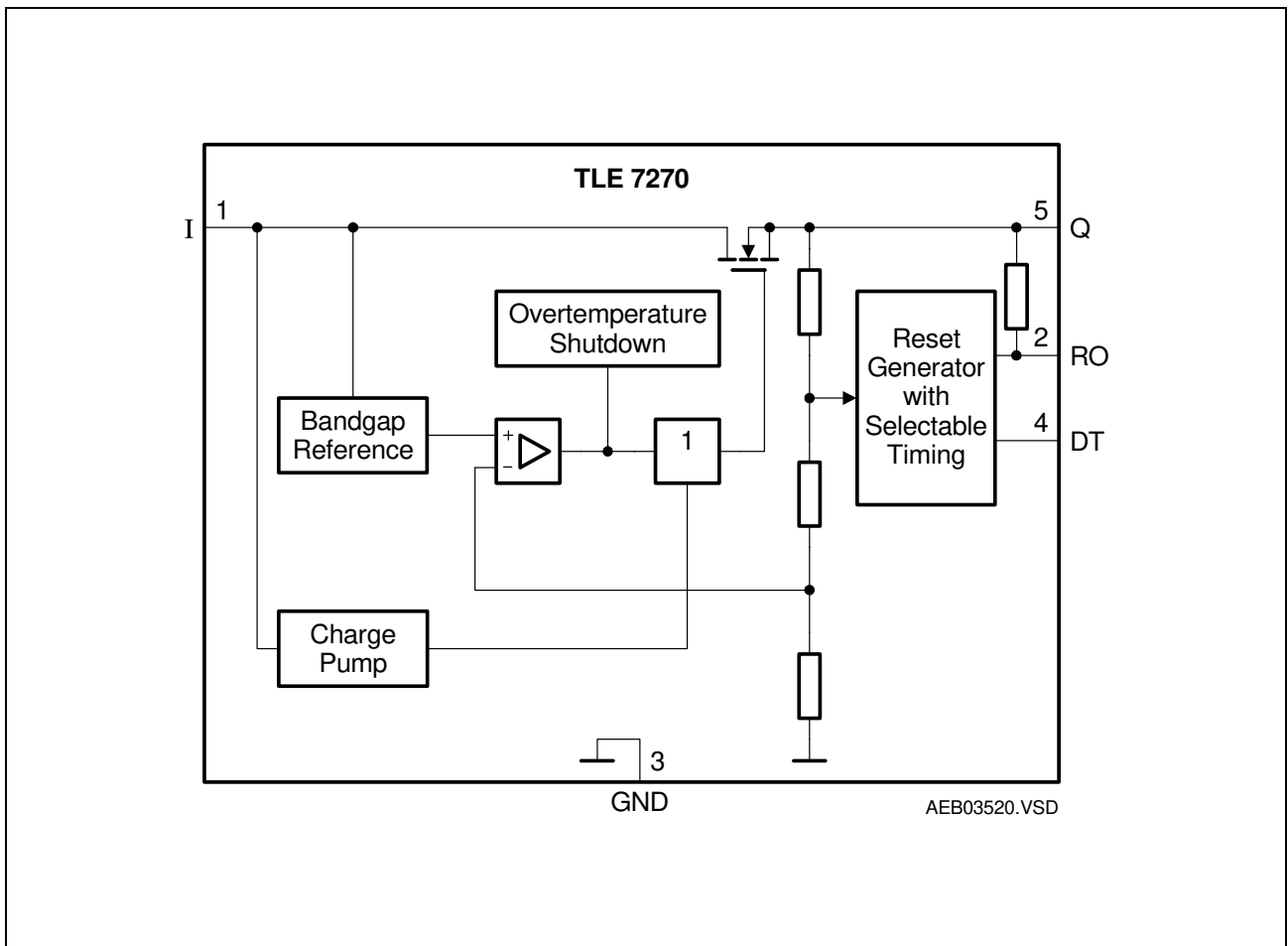
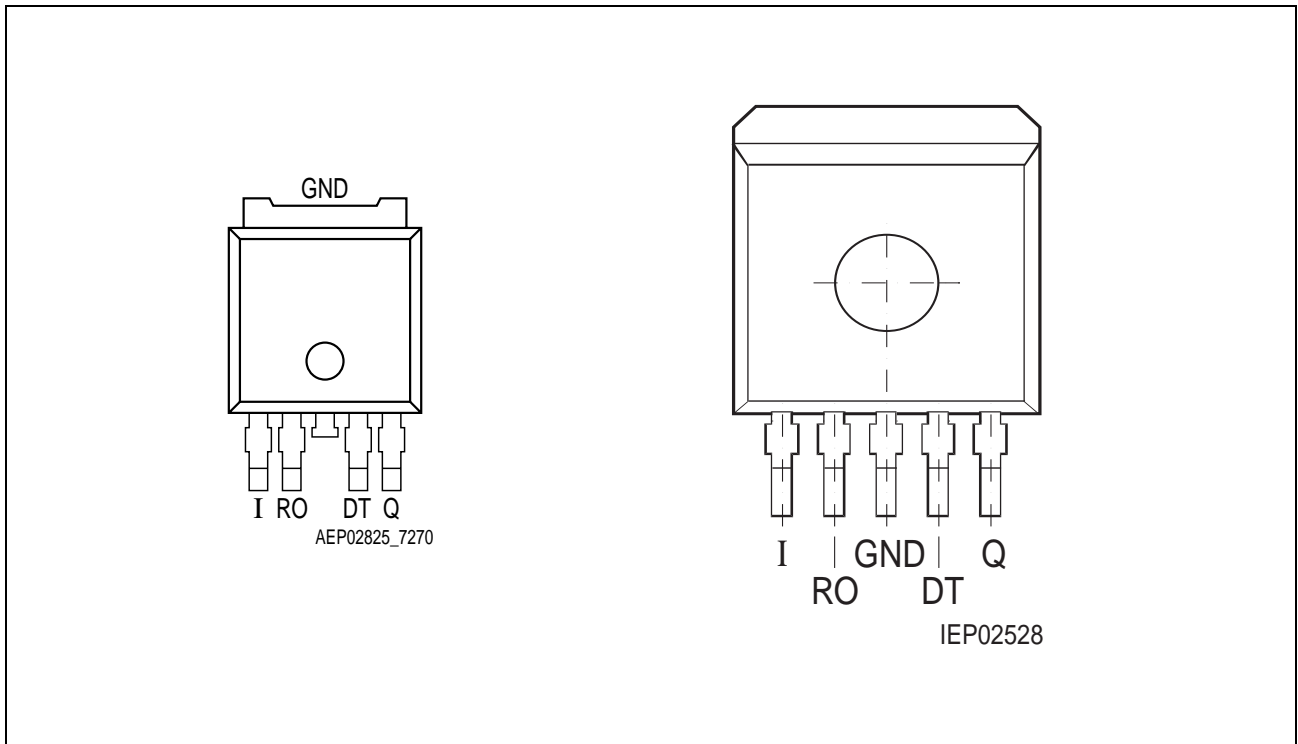


Figure 1 Block Diagram



**Figure 2** Pin Configuration P-TO252-5-1 (D-PAK), P-TO263-5-1 (D<sup>2</sup>-PAK) (top view)

**Table 1** Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	<b>Input</b> ; block to ground directly at the IC with a ceramic capacitor.
2	RO	<b>Reset Output</b> . Open Collector Output with integrated pull-up resistor of typically 30kΩ. Optional external pull-up resistor of $\geq 10 \text{ k}\Omega$ to pin Q.
3	GND	<b>Ground</b> ; Pin 3 internally connected to heatsink.
4	DT	<b>Delay Time</b> ; connect to Q or GND to choose reset delay time.
5	Q	<b>Output</b> ; block to ground with a ceramic capacitor, $C \geq 470 \text{ nF}$ .

**Table 2 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
<b>Input I</b>					
Voltage	$V_I$	-0.3	45	V	–
Current	$I_I$	-1	–	mA	–
<b>Output Q</b>					
Voltage	$V_Q$	-0.3	5.5	V	–
Voltage	$V_Q$	-0.3	6.2	V	$t < 10 \text{ s}^1$ )
Current	$I_Q$	-1	–	mA	–
<b>Reset Output RO</b>					
Voltage	$V_{RO}$	-0.3	5.5	V	–
Voltage	$V_{RO}$	-0.3	6.2	V	$t < 10 \text{ s}^1$ )
Current	$I_{RO}$	-1	1	mA	–
<b>Delay Time DT</b>					
Voltage	$V_{DT}$	-0.3	5.5	V	–
Voltage	$V_{DT}$	-0.3	6.2	V	$t < 10 \text{ s}^1$ )
Current	$I_{DT}$	-1	1	mA	–
<b>Temperature</b>					
Junction temperature	$T_j$	-40	150	°C	–
Storage temperature	$T_{stg}$	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods ( $t > 10 \text{ s}$ ) may affect device reliability.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Table 3 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	$V_I$	5.5	42	V	–
Junction temperature	$T_j$	-40	150	°C	–

*Note: In the operating range, the functions given in the circuit description are fulfilled.*

**Table 4 Thermal Resistance**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Junction case	$R_{thj-c}$	–	8	K/W	–
Junction ambient	$R_{thj-a}$	–	80	K/W	TO252 <sup>1)</sup>
Junction ambient	$R_{thj-a}$	–	55	K/W	TO263 <sup>2)</sup>

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm<sup>3</sup>, heat sink area 300 mm<sup>2</sup>

2) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm<sup>3</sup>, heat sink area 300 mm<sup>2</sup>

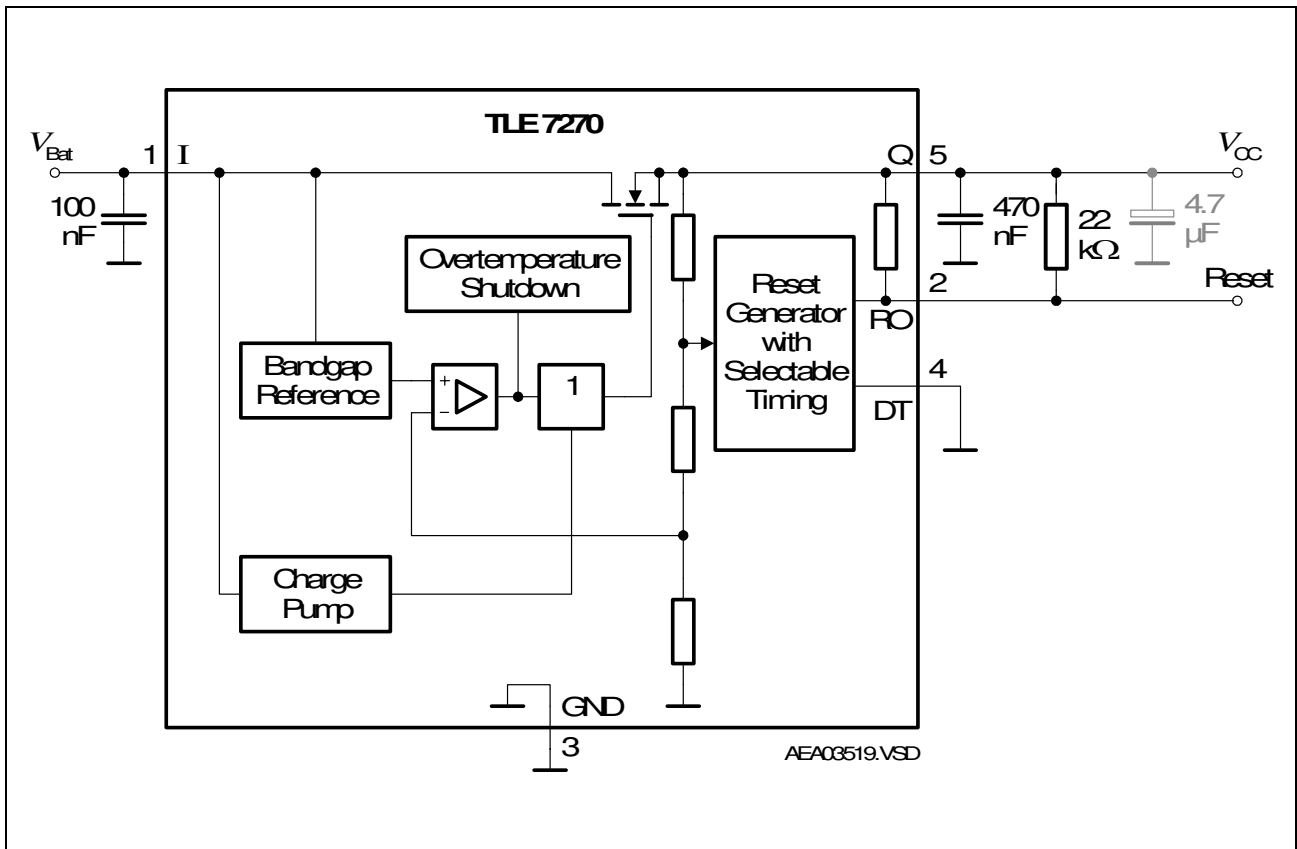
**Table 5 Electrical Characteristics**
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
<b>Output Q</b>						
Output voltage	$V_Q$	4.9	5.0	5.1	V	$0.1 \text{ mA} < I_Q < 300 \text{ mA};$ $6 \text{ V} < V_I < 16 \text{ V}$
Output voltage	$V_Q$	4.9	5.0	5.1	V	$0.1 \text{ mA} < I_Q < 100 \text{ mA};$ $6 \text{ V} < V_I < 40 \text{ V}$
Output current limitation	$I_Q$	320	–	–	mA	1)
Output current limitation	$I_Q$			800	mA	$V_Q = 0\text{V}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	20	30	$\mu\text{A}$	$I_Q = 0.1 \text{ mA};$ $T_j = 25 \text{ }^\circ\text{C}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	–	40	$\mu\text{A}$	$I_Q = 0.1 \text{ mA};$ $T_j \leq 80 \text{ }^\circ\text{C}$
Drop voltage	$V_{\text{dr}}$	–	200	500	mV	$I_Q = 200 \text{ mA}$ $V_{\text{dr}} = V_I - V_Q$ 1)
Load regulation	$\Delta V_{Q, \text{lo}}$	– 40	15	40	mV	$I_Q = 5 \text{ mA to } 250 \text{ mA}$
Line regulation	$\Delta V_{Q, \text{li}}$	– 20	5	20	mV	$V_I = 10 \text{ V to } 32 \text{ V};$ $I_Q = 5 \text{ mA}$
Power supply ripple rejection	$PSRR$	–	60	–	dB	$f_r = 100 \text{ Hz};$ $V_r = 0.5 \text{ Vpp}$
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–
Output Capacitor	$C_Q$	470	–	–	nF	$\text{ESR} < 3 \Omega$
<b>Reset Output RO</b>						
Reset switching threshold	$V_{\text{RT}}$	4.50	4.65	4.80	V	$V_Q$ decreasing $V_i = 6\text{V}$
Reset Head Room	$V_{\text{RH}}$	–	350	–	mV	
Reset output low voltage	$V_{\text{ROL}}$	–	0.2	0.4	V	$R_{\text{RO}} = 10 \text{ k}\Omega;$ $V_Q > 1 \text{ V}$
Internal reset pull up resistor	$R_{\text{R,int}}$	15	30	45	$\text{k}\Omega$	
External reset pull up resistor	$R_{\text{R,ext}}$	10		$\infty^2)$	$\text{k}\Omega$	see Fig. 3

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Reset delay time	$t_{rd}$	10	16	22	ms	DT connected to GND
Reset delay time	$t_{rd}$	80	128	176	ms	DT connected to Q
Reset reaction time	$t_{rr}$	–	–	12	$\mu$ s	–

- 1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5$  V.
- 2) An external reset pull up resistor is not required.

### Application Information



**Figure 3 Application Diagram**

#### Input, Output

An input capacitor is necessary for damping line influences. A resistor of approx. 1 Ω in series with  $C_i$ , can damp the LC of the input inductivity and the input capacitor.

The TLE 7270 requires a ceramic output capacitor of at least 470 nF to assure stability of the regulation loop. In order to damp influences resulting from load current surges it is recommended to add an additional electrolytic capacitor of 4.7 μF to 47 μF at the output as shown in **Figure 3**.



Additionally a buffer capacitor  $C_B$  of  $> 10\mu\text{F}$  should be used for the output to suppress influences from load surges to the voltage levels. This one can either be an aluminum electrolytic capacitor or a tantalum capacitor following the application requirements.

A general recommendation is to keep the drop over the equivalent serial resistor (ESR) together with the discharge of the blocking capacitor below the Reset Headroom (e.g. typ.  $V_{RH} = 350\text{mV}$ ).

Since the regulator output current roughly rises linearly with time the discharge of the capacitor can be calculated as follows:

$$dV_{C_B} = dI_Q \cdot dt / C_B$$

The drop across the ESR calculates as:

$$dV_{ESR} = dI \cdot ESR$$

To prevent a reset the following relationship must be fulfilled:

$$dV_C + dV_{ESR} < V_{RH} = 350\text{mV}$$

Example: Assuming a load current change of  $dI_Q = 100\text{mA}$ , a blocking capacitor of  $C_Q = 22\mu\text{F}$  and a typical regulator reaction time under normal operating conditions of  $dt \sim 25\mu\text{s}$  and for special dynamic load conditions, such as load step from very low base load, a reaction time of  $dt \sim 75\mu\text{s}$ .

$$dV_C = dI_Q \cdot dt / C_B = 100\text{mA} \cdot 25\mu\text{s} / 22\mu\text{F} = 113\text{mV}$$

So for the ESR we can allow

$$dV_{ESR} = V_{RH2} - dV_C = 350\text{mV} - 113\text{mV} = 236\text{mV}$$

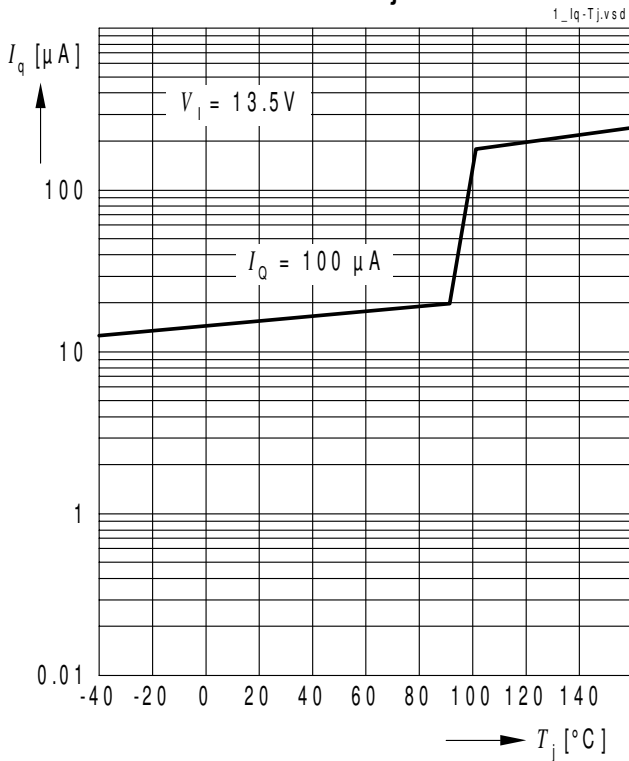
The permissible ESR becomes:

$$ESR = dV_{ESR} / dI_Q = 236\text{mV} / 100\text{mA} = 2.36\Omega$$

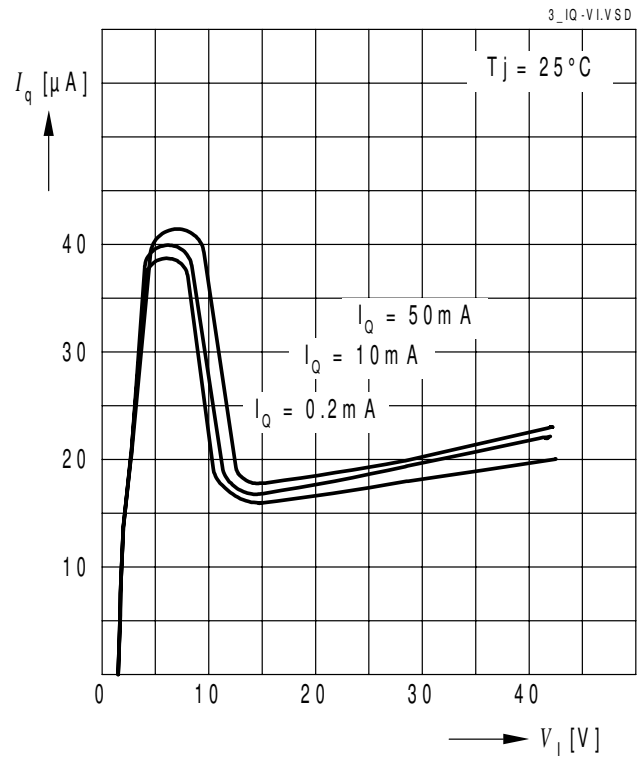
During design-in of the TLE7469 product family, special care needs to be taken with regards to the regulators reaction time to sudden load current changes starting from very low pre-load as well as cyclic load changes. The application note "*TLE7x Voltage Regulators - Application Note about Transient Response at ultra low quiescent current Voltage Regulators*" (see 3\_cip05405.pdf) gives important hints for successful design-in of the Voltage Regulators of the TLE7x family.

### Typical Performance Characteristics

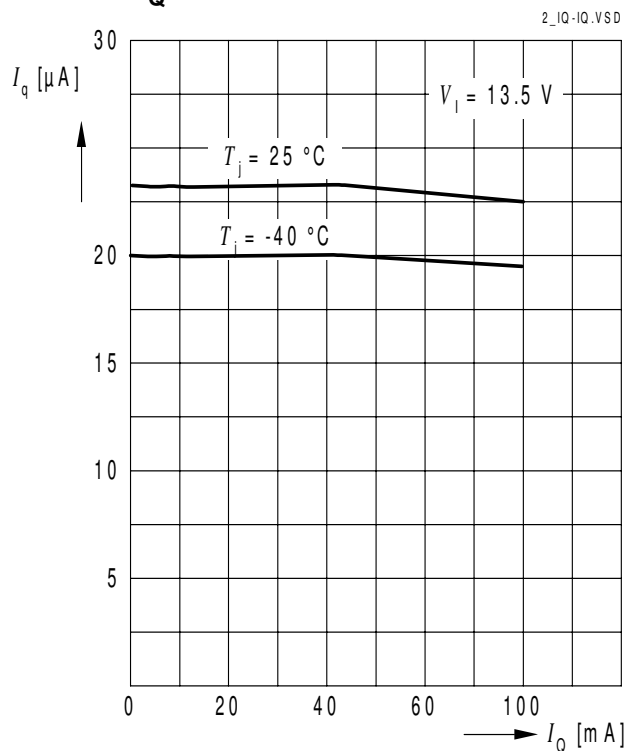
**Current Consumption  $I_q$  versus Junction Temperature  $T_j$**



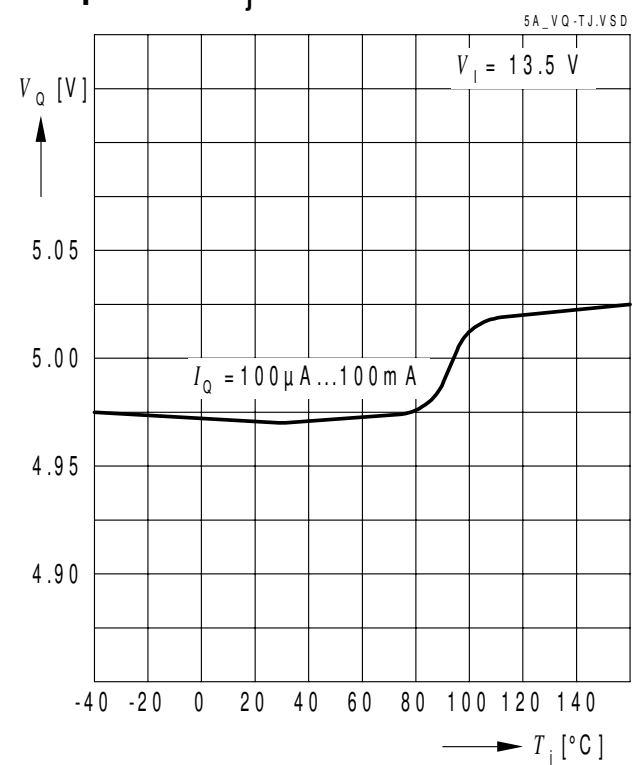
**Current Consumption  $I_q$  versus Input Voltage  $V_i$**



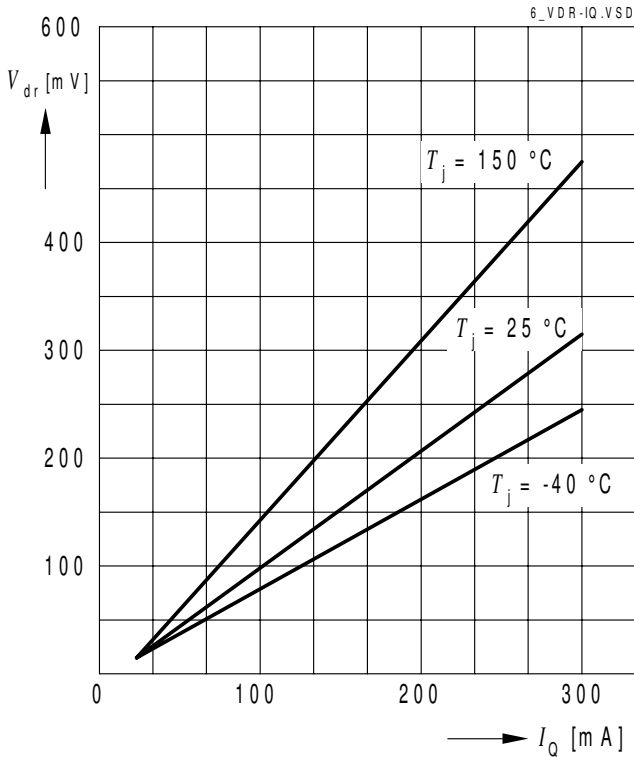
**Current Consumption  $I_q$  versus Output Current  $I_Q$**



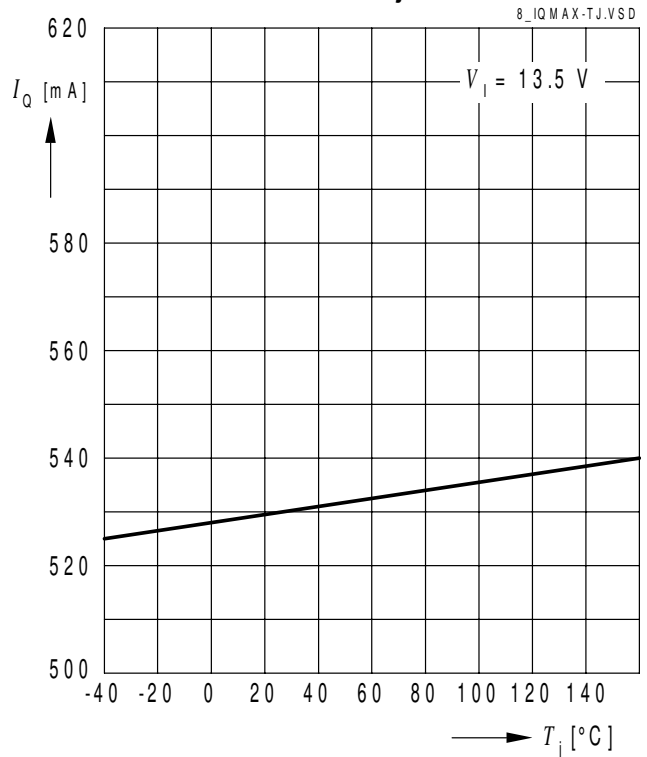
**Output Voltage  $V_Q$  versus Junction Temperature  $T_j$**



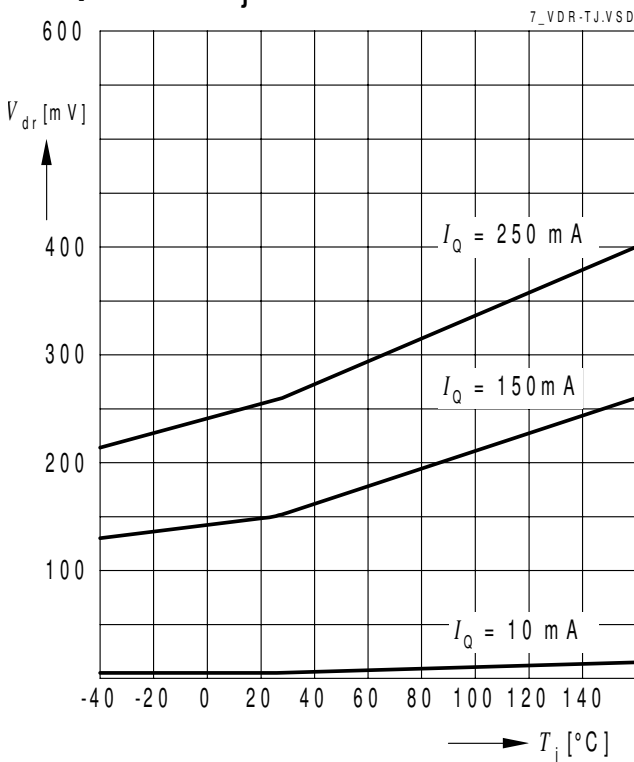
**Dropout Voltage  $V_{dr}$  versus Output Current  $I_Q$**



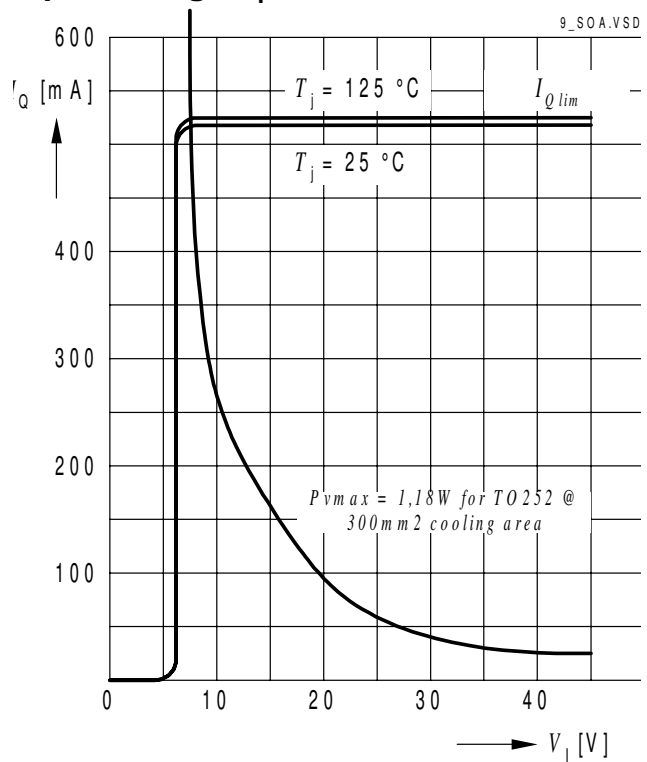
**Maximum Output Current  $I_Q$  versus Junction Temperature  $T_j$**



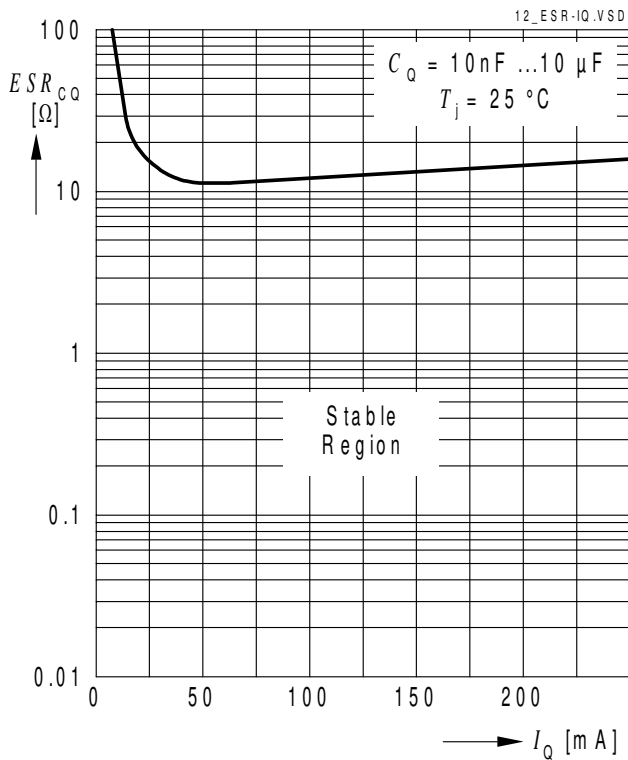
**Dropout Voltage  $V_{dr}$  versus Junction Temperature  $T_j$**



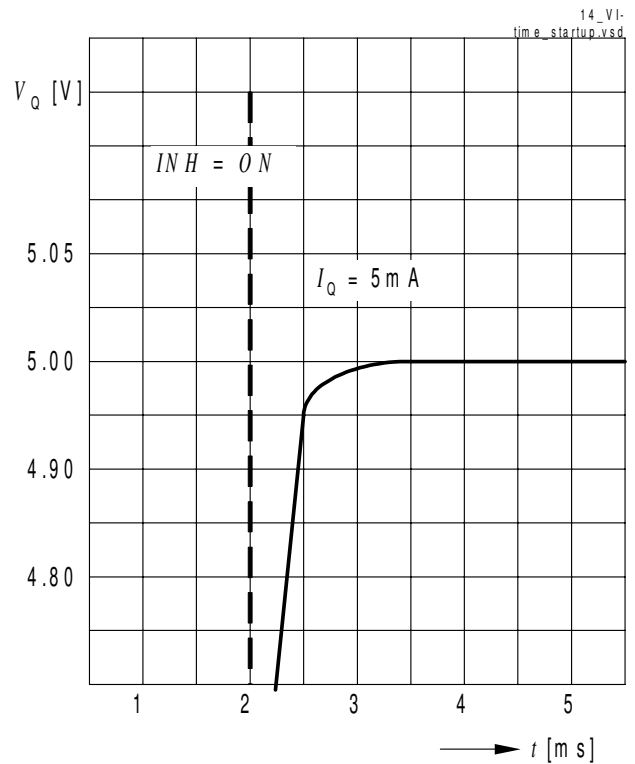
**Maximum Output Current  $I_Q$  versus Input Voltage  $V_I$**



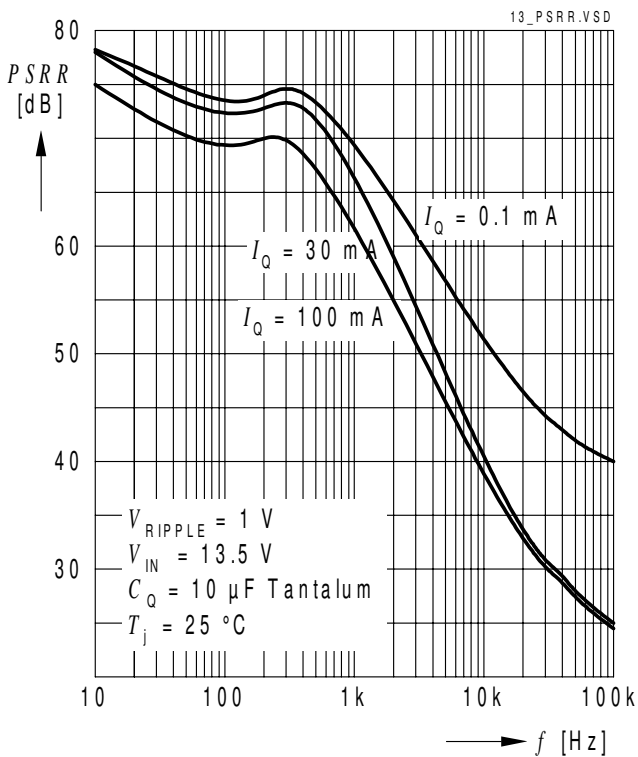
### Region of Stability



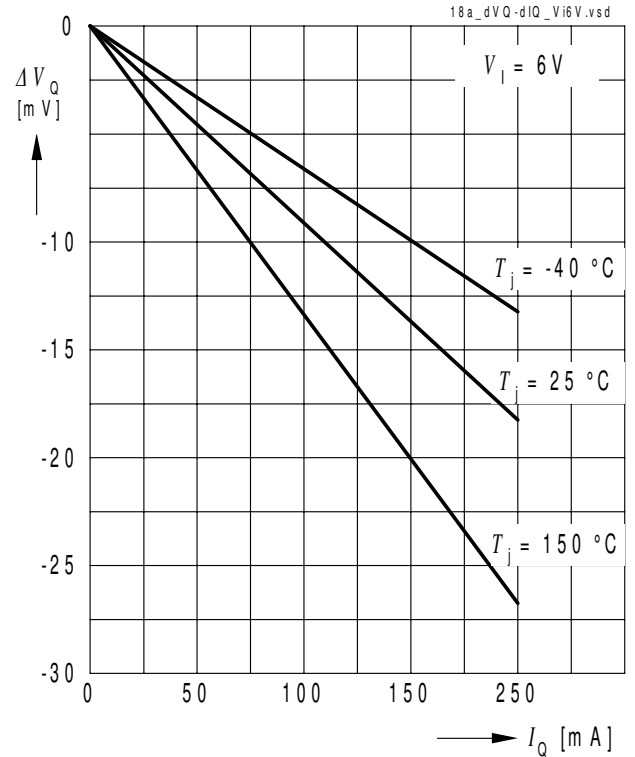
### Output Voltage $V_Q$ Start-up behaviour



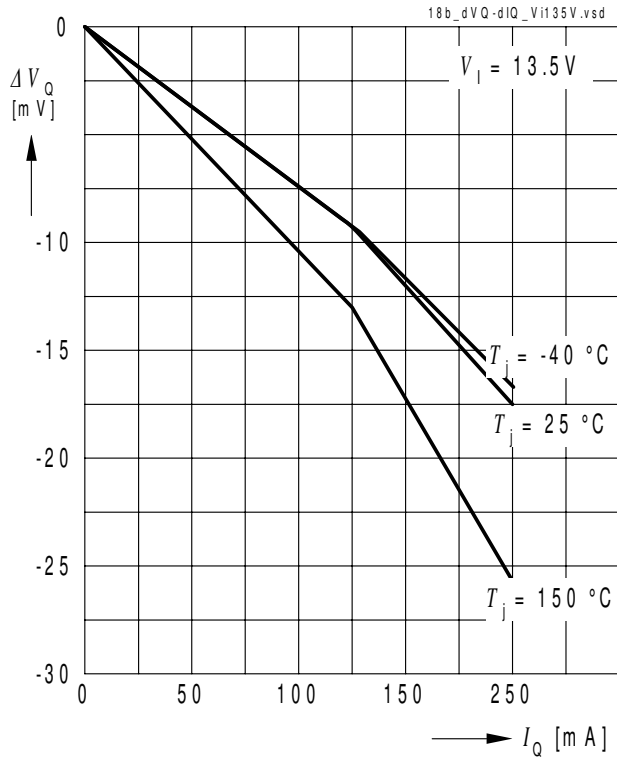
### Power Supply Ripple Rejection PSRR versus Frequency $f$



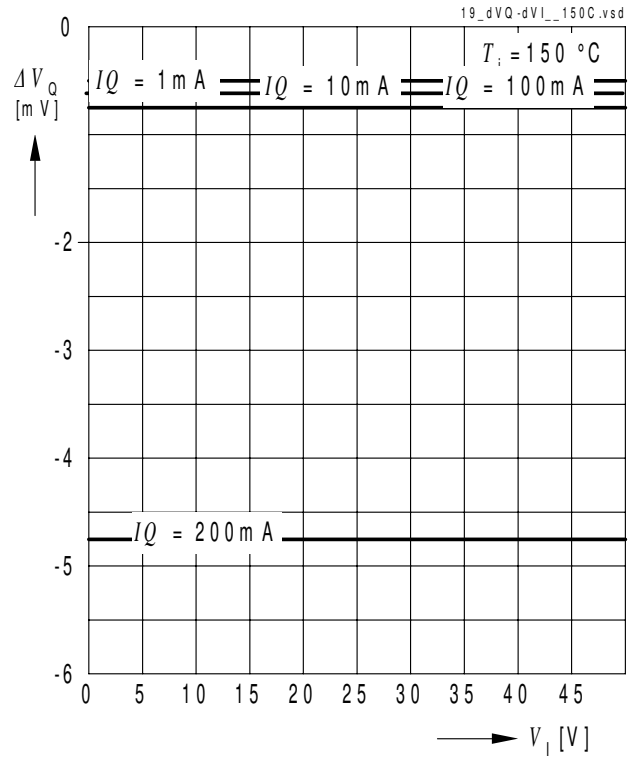
### Load Regulation $dV_Q$ versus Output Current Change $dI_Q$



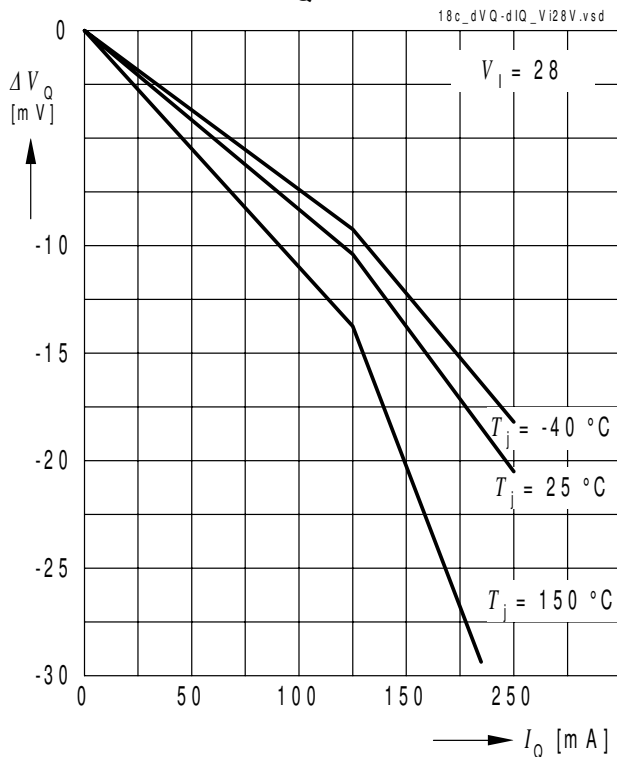
**Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$**



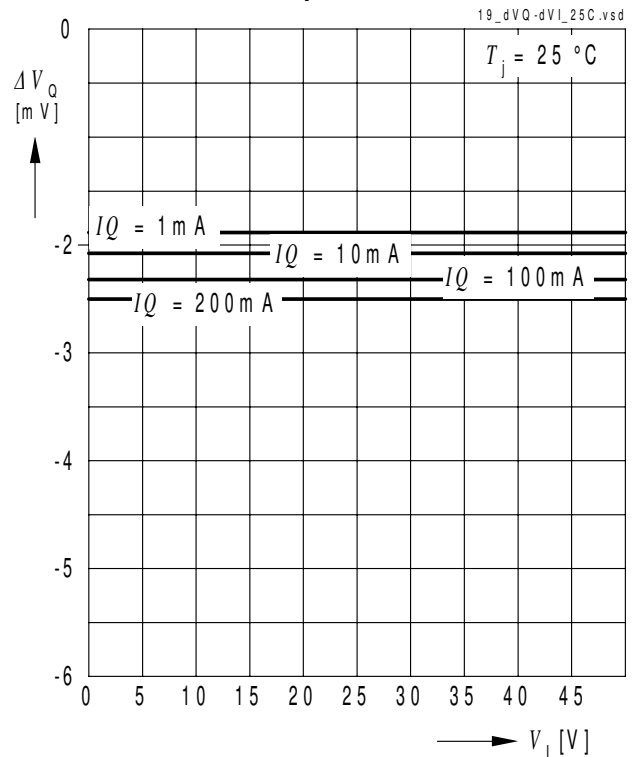
**Line Regulation  $dV_Q$  versus Input Voltage Changed  $V_I$**



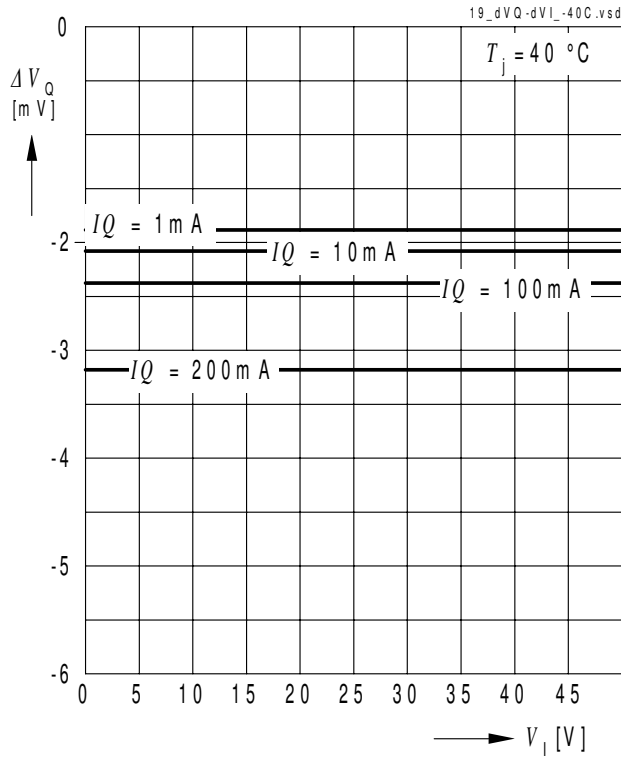
**Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$**



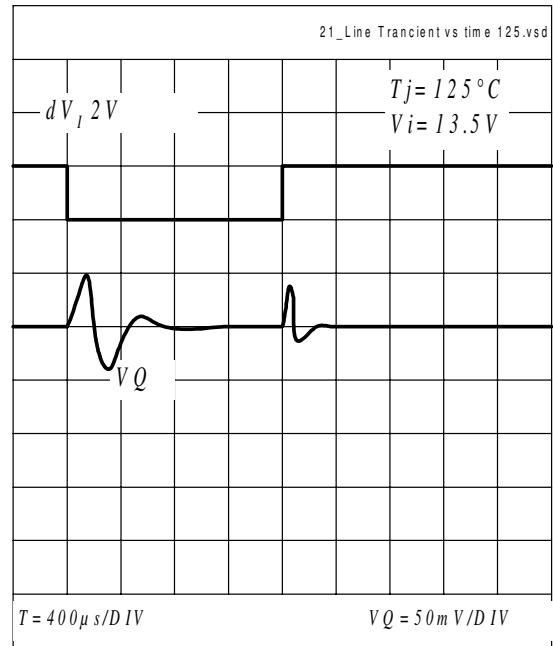
**Line Regulation  $dV_Q$  versus Input Voltage Changed  $V_I$**



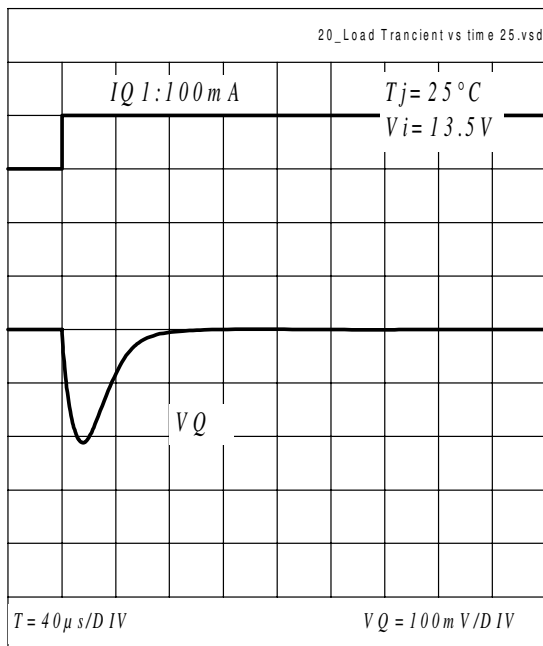
**Line Regulation  $dV_Q$  versus Input Voltage Changed  $V_i$**



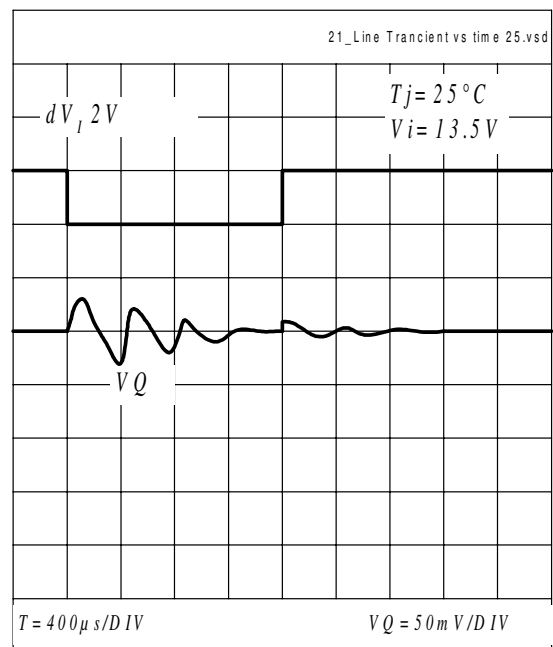
**Load Transient Response Peak Voltage  $dV_Q$**



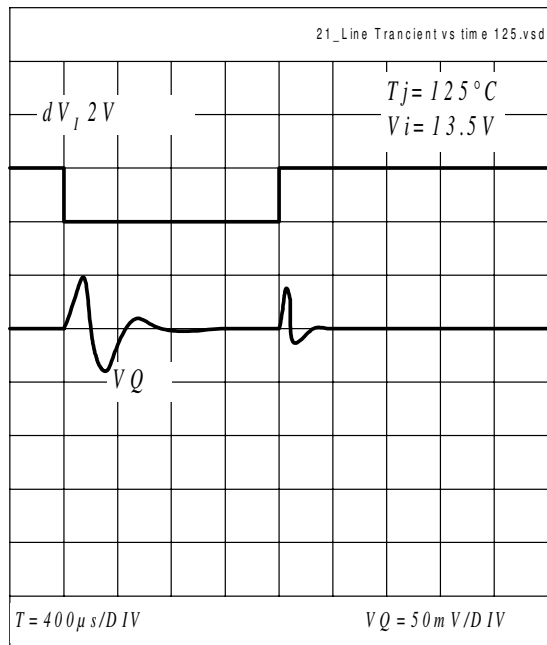
**Load Transient Response Peak Voltage  $dV_Q$**



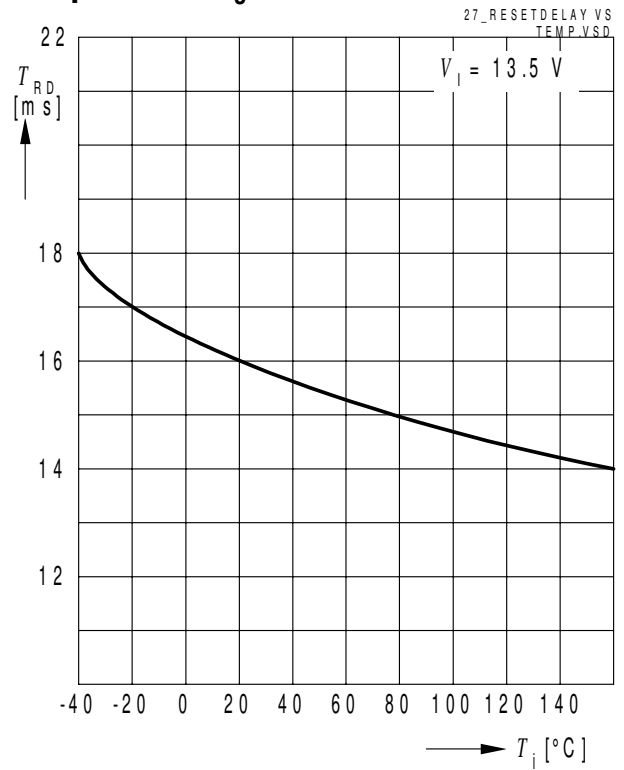
**Line Transient Response Peak Voltage  $dV_Q$**



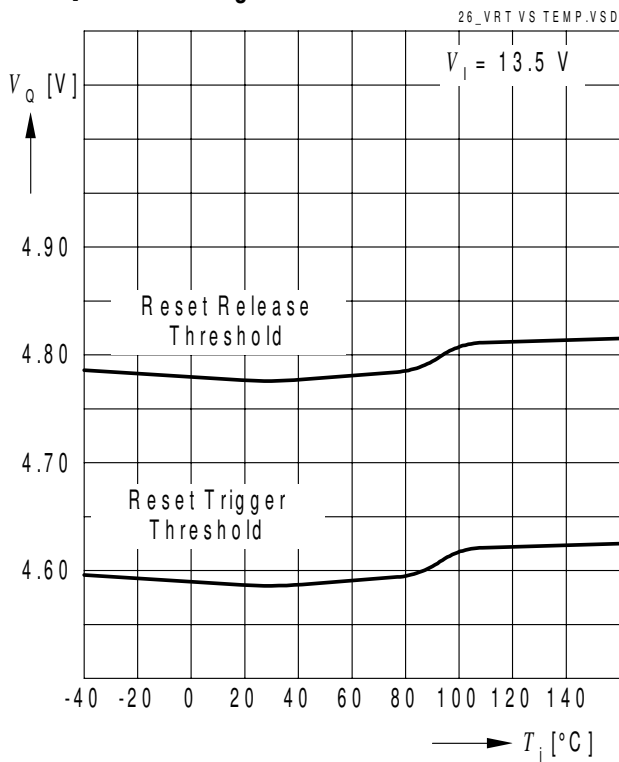
### Line Transient Response Peak Voltage $dV_Q$



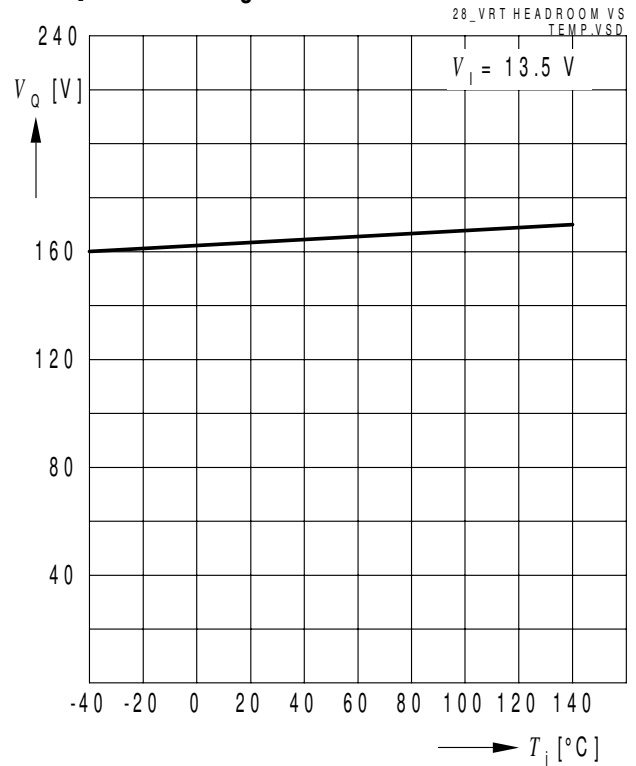
### Reset Delay $T_{RD}$ Time versus Junction Temperature $T_j$



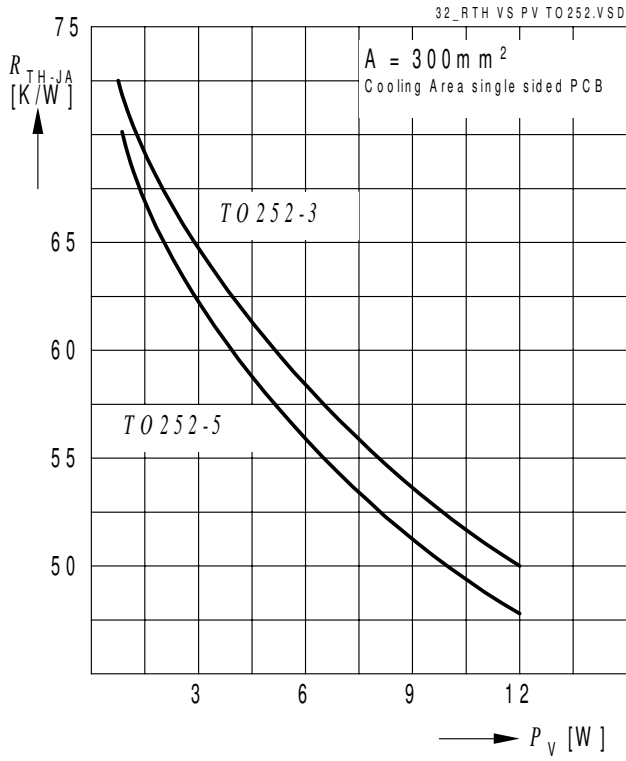
### Reset Threshold $V_{RT}$ versus Junction Temperature $T_j$



### Reset Headroom versus Junction Temperature $T_j$



### Thermal Resistance Junction-Ambient $R_{THJA}$ versus Power Dissipation $P_V$





Package Outlines

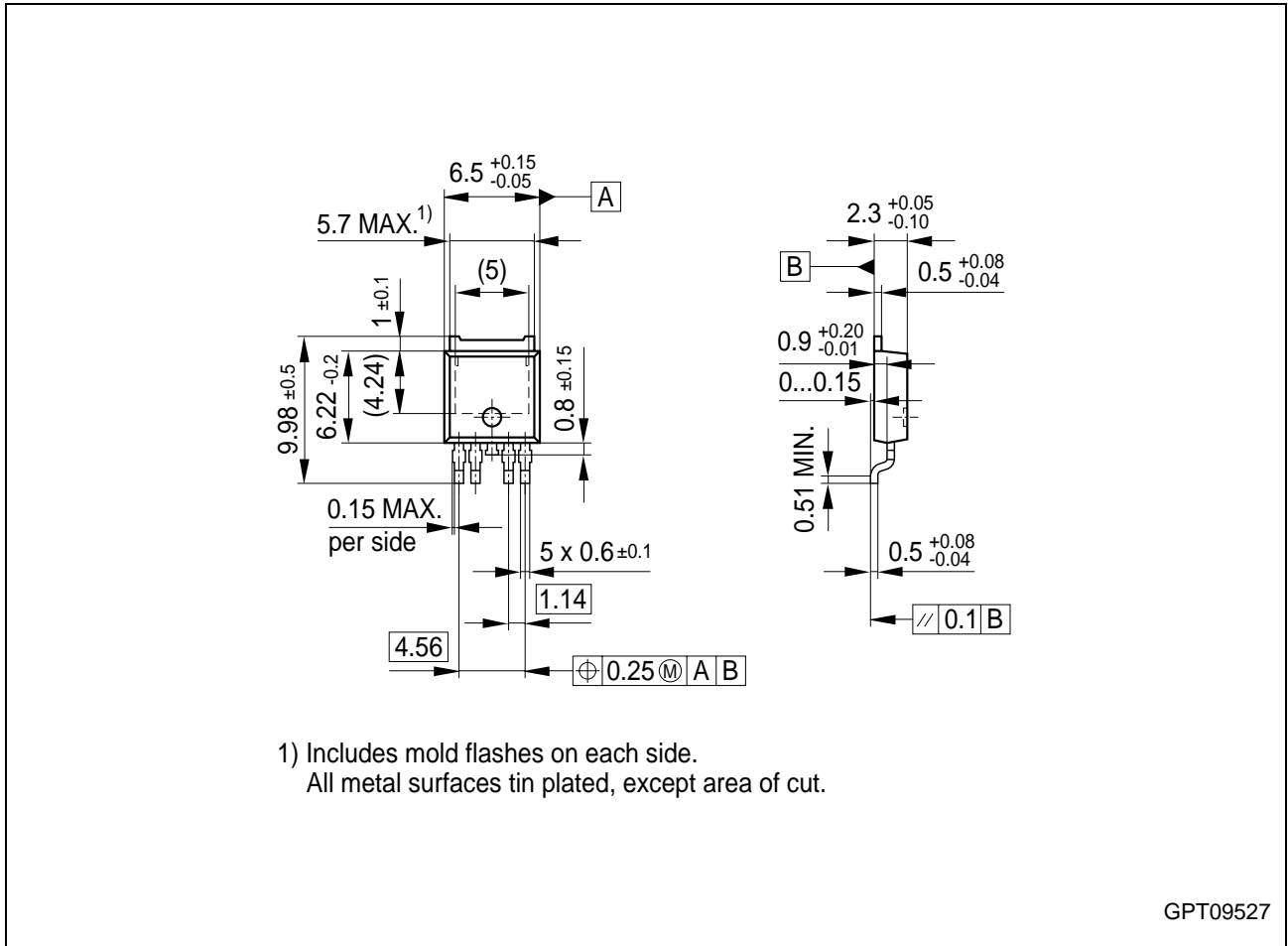
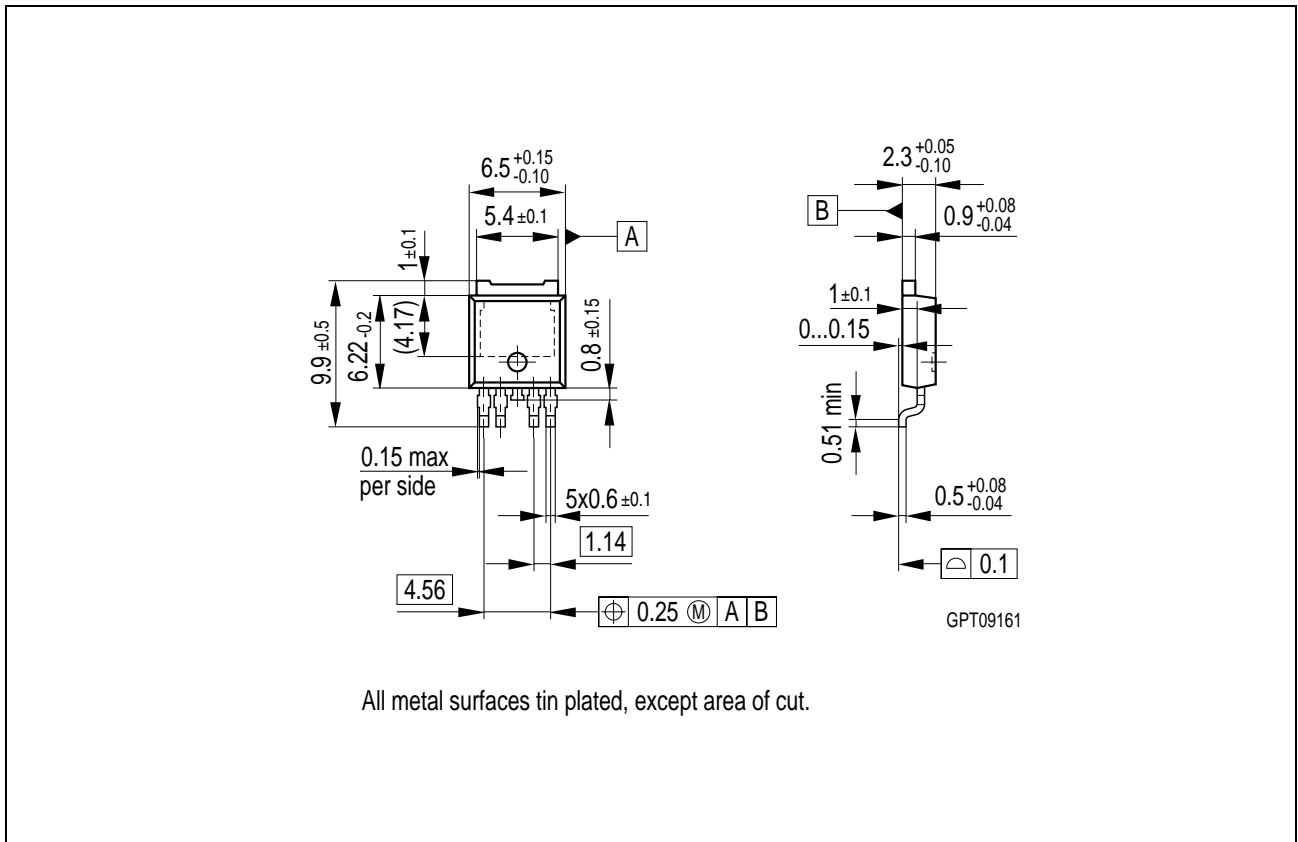
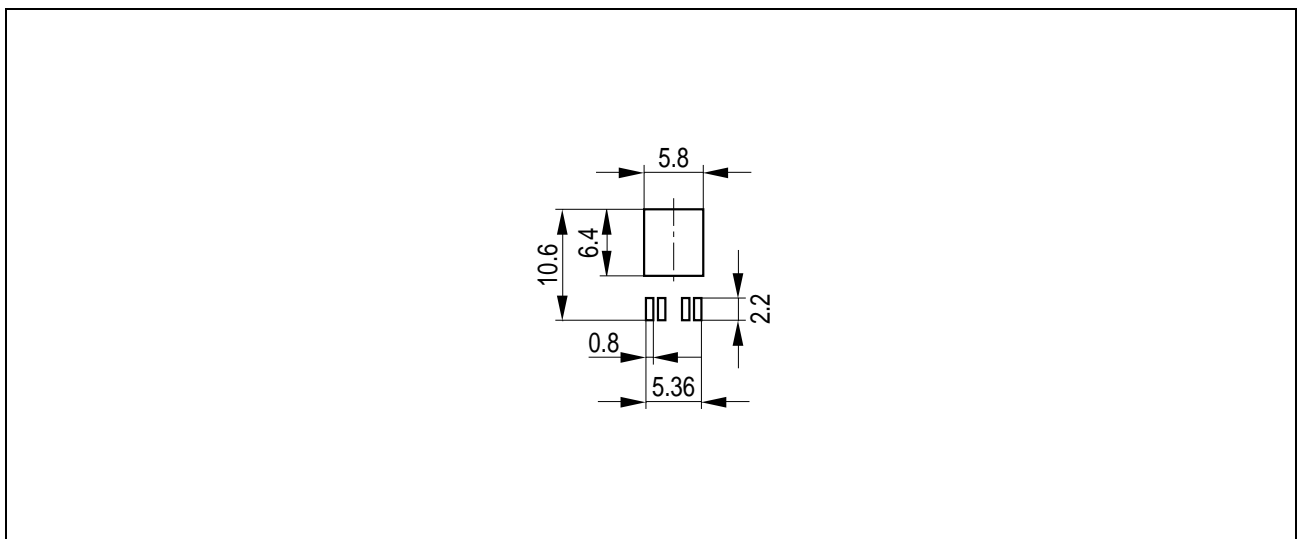


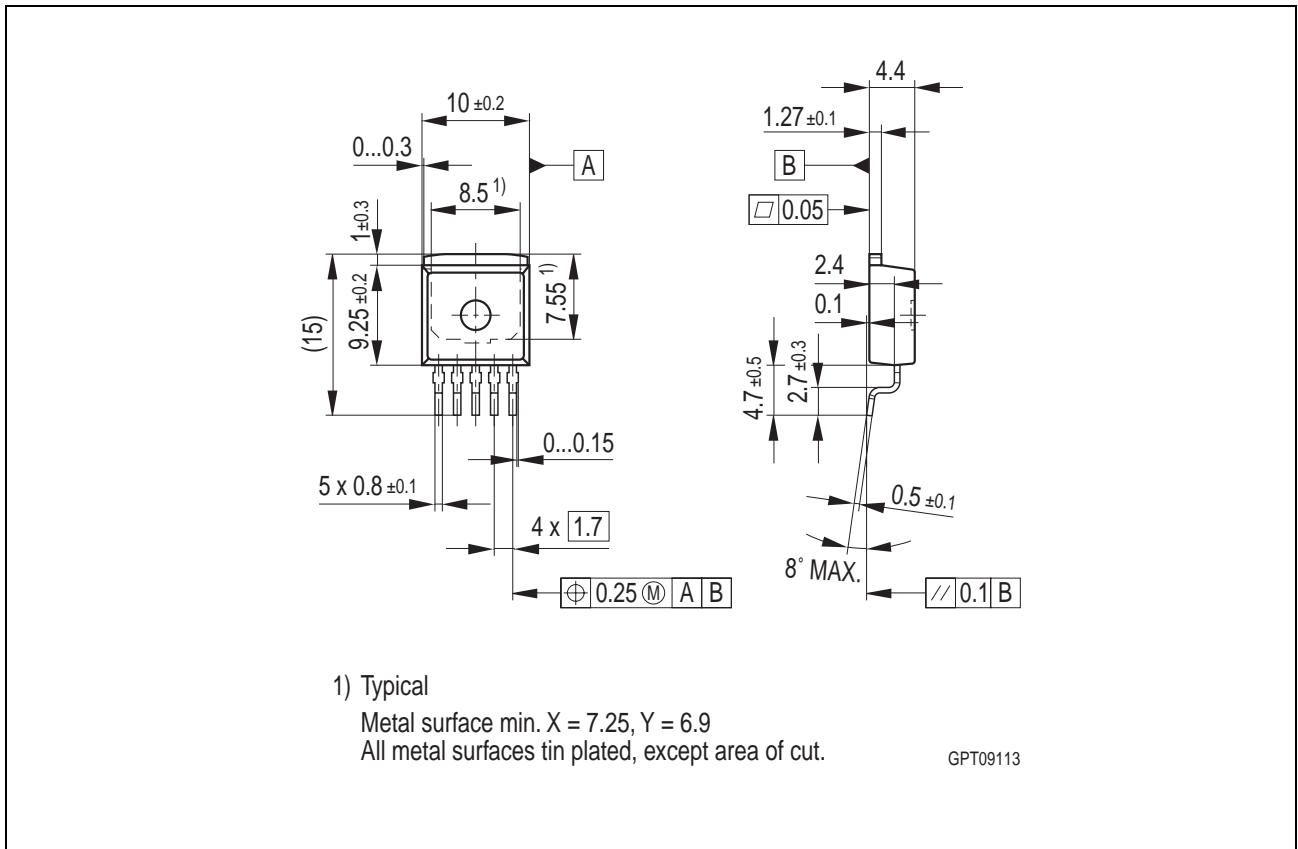
Figure 4 P-TO252-5-11 (Plastic Transistor Single Outline)



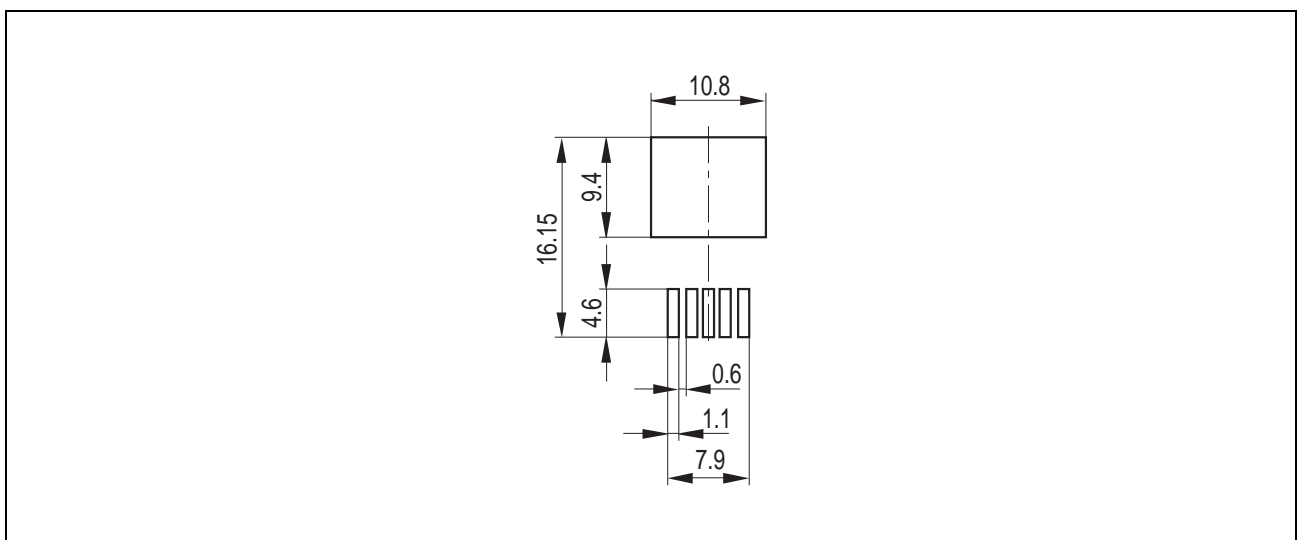
**Figure 5** P-TO252-5-1 (Plastic Transistor Single Outline)



**Figure 6** Foot Print for P-TO-252-5-1 and P-TO-252-5-11 (Plastic Transistor Single Outline)



**Figure 7** P-TO263-5-1 (Plastic Transistor Single Outline)



**Figure 8** Foot Print for P-TO263-5-1 (Plastic Transistor Single Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

**Remarks**

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