

## Precision Differential 3.3V Low-Skew LVPECL 1:4 Fanout Buffer

### Features

- Provides Four Differential 3.3V LVPECL Copies
- Selects between Differential CLK, /CLK, or LVPECL Clock Inputs
- CLK, /CLK Pair Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL Input Levels
- PCLK, /PCLK Pair Accepts LVPECL, CML, SSTL Input Levels
- Guaranteed AC Performance over Temperature and Supply Voltage:
  - 650 MHz Maximum Output Frequency
  - <1.4 ns Propagation Delay (In-to-Q)
  - <30 ps Output Skew
  - <150 ps Part-to-Part Skew
  - Additive Phase Jitter, RMS: 145 fs (Typical)
- 3.3V  $\pm$ 5% Supply Voltage
- 0°C to +70°C Operating Temperature Range
- Available in a 20-Lead TSSOP Package

### Applications

- SONET Clock Distribution
- Backplane Distribution

### Markets

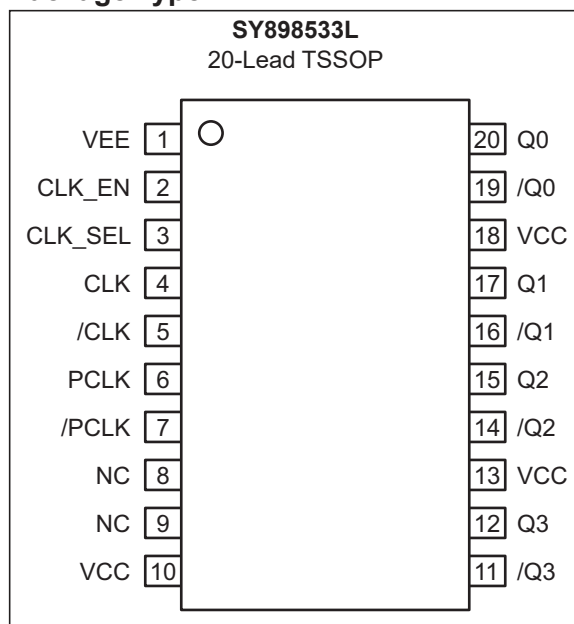
- LAN/WAN
- Enterprise Servers
- ATE
- Test and Measurement

### General Description

The SY898533L is a 3.3V, low-skew, 1:4 LVPECL fanout buffer with two selectable clock input pairs. Most standard differential input levels can be applied to the CLK, /CLK pair while LVPECL, CML, or SSTL input levels can be applied to the PCLK, /PCLK pair. To eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin, the clock enable is synchronized with the input signal.

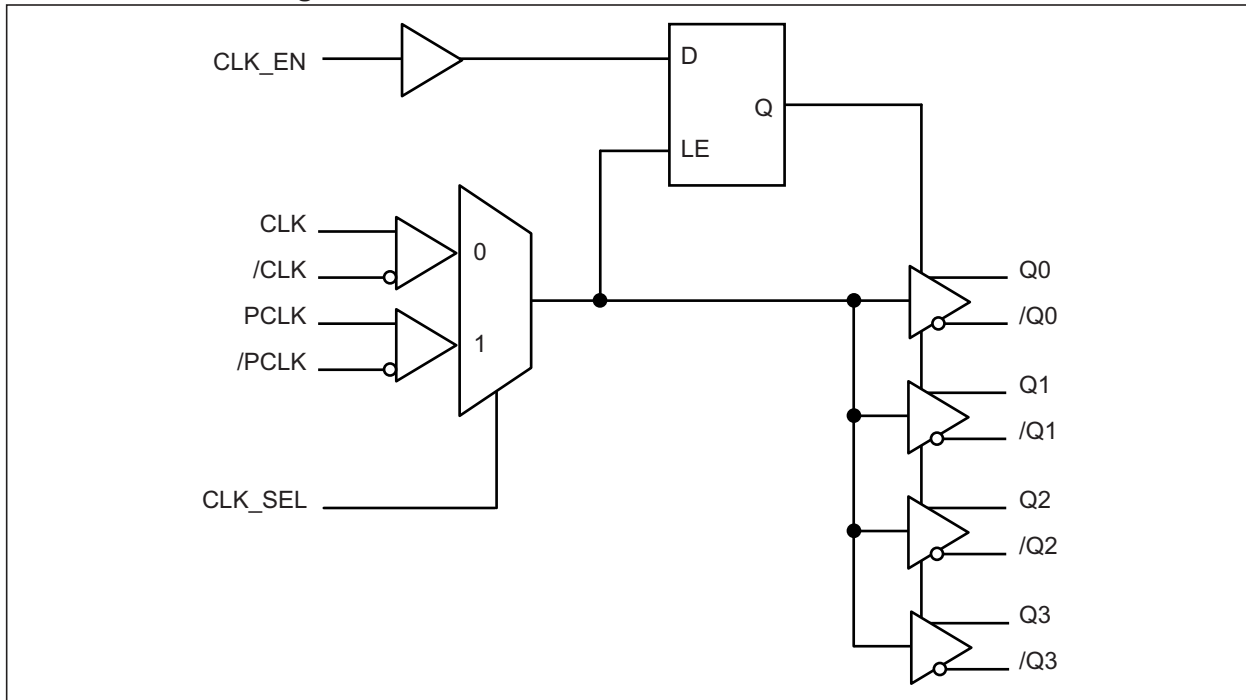
The SY898533L operates from a 3.3V  $\pm$ 5% supply and is guaranteed over the 0°C to +70°C temperature range. The SY898533L is part of Microchip's high-speed, Precision Edge<sup>®</sup> product line.

### Package Type



# SY898533L

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC} + 0.5V$
LVPECL Continuous Output Current ( $I_{OUT}$ )	50 mA
LVPECL Surge Output Current ( $I_{OUT}$ )	100 mA
Lead Temperature (Soldering, 20 sec.)	+260°C
Storage Temperature ( $T_S$ )	-65°C to +150°C

### Operating Ratings ‡

Supply Voltage ( $V_{CC}$ )	+3.135V to +3.465V
Ambient Temperature ( $T_A$ )	0°C to +70°C
Package Thermal Resistance (TSSOP, $\theta_{JA}$ , Still-Air)	73.2°C/W (Note 1)

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

**Note 1:**  $\theta_{JA}$  value is determined for a 4-layer board in still air unless otherwise stated.

**TABLE 1-1: DC ELECTRICAL CHARACTERISTICS**

**Electrical Characteristics:**  $V_{CC} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Power Supply</b>						
Power Supply	$V_{CC}$	3.135	3.3	3.465	V	—
Power Supply Current	$I_{EE}$	—	—	50	mA	No load, max. $V_{CC}$
<b>LVCMOS/LVTTL</b>						
Input High Voltage	$V_{IH}$	2	—	$V_{CC}+0.3$	V	—
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V	—
Input High Current	$I_{IH}$	—	—	5	$\mu A$	CLK_EN, $V_{IN} = V_{CC} = 3.465V$
		—	—	150		CLK_SEL, $V_{IN} = V_{CC} = 3.465V$
Input Low Current	$I_{IL}$	-150	—	—	$\mu A$	CLK_EN, $V_{IN} = 0V$ , $V_{CC} = 3.465V$
		-5	—	—		CLK_SEL, $V_{IN} = 0V$ , $V_{CC} = 3.465V$
<b>Differential</b>						
Input High Current	$I_{IH}$	—	—	150	$\mu A$	CLK, $V_{IN} = V_{CC} = 3.465V$
		—	—	5		/CLK, $V_{IN} = V_{CC} = 3.465V$
Input Low Current	$I_{IL}$	-5	—	—	$\mu A$	CLK, $V_{IN} = 0.5V$ , $V_{CC} = 3.465V$
		-150	—	—		/CLK, $V_{IN} = 0.5V$ , $V_{CC} = 3.465V$
Peak-to-Peak Input Voltage	$V_{PP}$	0.15	—	1.3	V	—
Common Mode Input Voltage	$V_{CMR}$	$V_{EE}+0.5$	—	$V_{CC}-0.85$	V	<a href="#">Note 2</a> , <a href="#">Note 3</a>
<b>LVPECL</b>						
Input High Current	$I_{IH}$	—	—	150	$\mu A$	PCLK, $V_{IN} = V_{CC} = 3.465V$
		—	—	5		/PCLK, $V_{IN} = V_{CC} = 3.465V$
Input Low Current	$I_{IL}$	-5	—	—	$\mu A$	PCLK, $V_{IN} = 0V$ , $V_{CC} = 3.465V$
		-150	—	—		/PCLK, $V_{IN} = 0V$ , $V_{CC} = 3.465V$

# SY898533L

**TABLE 1-1: DC ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Characteristics:**  $V_{CC} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Peak-to-Peak Input Voltage	$V_{PP}$	0.3	—	1	V	—
Common Mode Input Voltage	$V_{CMR}$	$V_{EE}+1.5$	—	$V_{CC}$	V	<a href="#">Note 2</a> , <a href="#">Note 3</a>
Output High Voltage	$V_{OH}$	$V_{CC}-1.4$	—	$V_{CC}-0.9$	V	<a href="#">Note 4</a>
Output Low Voltage	$V_{OL}$	$V_{CC}-2.0$	—	$V_{CC}-1.7$	V	<a href="#">Note 4</a>
Peak-to-Peak Output Voltage Swing	$V_{SWING}$	0.6	—	1.0	V	—

**Note 1:** The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

- 2:** Maximum input voltage for PCLK and /PCLK is  $V_{CC} + 0.3V$  for single-ended applications.
- 3:**  $V_{IH}$  is defined as the common mode voltage.
- 4:**  $50\Omega$  to  $V_{CC} - 2V$  terminated outputs.

**TABLE 1-2: AC ELECTRICAL CHARACTERISTICS**

**Electrical Characteristics:**  $V_{CC} = 3.3V \pm 5\%$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise stated. [Note 1](#).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	$f_{MAX}$	650	—	—	MHz	—
Differential Propagation Delay IN-to-Q	$t_{PD}$	1.0	—	1.4	ns	$f \leq 650$ MHz
Output-to-Output Skew	$t_{SKEW}$	—	—	30	ps	<a href="#">Note 2</a>
Part-to-Part Skew		—	—	150		<a href="#">Note 3</a>
Additive Phase Jitter	$t_{JITTER}$	—	145	—	$f_{RMS}$	<a href="#">Note 4</a> , 12 kHz to 20 MHz @ 622 MHz
Output Rise/Fall Time	$t_r/t_f$	300	—	700	ps	20% to 80% @ 50 MHz
Output Duty Cycle	ODC	47	—	53	%	—

**Note 1:** High-frequency AC parameters are guaranteed by design and characterization.

- 2:** Output-to-Output skew is measured between two different outputs under identical transitions.
- 3:** Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. This parameter is defined in accordance with JEDEC Standard 65.
- 4:** Driving only one input clock.

## TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Maximum Junction Temperature	$T_J$	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature	$T_S$	-65	—	+150	°C	—
Ambient Operating Temperature	$T_A$	0	—	+70	°C	Note 1
<b>Package Thermal Resistance</b>						
Thermal Resistance, 20-Ld TSSOP	$\theta_{JA}$	—	73.2	—	°C/W	Still-Air

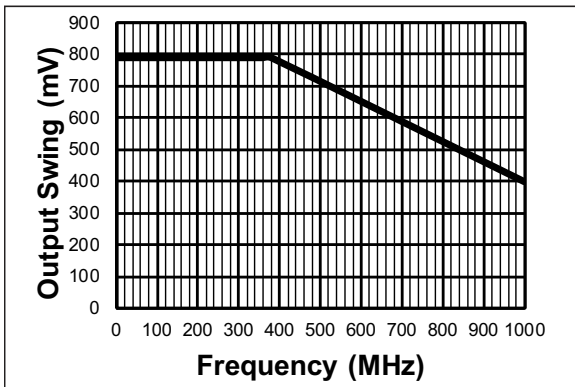
**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

# SY898533L

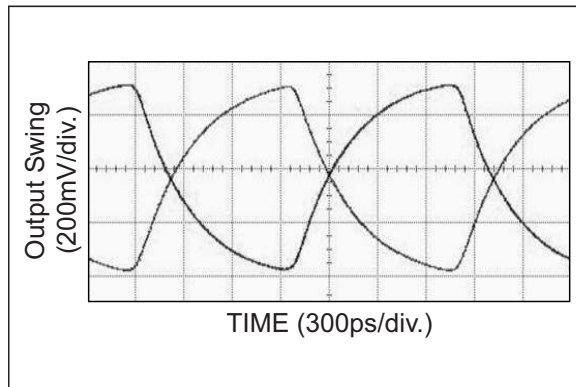
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

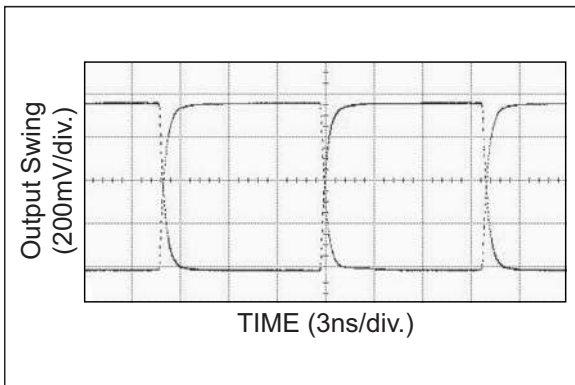
$V_{CC} = 3.3V$ ,  $V_{EE} = 0V$ ,  $V_{IN} = 800\text{ mV}$ ,  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise stated.



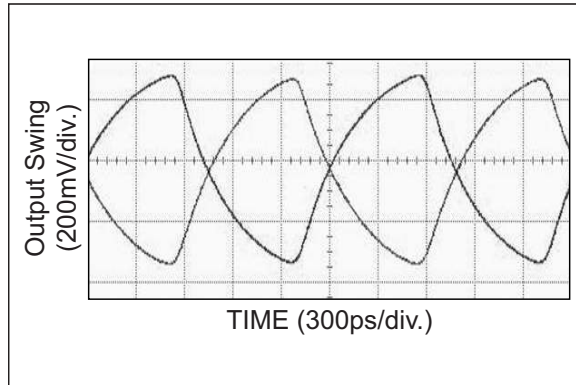
**FIGURE 2-1:** Output Swing vs. Frequency.



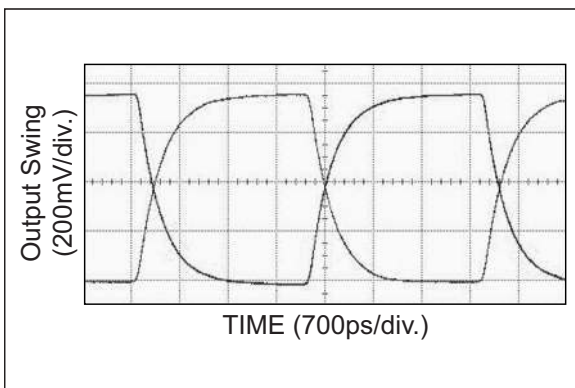
**FIGURE 2-4:** 500 MHz Clock.



**FIGURE 2-2:** 50 MHz Clock.



**FIGURE 2-5:** 650 MHz Clock.



**FIGURE 2-3:** 200 MHz Clock.

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

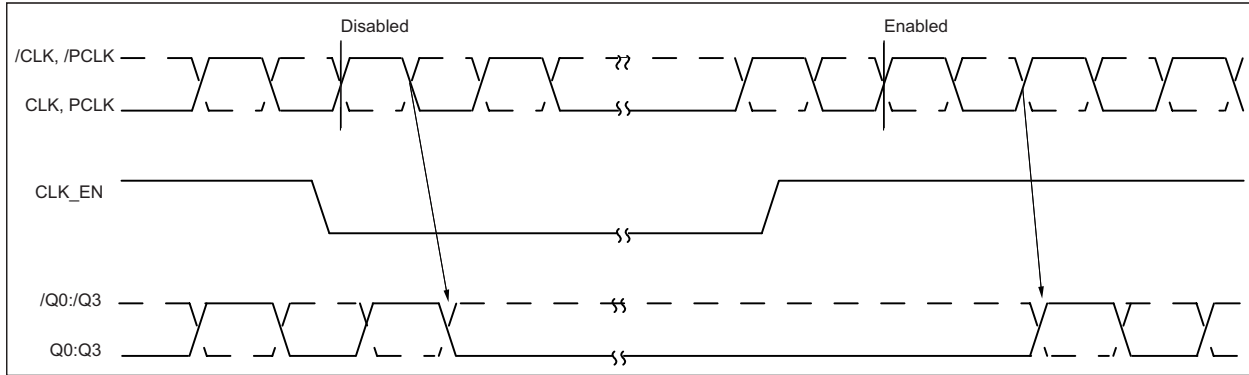
**TABLE 3-1: SY898533L PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	VEE	Ground.
2	CLK_EN	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q3 outputs. It is internally connected to a 50 kΩ pull-up resistor and will default to a logic high state if left open. When disabled, Q goes low and /Q goes high. CLK_EN being synchronous, outputs will be enabled/disabled following a rising and a falling edge of the input clock. $V_{TH}$ is approximately 1.5V.
3	CLK_SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the input to the multiplexer. Note that this input is internally connected to a 50 kΩ pull-down resistor and will default to logic low state if left open. $V_{TH}$ is approximately 1.5V.
4, 5	CLK, /CLK	Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. CLK is internally connected to a 28 kΩ pull-down resistor and will default to a logic low state if left open while /CLK is connected to a 50 kΩ pull-up resistor and will default to a logic high state if left open. This input pair is selected when CLK_SEL is set to logic low.
6, 7	PCLK, /PCLK	Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. PCLK is internally connected to a 50 kΩ pull-down resistor and will default to a logic low state if left open while /PCLK is connected to a 50 kΩ pull-up resistor and will default to a logic high state if left open. This input pair is selected when CLK_SEL is set to logic high.
8, 9	NC	Unused Pins.
10, 13, 18	VCC	Positive Power Supply Pins: Bypass with 0.1 μF  0.01 μF low-ESR capacitors as close to the VCC pins as possible.
20, 19 17, 16 15, 14 12, 11	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVPECL Differential Output Pairs: Differential buffered output copies of the selected input signal. The output swing is typically 800 mV. Unused output pairs may be left floating with no impact on jitter. These differential LVPECL outputs are a logic function of the CLK, /CLK and PCLK, /PCLK, and CLK_SEL inputs. See <a href="#">Table 3-2</a> .

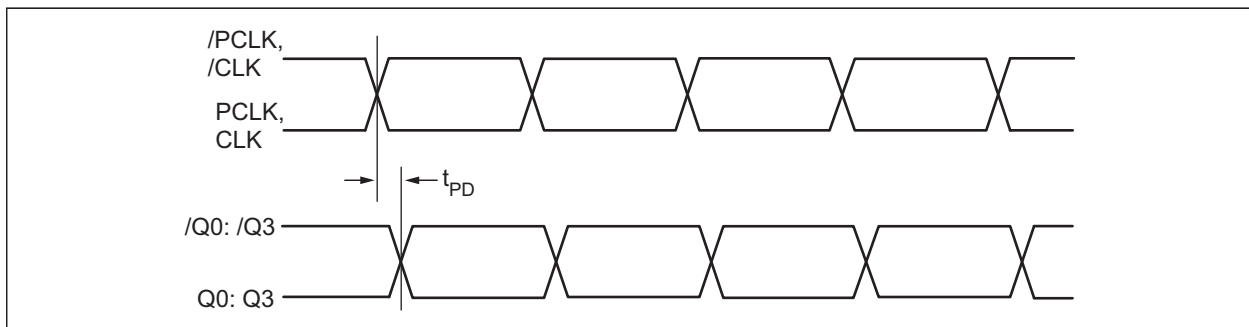
**TABLE 3-2: TRUTH TABLE**

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	/Q0:/Q3
0	0	CLK, /CLK	Disabled:Low	Disabled:High
0	1	PCLK, /PCLK	Disabled:Low	Disabled:High
1	0	CLK, /CLK	CLK	/CLK
1	1	PCLK, /PCLK	PCLK	/PCLK

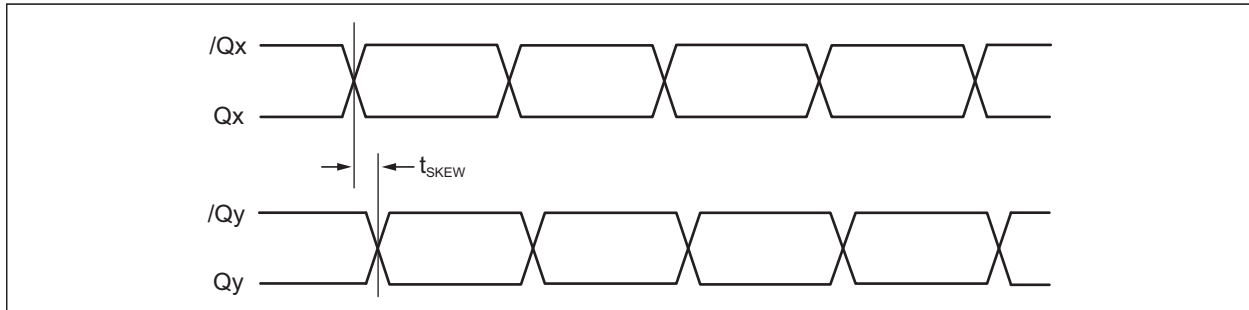
## 4.0 TIMING DIAGRAMS



**FIGURE 4-1:** CLK\_EN Timing Diagram.



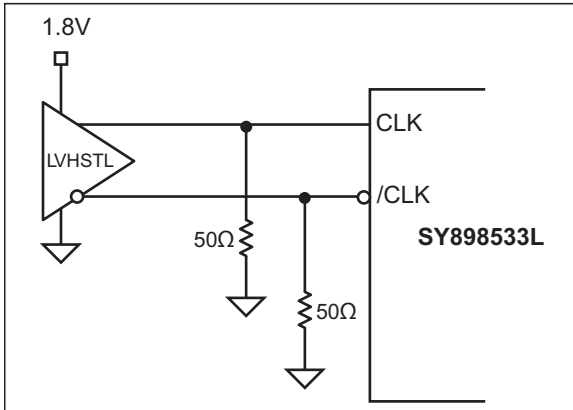
**FIGURE 4-2:** Propagation Delay.



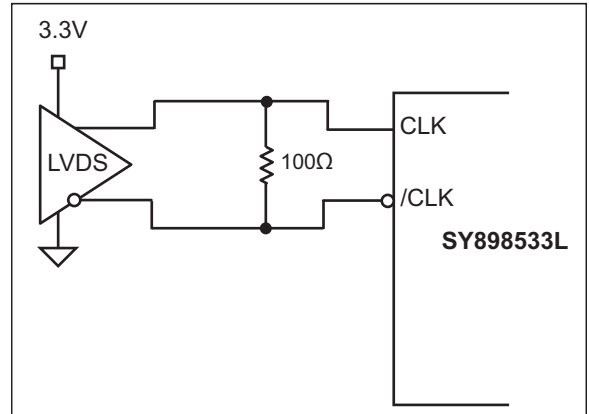
**FIGURE 4-3:** Output-to-Output Skew.



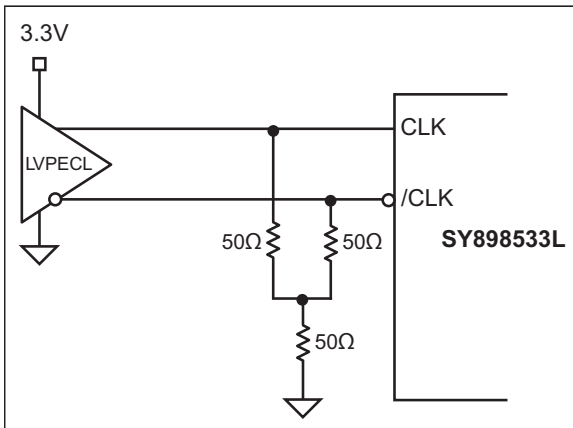
## 5.0 CLK, /CLK INPUT INTERFACE APPLICATIONS



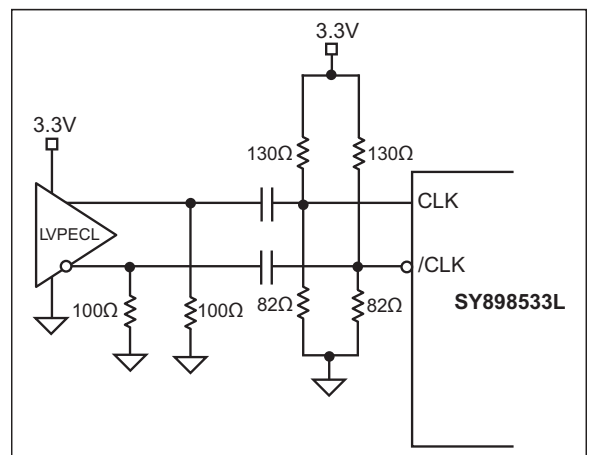
**FIGURE 5-1:** LVHSTL Interface (DC-Coupled).



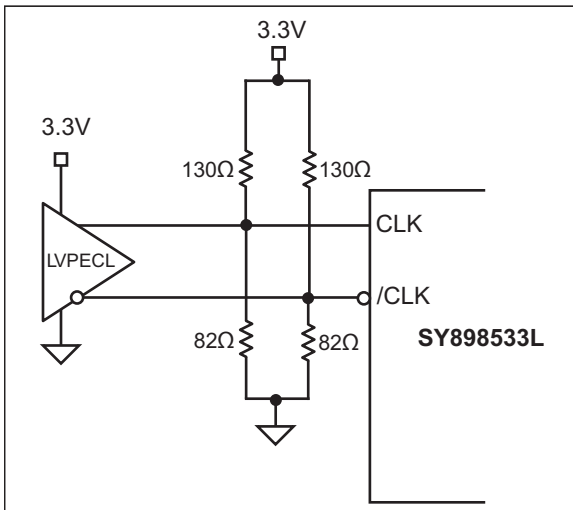
**FIGURE 5-4:** LVDS Interface (DC-Coupled).



**FIGURE 5-2:** LVPECL Interface (DC-Coupled).



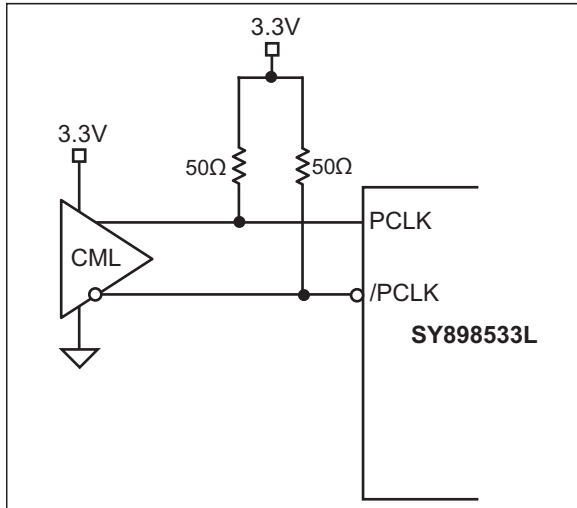
**FIGURE 5-5:** LVPECL Interface (AC-Coupled).



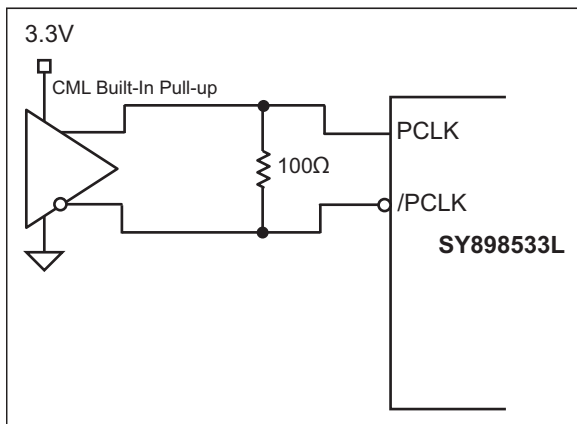
**FIGURE 5-3:** LVPECL Interface (DC-Coupled).

# SY898533L

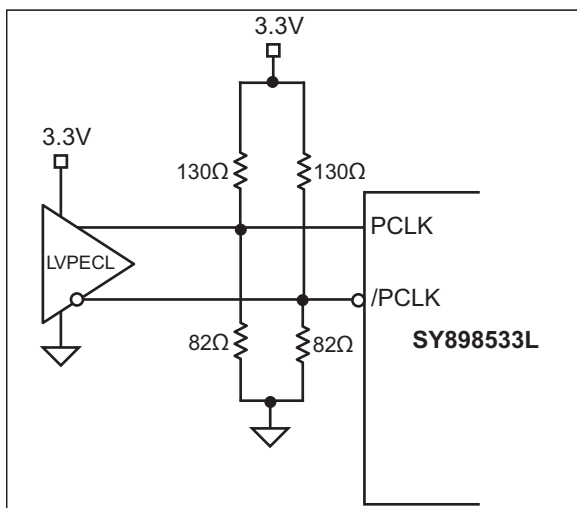
## 6.0 PCLK, /PCLK INPUT INTERFACE APPLICATIONS



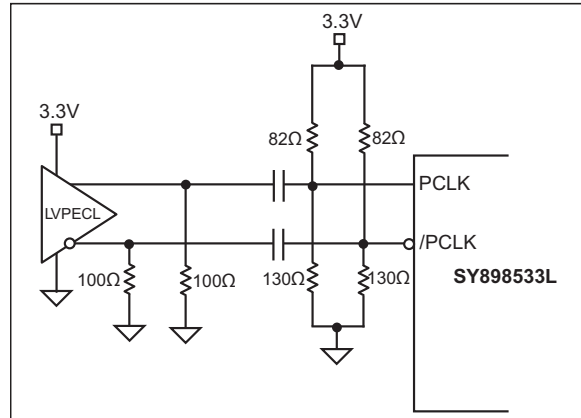
**FIGURE 6-1:** CML Open Collector Interface (DC-Coupled).



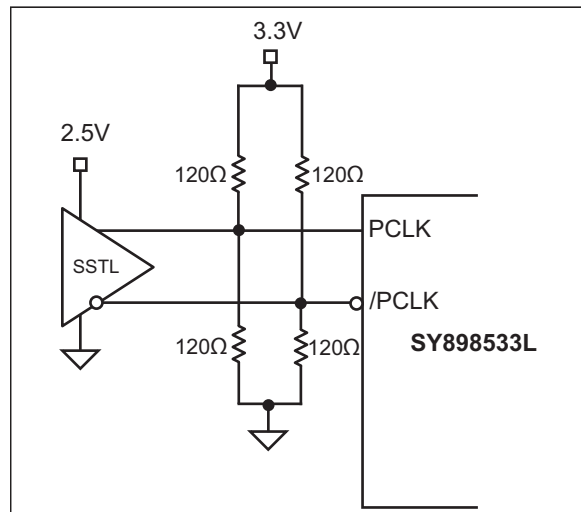
**FIGURE 6-2:** CML Built-In Pull-Up Interface (DC-Coupled).



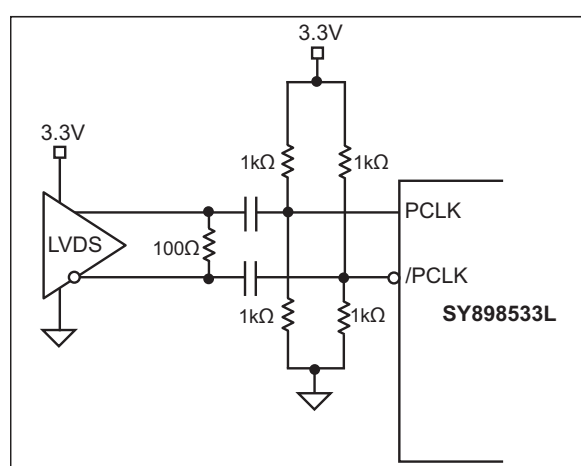
**FIGURE 6-3:** LVPECL Interface (DC-Coupled).



**FIGURE 6-4:** LVPECL Interface (AC-Coupled).



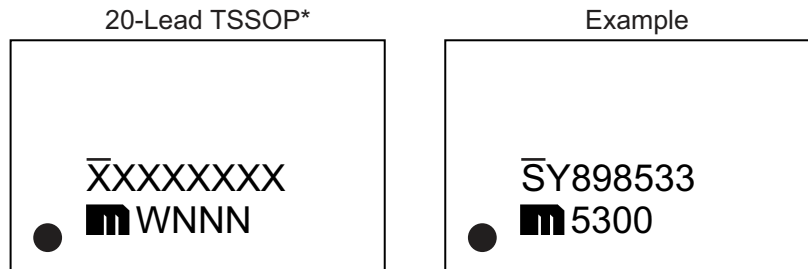
**FIGURE 6-5:** SSTL Interface (DC-Coupled).



**FIGURE 6-6:** LVDS Interface (AC-Coupled).

## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information



<b>Legend:</b>	<p>XX...X Product code or customer-specific information</p> <p>Y Year code (last digit of calendar year)</p> <p>YY Year code (last 2 digits of calendar year)</p> <p>WW Week code (week of January 1 is week '01')</p> <p>SSS Alphanumeric traceability code</p> <p>(e3) Pb-free JEDEC® designator for Matte Tin (Sn)</p> <p>* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.</p> <p>•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).</p>
<b>Note:</b>	<p>In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.</p> <p>Underbar ( _ ) and/or Overbar ( ¯ ) symbol may not be to scale.</p>

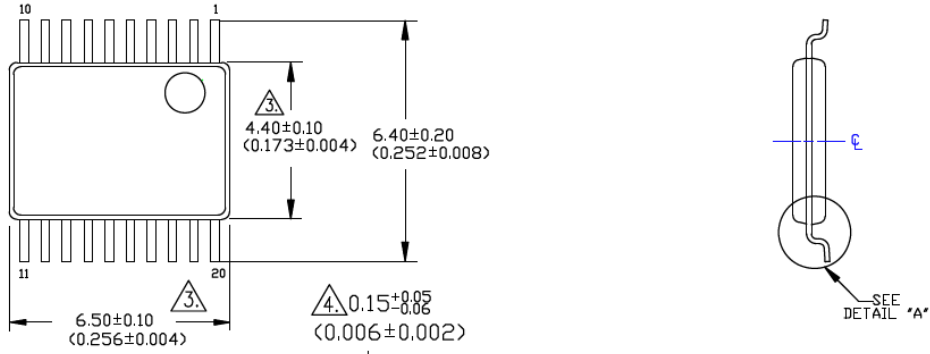
# SY898533L

## 20-Lead TSSOP Package Outline and Recommended Land Pattern

**TITLE**

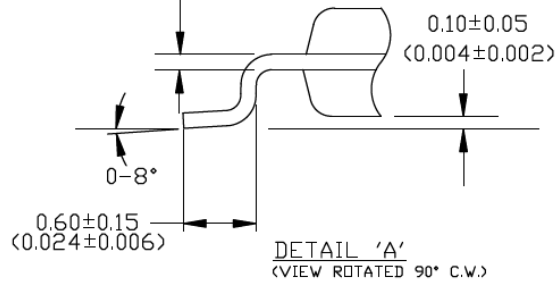
20 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-20LD-PL-1	UNIT	MM [INCH]
-----------	-----------------	------	-----------

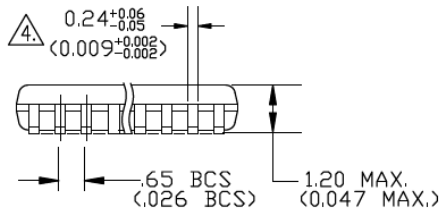


**TOP VIEW**  
NOTES : 1, 2, 3

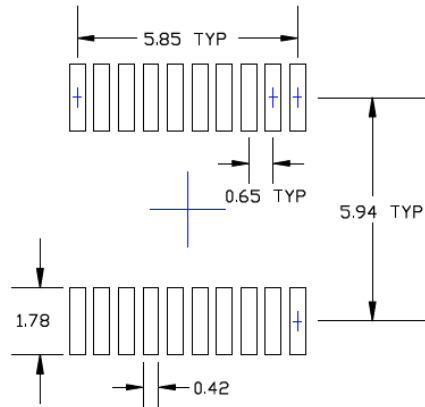
**END VIEW**



**DETAIL 'A'**  
(VIEW ROTATED 90° C.W.)



**SIDE VIEW**  
NOTES : 1, 2, 4



**RECOMMENDED LAND PATTERN**

**NOTES:**

1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (April 2019)

- Converted Micrel document SY898533L to Microchip data sheet DS20006043A.
- Minor text changes throughout.
- Updated Additive Phase Jitter value in [Features](#).
- Updated Additive Phase Jitter value and conditions in [Table 1-2](#).
- Updated temperature range in the following sections: [Features](#), [General Description](#), [Operating Ratings](#) ‡, [Table 1-1](#), [Table 1-2](#), [Product Identification System](#).

# SY898533L

---

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	X	X	X	-XX
Device	Voltage Option	Package Type	Temperature Range	Special Processing
<b>Device:</b>	SY898533:	Precision Differential 3.3V Low-Skew LVPECL	1:4 Fanout Buffer	
<b>Voltage Option:</b>	L	=	3.3V Only	
<b>Package Type:</b>	K	=	20-Lead TSSOP	
<b>Temperature Range:</b>	Z	=	0°C to +70°C	
<b>Special Processing:</b>	<blank>	=	74/Tube	
	TR	=	1,000/Reel	

**Examples:**

a) SY898533LKZ: SY898533, 3.3V Voltage Option, 20-Lead TSSOP, 0°C to 70°C Temperature Range, 74/Tube

b) SY898533LKZ-TR: SY898533, 3.3V Voltage Option, 20-Lead TSSOP, 0°C to 70°C Temperature Range, 1,000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

# SY898533L

---

NOTES:



---

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
= ISO/TS 16949 =**

### Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, Klear, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntellIMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, memBrain, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019, Microchip Technology Incorporated, All Rights Reserved.  
ISBN: 978-1-5224-4446-6



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453  
Tel: 317-536-2380

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608  
Tel: 951-273-7800

**Raleigh, NC**  
Tel: 919-844-7510

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110  
Tel: 408-436-4270

**Canada - Toronto**  
Tel: 905-695-1980  
Fax: 905-695-2078

### ASIA/PACIFIC

**Australia - Sydney**  
Tel: 61-2-9868-6733

**China - Beijing**  
Tel: 86-10-8569-7000

**China - Chengdu**  
Tel: 86-28-8665-5511

**China - Chongqing**  
Tel: 86-23-8980-9588

**China - Dongguan**  
Tel: 86-769-8702-9880

**China - Guangzhou**  
Tel: 86-20-8755-8029

**China - Hangzhou**  
Tel: 86-571-8792-8115

**China - Hong Kong SAR**  
Tel: 852-2943-5100

**China - Nanjing**  
Tel: 86-25-8473-2460

**China - Qingdao**  
Tel: 86-532-8502-7355

**China - Shanghai**  
Tel: 86-21-3326-8000

**China - Shenyang**  
Tel: 86-24-2334-2829

**China - Shenzhen**  
Tel: 86-755-8864-2200

**China - Suzhou**  
Tel: 86-186-6233-1526

**China - Wuhan**  
Tel: 86-27-5980-5300

**China - Xian**  
Tel: 86-29-8833-7252

**China - Xiamen**  
Tel: 86-592-2388138

**China - Zhuhai**  
Tel: 86-756-3210040

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444

**India - New Delhi**  
Tel: 91-11-4160-8631

**India - Pune**  
Tel: 91-20-4121-0141

**Japan - Osaka**  
Tel: 81-6-6152-7160

**Japan - Tokyo**  
Tel: 81-3-6880-3770

**Korea - Daegu**  
Tel: 82-53-744-4301

**Korea - Seoul**  
Tel: 82-2-554-7200

**Malaysia - Kuala Lumpur**  
Tel: 60-3-7651-7906

**Malaysia - Penang**  
Tel: 60-4-227-8870

**Philippines - Manila**  
Tel: 63-2-634-9065

**Singapore**  
Tel: 65-6334-8870

**Taiwan - Hsin Chu**  
Tel: 886-3-577-8366

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-8600

**Thailand - Bangkok**  
Tel: 66-2-694-1351

**Vietnam - Ho Chi Minh**  
Tel: 84-28-5448-2100

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**Finland - Espoo**  
Tel: 358-9-4520-820

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Garching**  
Tel: 49-8931-9700

**Germany - Haan**  
Tel: 49-2129-3766400

**Germany - Heilbronn**  
Tel: 49-7131-67-3636

**Germany - Karlsruhe**  
Tel: 49-721-625370

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Rosenheim**  
Tel: 49-8031-354-560

**Israel - Ra'anana**  
Tel: 972-9-744-7705

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Padova**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Norway - Trondheim**  
Tel: 47-7288-4388

**Poland - Warsaw**  
Tel: 48-22-3325737

**Romania - Bucharest**  
Tel: 40-21-407-87-50

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Gothenberg**  
Tel: 46-31-704-60-40

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820