

MAX40070/MAX40072

Click [here](#) to ask an associate for production status of specific part numbers.

High Voltage, Low Power Comparator

General Description

MAX40070/MAX40072 is a family of single micropower comparators ideal for a wide variety of battery operated devices in computing, industrial, medical, and IoT applications that have extremely tight board space and power constraints while requiring high levels of precision. These comparators are offered with an open-drain output in a small 8-bump (0.35 μ m pitch) wafer level package as well as a TDFN package.

The MAX40070/MAX40072 family features a rail-to-rail input voltage range of 0V to +27.5V on IP pin, independent of the supply voltage. It also features internal filtering to provide high EMI immunity.

The MAX40070/MAX40072 uses a high-precision integrated reference voltage (1.6V) as well as a precision internal current source that allows customized comparator threshold and hysteresis by using two external resistors.

These comparators consume only 16 μ A (typ) supply current with a propagation delay of 2 μ s. They all operate over the extended -40°C to +125°C temperature range.

Applications

- Notebook and Tablet Computers
- Portable Medical Devices
- Industrial Equipment
- IoT

Simplified Block Diagram

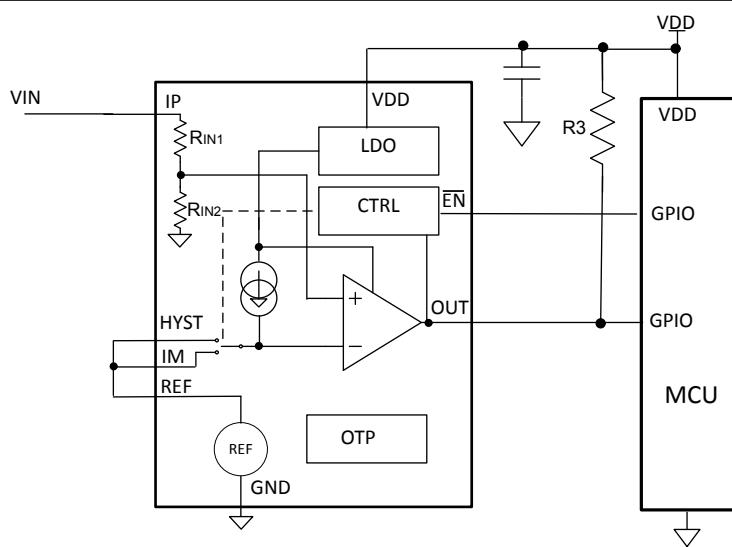


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Absolute Maximum Ratings

V _{DD} to GND.....	-0.3V to +40V	Continuous Power Dissipation (WLP-6) (T _A = +70°C, derate 10.9mW/°C above +70°C.)	872mW
I _P to GND	-0.3V to +40V	Continuous Power Dissipation (TDFN-8) (T _A = +70°C, derate 6.2mW/°C above +70°C.)	496mW
I _M , HYST, \overline{EN} , REF to GND.....	-0.3V to +6V		
OUT to GND.....	-0.3V to +8V		
Continuous current into any pin.....	0.02A	Operating Temperature Range	
		Reduced performance temperature range	-40°C to 125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	N81B1+1
Outline Number	21-100566
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	91.72°C/W
Junction to Case (θ_{JC})	N/A

TDFN

Package Code	T822C+6C
Outline Number	21-100514
Land Pattern Number	90-100183
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	162°C/W
Junction to Case (θ_{JC})	20°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{DD} = 3.3V$, $V_{EN} = GND$, $IP = 0V$, $IM = HYST = REF$, OUT connected to $100k\Omega$ pull-up to V_{DD} ([Note 1](#))).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS		
POWER SUPPLY									
Supply Voltage Range	V_{DD}	Guaranteed by PSRR		2.2		36	V		
Supply Current	I_{DD}	MAX40070/2, No Load	$T_A = 25^\circ C$ $-40^\circ C \leq T_A \leq +125^\circ C$	16	22	26	μA		
Supply Current	I_{SHDN}	$\overline{EN} = V_{DD}$	$-40^\circ C \leq T \leq +125^\circ C$	400	1,000		nA		
Power Supply Rejection Ratio	PSRR	$2.2V \leq V_{DD} \leq 36V$		56	70		dB		
Turn-On Time	t_{EN}	Turn-on from shutdown	$V_{EN} = 1.8V$ to 0V, Measured at 90% of nominal final value		250		μs		
Power-On Time	t_{ON}	$V_{DD} = 0V$ to 3.3V, Measured at 90% of nominal final value			500		us		
COMPARATOR									
COMPARATOR / INPUT THRESHOLD									
Current Source	IREF	$-40^\circ C \leq T_A \leq +85^\circ C$		2.94	3	3.07	μA		
		$-40^\circ C \leq T_A \leq +125^\circ C$		2.94	3	3.11			
Input Common Mode Range	V_{IP}	IP Input		0		27.5	V		
	V_{IM}	IM Input		0		2.5			
Input Divider Resistance	R_{IP}	IP Input			6.6		MΩ		
Input Offset Voltage	V_{OS}	Referred to IP	$T = 25^\circ C$		3.3	12	mV		
			$-40^\circ C \leq T \leq +85^\circ C$			43			
			$-40^\circ C \leq T \leq +125^\circ C$			50			
Input Hysteresis	V_{HYST}	Referred to IP		45	90		mV		
Input Bias Current	I_B	Referred to IP, $IP = 17.6V$			2.5	5	μA		
		Referred to IM			0.1	5	nA		
Input Capacitance	C_{IN}	IP Input			4		pF		
Common Mode Rejection Ratio	CMRR	DC, over the entire common mode input range	IP, $0 \sim 27.5V$	43	50		dB		
Output Voltage Swing Low	V_{OL}	Sinks 2mA				0.4	V		
Open Drain Leakage Current	I_{OH}	$OUT = 8V$			1	12	nA		
Propagation Delay	t_P	20mV overdrive, Output L → H			3.5		μs		
		20mV overdrive, Output H → L			2				
Fall Time	t_F	80% to 20%			400		ns		

Electrical Characteristics (continued)

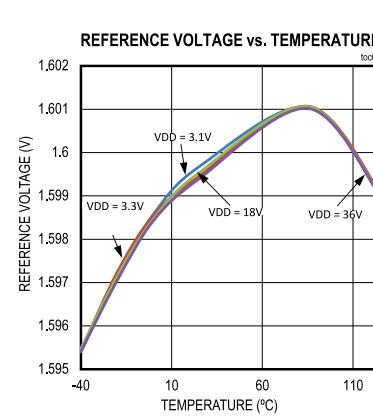
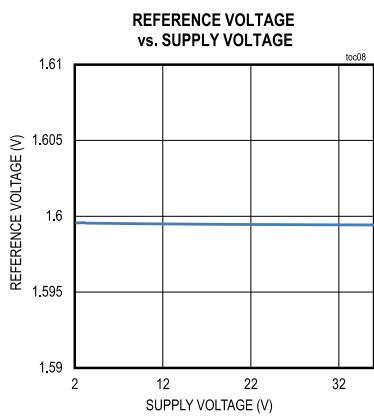
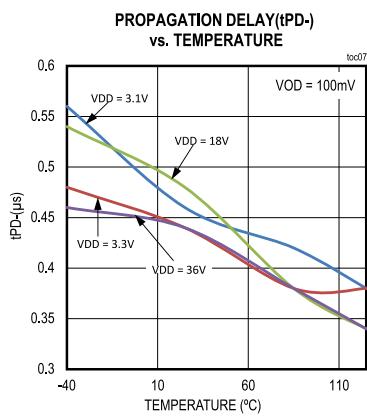
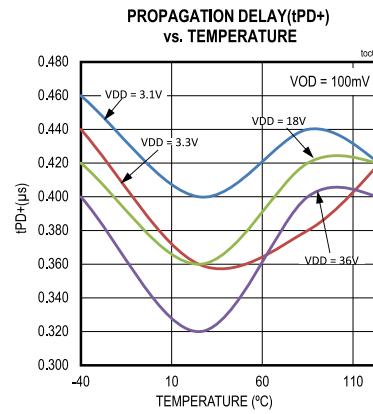
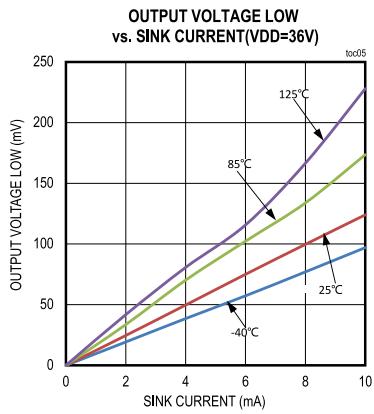
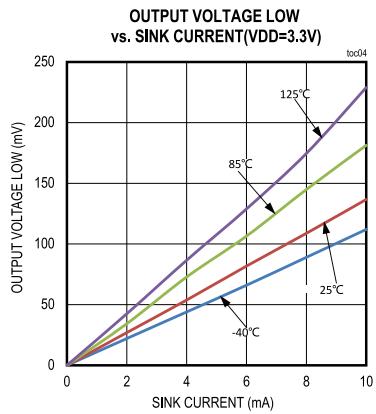
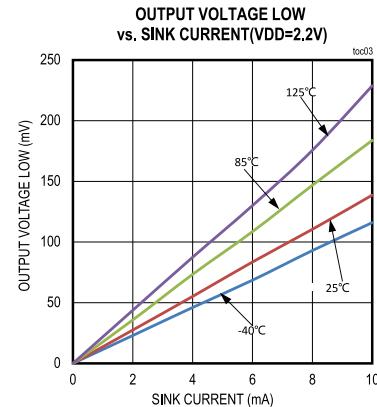
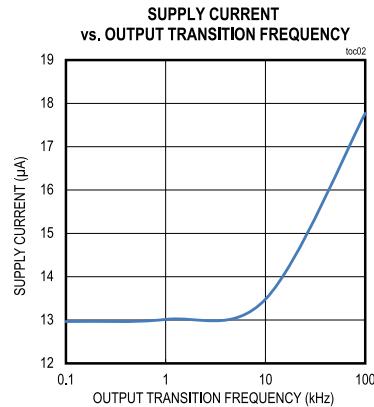
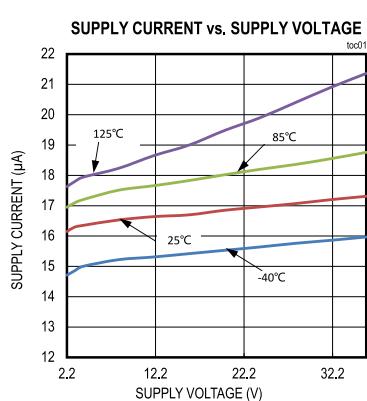
($V_{DD} = 3.3V$, $V_{EN} = GND$, $IP = 0V$, $IM = HYST = REF$, OUT connected to $100k\Omega$ pull-up to V_{DD} ([Note 1](#))).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE VOLTAGE						
Reference Voltage	V_{REF}		1.6			V
Reference Voltage Accuracy			-1.3		1.3	%
Reference Voltage Thermal Drift			15			ppm/ $^{\circ}C$
Line Regulation			100			ppm/V
Load Regulation		$ V_{REF_OUT} = +/-100nA$	0.002			mV/nA
Output Current			2			μA
Voltage Noise		0.1Hz to 10Hz	82			μV_{pp}
Voltage Noise Density		$C_{REF} = 1nF$ 10Hz to 6kHz	2.2			$\mu V/\sqrt{Hz}$
Capacitive Load Capability			100			pF
ENABLE INPUT DC CHARACTERISTICS						
Input Low Level	V_{IL}		0.55			V
Input High Level	V_{IH}		0.9			V
Input Leakage Current	I_L		5			nA

Note 1: Limits are 100% tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

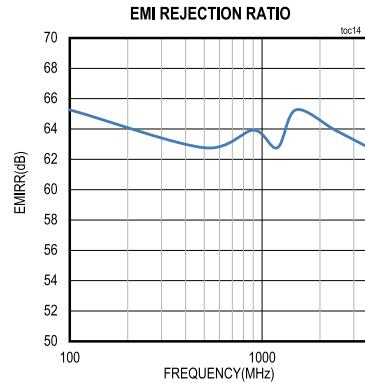
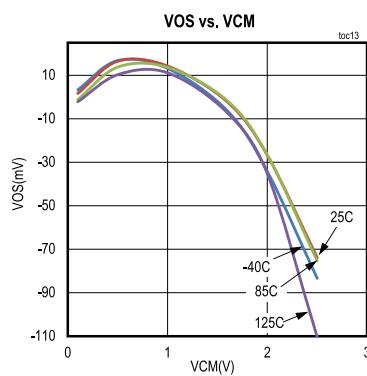
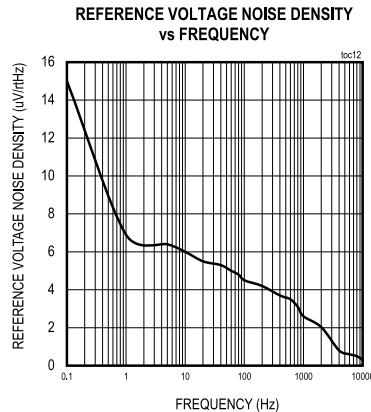
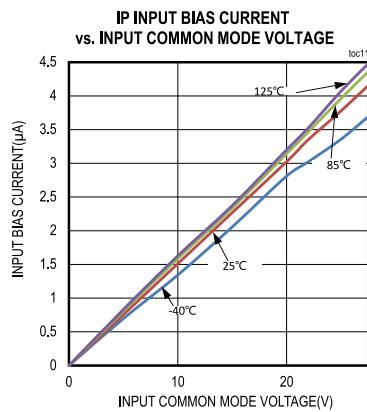
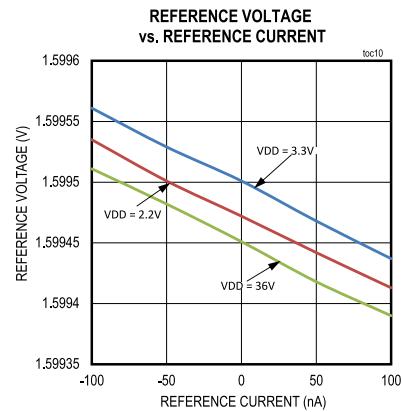
Typical Operating Characteristics

($V_{DD} = 3.3V$, $V_{EN} = GND$, $IP = 0V$, $IM = HYST = REF$, OUT connected to $100k\Omega$ pullup resistor to V_{DD} .)



Typical Operating Characteristics (continued)

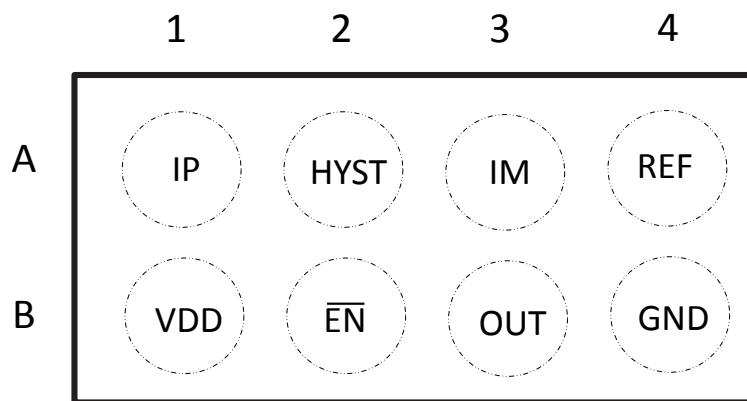
($V_{DD} = 3.3V$, $V_{EN} = GND$, $IP = 0V$, $IM = HYST = REF$, OUT connected to $100k\Omega$ pullup resistor to V_{DD} .)



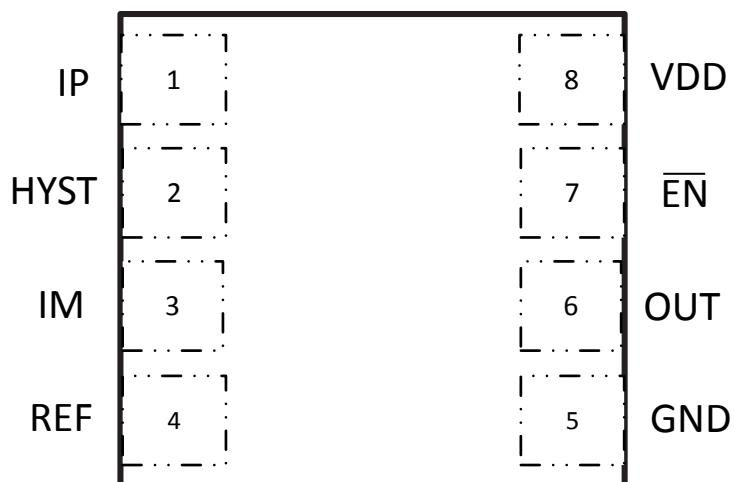
Pin Configurations

WLP

TOP VIEW - BUMPS SIDE DOWN



8-Bump WLP

TDFN**TOP VIEW – PINS AT THE BOTTOM**

8-pin TDFN, 2mm x 2mm

Pin Description

PIN		NAME	FUNCTION
WLP	TDFN		
A1	1	IP	High-Voltage Non-inverting Input
A2	2	HYST	Hysteresis Input
A3	3	IM	Inverting input
A4	4	REF	Reference Output Voltage
B4	5	GND	Ground
B3	6	OUT	Open-Drain Output
B2	7	EN	Device Enable (Active Low)
B1	8	VDD	Positive Supply

Detailed Description

The MAX40070/MAX40072 feature an onboard voltage reference with 1.3% accuracy. The common-mode voltage range of this family can extend beyond the rails, up to 27.5V. The 90mV (IP referred) internal hysteresis ensures clean output switching even with slow moving input signals. The output has an open-drain stage that can be pulled beyond V_{DD} to a maximum of 8V above GND. Multiple comparators with open-drain outputs (OUT) can be connected together in parallel and share a single pullup resistor. This enables the user to detect if there is any fault if at least one comparator is tripped differently from other comparators.

Input Stage Circuitry

The input common-mode voltage range extends from 0 to 27.5V, independent of V_{DD} . Input bias current is typically 2.5 μ A if the input voltage is between the supply rails.

Output Stage Structure

The devices contain a unique break-before-make output stage capable of rail-to-rail operation with up to ± 2 mA loads. Many comparators consume orders of magnitude more current during switching than during steady-state operation. In the [Typical Operating Characteristics](#), TOC2 shows the minimal supply-current increase as the output switching frequency approaches 1kHz. This characteristic reduces the need for power-supply filter capacitors to reduce glitches created by comparator switching currents. In battery-powered applications, this characteristic results in a substantial increase in battery life.

Voltage Reference

The MAX40070/MAX40072 come with an internal voltage reference of 1.6V that has an accuracy of 1.3%. The devices' internal reference has a typical temperature coefficient of 15ppm/ $^{\circ}$ C over the full -40 $^{\circ}$ C to +125 $^{\circ}$ C temperature range. The reference is a very-low-power bandgap cell, with a maximum 2k Ω output impedance. REF pin can source and sink up to 100nA to external circuitry. For applications that need increased drive, buffer REF with a low input-bias current op-amp. Most applications do not require a bypass capacitor on the REF pin.

Applications Information

Internal Hysteresis

Many comparators oscillate in the linear region of operation because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal or very close to the voltage on the other input. The MAX40070/MAX40072 have internal 90mV hysteresis to counter parasitic effects and noise.

The hysteresis in a comparator creates two trip points: one for upper threshold (V_{TRIP+}) and the other for lower threshold (V_{TRIP-}) for voltage transitions on the input signal (Figure 1). The difference between the trip points is the hysteresis band (V_{HYS}). When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input to move quickly past the other, thus taking the input out of the region where oscillation occurs. Figure 1 illustrates the case in which IM has a fixed voltage applied, and IP is varied.

Adding External Hysteresis And Customized Threshold

In applications requiring more than the internal 90mV hysteresis of the devices, additional hystereses can be added with an external resistor. Meanwhile, the threshold can be customized as well. See the [Typical Application Circuits](#) for detail.

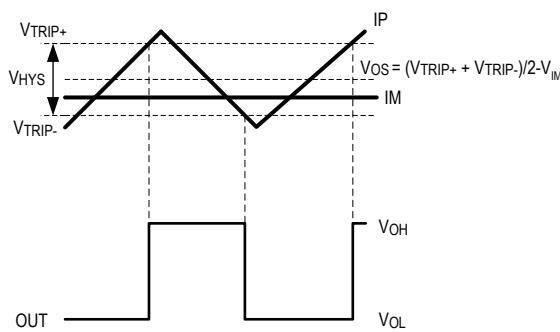


Figure 1. Hysteresis Band

Disabling the Device

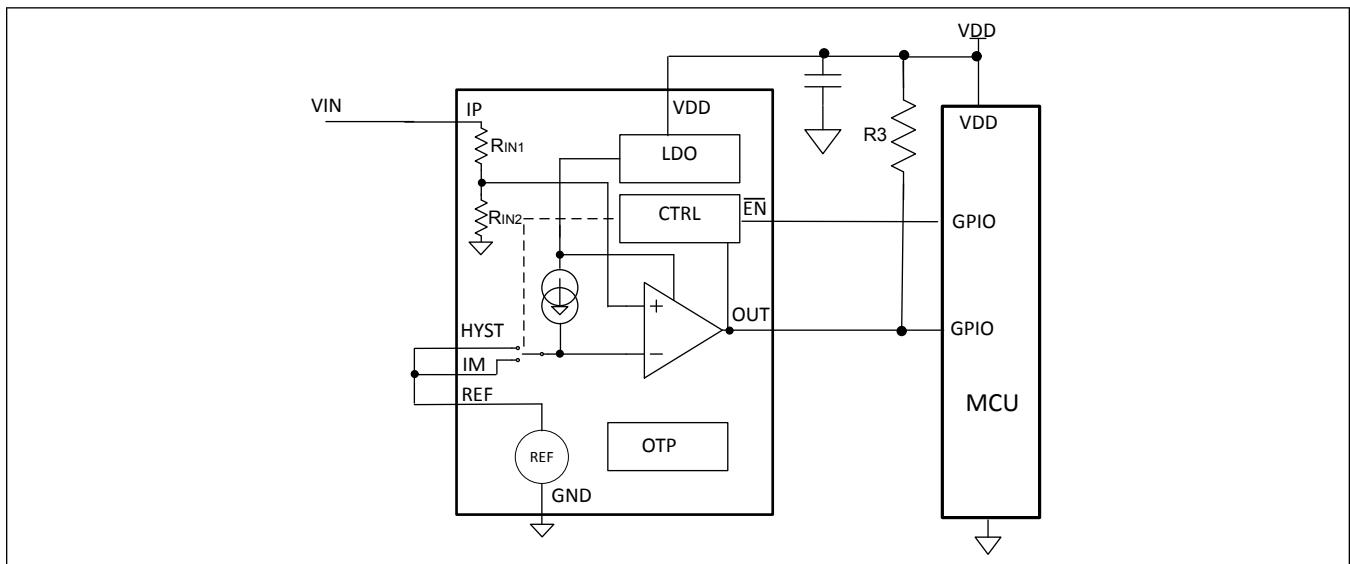
MAX40070/40072 can be disabled with \overline{EN} pin to save the power. The IDD can be reduced to 1000nA (max).

Typical Application Circuits

Application Circuit with Internal Hysteresis

Hysteresis is internal 90mV (typ).

Threshold is equal to internal REF (1.6V typ).



Typical Application Circuits (continued)

Application Circuit with Customized External Threshold and Hysteresis

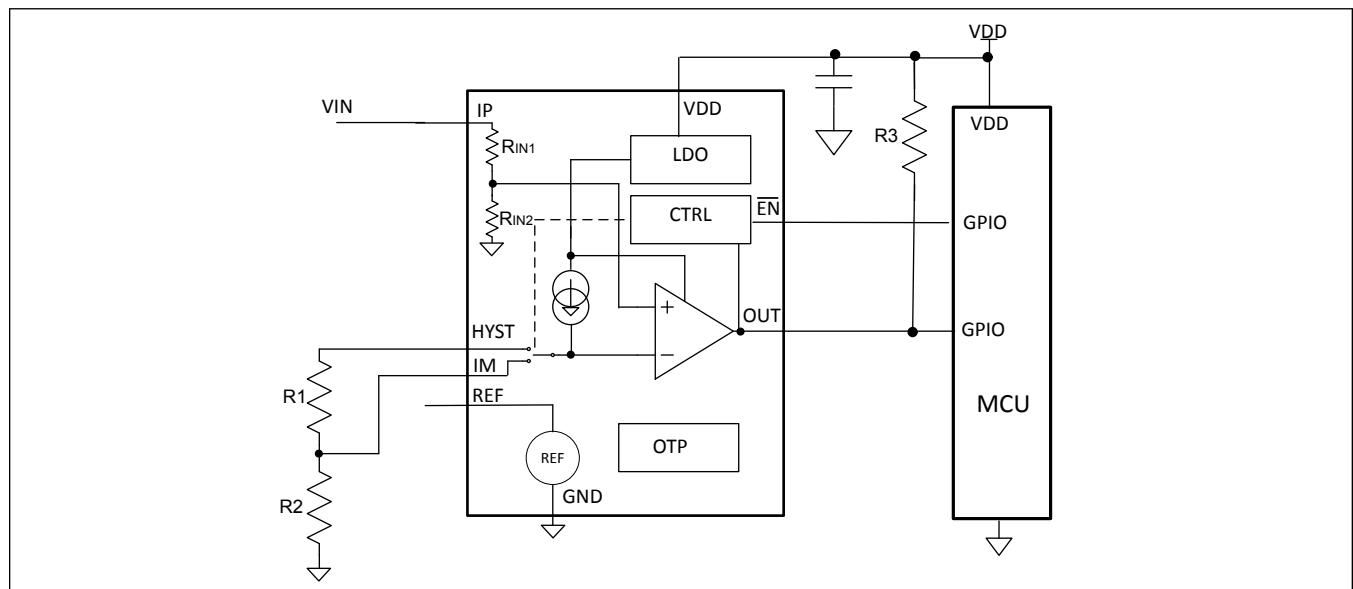
Adding external hysteresis to V_{TRIP+} . Total hysteresis is defined by internal hysteresis and R_1 , shown in the following equation:

$$HYST = 90mV \text{ (typ)} + R_1 \times 3\mu A$$

Customized External Threshold is defined by R_2 , shown in the following equation:

$$\text{Threshold} = R_2 \times 3\mu A$$

The internal REF is not used and it is floating here.



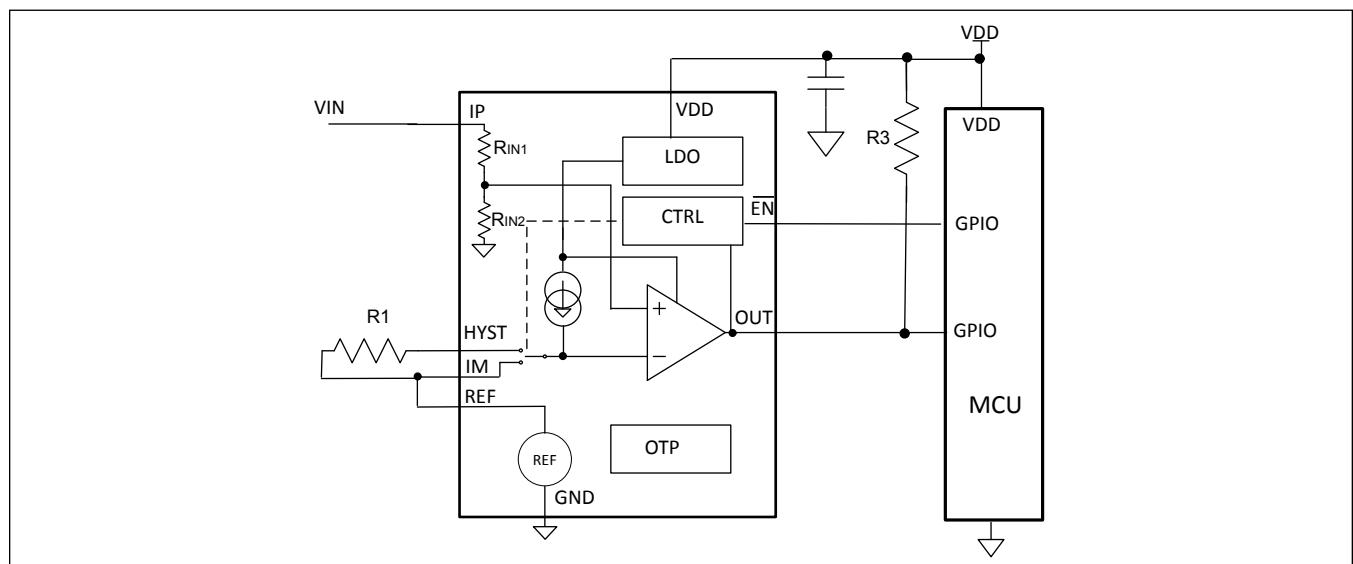
Typical Application Circuits (continued)

Application Circuit with Customized Hysteresis

Adding external hysteresis to V_{TRIP+} . Total hysteresis is defined by internal hysteresis and R_1 , as shown in the following equation:

$$HYST = 90\text{mV (typ)} + R_1 \times 3\mu\text{A}$$

Threshold is equal to internal REF (1.6V typ).



Typical Application Circuits (continued)

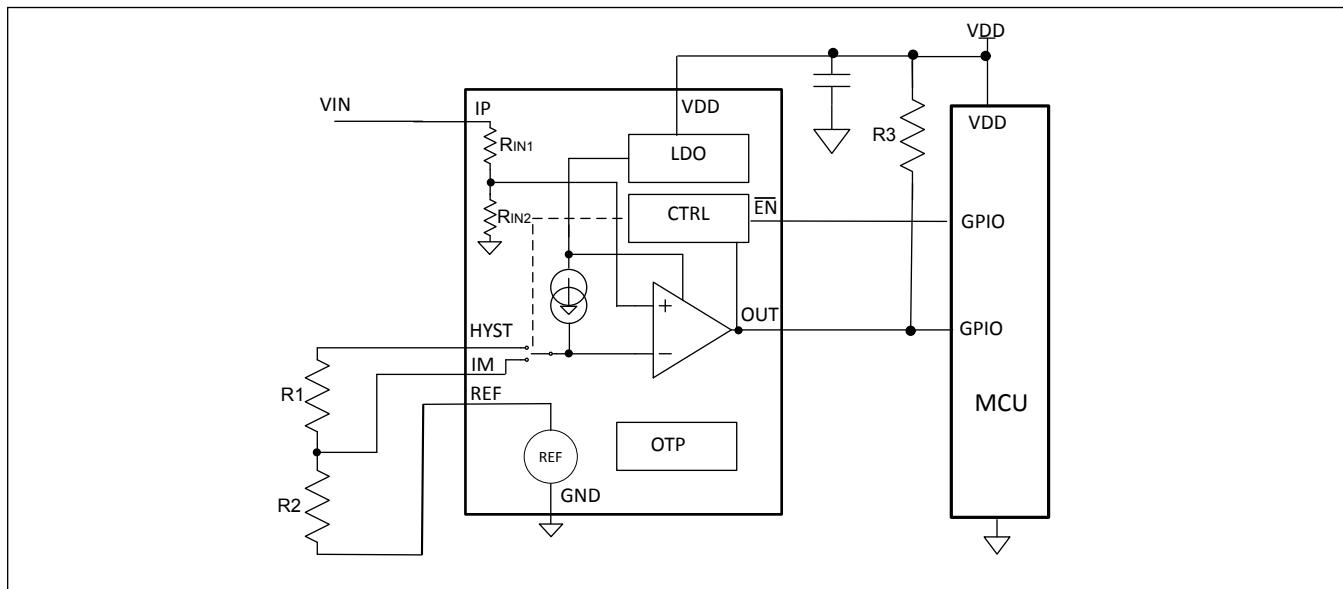
Application Circuit with External Hysteresis and Customized Threshold

Adding external hysteresis to V_{TRIP+} . Total hysteresis is defined by internal hysteresis and R1, as shown in the following equation:

$$HYST = 90\text{mV} (\text{typ}) + R_1 \times 3\mu\text{A}$$

Threshold is defined by internal REF and R2, as shown in the following equation:

$$\text{Threshold} = 1.6\text{V} (\text{typ}) + R_2 \times 3\mu\text{A}$$



Customized Hysteresis and Threshold

The internal current source ($3\mu\text{A}$) combined with external resistor $R1/R2$ generates extra hysteresis and threshold.

For example, if $R1 = 3.3\text{k}\Omega$ and $R2 = 500\text{k}\Omega$, there is 10mV extra hysteresis and 1.5V extra threshold.

If the setup is as "Application Circuit with Customized External Threshold and Hysteresis", the total hysteresis is 10mV plus internal value and the threshold is 1.5V .

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX40070ANA16+T	-40°C to +125°C	8 WLP
MAX40072ATA16+T*	-40°C to +125°C	8 TDFN

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

*Future product—contact factory for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/22	Release for Market Intro	—