TEXAS INSTRUMENTS

TPD2E009

SLVS953B – JUNE 2009 – REVISED AUGUST 2015

TPD2E009 2-Channel ESD Solution for High-Speed (6-Gbps) Differential Interface

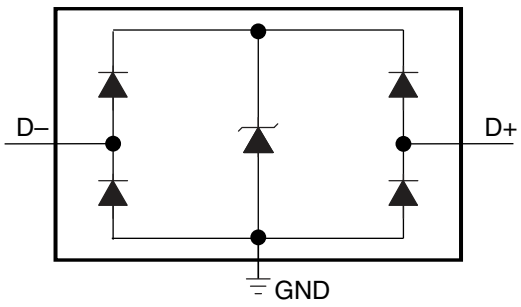
1 Features

- Supports Data Rates up to 6 Gbps
- IEC 61000-4-2 ESD Protection
  - ±8-kV Contact Discharge
  - ±8-kV Air-Gap Discharge
- IEC 61000-4-5 Surge Protection
  - 5 A (8/20 µs)
- Low Capacitance
  - DRT: 0.7-pF (Typ)
  - DBZ: 0.9-pF (Typ)
- 0.05-pF Matching Capacitance Between the Differential Signal Pair
- Dual-Matching TVS Diodes to Protect the Differential Data and Clock Lines of HDMI, LVDS, SATA, Ethernet, or USB Interfaces
- Space-Saving DRT and DBZ Package Options
- Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing the ESD-Protection Chip Near the Connector

2 Applications

- End Equipment:
  - Notebooks
  - Set-Top Boxes
  - Portable Computers
  - DVD Players
  - Media Players
- Interfaces:
  - HDMI 2.0
  - USB 3.0
  - eSATA
  - Ethernet

TPD2E009 Circuit



3 Description

The TPD2E009 device provides two ESD protection diodes with flow-through pin mapping for ease of board layout. This device has been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. The TPD2E009 offers transient voltage suppression for Level 4 of IEC 61000-4-2 Contact ESD protection. TVS protection up to a 5-A (8/20 µs) peak pulse-current rating per the IEC 61000-4-5 (lightning) specification is also provided.

The monolithic silicon technology allows matching between the differential signal pairs. The less than 0.05-pF differential capacitance ensures that the differential signal distortion due to added ESD circuit protection remains minimal. The low capacitance (0.7-pF) is suitable for high-speed data rates up to 6 Gbps.

The TPD2E009 TVS diode is offered in a DRT (1 mm × 0.8 mm) package for space-saving portable applications. The industry standard DBZ (2.92 mm × 1.3 mm) package offers additional flexibility in the board layout for the system designer.

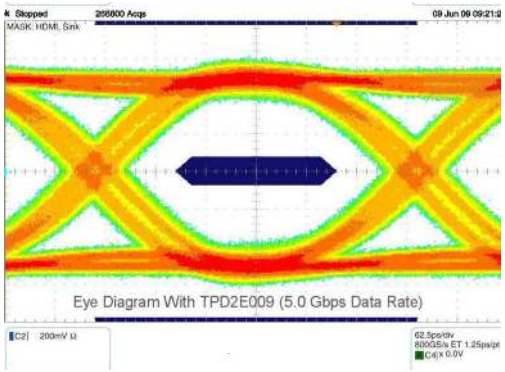
Typical applications for the TPD2E009 line of ESD protection products are: HDMI, USB, eSATA, and ethernet interfaces in notebooks, DVD and media players, set-top boxes, and portable computers.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2E009	SOT (3)	2.92 mm × 1.30 mm
		1.00 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPD2E009 Application Curve



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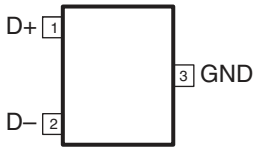
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2009) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DBZ, DRT Packages
3-Pin SOT
TOP VIEW



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D+	1	ESD port	High-speed ESD clamp provides ESD protection to the high-speed differential data lines
D–	2		
GND	3	GND	Ground

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating temperature		–40	85	°C
I/O voltage tolerance	D+, D– pins	0	6	V
Peak pulse current (t_p = 8/20 µs)			5	A
Peak pulse power (t_p = 8/20 µs)			45	W
Storage temperature, T_{stg}		–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±15000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
	IEC 61000-4-2 contact discharge	D+, D– pins	±8000	
	IEC 61000-4-2 air-gap discharge	D+, D– pins	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		–40		85	°C
Operating voltage	Pin 1 or 2 to 3 or Pin 3 to 1 or 2	0		5.5	V

6.4 Thermal Information

THERMAL METRIC[1]		TPD2E009		UNIT
		DBZ (SOT)	DRT (SOT)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	461.8	610	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	216.2	288	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	195.6	118.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70.1	20.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	193.7	116.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	D+, D– pins to ground				5.5	V
V_{CLAMP}	Clamp voltage	D+, D– pins to ground,	I_{IO} = 1 A			8	V
I_{IO}	Current from I/O port to supply pins	V_{IO} = 2.5 V			0.01	0.1	µA
V_D	Diode forward voltage	D+, D– pins, lower clamp diode,	V_{IO} = 2.5 V, I_D = 8 mA	0.6	0.8	0.95	V
		D+, D– pins, upper clamp diode, DRY package	V_{CC} = 0 V, I_D = –8 mA	0.6	0.8	0.95	
R_{DYN}	Dynamic resistance	D+, D– pins,	I = 1 A		1		Ω
C_{IO}	I/O capacitance	D+, D– pins, DBZ Package	V_{IO} = 2.5 V, *f* = 10 MHz		0.9		pF
		D+, D– pins, DRT Package	V_{IO} = 2.5 V, *f* = 10 MHz		0.7		pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA		7			V

6.6 Typical Characteristics

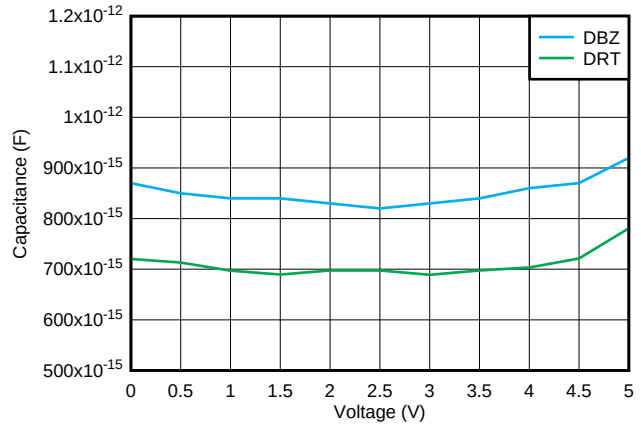


Figure 1. I/O Capacitance vs I/O Voltage (T_A= 25°C)

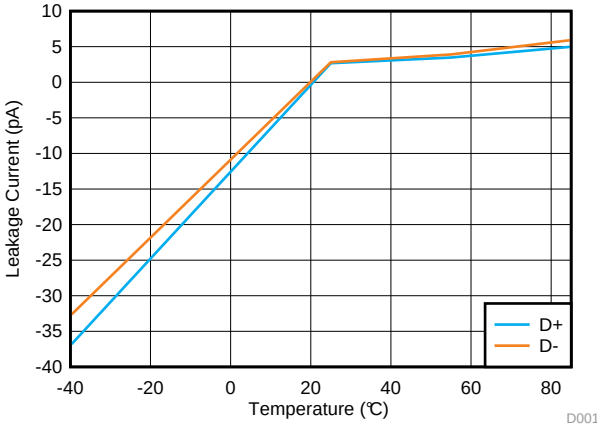


Figure 2. Leakage Current vs Temperature (V_{IO} = 2.5 V)

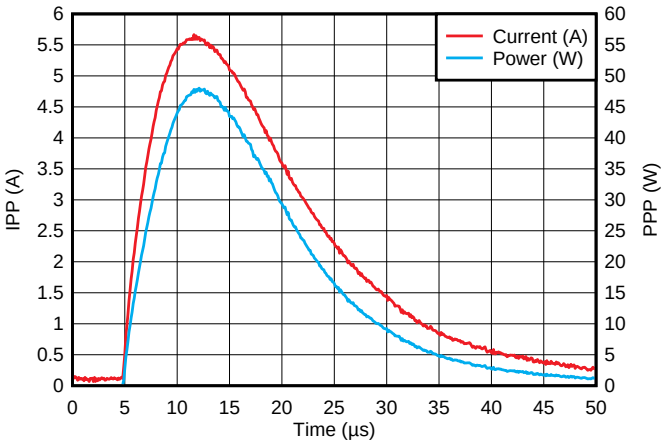


Figure 3. Peak Pulse Waveforms, (Measured at One I/O, With the Other I/O Open)

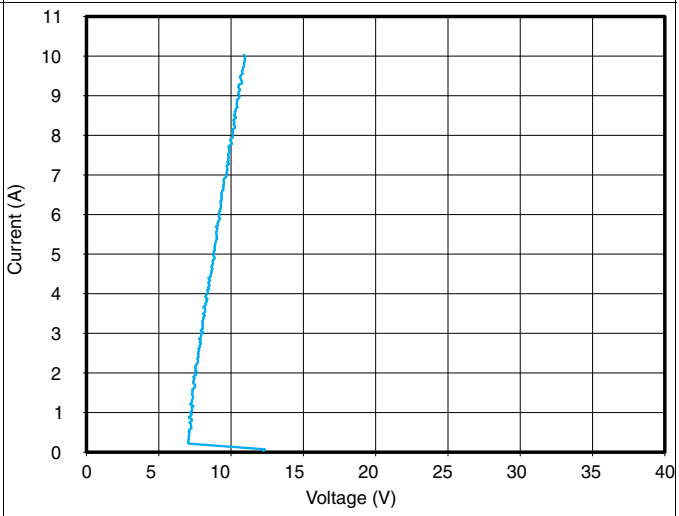


Figure 4. D+, D– Transmission Line Pulser Plot (100-ns Pulse, 10-ns Rise Time)

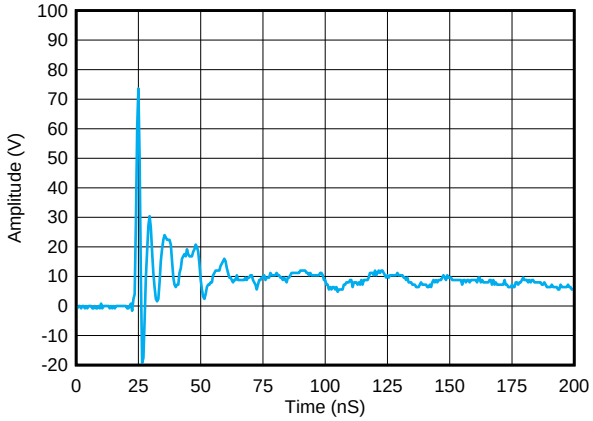


Figure 5. IEC Clamping Waveforms (8-kV Contact)

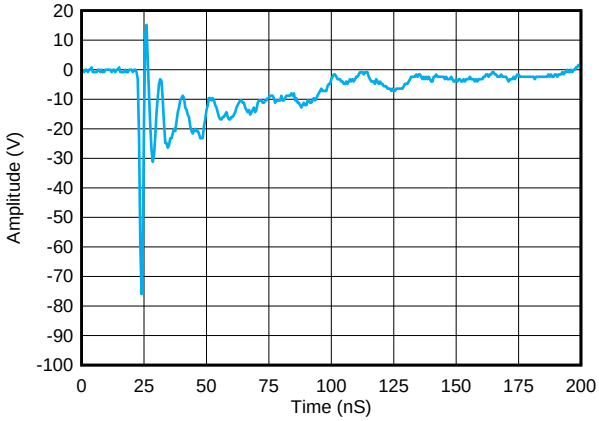


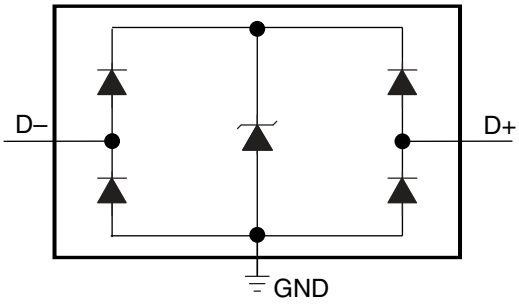
Figure 6. IEC Clamping Waveforms (–8-kV Contact)

7 Detailed Description

7.1 Overview

TPD2E009 is a two-channel ESD TVS that provides ±8-kV IEC 61000-4-2 contact and air-gap ESD protection. The 0.7-pF unidirectional diode architecture is suitable for signals that range from 0 V to 5.5 V and can support data rates up to 6 Gbps. The industry-standard packages are convenient for placement in applications with limited space.

7.2 Functional Block Diagram



7.3 Feature Description

TPD2E009 is a unidirectional TVS offering IEC 61000-4-2 Level 4 Contact ESD protection. This device protects circuits from ESD strikes up to ±8-kV contact and ±8-kV air-gap. The device can also handle up to 5-A surge current (IEC 61000-4-5 8/20 µs). The low capacitance of 0.7 pF supports a data rate up to 6 Gbps. TPD2E009 has a small dynamic resistance of 1 Ω, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 8 V when the device is taking a 1-A transient current. Low leakage allows the diode to conserve power when working below the V_{RWM}.

7.4 Device Functional Modes

The TPD2E009 device is a passive clamp that has low leakage during normal operation when the voltage between an I/O pin and GND is below V_{RWM}. The device activates when the voltage is between an I/O pin and GND goes above V_{BR}. During ESD events, transient voltages as high as ±8 kV can be clamped between the protected line and ground. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low-leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD2E009 device is a diode-array type TVS typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human-interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

The TPD2E009 device is typically used to protect a single high-speed differential pair. Multiple TPD2E009 devices can be used to provide protection for connectors with multiple differential data lanes. This example is applicable to many interface types including:

- HDMI
- USB
- eSATA
- ethernet interfaces

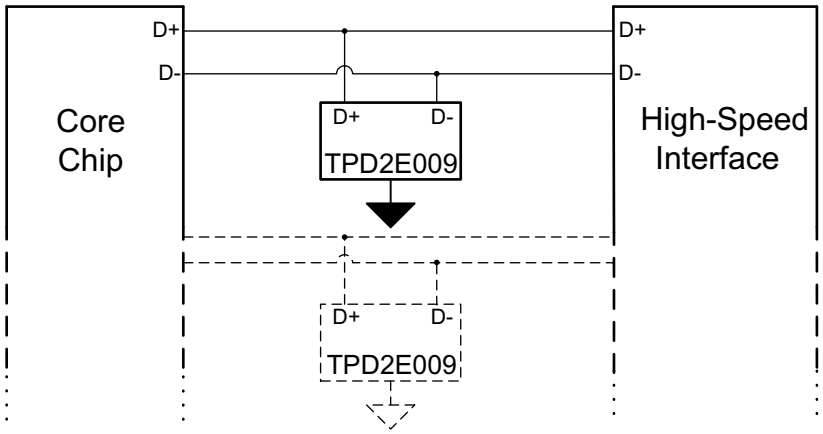


Figure 7. TPD2E009 in a High-Speed Interface

8.2.1 Design Requirements

For this design example, TPD2E009 is used to protect any differential data pair meeting the design requirements shown in the following table.

DESIGN PARAMETER	VALUE
Maximum signal range on D+ and D–	0 V to 5.5 V
Maximum Operating Frequency	3 GHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must know the following:

- The signal voltage range on the protected lines
- The maximum operating frequency

8.2.3 Application Curves

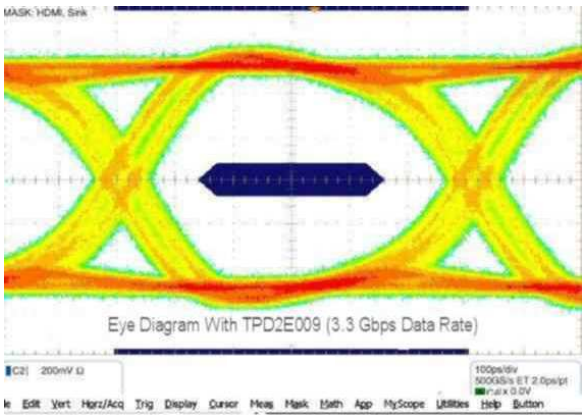


Figure 8. Eye Diagram With TPD2E009 (3.3-Gbps Data Rate) (3-Pin DBZ Package)

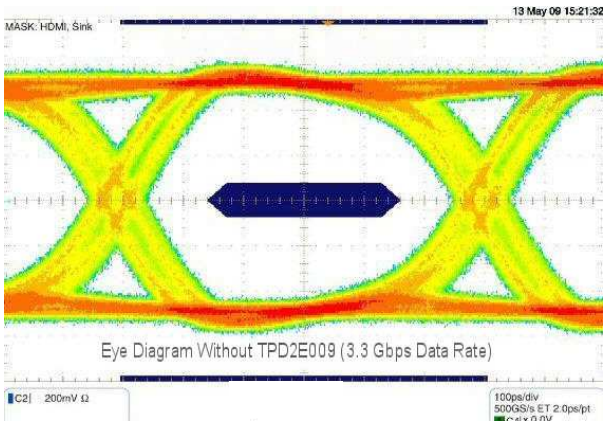


Figure 9. Eye Diagram Without TPD2E009 (3.3-Gbps Data Rate) (3-Pin DBZ Package)

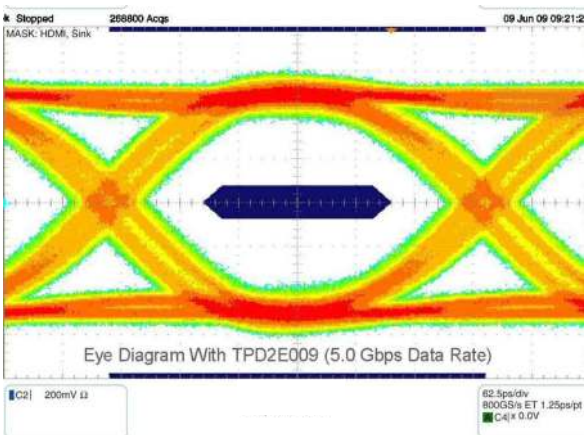


Figure 10. Eye Diagram With TPD2E009 (5-Gbps Data Rate) (3-Pin DBZ Package)

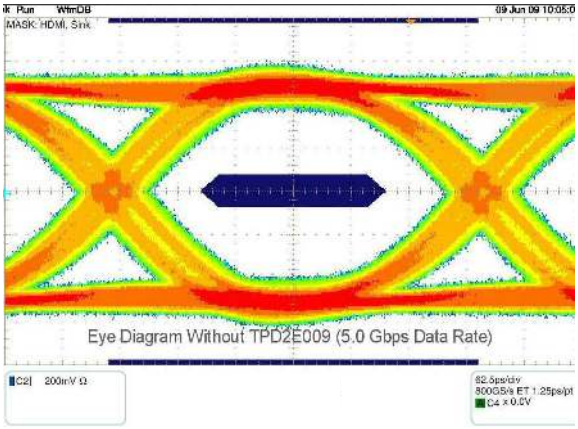


Figure 11. Eye Diagram Without TPD2E009 (5-Gbps Data Rate) (3-Pin DBZ Package)

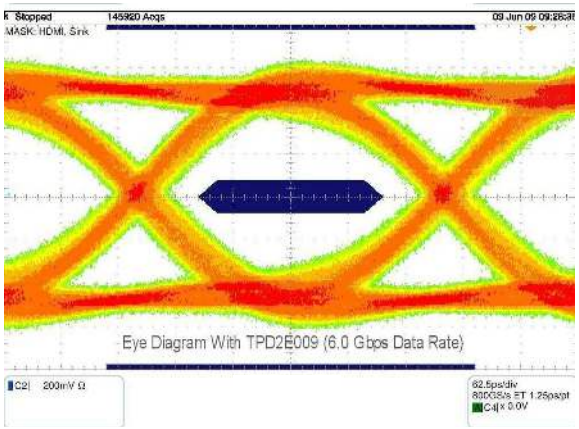


Figure 12. Eye Diagram With TPD2E009 (6-Gbps Data Rate) (3-Pin DBZ Package)

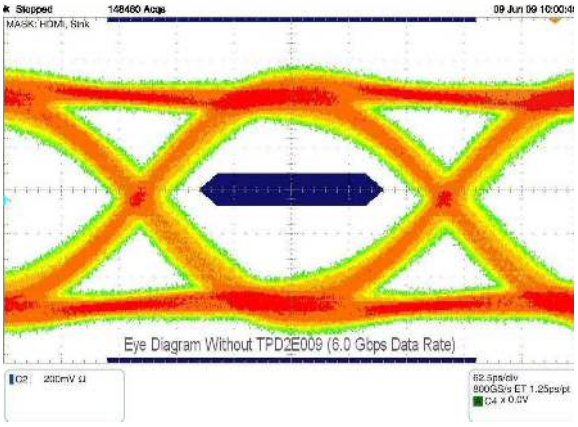


Figure 13. Eye Diagram Without TPD2E009 (6-Gbps Data Rate) (3-Pin DBZ Package)

9 Power Supply Recommendations

The TPD2E009 device is a passive ESD-protection device, and therefore, does not require a power supply. Care must be taken to avoid violating the maximum-voltage specification to ensure that the device functions properly. The D+ and D– lines share a TVS diode that can tolerate up to 5.5 V.

10 Layout

10.1 Layout Guidelines

Layout considerations such as package selection, trace routing, and so forth, must be accounted for while designing the ESD clamp circuit for a high-speed interface. Difficult routing can lead the designer to use vias or stubs in the board traces, which creates significant disruption in the line impedance in the high-speed signal path. Poor package choice can force the designer to route differential traces with unequal lengths and add the skew in the signals. TI recommends coupling the differential traces closely to reduce the EMI interference.

The TPD2E009 can provide system-level ESD protection to the high-speed differential ports (up to 6-Gbps data rate). The flow-through package offers flexibility for board routing with traces up to 15 mils (0.38 mm) wide. Figure 14 and Figure 15 show the board layout scheme for the D+ and D– lines of a single differential pair, which allows the differential signal pairs to couple together right after they touch the ESD ports (pin 1 and pin 2) of the TPD2E009.

10.2 Layout Examples

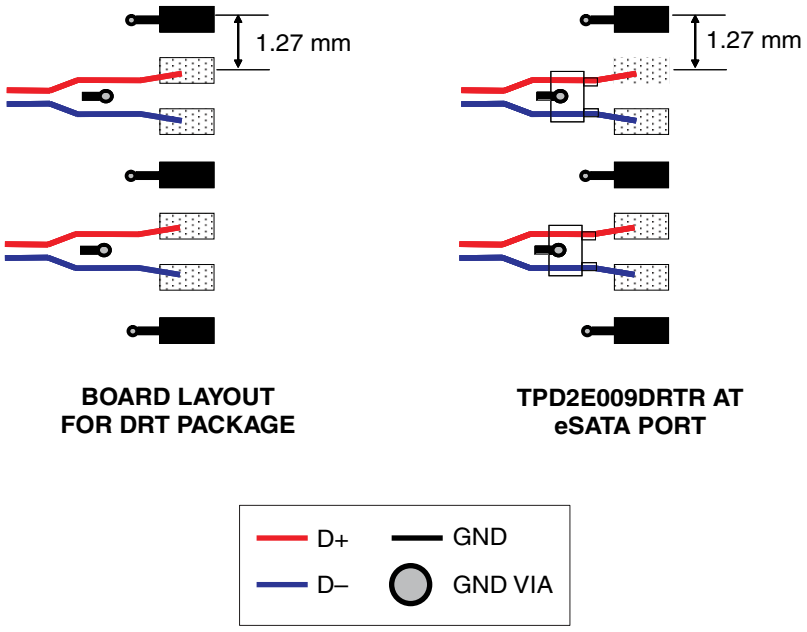


Figure 14. TPD2E009DRTR at eSATA Connector Interface

Layout Examples (continued)

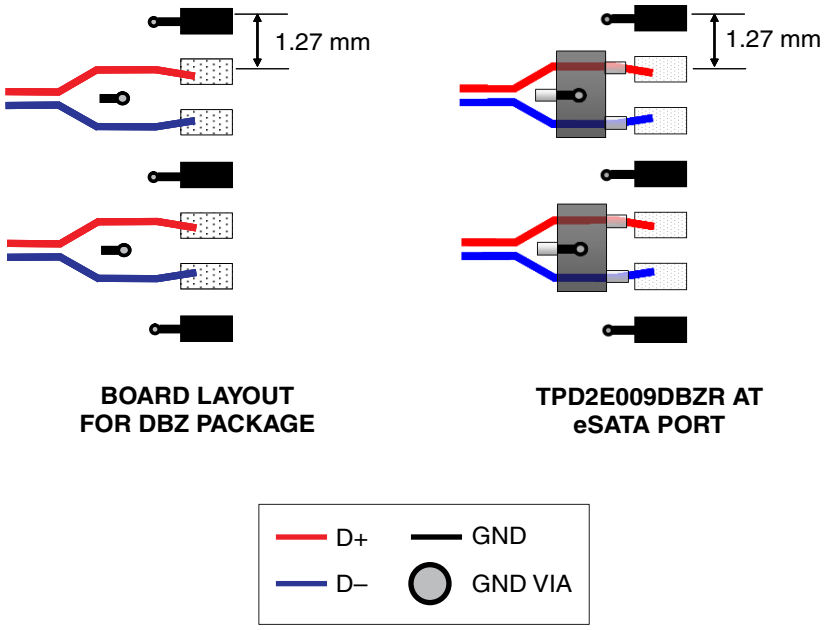


Figure 15. TPD2E009DBZR at eSATA Connector Interface

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E009DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(NFLO, NFLR)	Samples
TPD2E009DRTR	ACTIVE	SOT-9X3	DRT	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

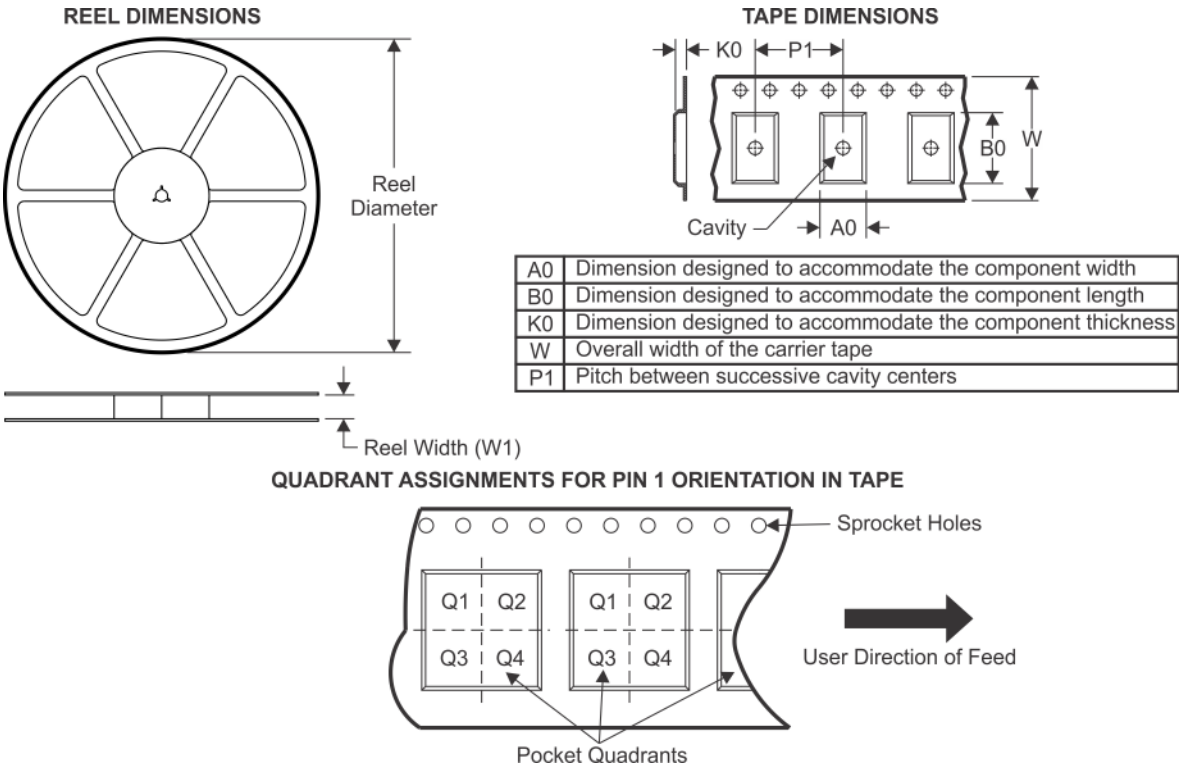
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

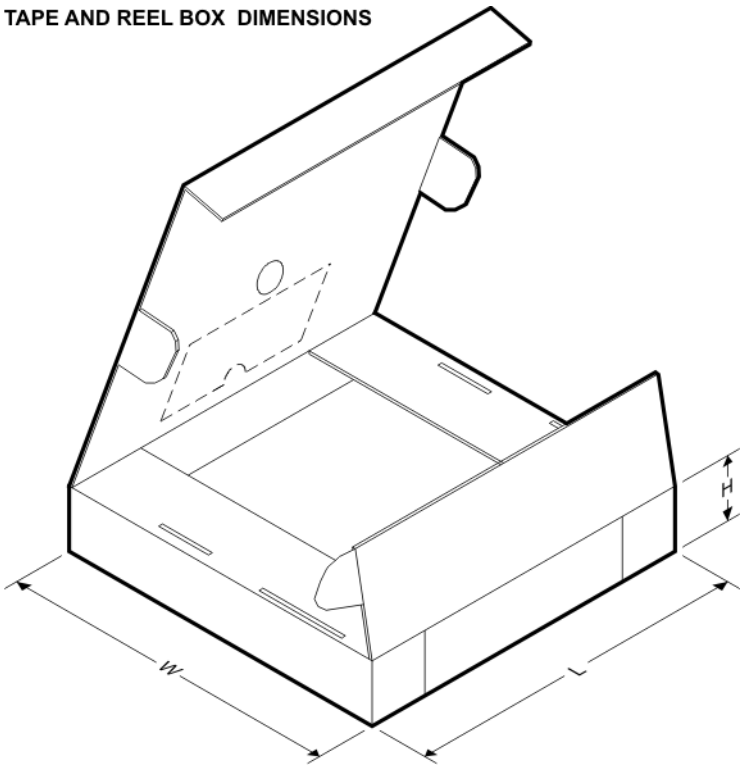


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E009DBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TPD2E009DRTR	SOT-9X3	DRT	3	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

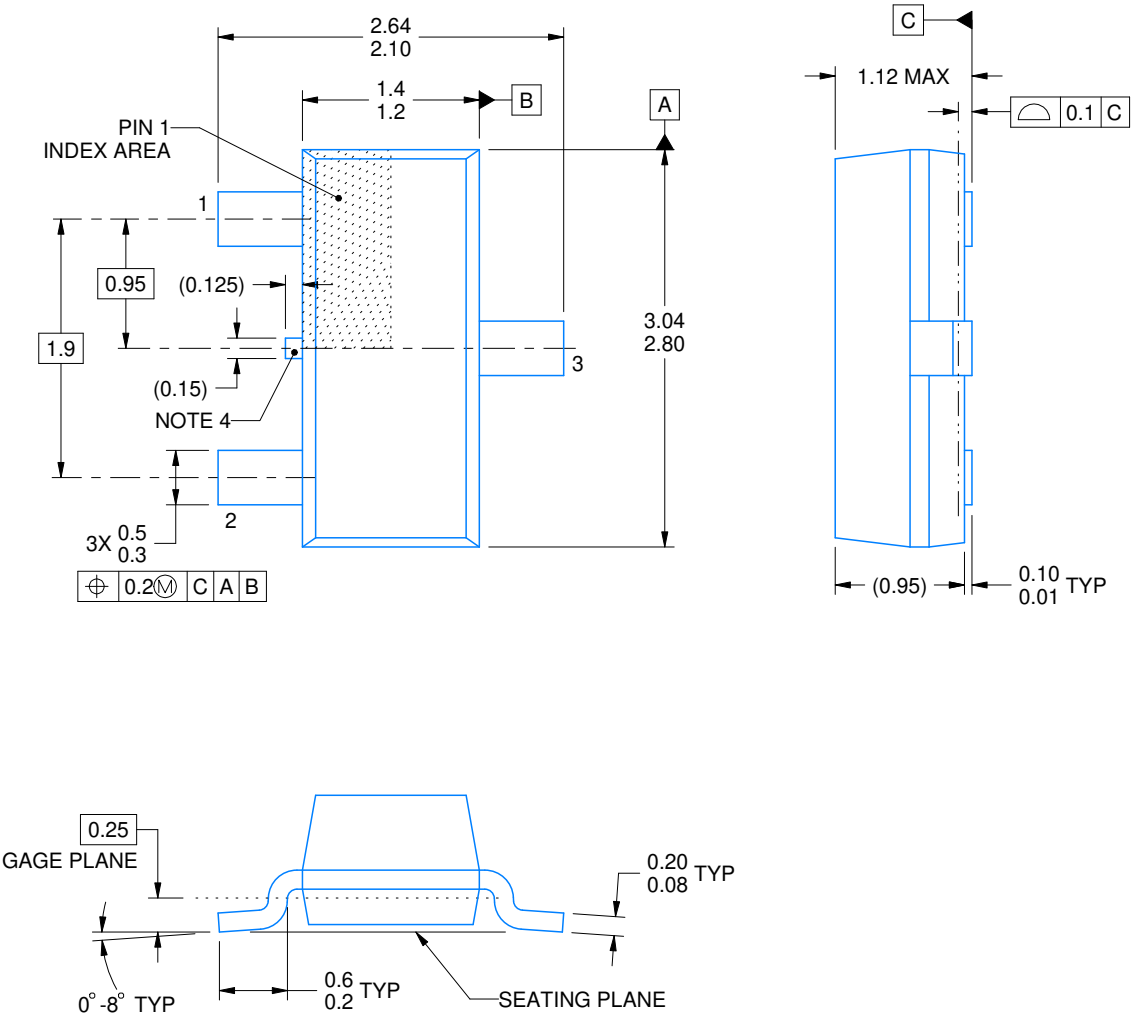
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E009DBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TPD2E009DRTR	SOT-9X3	DRT	3	3000	202.0	201.0	85.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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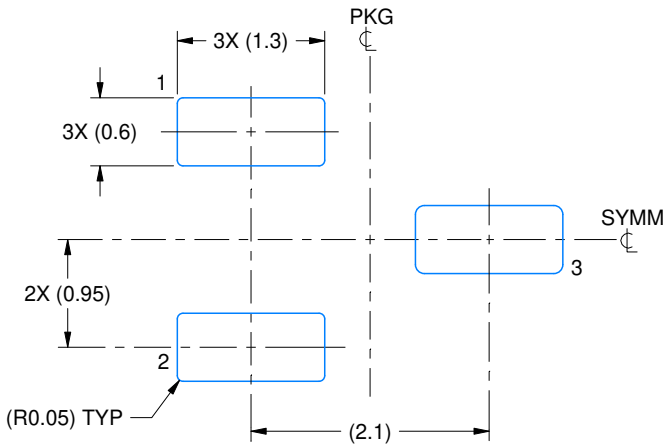
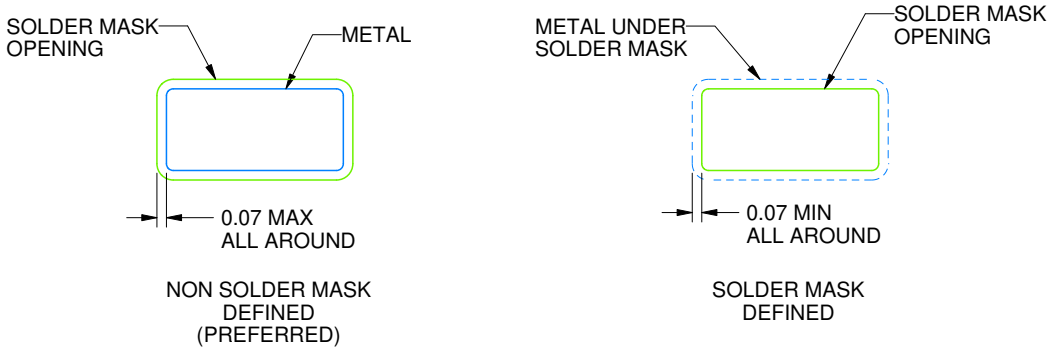
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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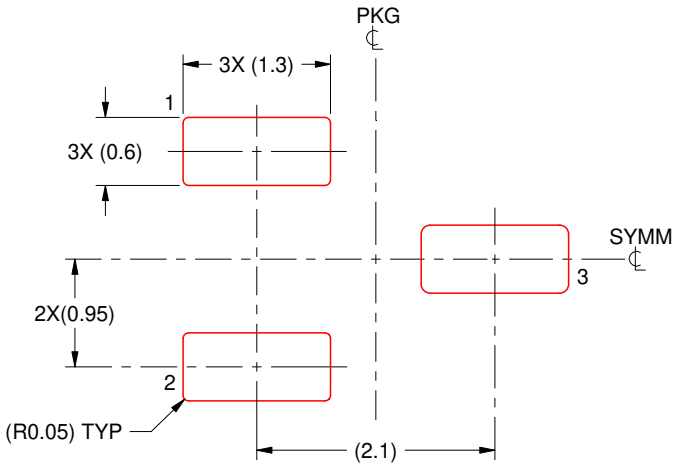
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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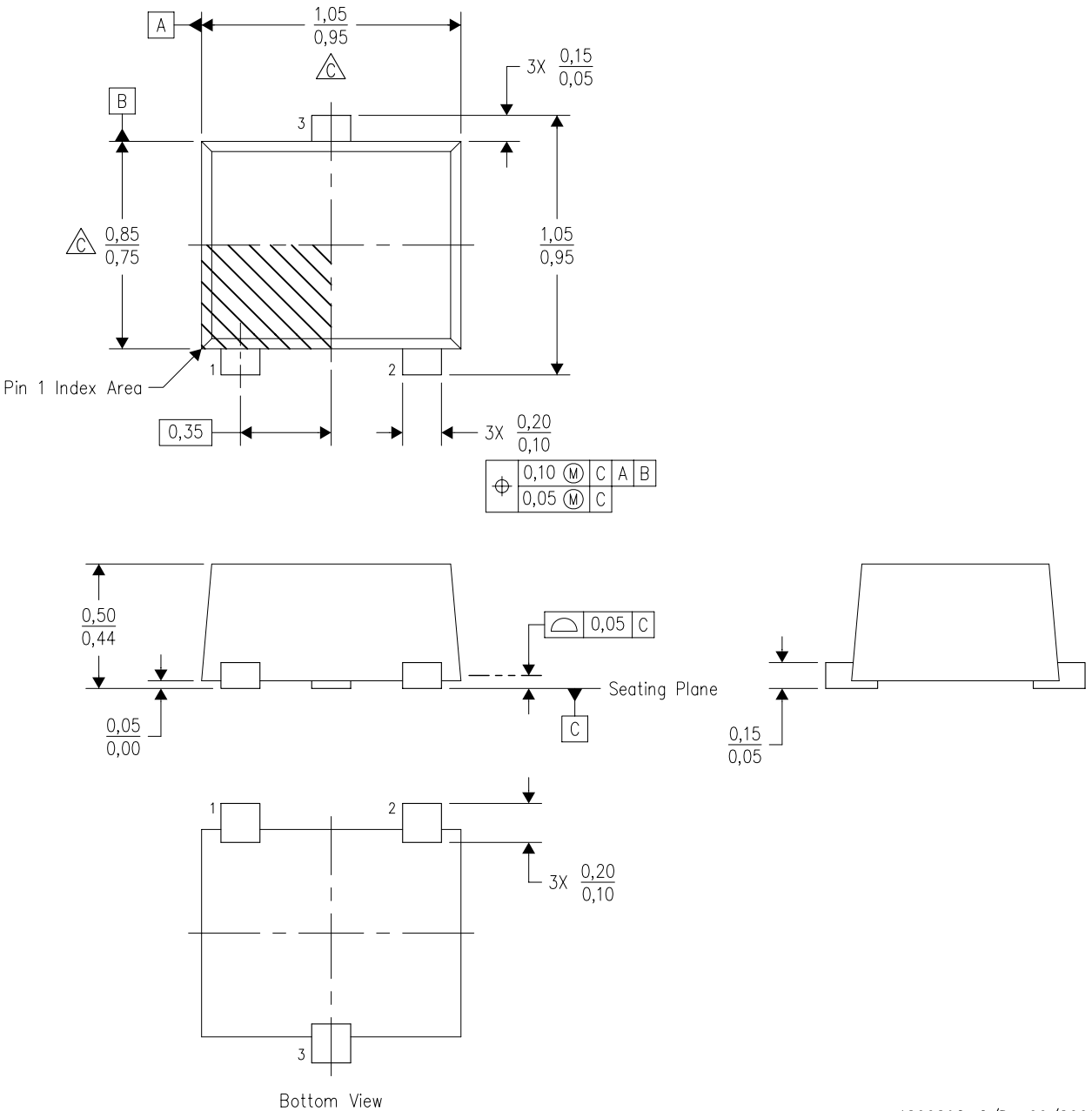
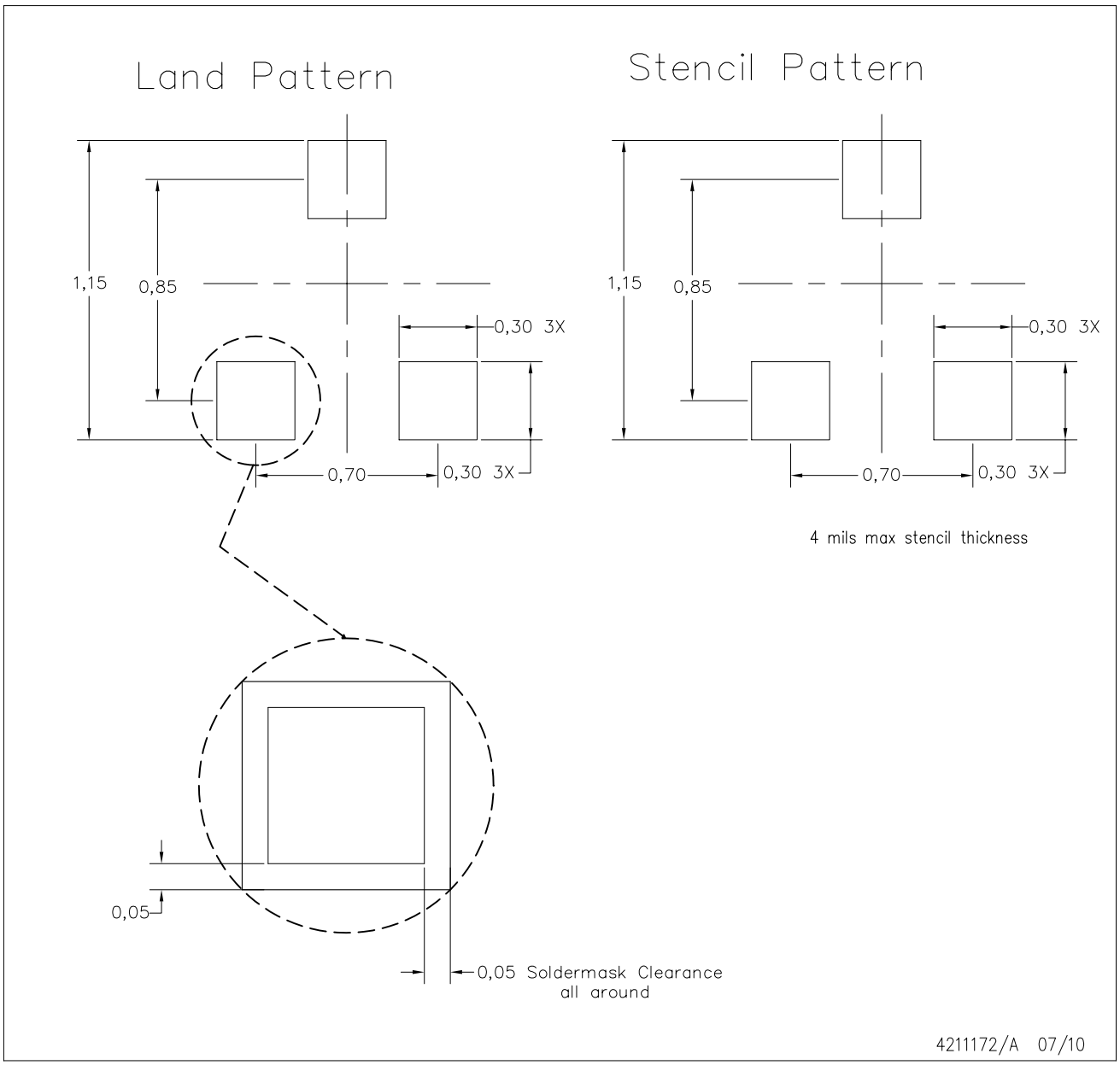
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
D. JEDEC package registration is pending.

DRT (S–PDSO–N3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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