CDB42324

Evaluation Board for CS42324

Features

- 2 Vrms Single-Ended Analog Inputs
- 2 Vrms Single-Ended Analog Outputs
- CS8406 S/PDIF Digital Audio Transmitter
- CS8416 S/PDIF Digital Audio Receiver
- Independent ADC and DAC Clock Domains
- Header for Optional External Software Configuration of CS42324
- Header for External PCM Serial Audio I/O
- 3.3 V Logic Interface
- Pre-Defined Software Scripts
- Demonstrates Recommended Layout and Grounding Arrangements
- Windows® Compatible Software Interface to Configure CS42324 and Intra-board Connections

Description

The CDB42324 evaluation board is an excellent means for evaluating the CS42324 CODEC. Evaluation requires an analog signal source and analyzer and power supplies. A Windows PC-compatible computer must be used to evaluate the CS42324.

System timing for the I²S and Left-Justified interface formats can be provided by the CS42324, the CS8416, the CS8406, or by a PCM I/O stake header with an external source connected.

RCA phono jacks are provided for the CS42324 analog inputs and outputs. Digital data I/O is available via RCA phono or optical connectors to the CS8416 and CS8406.

The Windows software provides a GUI to make configuration of the CDB42324 easy. The software communicates through the PC's USB port to configure the control port registers so that features of the CS42324 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB42324	Evaluation Board

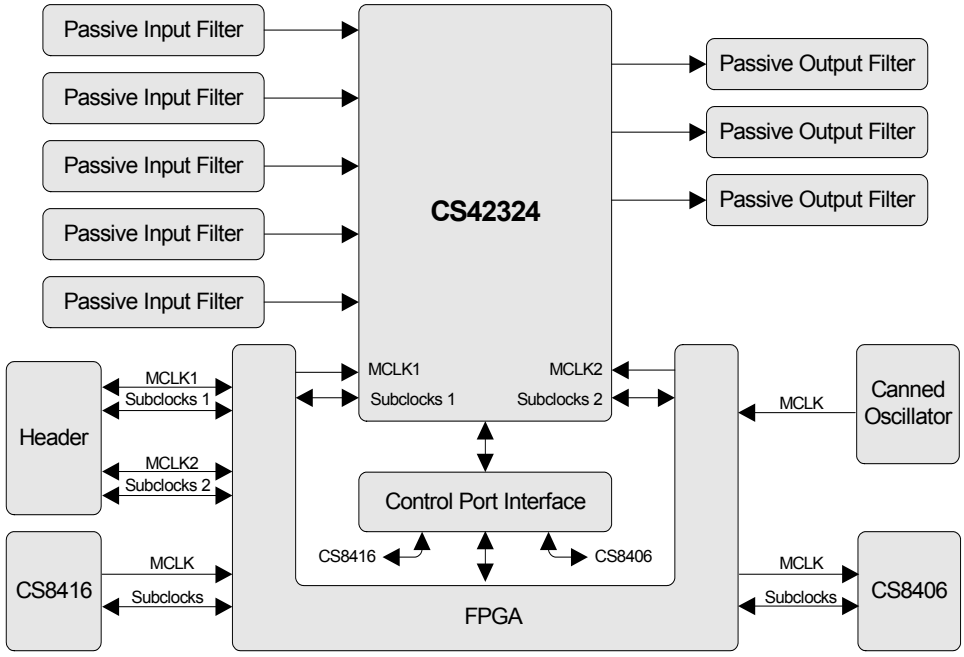

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. SYSTEM OVERVIEW

The CDB42324 evaluation board is an excellent means for evaluating the CS42324 CODEC. Analog and digital audio signal interfaces are provided, an on-board FPGA is used for easily configuring the evaluation platform, and a USB cable is included for use with the supplied Windows configuration software.
The CDB42324 schematic set is shown in Figures 5 through 11.

1.1 Power

Power must be supplied to the evaluation board through the Yellow +9.0 V to +12.0 V binding post. On-board regulators provide 5 V, 3.3 V, and 1.8 V supplies. All voltage inputs must be referenced to the single black binding post ground connector (Table 8).

WARNING: Please refer to the CS42324 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS42324 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 5 provides an overview of the connections to the CS42324. Figure 12 shows the component placement. Figure 14 shows the top layout. Figure 15 shows the bottom layout. The decoupling capacitors are located as close to the CS42324 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 CS42324 Audio CODEC

A complete description of the CS42324 is included in the CS42324 product data sheet.

The required configuration settings of the CS42324 are made in its control port registers, accessible through the CS42324 tabs of the Cirrus Logic FlexGUI software.

Clock and data source selections are made through the control port of the FPGA. Basic routing selections can be made using the Board Setup tab in the GUI software application. Advanced options are accessible through the Board Configuration sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software. See Section 6. FPGA Register Description for complete information.

1.4 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter (Figure 9) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS42324 to the standard S/PDIF data stream. The CS8406 can operate in either master or slave mode, accepts 128 Fs, 256 Fs, 384 Fs, and 512 Fs master clocks on the OMCK input pin, and can operate in the Left-Justified, I²S, Right-Justified 16-bit, and Right-Justified 24-bit interface formats.

The most common operations of the CS8406 may be controlled via the Board Setup tab in the GUI software application. Advanced options are accessible through the CS8406 sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software.

1.5 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 9) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data for the CS42324 and operates in master or slave mode, generating either a 128 Fs or 256 Fs master clock on the RMCK output pin, and can operate in the Left-Justified, I²S, Right-Justified 16-bit, and Right-Justified 24-bit interface formats.

The most common operations of the CS8416 may be controlled via the Board Setup tab in the GUI software application. Advanced options are accessible through the CS8416 sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software.

1.6 FPGA

The FPGA handles both clock and data routing on the CDB42324. Clock and data routing selections made via the Board Setup tab in the GUI will be handled by the FPGA with no user intervention required. For advanced information regarding the internal registers and operation of the FPGA, see Sections 5 and 6.

1.7 Canned Oscillator

A canned oscillator, Y6, is available to provide a master clock source to the CDB42324.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The board is shipped with a 12.2880 MHz crystal oscillator populated.

1.8 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J1 and J46.

The 20-pin, 2 row header, J1, provides access to the serial audio signals required to interface Serial Audio Port 1 and Port 2 of the CS42324 with a DSP (see Figure 8).

The direction of the signals on header J1 can be configured using the controls located within the Board Setup tab in the provided GUI software.

The 15-pin, 3 row header, J46, allows the user bidirectional access to the SPI™/I²C® control signals by simply removing all the shunt jumpers from the “INT” position. The user may then choose to connect a ribbon cable to the “EXT” position. A single “GND” row for the ribbon cable’s ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I²C power rail.

1.9 Analog Inputs

RCA connectors supply the CS42324 analog inputs through single-ended, unity gain, passive circuits. Refer to the CS42324 data sheet for the ADC full-scale level.

1.10 Analog Outputs

The CS42324 DAC analog outputs are routed through a single-pole passive RC filter. The output of the filter is connected to RCA jacks for easy evaluation.

1.11 Muting

The CDB42324 incorporates optional off-chip muting circuitry to complement the CS42324's mute control pins. There are 2-pin headers by each analog output jack which correspond to the mute for each channel. These headers allow a disconnection point for evaluation of the analog output without the mute circuitry attached to the signal.

1.12 USB Control Port

A graphical user interface is included with the CDB42324 to allow easy manipulation of the registers in the CS42324, CS8416, CS8406, and FPGA. See the device-specific data sheets for the CS42324, CS8416, and CD8406 internal register descriptions. The internal register map for the FPGA is located in Section 5.

Connecting a cable to the USB connector (J44) and launching the Cirrus Logic FlexGUI software (FlexLoader.exe) will enable the CDB42324.

Refer to PC Software Control for a description of the Graphical User Interface (GUI).

2. SYSTEM CLOCKING

The CDB42324 implements two discrete clocking domains. One discrete domain services Serial Audio Port 1 of the CS42324, and the other discrete domain services Serial Audio Port 2 of the CS42324. The two clock domains may operate independently, or may be tied together. Configuration of the clocking domains is achieved using the controls within the Board Setup tab in the GUI software application.

2.1 Clock Domain 1

Clock Domain 1 comprises Serial Audio Port 1 of the CS42324.

The master clock signal (MCLK1) may be sourced from Oscillator (Y6), Pin 2 of the CLK & DATA I/O header (J1), or from the CS8416 RMCK pin (PLL recovered clock from the S/PDIF input).

The sub-clock signals (SCLK1 and LRCK1) may be sourced from the CS42324 in Master Mode, from the CS8406 in Master Mode, from pins 3 through 6 of the CLK & DATA I/O header (J1 - pins 3 and 4 for SCLK1, pins 4 and 5 for LRCK1), or from the CS8416 in Master Mode.

Configuration of Clock Domain 1 is achieved using the MCLK 1 Source and Subclock 1 Source controls within the Clock Source Select group box on the Board Setup tab in the GUI software application.

2.2 Clock Domain 2

Clock Domain 2 comprises Serial Audio Port 2 of the CS42324.

The master clock signal (MCLK2) may be sourced from Oscillator (Y6), Pin 10 of the CLK & DATA I/O header (J1), from the CS8416 RMCK pin (PLL recovered clock from the S/PDIF input), or it can be left disabled.

The sub-clock signals (SCLK2 and LRCK2) may be sourced from the CS42324 in Master Mode, from the CS8406 in Master Mode, from pins 11 through 14 of the CLK & DATA I/O header (J1 - pins 11 and 12 for SCLK2, pins 13 and 14 for LRCK2), from the CS8416 in Master Mode, or it can be left disabled.

Configuration of Clock Domain 2 is achieved using the MCLK 2 Source and Subclock 2 Source controls within the Clock Source Select group box on the Board Setup tab in the GUI software application.

3. SYSTEM DATA ROUTING

The CDB42324 implements comprehensive data routing capabilities. The SDIN1 and SDIN2 source for the CS42324, the CS8406 SDIN, and the SDOUT on the CLK & DATA I/O header (J1) may be easily selected using the provided GUI software application.

The CS8416 S/PDIF receiver, the SDIN1 and SDIN2 on the CLK & DATA I/O header (J1), or the CS42324 serial data output (SDOUT) may source the serial data. Configuration of the sources are achieved using the drop-down menus in the Data Source Select group box on the Board Setup tab in the GUI software application.

4. PC SOFTWARE CONTROL

A Microsoft Windows-based graphical user interface which allows software control over the CDB42324 is available for download from http://www.cirrus.com/msasoftware. Specifically, this software provides high and low level control over the CS42324, CS8416, CS8406, and FPGA. The board control software communicates with the CDB42324 over the USB interface using the PC's USB port.

To use the board control software, please download a copy from http://www.cirrus.com/msasoftware and follow the installation instructions which are provided from that Website. Once the USB cable has been connected between the CDB42324 and the host PC, load FlexLoader.exe from the Cirrus Logic directory. When the software loads, all devices will be reset to their default reset state.

The GUI's File menu provides the ability to save and load script files containing all of the register settings. Pre-configured script files are provided for basic functionality. Refer to Preconfigured Script Files for details.

4.1 CS42324 System Controls Tab

The CS42324 System Controls tab provides a high-level, intuitive interface to many of the configuration options of the CS42324 operational, port, interrupt, and system clocking controls. The controls on this tab (with the exception of the AD0 and AD1 controls) control the internal registers of the CS42324. Care must be taken to set up the FPGA to use the complimentary mode (master/slave, etc.) in the Board Setup Tab.

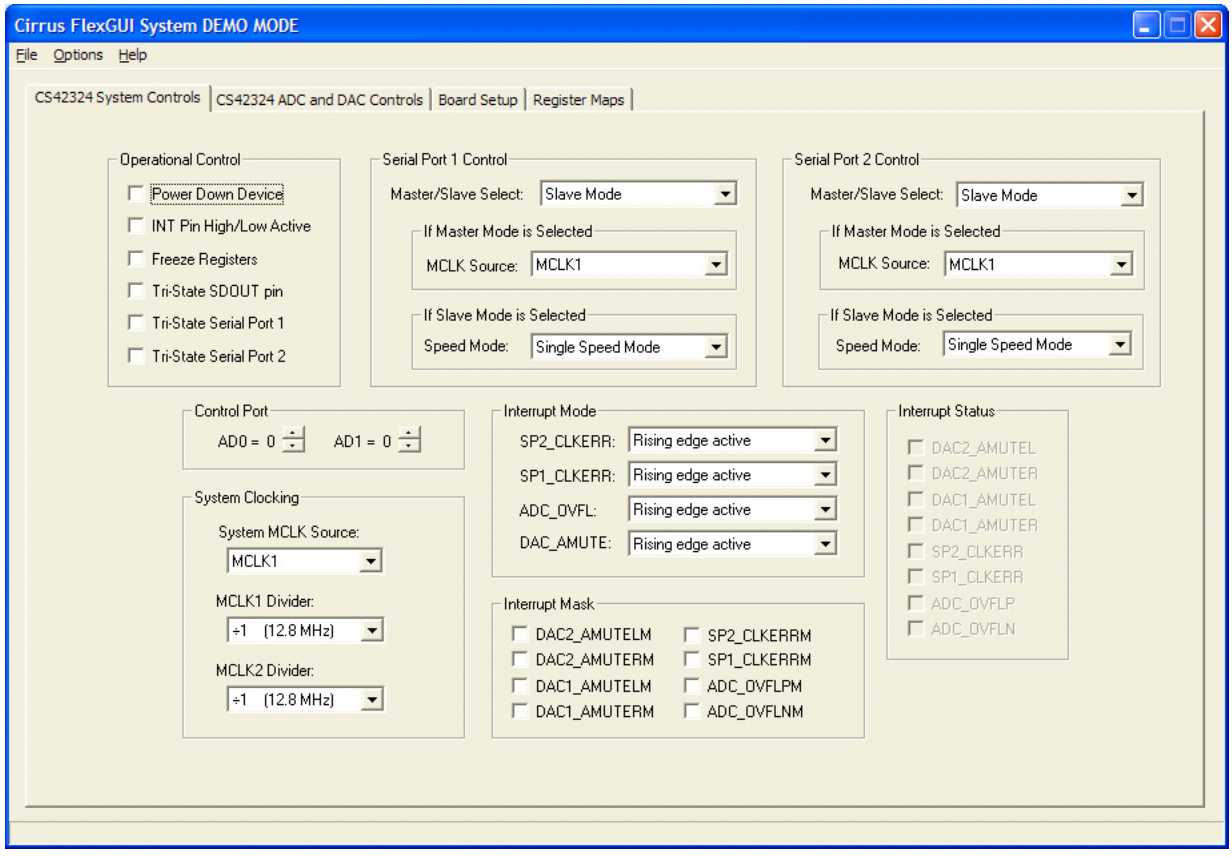

Figure 1. CS42324 System Controls Tab

4.2 CS42324 ADC and DAC Controls Tab

The CS42324 ADC and DAC Controls tab provides a high-level, intuitive interface to many of the configuration options of the CS42324 ADC and DAC controls. The controls on this tab control the internal registers of the CS42324. Care must be taken to set up the FPGA to use the complimentary mode (master/slave, etc.) in the Board Setup Tab.

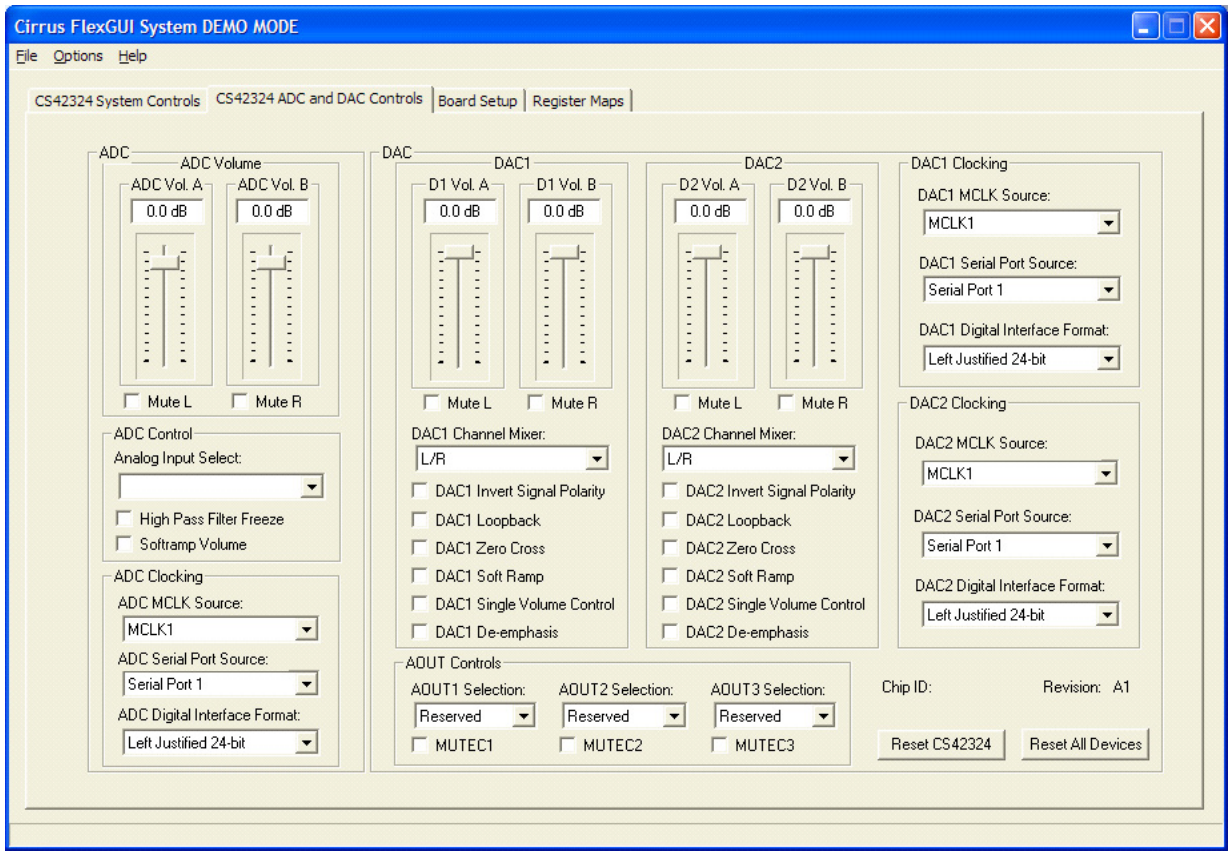

Figure 2. CS42324 ADC and DAC Controls Tab

4.3 Board Setup Tab

This tab sets up the clock and data routing on the FPGA as well as sets up the CS8416 and CS8406. When the CDB42324 is configured to make use of the CS8416 S/PDIF receiver or CS8406 S/PDIF transmitter, these devices must be configured for proper operation. The Board Setup tab provides a high-level, intuitive interface to the most common configuration options of the CS8416 and CS8406.

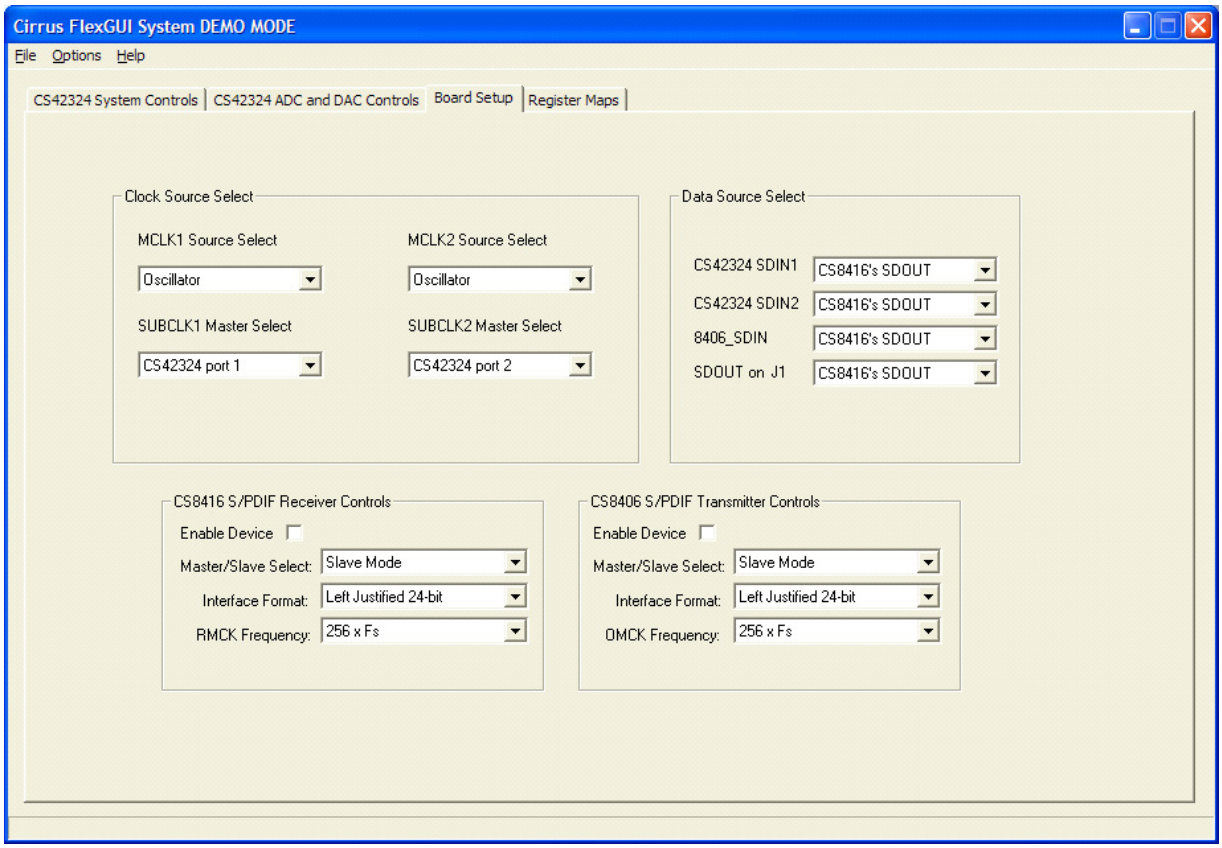

Figure 3. Board Setup Tab

4.4 Register Maps Tab

The Register Maps tab provides low level control over the register level settings of the CS42324, CS8416, CS8406, and FPGA. Each device is displayed on a separate tab. Register values can be modified bit-wise or byte-wise. For bit-wise changes, click the appropriate push button for the desired bit. For byte-wise changes, the desired hex value can be typed directly in the register address box in the register map.

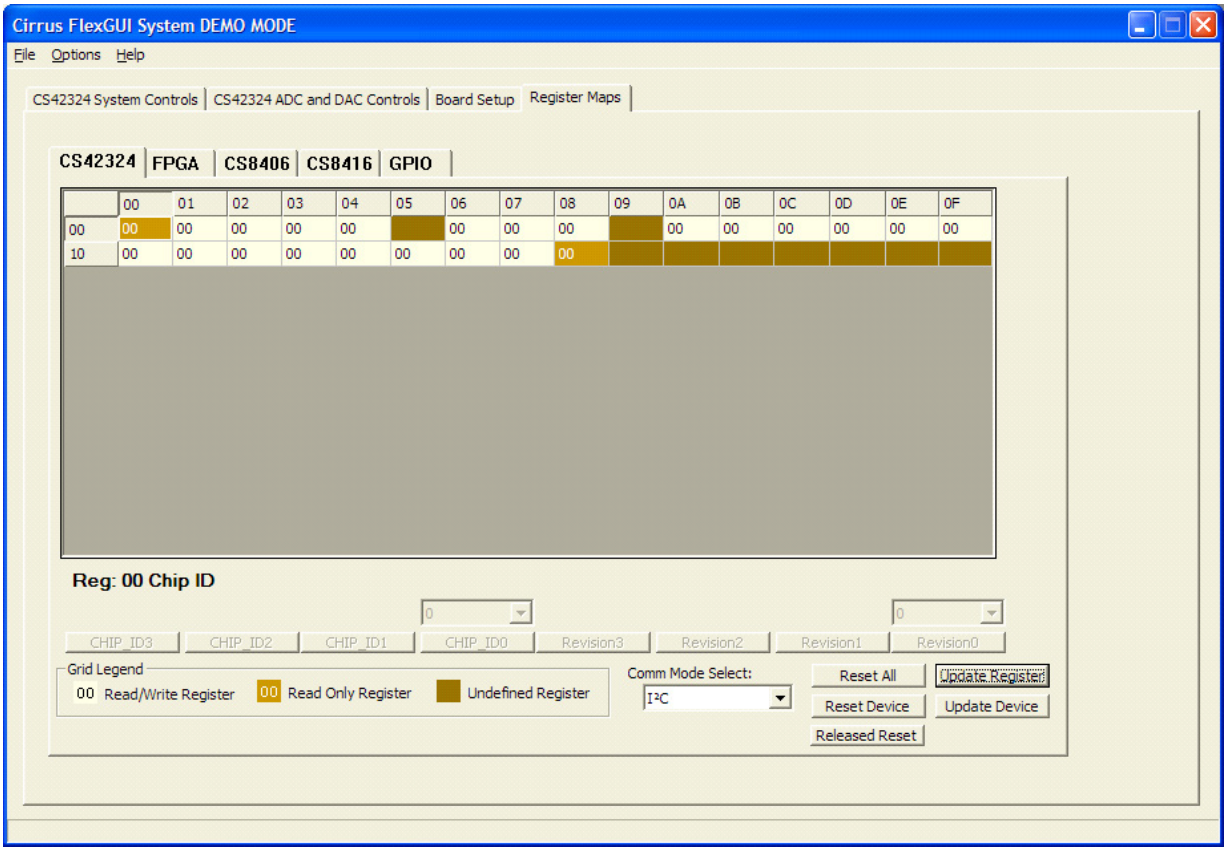

Figure 4. Register Maps Tab

4.5 Preconfigured Script Files

Preconfigured script files are provided with the CDB42324 to allow easy initial board bring-up. The board configurations stored within these files are described in Sections 4.5.1 and 4.5.2.

4.5.1 Oscillator Clock - ADC Ch 1 to DAC & SPDIF Out

Using the pre configured script file named “Oscillator Clock - ADC Ch 1 to DAC & SPDIF Out.txt”, an analog input signal applied to AIN1A/1B of the CS42324 input multiplexer will be digitized by the ADC, transmitted in S/PDIF format by the CS8406, digitally looped internally and converted to analog by the CS42324 DAC1 and 2 and output on AOUT1A/1B and AOUT2A/2B, while the analog signal on AIN1A/1B will be passed through to AOUT3A/3B with no digital conversion.

The CS42324 is in synchronous mode, with the oscillator as the source of MCLK for Clock Domain 1 and 2. The CS42324 Serial Audio Port 1 is the sub-clock master to the CS8406 and the CS42324 Serial Audio Port 2.

4.5.2 SPDIF Recovered Clock - SPDIF to DAC & ADC to SPDIF

Using the preconfigured script file named “SPDIF Recovered Clock - SPDIF to DAC & ADC to SPDIF.txt”, an analog input signal applied to AIN1A/1B of the CS42324 input multiplexer will be digitized by the ADC, transmitted in S/PDIF format by the CS8406. A S/PDIF signal input to the CS8416 will be converted to analog by the CS42324 DAC and output through the passive output filter and output on AOUT1A/1B, while the analog signal on AIN1A/1B will be passed through to AOUT3A/3B with no digital conversion. For proper operation of this script, a valid S/PDIF signal must be applied.

The CS42324 is in synchronous mode, with the CS8416 as the source of MCLK for Clock Domain 1 and 2. The CS8416 is the sub-clock master to both the CS42324 Serial Audio Port 1 and 2, as well as the CS8406.

5. FPGA REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Code Rev. ID	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0
R		x	x	x	x	x	x	x	x
02h	MCLK Source	Reserved	Reserved	MCLK2.1	MCLK2.0	Reserved	Reserved	MCLK1.1	MCLK1.0
R/W		0	0	0	0	0	0	0	0
03h	Subclock Source	Reserved	Reserved	SP2.1	SP2.0	Reserved	Reserved	SP1.1	SP1.0
R/W		0	0	0	0	0	0	0	0
04h	Data Source	HDRin.1	HDRin.0	8406in.1	8406in.0	SDIN2.1	SDIN2.0	SDIN1.1	SDIN1.0
R/W		0	1	0	1	0	1	0	1
05h	CS42324 Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AD1	AD0
R/W		0	0	0	0	0	0	0	0
06h	LED Status	Reserved	Reserved	MUTEC3	MUTEC2	MUTEC1	OVFL	INT	SPDIF.lock
R		x	x	x	x	x	x	x	x

6. FPGA REGISTER DESCRIPTION

6.1 Code Revision ID - Address 01h

7	6	5	4	3	2	1	0
Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0

Function:

Identifies the revision of the FPGA code. This register is Read-Only.

6.2 MCLK Source Control - Address 02h

7	6	5	4	3	2	1	0
Reserved	Reserved	MCLK2.1	MCLK2.0	Reserved	Reserved	MCLK1.1	MCLK1.0

6.2.1 MCLK2 Source (Bits 5:4)

Default = 00
Function:

These bits select the source of the CS42324 MCLK2 signal. Table 1 shows the available settings.

MCLK2.1	MCLK2.0	MCLK2 Source
0	0	Oscillator
0	1	MCLK2 position on Header J1
1	0	CS8416 RMCK
1	1	Disabled

Table 1. MCLK2 Source

6.2.2 MCLK1 Source (Bits 1:0)

Default = 00
Function:

This bit selects the source of the CS42324 MCLK1 signal. Table 2 shows the available settings.

MCLK1.1	MCLK1.0	MCLK1 Source
0	0	Oscillator
0	1	MCLK1 position on Header J1
1	0	CS8416 RMCK
1	1	Disabled

Table 2. MCLK1 Source

6.3 Subclock Source Control - Address 03h

7	6	5	4	3	2	1	0
Reserved	Reserved	SP2.1	SP2.0	Reserved	Reserved	SP1.1	SP1.0

6.3.1 SP2 Subclock Source (Bits 5:4)

Default = 01
Function:

These bits select the source of the CS42324 SCLK2 and LRCK2 signals. Table 3 shows the available settings.

SP2.1	SP2.0	SP2 Subclock Source
0	0	- CS42324 is Master - CS8416 is Slave to CS42324 - Header J1 Subclocks ending in 2 are Output from CS42324
0	1	- CS42324 is Slave to CS8416 - CS8416 is Master - Header J1 Subclocks ending in 2 are Output from CS8416
1	0	- CS42324 is Slave to Header - CS8416 is Slave to Header - Header J1 Subclocks ending in 2 are Input for Master
1	1	- CS42324 is Slave to CS8406 - CS8406 is Master - Header J1 Subclocks ending in 2 are Output from CS8406

Table 3. SP2 Subclock Source

6.3.2 SP1 Subclock Source (Bits 1:0)

Default = 01
Function:

This bit selects the source of the CS42324 SCLK1 and LRCK1 signals. Table 4 shows the available settings.

SP1.1	SP1.0	SP1 Subclock Source
0	0	- CS42324 is Master - CS8406 is Slave to CS42324 - Header J1 Subclocks ending in 1 are Output from CS42324
0	1	- CS42324 is Slave to CS8406 - CS8406 is Master - Header J1 Subclocks ending in 1 are Output from CS8406
1	0	- CS42324 is Slave to Header - CS8406 is Slave to Header - Header J1 Subclocks ending in 1 are Input for Master
1	1	- CS42324 is Slave to CS8416 - CS8416 is Master - Header J1 Subclocks ending in 1 are Output from CS8416

Table 4. SP1 Subclock Source

6.4 CS42324 SDIN Source Control - Address 04h

7	6	5	4	3	2	1	0
HDRin.1	HDRin.0	8406in.1	8406in.0	SDIN2.1	SDIN2.0	SDIN1.1	SDIN1.0

6.4.1 J1 SDOUT (pin 8) Source (Bits 1:0)
CS8406 SDIN Source (Bits 1:0)
CS42324 SDIN2 Source (Bits 1:0)
CS42324 SDIN1 Source (Bits 1:0)

Default = 01
Function:

These bits select the source of the SDATA signals. Table 5 shows the available settings.

xxx.1	xxx.0	SDATA Source
0	0	CS8416 SDOUT
0	1	CS42324 SDOUT
1	0	SDIN1 from Header
1	1	SDIN2 from Header

Table 5. SDATA Source

6.5 Misc Control - Address 05h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AD1	AD0

6.5.1 AD0 (Bit 0)

Default = 0
Function:

This bits selects the state of the AD0 pin. Table 6 shows the available settings.

AD0	CS42324 AD0 state
0	Low
1	High

Table 6. CS42324 AD0 State

6.5.2 AD1 (Bit 1)

Default = 0
Function:

This bits selects the state of the AD1 pin. Table 7 shows the available settings.

AD1	CS42324 AD1 State
0	Low
1	High

Table 7. CS42324 AD1 State

6.6 LED Status - Address 06h

7	6	5	4	3	2	1	0
Reserved	Reserved	MUTEC3	MUTEC2	MUTEC1	OVFL	INT	SPDIF.lock

6.6.1 MUTEC3 (BIT 5)

6.6.2 MUTEC2 (BIT 4)

6.6.3 MUTEC1 (BIT 3)

6.6.4 $\overline{\text{OVFL}}$ (BIT 2)

6.6.5 $\overline{\text{INT}}$ (BIT 1)

6.6.6 SPDIF LOCK (Bit 0)

Function:

These bits are Read Only and indicate the status of the named signal (similar to the LED on the board).

7. CDB CONNECTORS, JUMPERS, AND SWITCHES

CONNECTOR	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
VA-H	J7	Input	+9 V to +12 V power supply binding post, Please see CS42324 datasheet for Limits
GND	J5	Input	Ground Reference
S/PDIF OUT	J55	Output	CS8406 digital audio output via coaxial cable
S/PDIF OUT	OPT2	Output	CS8406 digital audio output via optical cable
S/PDIF IN	OPT1	Input	CS8416 digital audio input via optical cable
S/PDIF IN	J53	Input	CS8416 digital audio input via coaxial cable
USB I/O	J44	Input/Output	USB connection to PC for SPI / I²C control port signals
CLK & DATA I/O	J1	Input/Output	I/O for Serial Audio Port Clocks & Data
EXT | INT	J46	Input/Output	I/O for external SPI / I²C control port signals.
C2	J45	Input/Output	I/O for programming the micro controller (U4)
JTAG	J54	Input/Output	I/O for programming the FPGA (U23)
RESET	S3	Input	Reset for the micro controller (U4)
FPGA PRGM	S1	Input	Reset for the FPGA (U35)
AIN1A, AIN1B AIN2A, AIN2B AIN3A, AIN3B AIN4A, AIN4B AIN5A, AIN5B	J29, J27 J11, J13 J16, J22 J25, J34 J6, J39	Input	RCA phono jacks for analog input signal to CS42324. Passive input filter.
AOUT1A, AOUT1B AOUT2A, AOUT2B AOUT3A, AOUT3B	J18, J20 J14, J23 J38, J30	Output	RCA phono jacks for analog outputs. Passive output filter.
VA-H VA 3.3V (VL) VD	J60 J59 J61 J100	Output	Header for current consumption measurements (measure voltage drop across 1 Ω)

Table 8. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J78	Shunt to power VA with 3.3 V regulator	*Shunted	Voltage source is +3.3 V regulator.
J46	Allows a junction point for external cabling in of control (I²C/SPI) data or passes on board signals	EXT *INT	Connect ribbon cable here for external I²C Shunts placed here for on board configuration.
J10, J3 J9, J28 J33, J32	Attaches the external mute circuitry, driven from the CS42324 $\overline{\text{MUTEC}}$ output, to the analog outputs	*Shunted Open	Activate analog mute circuit. Disconnect mute circuitry from signal.

*Default factory settings

Table 9. System Jumper Settings

8. SCHEMATICS AND LAYOUT

Note: Schematic net names and test point names silk-screened on the PCB should be interpreted as follows:

- Those ending in A should be interpreted as ending in 1 (for example, MCLKA should be interpreted as MCLK1).
- Those ending in D should be interpreted as ending in 2 (for example, MCLKD should be interpreted as MCLK2).

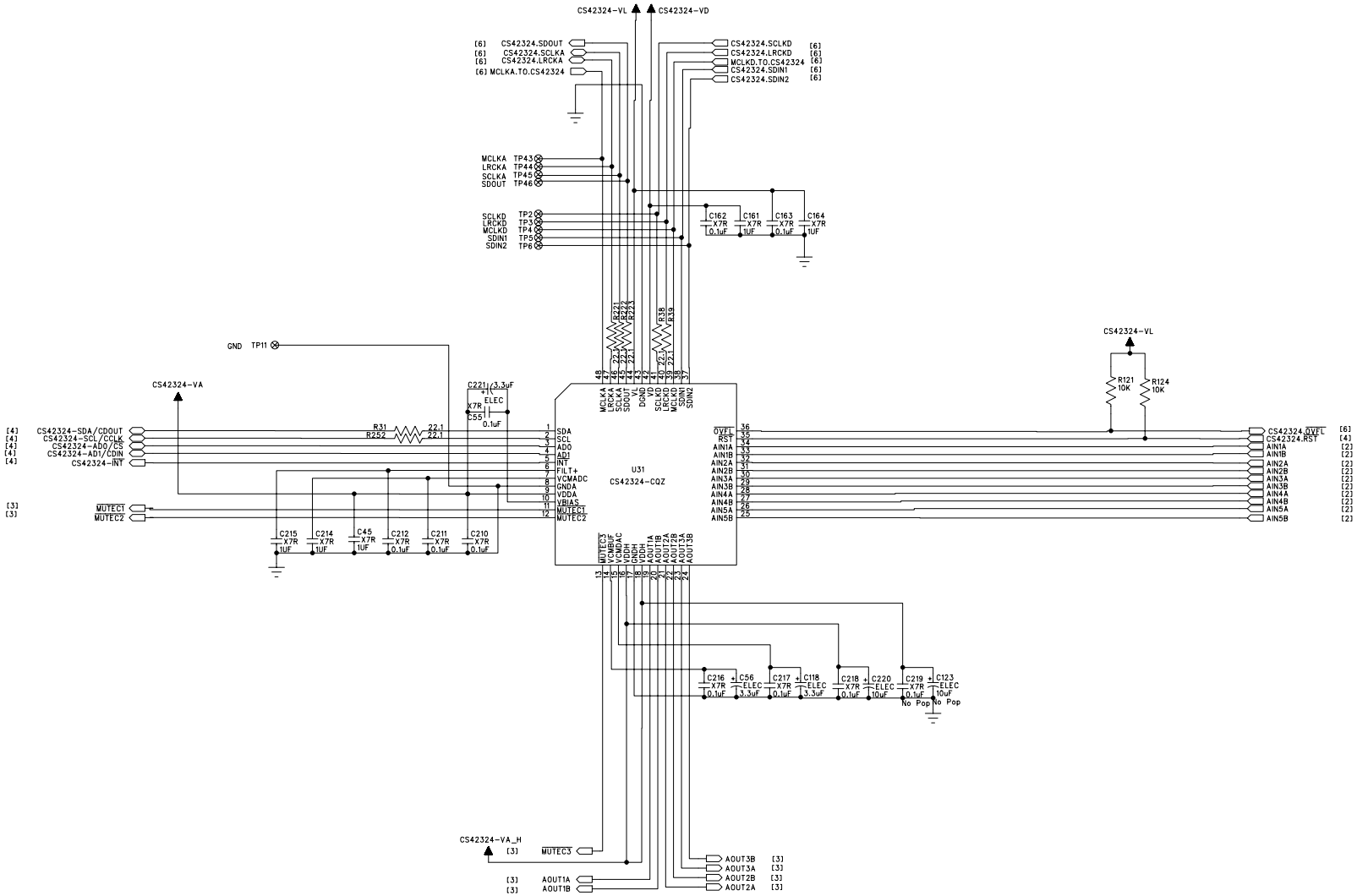

Figure 5. CS42324 - Schematic Page 1

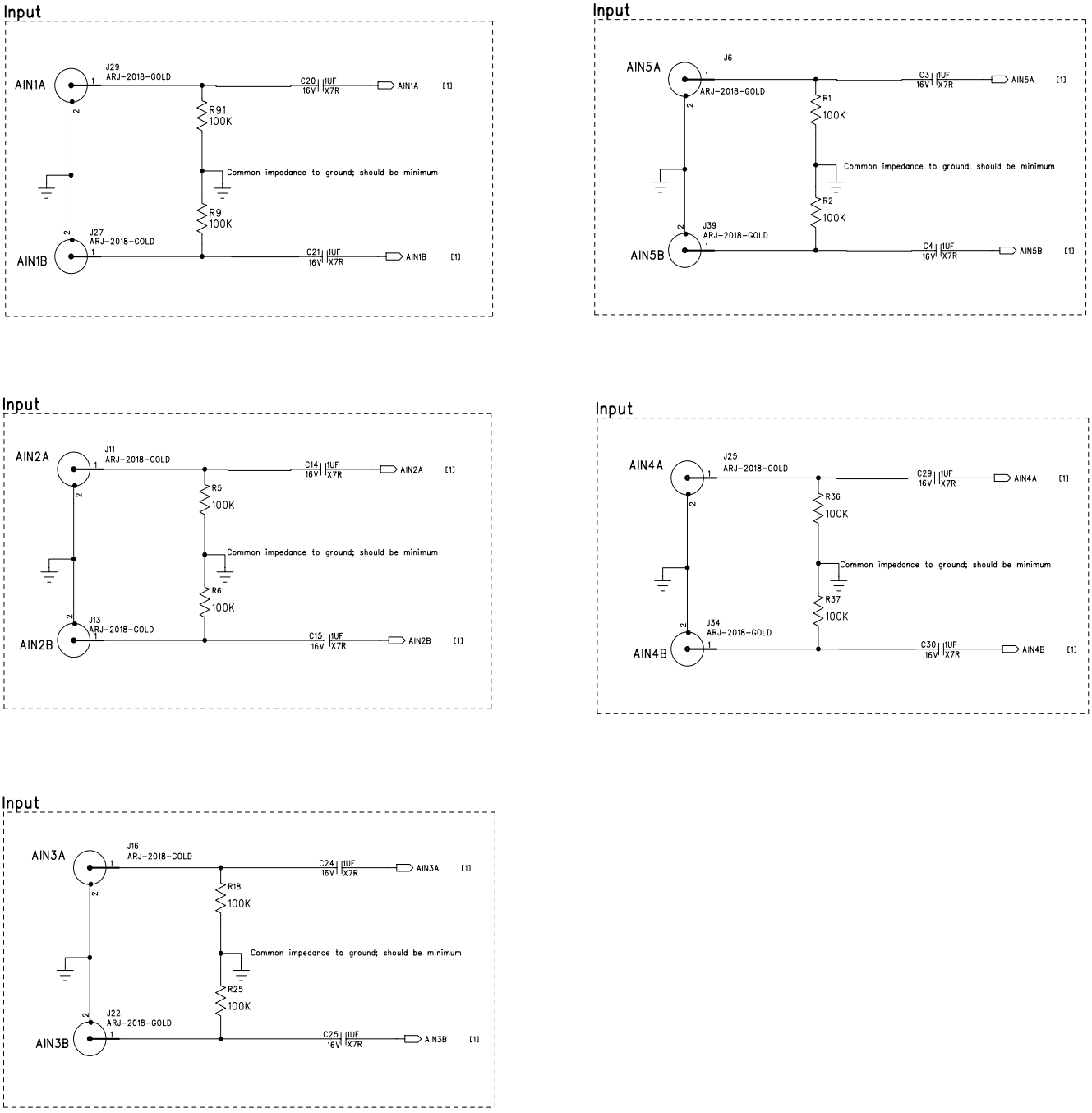

Figure 6. Analog Inputs - Schematic Page 2

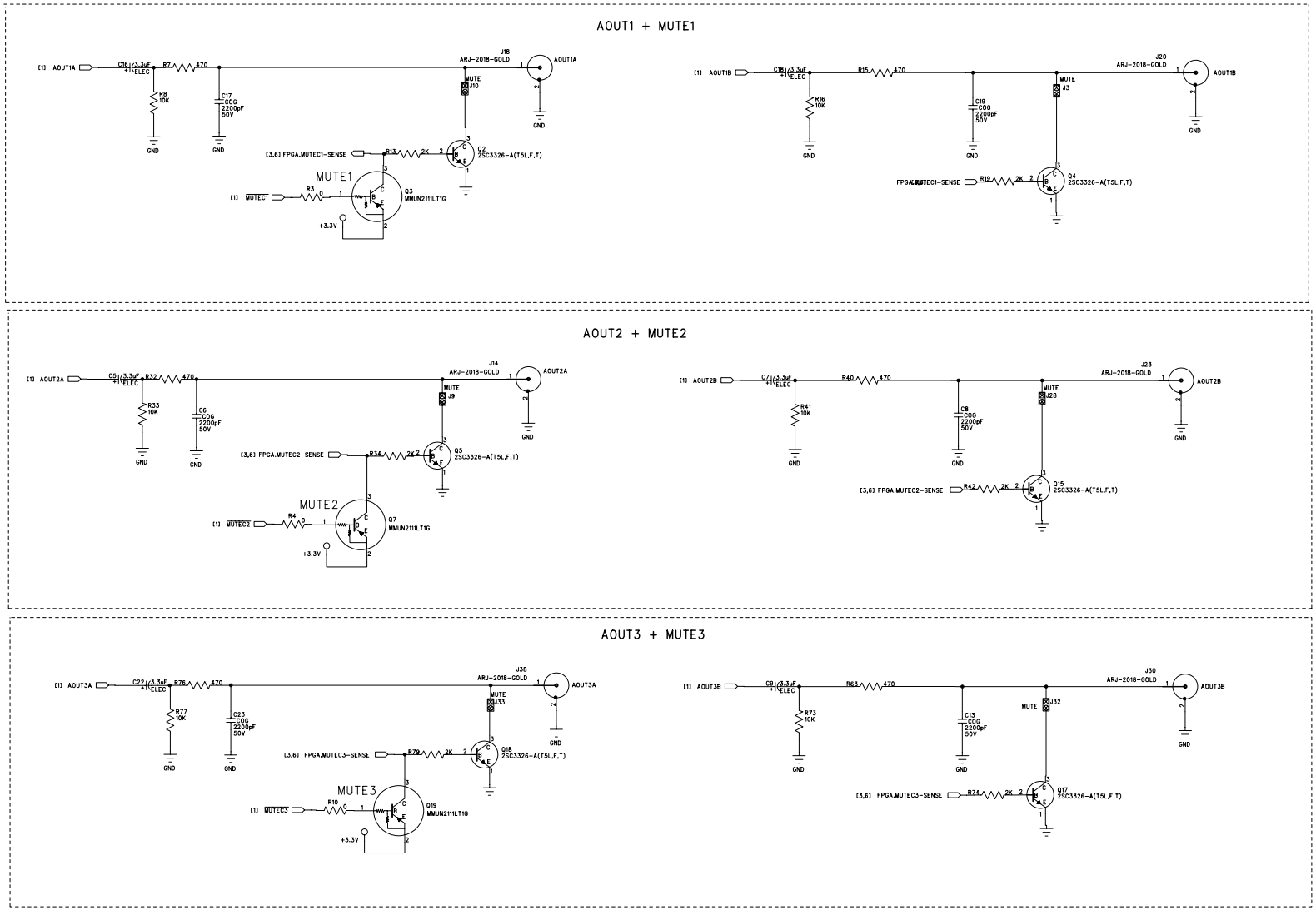

Figure 7. Analog Outputs - Schematic Page 3

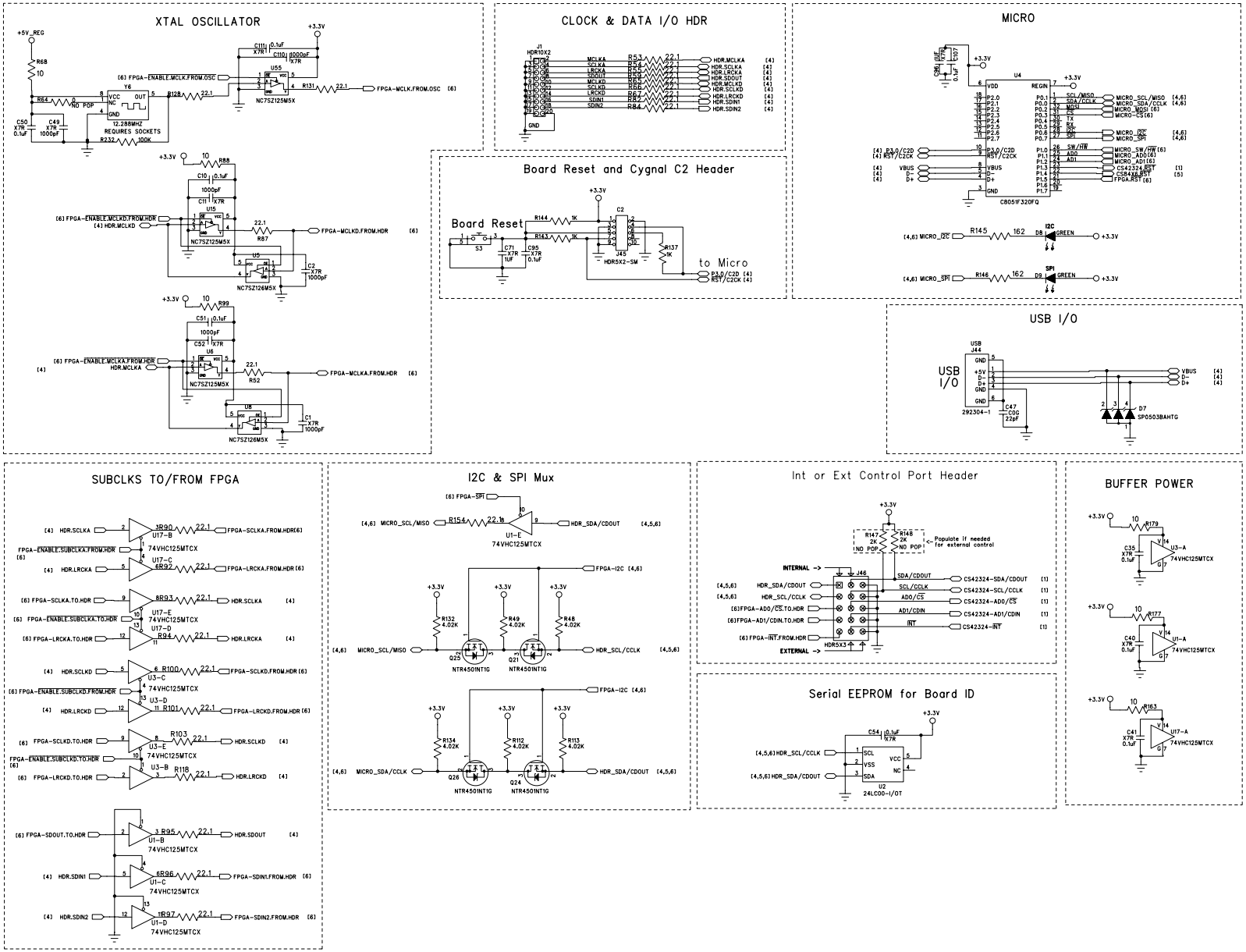

Figure 8. Clock Routing and Board Control - Schematic Page 4

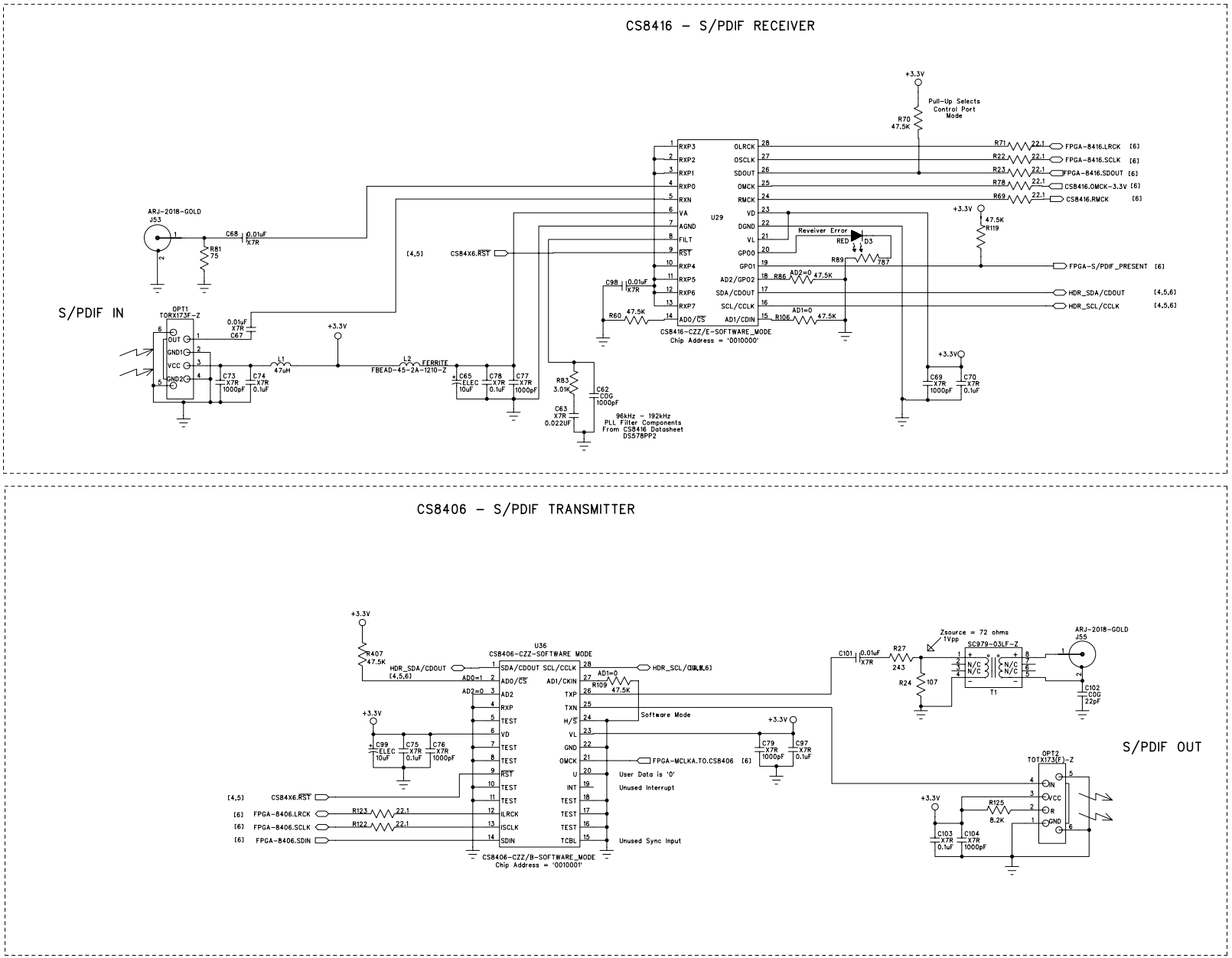

Figure 9. S/PDIF I/O - Schematic Page 5

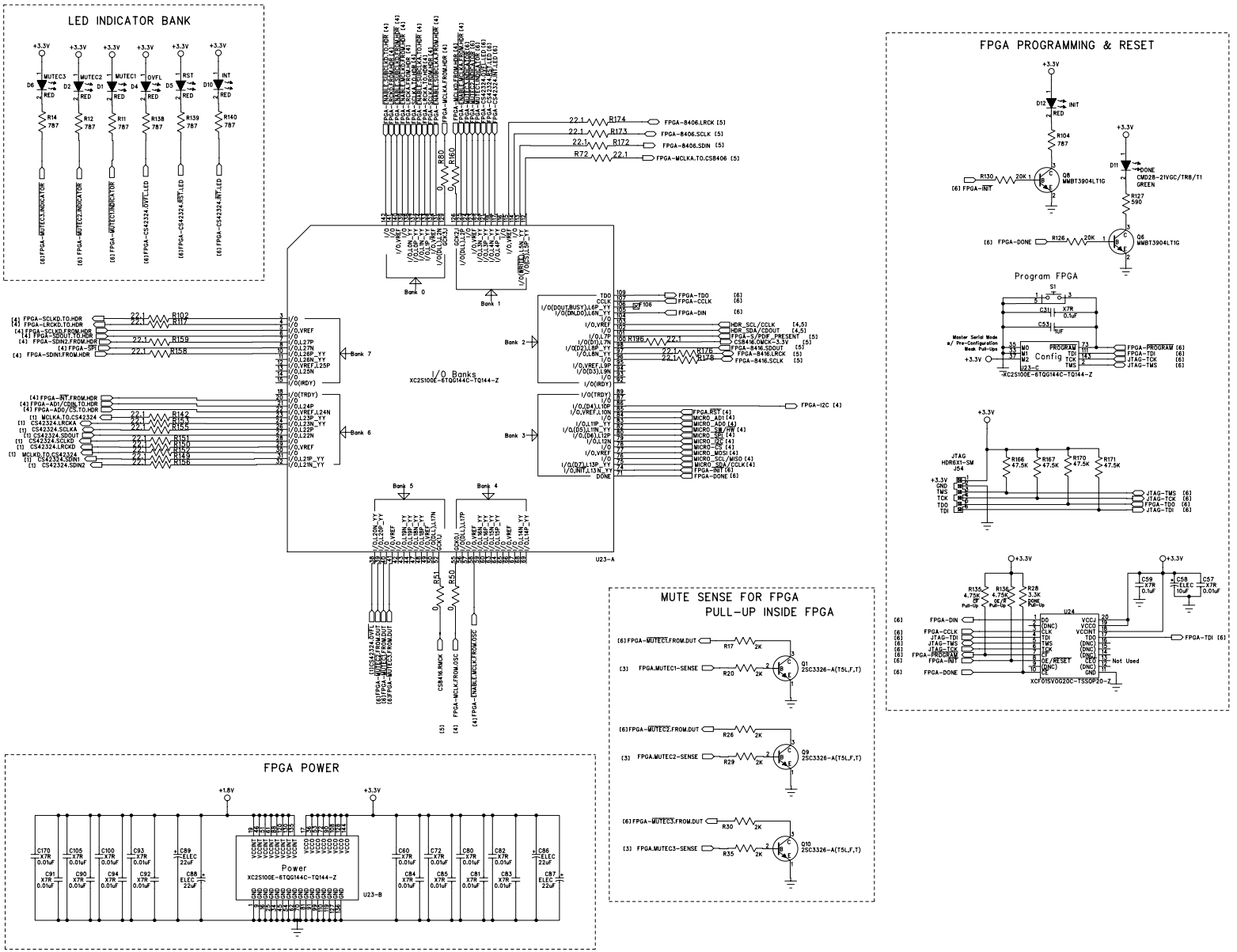

Figure 10. FPGA - Schematic Page 6

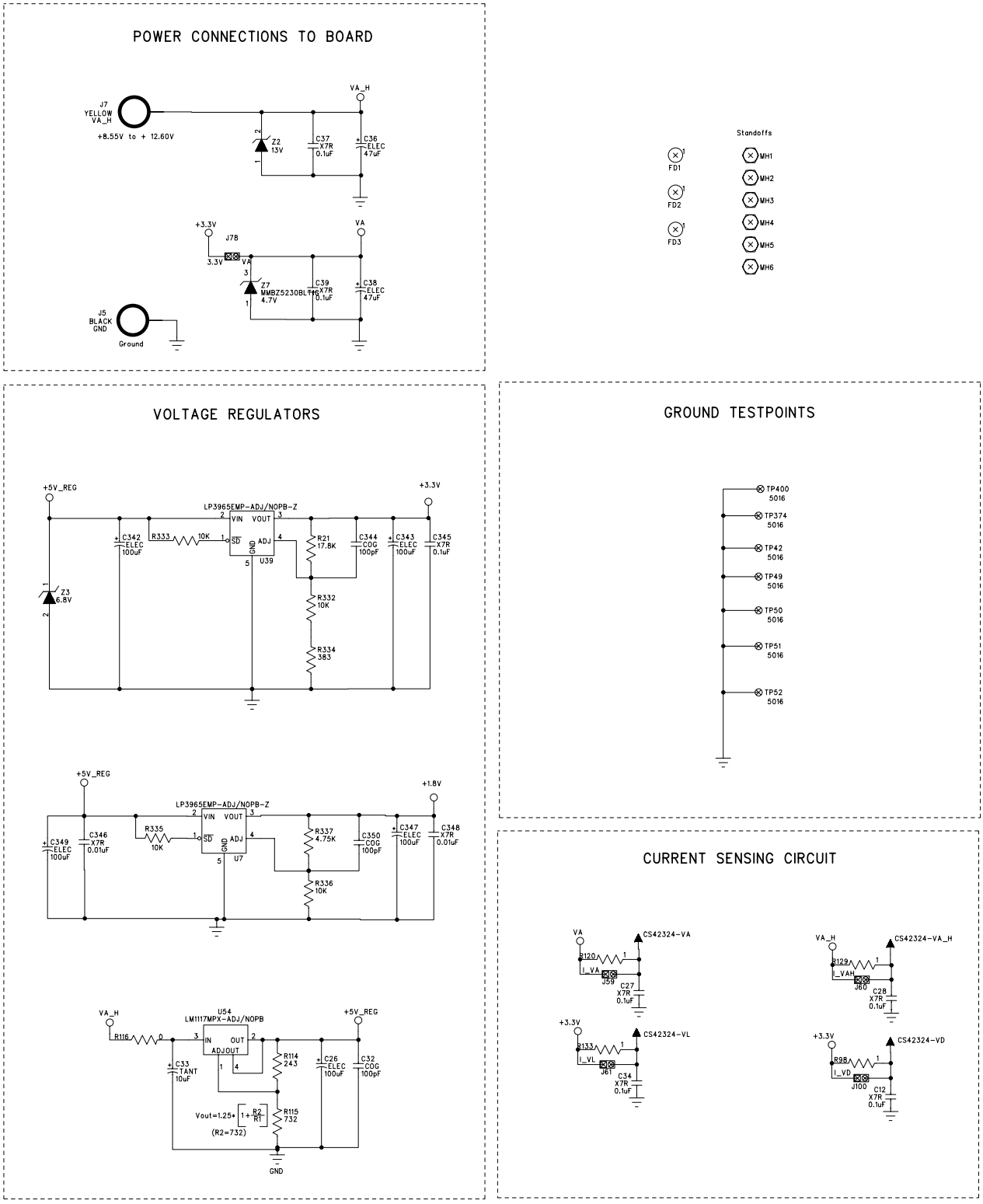

Figure 11. Power - Schematic Page 7

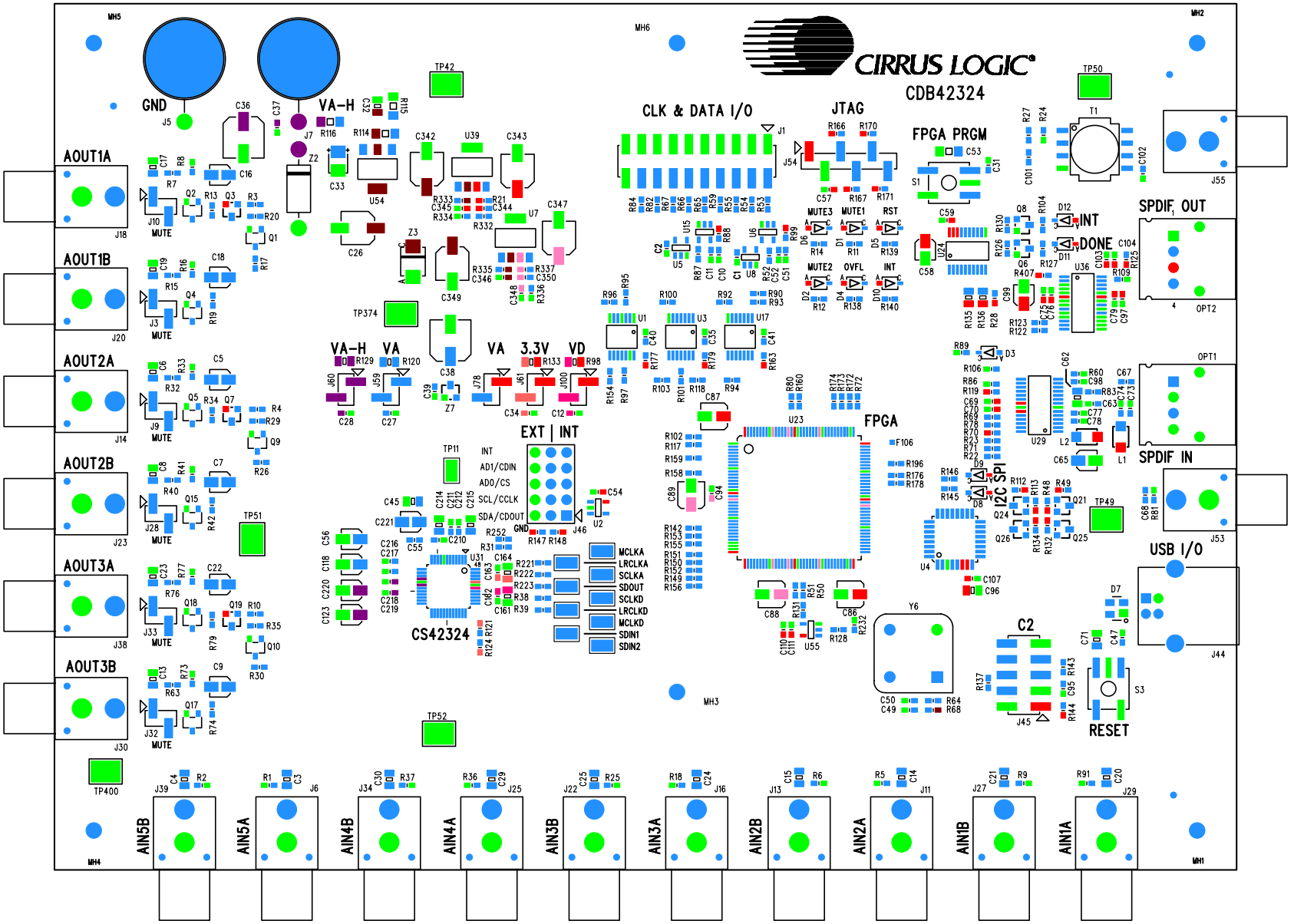

Figure 12. Silk-screen Top

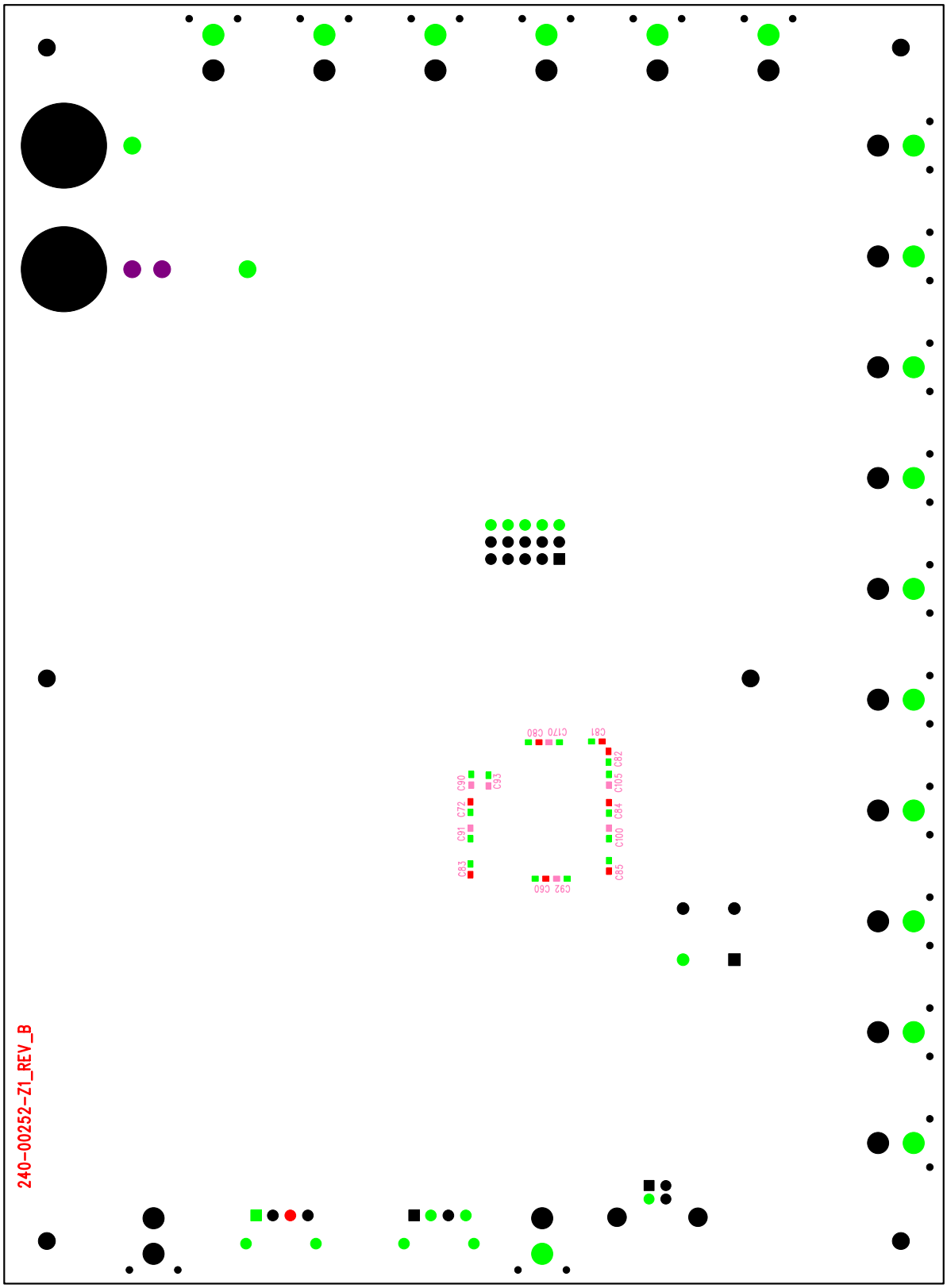

Figure 13. Silk-screen Bottom

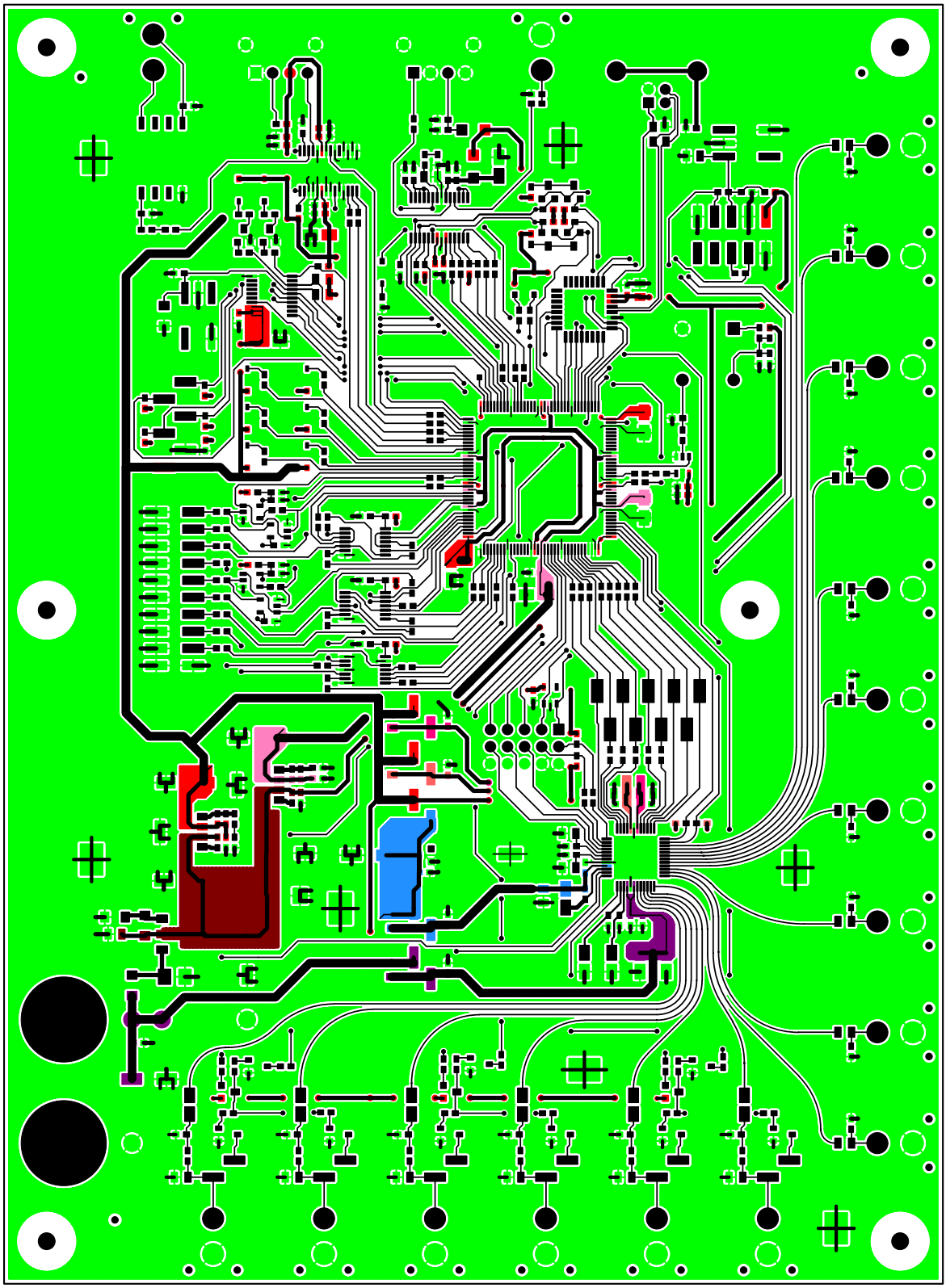

Figure 14. Top Layer Routing

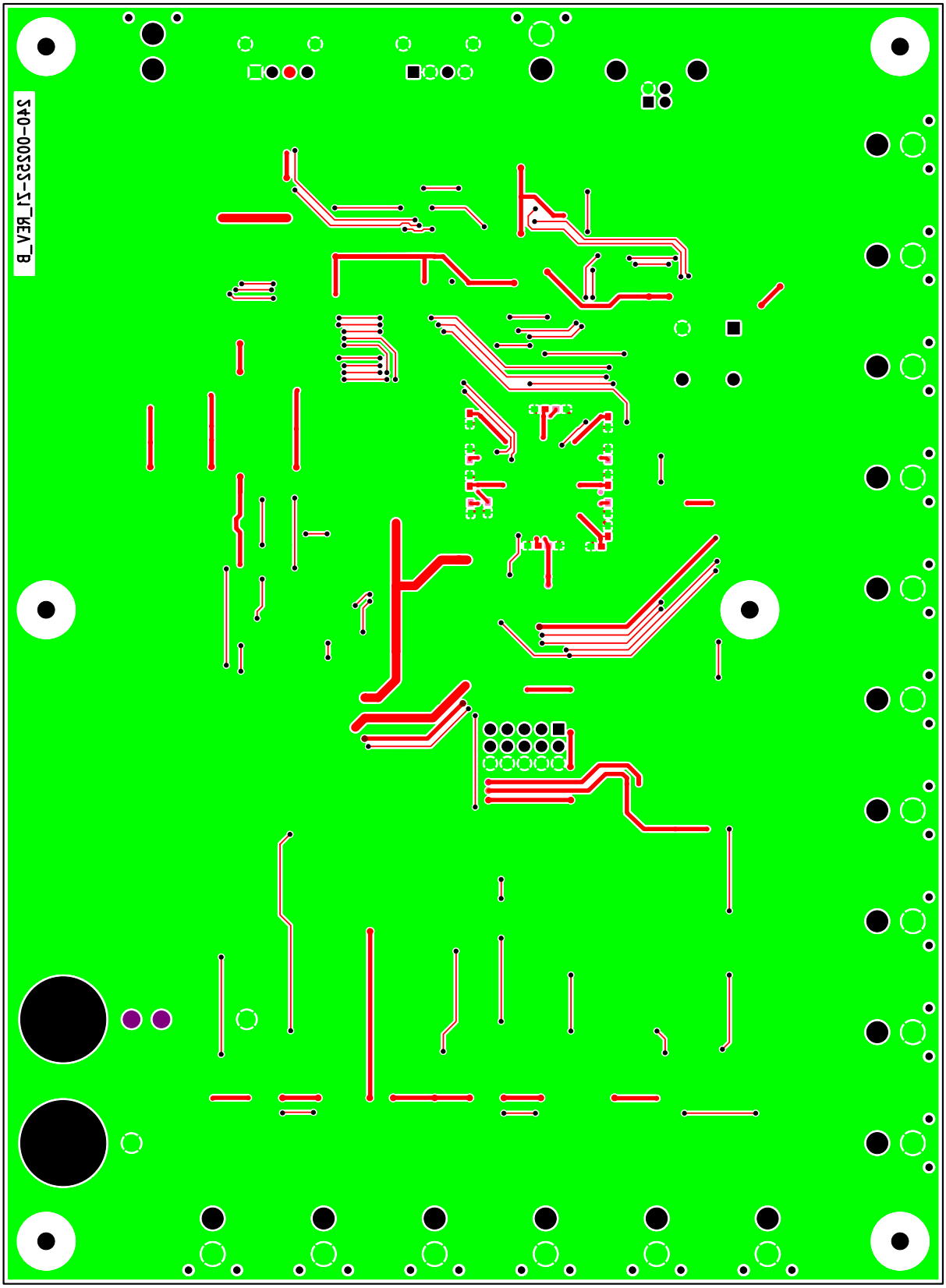

Figure 15. Bottom Layer Routing

9. REVISION HISTORY

Revision	Changes
DB1	Initial Release.
DB2	Changed MCLK and serial port names.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.