HARRIS SEMICONDUCTOR

RFD16N05L
RFD16N05LSM

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

June 1992

Features

- 16A, 50V
- $r_{DS}(ON) = 0.047\Omega$
- UIS SOA Rating Curves (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature +150°C

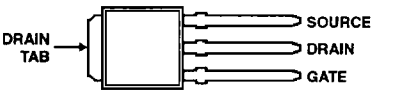
Description

The RFD16N05L and RFD16N05LSM N-channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFD16N05L and RFD16N05LSM were designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

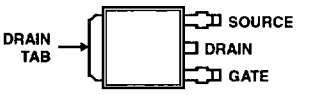
The RFD16N05L is supplied in the JEDEC TO-251 plastic package and the RFD16N05LSM in the JEDEC TO-252 plastic package.

Package

TO-251AA
TOP VIEW

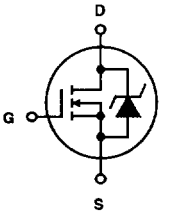


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	45	A
Single Pulse Avalance Rating		Refer to UIS SOA Curve	
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2269.1**

Electrical Characteristics At Case Temperature (Tc) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 2.05mA, V_{GS} = 0V		50	-	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 2.05mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V T_C = 150°C		-	1 50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GC} = ±10V, V_{DS} = 0V		-	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D ≈ 16A, V_{GS} = 5V I_D ≈ 16A, V_{GS} = 4V		- -	0.047 0.056	W
Turn-On Time	t(on)	V_{DD} = 25V, I_D = 8A, I_{G1} = I_{G2} = 0.4A, V_{GS} (clamp) + 5V, -0.6V, R_L = 3.125Ω		-	60	ns
Turn-On Delay Time	$t_d(on)$			-	14(typ)	ns
Rise Time	t_r			-	30 (typ)	ns
Turn-Off Delay Time	$t_d(off)$			-	42 (typ)	ns
Fall Time	t_f			-	14 (typ)	ns
Turn-Off Time	t(off)			-	100	ns
Total Gate Charge	$Q_g(total)$	V_{GS} = 0-10V	V_{DD} = 40V I_D = 16A R_L = 2.5Ω	-	80	nC
Gate Charge at 5V	Qg(5)	V_{GS} = 0-5V		-	45	nC
Threshold Gate Charge	Qg(th)	V_{GS} = 0-1V		-	3	nC
Plateau Voltage	V(plateau)	I_D = 16A, V_{DS} = 15V		-	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 8A, R_L = 3.125Ω, L = 0.2µH, I_{g1} = I_{g2} = 0.8A, V_{GS}(clamp) +5V, -0.6V		-	19	µJ
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$			-	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$			-	100	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16A, dI_F/d_t = 100A/µs	-	125	ns

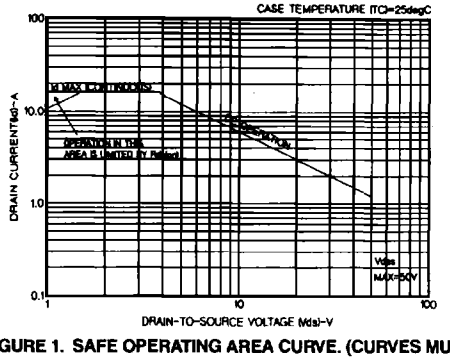


FIGURE 1. SAFE OPERATING AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN TEMP.)

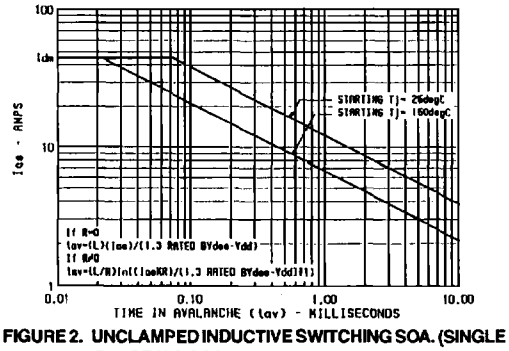


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING SOA. (SINGLE PULSE UIS SOA

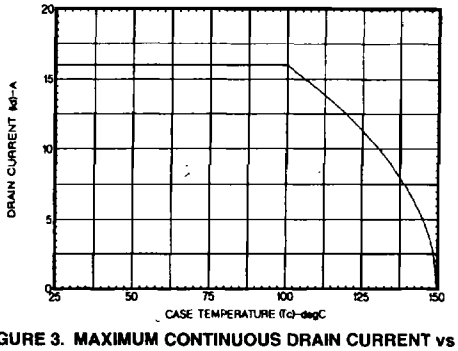


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

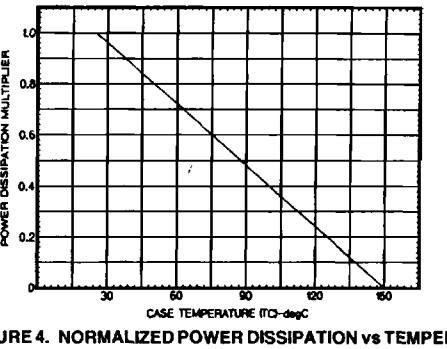


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

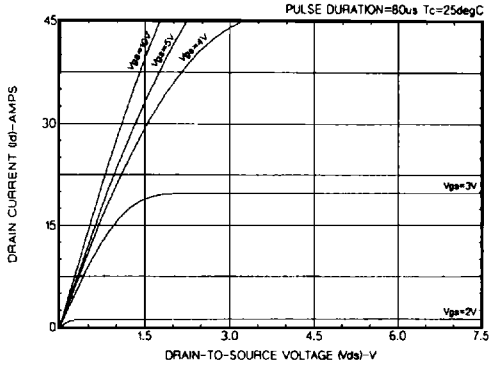


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

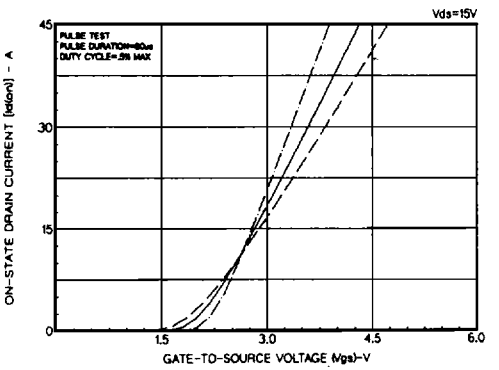


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

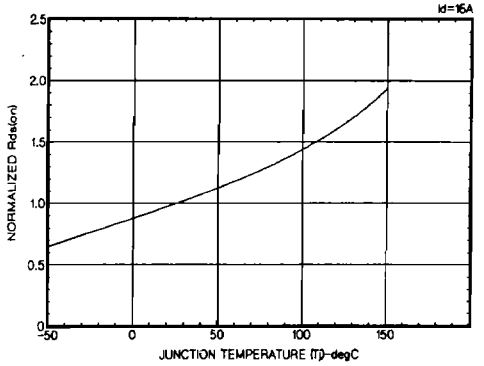


FIGURE 7. NORMALIZED $r_{DS}(on)$ vs JUNCTION TEMPERATURE

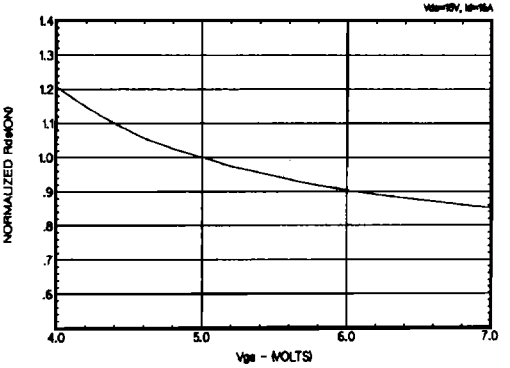


FIGURE 8. NORMALIZED $r_{DS}(on)$ vs V_{GS}

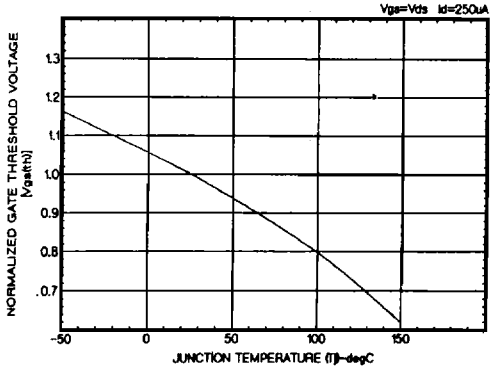


FIGURE 9. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE

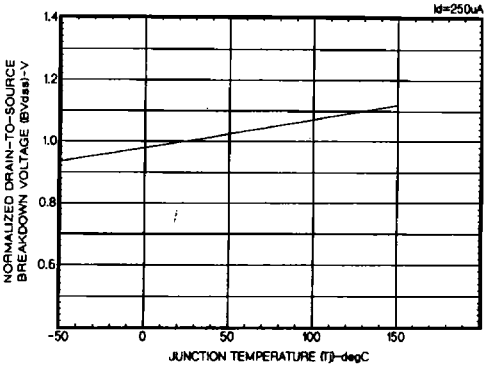


FIGURE 10. DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

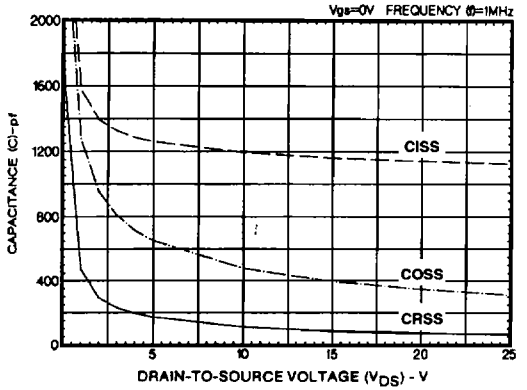


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

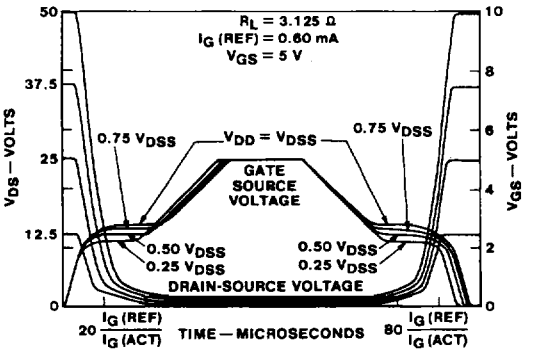


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260.

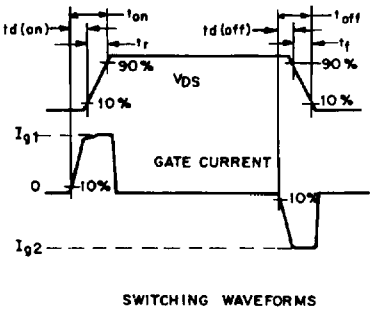


FIGURE 13. RESISTIVE SWITCHING

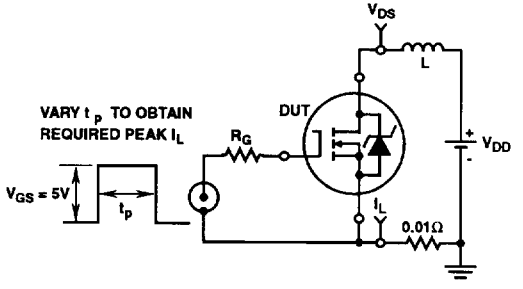


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

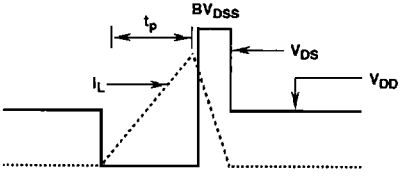


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Spice Model (RFD16N05L)

```
.SUBCKT RFD16N05L  2  1  3;  rev 04/08/92
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=2.054  KP=24.73  IS=1e-30  N=10  TOX=1  L=1u  W=1u)
Vto  21  6  0.448
Rsource  8  7  RDSMOD  0.614E-3
Rdrain  5  16  RDSMOD  27.38E-3
.MODEL RDSMOD RES (TC1=3.66E-3  TC2=1.46E-5)
.MODEL RVTOMOD RES (TC1=-1.81E3  TC2=1.41E-6)
Ebreak 11  7  17  18  70.9
.MODEL RBKMOD RES (TC1=1.01E-3  TC2=5.21E-8)
.MODEL DBKMOD D (RS=8.82E-2  TRS1=-2.01E-3  TRS2=7.32E-10)
.MODEL DBDMOD D (IS=1.34E-13  RS=1.21E-2  TRS1=1.64E-3  TRS2=2.59E-6  +CJO=1.13E-9  TT=4.14E-8)
Cin  6  8  1.21E-9
Ca  12  8  3.33E-9
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-4.25  VOFF=-2.25)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=-4.25)
.MODEL DPLCAPMOD D (CJO=5.22E-10  IS=1e-30  N=10)
Cb  15  14  3.11E-9
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-0.65  VOFF=4.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=4.35  VOFF=-0.65)
Rgate  9  20  2.98
Lgate  1  9  1.38E-9
Ldrain  2  5  1.0E-12
Lsource  3  7  1.0E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```