

## **AN-1588 LM5001 Evaluation Board**

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### **1 Introduction**

The LM5001 evaluation board is designed to provide the design engineer with a fully functional isolated flyback power converter based on current mode control to evaluate the LM5001 switching regulator IC. The evaluation board provides a 5V output with 1A current capability. The input voltage ranges from 16V to 42V. The design operates at 250kHz, a good compromise between conversion efficiency and solution size. The printed circuit board consists of two layers of two ounce copper on FR4 material with a thickness of 0.062 inches. This application note contains the evaluation board schematic, Bill-of-Materials (BOM) and a quick setup procedure.

Refer to the *LM5001 High Voltage Switch Mode Regulator* ([SNVS484](#)) data sheet for complete circuit design information.

The performance of the evaluation board is as follows:

Input Range: 16 to 42V

Output Voltage: 5V,  $\pm 2\%$

Output Current: 0 to 1A

Frequency of Operation: 250 kHz

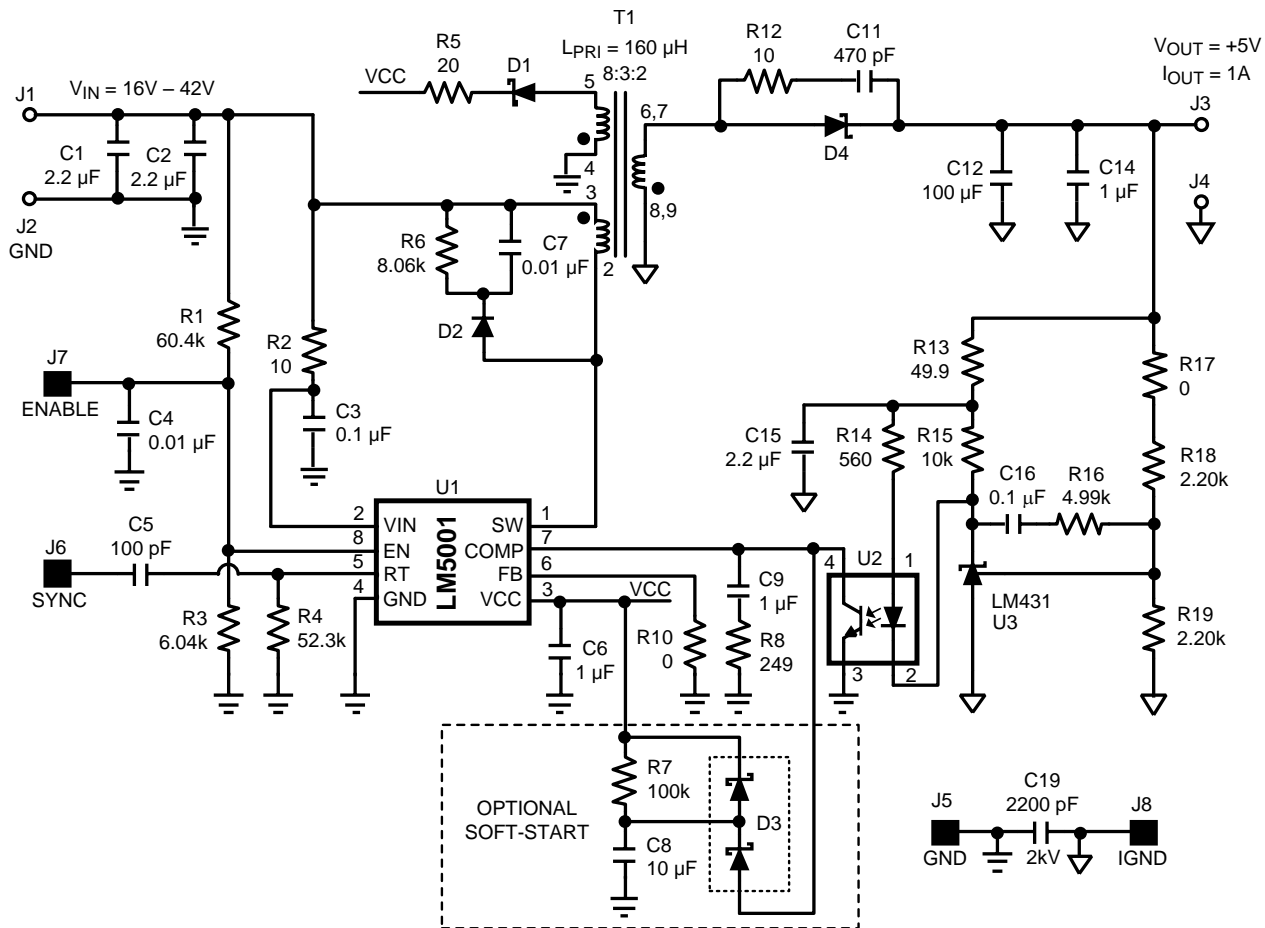
Board Size: 2.75 X 1.75 X 0.6 inches

Load Regulation: 0.1%

Line Regulation: 0.1%

Over Current Limiting

## 2 Evaluation Board Schematic



## 3 Powering and Loading Considerations

Read this entire page prior to attempting to power the evaluation board.

### 3.1 Quick Setup Procedure

**Step 1:** Set the input source current limit to 1A. Turn off the input source. Connect the positive output of the input source to J1 and the negative output to J2.

**Step 2:** Connect the load, with 1A capability, to J3 for the positive connection and J4 for the negative connection.

**Step 3:** The ENABLE pin, J7, should be left open for normal operation.

**Step 4:** Set the input source voltage to 28V and the load to 0.1A. The load voltage should be in regulation with a nominal 5V output.

**Step 5:** Slowly increase the load while monitoring the load voltage at J3 and J4. It should remain in regulation with a nominal 5V output as the load is increased up to 1 Amp.

**Step 6:** Slowly sweep the input source voltage from 16V to 42V. The load voltage should remain in regulation with a nominal 5V output.

**Step 7:** Temporally short the ENABLE pin (J7) to GND (J5) to check the shutdown function.

**Step 8:** Increase the load beyond the normal range to check current limiting while the input source is set to 28V. The output current should limit at approximately 1.9A. The input source current limit should be increased for this step. Fan cooling is critical during this step.

### 3.2 Air Flow

Prolonged operation at full power and high ambient temperature will cause the thermal shutdown circuit within the regulator IC to activate. A fan with a minimum of 200 LFM should always be provided.

### 3.3 Powering Up

Using the ENABLE pin (J7) provided will allow powering up the input source with the current level set low. It is suggested that the load power be kept low during the first power up. Set the current limit of the input source to provide about 1.5 times the anticipated wattage of the load. As you remove the connection from the ENABLE pin to GND (J5), immediately check for 5 volts at the output.

A quick efficiency check is the best way to confirm that everything is operating properly. If something is amiss you can be reasonably sure that it will affect the efficiency adversely. Few parameters can be incorrect in a switching power supply without creating losses and potentially damaging heat.

### 3.4 Over Current Protection

The evaluation board is configured with cycle-by-cycle over-current protection. This function is completely contained in the LM5001. The Primary current is limited to approximately 1A. This equates to about 1.4A load current when the input voltage is 16V, and about 2.1A load current when the input is 42V. The thermal stress on various circuit components is quite severe while in an overloaded condition, therefore limit the duration of the overload and provide sufficient cooling (airflow).

### 3.5 Synchronization

A SYNC pin (J6) has been provided on the evaluation board. This pin can be used to synchronize the regulator to an external clock or multiple evaluation boards can be synchronized together by connecting their SYNC pins together. Refer to the *LM5001 High Voltage Switch Mode Regulator* ([SNVS484](#)) data sheet for complete information.

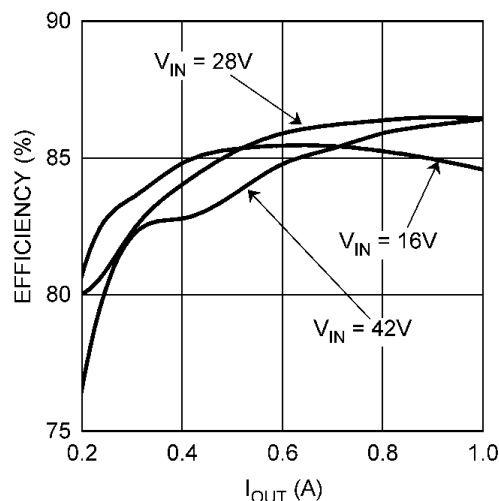
### 3.6 Flyback Topology

An excellent introduction to the isolated flyback converter is available on the Texas Instruments website. The Application Note AN-1095([SNVA005](#)) discusses both loop compensation with a secondary side error amplifier and the phase-shift caused by opto-couplers.

## 4 Performance Characteristics

### Efficiency Plots

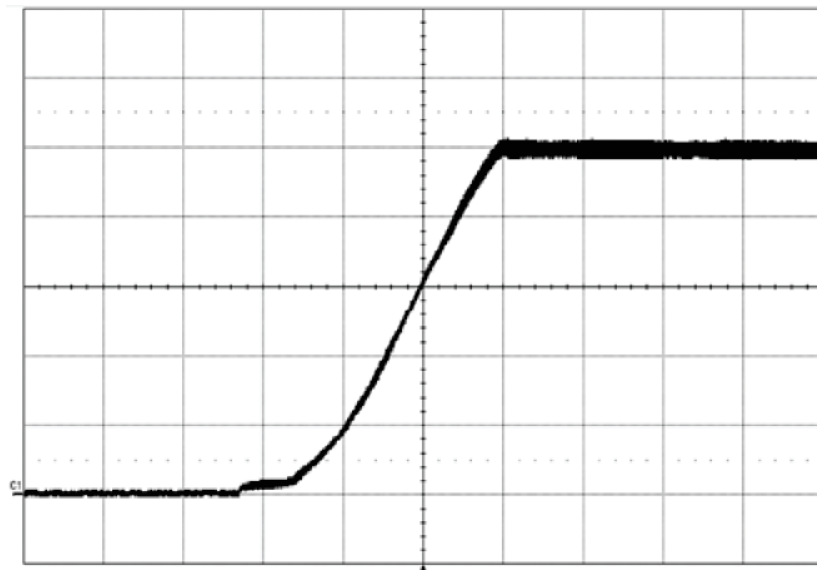
Figure 1 shows the conversion efficiency versus output current for several input voltage conditions.



**Figure 1. Conversion Efficiency vs Output Current**

### Turn-on Waveform

When applying power to the LM5001 evaluation board a soft-start sequence occurs. [Figure 2](#) shows the output voltage during a typical start-up sequence.

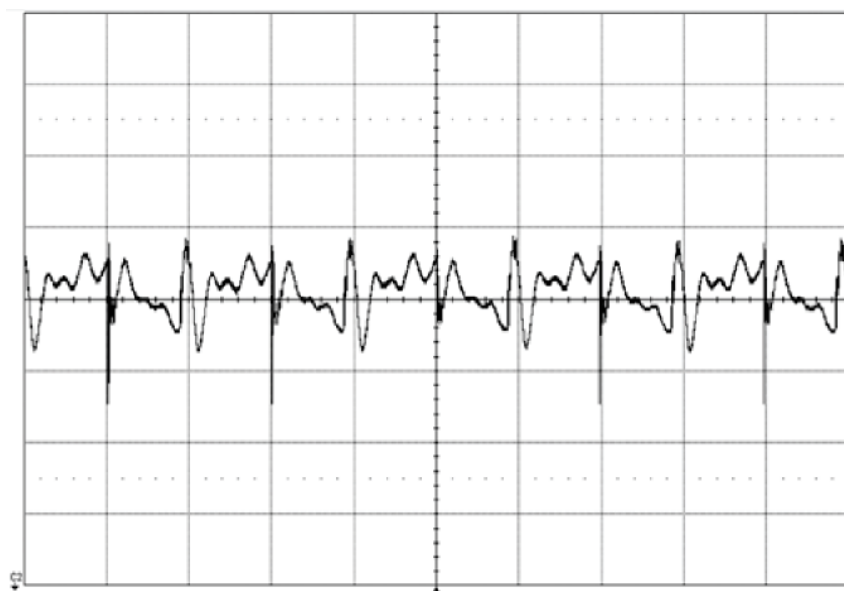


Conditions: Input Voltage = 28VDC, Output Current = 1A  
 Trace 1: Output Voltage Volts/div = 1V  
 Horizontal Resolution = 5ms/div

**Figure 2. Voltage During a Typical Start-up Sequence**

### Output Ripple Waveform

[Figure 3](#) shows the output voltage ripple. This measurement was taken with a very short ground clip and 20 MHz bandwidth limiting.

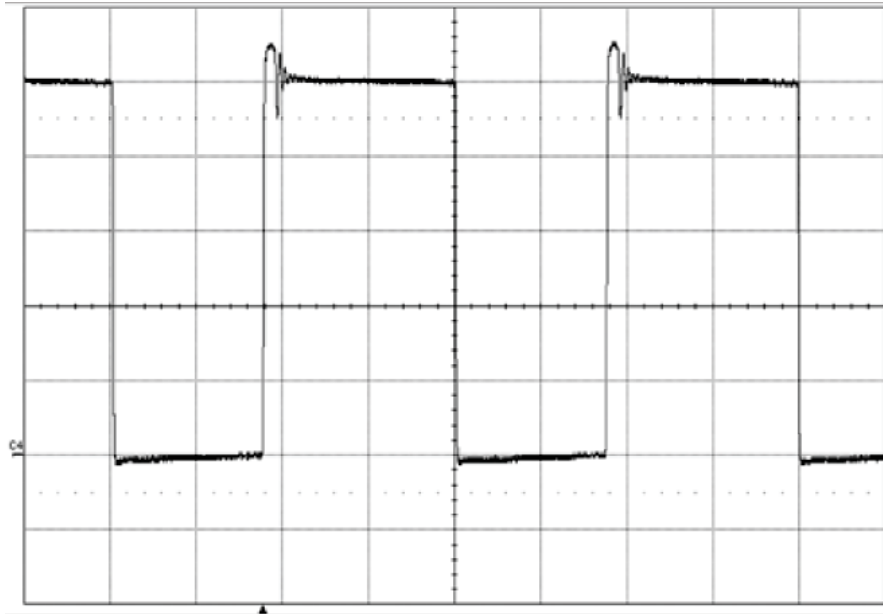


Conditions: Input Voltage = 28VDC, Output Current = 1A,  
 Bandwidth Limit = 20MHZ  
 Trace 1: Output Ripple Voltage Volts/div = 50mV  
 Horizontal Resolution = 2µs/div

**Figure 3. Output Voltage Ripple**

**Primary Switchnode Waveform**

Figure 4 shows the typical primary voltage during continuous conduction mode (CCM).



Conditions: Input Voltage = 28VDC, Output Current = 1A,  
 Bandwidth Limit = 20MHZ  
 Trace 1: LM5001 SW Pin Volts/div = 10V  
 Horizontal Resolution = 2μs/div

**Figure 4. Primary Voltage During CCM**

## 5 Layout and Bill of Materials

The bill of materials is shown in [Table 1](#), including the manufacturer and part number.

**Table 1. Bill of Materials**

DESIGNATOR	QTY	PART NUMBER	DESCRIPTION	VALUE
C1,2	2	C3225X7R1H225K	CAPACITOR, 1210 X7R CER, TDK	2.2 $\mu$ , 50V
C3,16	2	C2012X7R2A104K	CAPACITOR, 0805 X7R CER, TDK	0.1 $\mu$ , 100V
C4, 7	2	C2012X7R2A103K	CAPACITOR, 0805 X7R CER, TDK	0.01 $\mu$ , 100V
C5	1	C0805C101M5RAC	CAPACITOR, 0805 COG CER, KEMET	100p, 50V
C6, 9, 14	3	C2012X7R1A105K	CAPACITOR, 0805 X7R CER, TDK	1 $\mu$ , 10V
C8	1	C2012Y5V1A106Z	CAPACITOR, 0805 Y5V CER, TDK	10 $\mu$ , 10V
C11	1	C0805C471M5RAC	CAPACITOR, 0805 COG CER, KEMET	470p, 50V
C12	1	C1210C107M9PAC3810	CAPACITOR, 1210 X5R CER, KEMET	100 $\mu$ , 6.3V
C15	1	C2012X7R1C225K	CAPACITOR, 0805 X7R CER, TDK	2.2 $\mu$ , 16V
C19	1	C4532X7R3D222K	CAPACITOR, 1812, X7R CER, TDK	2200p, 2000V
D1	1	CMHSH-3	DIODE, SOD-123 SCHOTTKY, CENTRAL SEMI	200mA, 30V
D2	1	CMMR1U-2	DIODE, SOD-123F, CENTRAL SEMI	1A, 200V
D3	1	BAT54S	DIODE, SOT-23 SCHOTTKY, VISHAY	200mA, 30V
D4	1	CMSH5-40	DIODE, SMC SCHOTTKY, CENTRAL SEMI	5A, 40V
R1	1	CRCW08056042F	RESISTOR, 0805, VISHAY	60.4k
R2,12	2	CRCW080510R0F	RESISTOR, 0805, VISHAY	10
R3	1	CRCW08056041F	RESISTOR, 0805, VISHAY	6.04k
R4	1	CRCW08055232F	RESISTOR, 0805, VISHAY	52.3k
R5	1	CRCW080520R0F	RESISTOR, 0805, VISHAY	20
R6	1	CRCW08058061F	RESISTOR, 0805, VISHAY	8.06k
R7	1	CRCW08051003F	RESISTOR, 0805, VISHAY	100k
R8	1	CRCW08052490F	RESISTOR, 0805, VISHAY	249
R10,17	2	CRCW08050000Z0EA	RESISTOR, 0805, VISHAY	0
R13	1	CRCW080549R9F	RESISTOR, 0805, VISHAY	49.9
R14	1	CRCW08055600F	RESISTOR, 0805, VISHAY	560
R15	1	CRCW08051002F	RESISTOR, 0805, VISHAY	10.0k
R16	1	CRCW08054991F	RESISTOR, 0805, VISHAY	4.99k
R18,19	2	CRCW08052201F	RESISTOR, 0805, VISHAY	2.2k
T1	1	FA2636-AL	POWER XFR, COILCRAFT	160 $\mu$ H PRIMARY, 8:3:2
U1	1	LM5001	REGULATOR, TEXAS INSTRUMENTS	
U2	1	PS2811-1M	OPTO-COUPLER, NEC	100% - 200% CTR
U3	1	LM431	REFERENCE, SOT23, TEXAS INSTRUMENTS	2.500V
J1,2,3,4	4	7693	TERMINAL, 6-32 SCREW, 4 PIN, KEYSTONE	SNAP IN, PC MOUNT
J5,6,7,8	4	5002	TERMINAL, SINGLE PIN, KEYSTONE	TESTPOINT, LOOP

## 6 PCB Layout

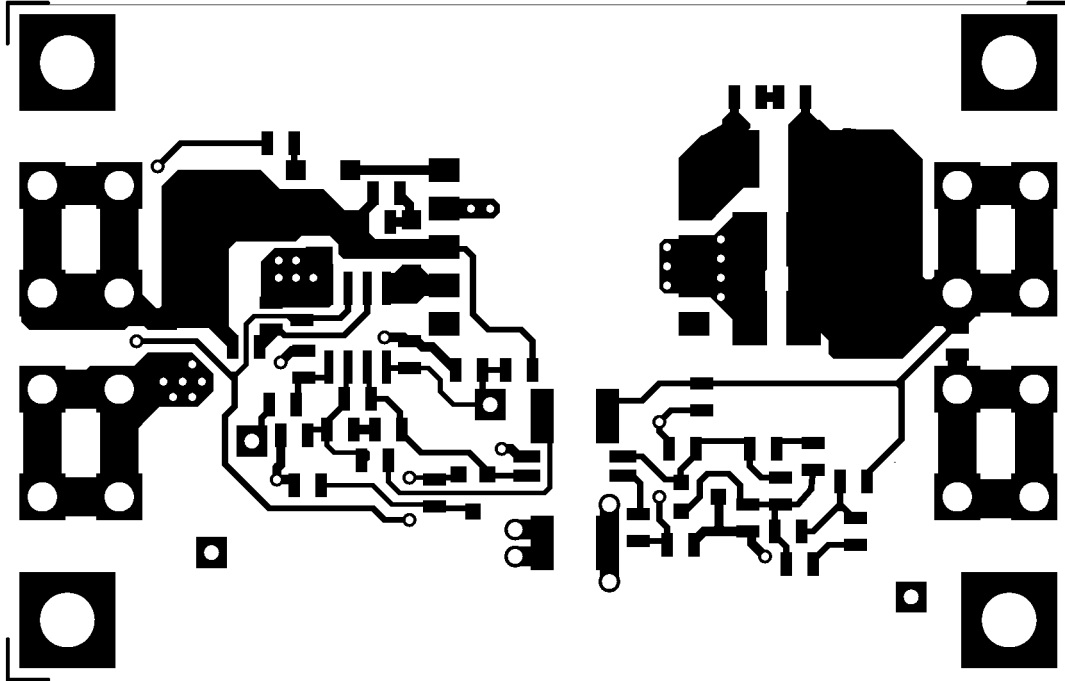


Figure 5. Component Side

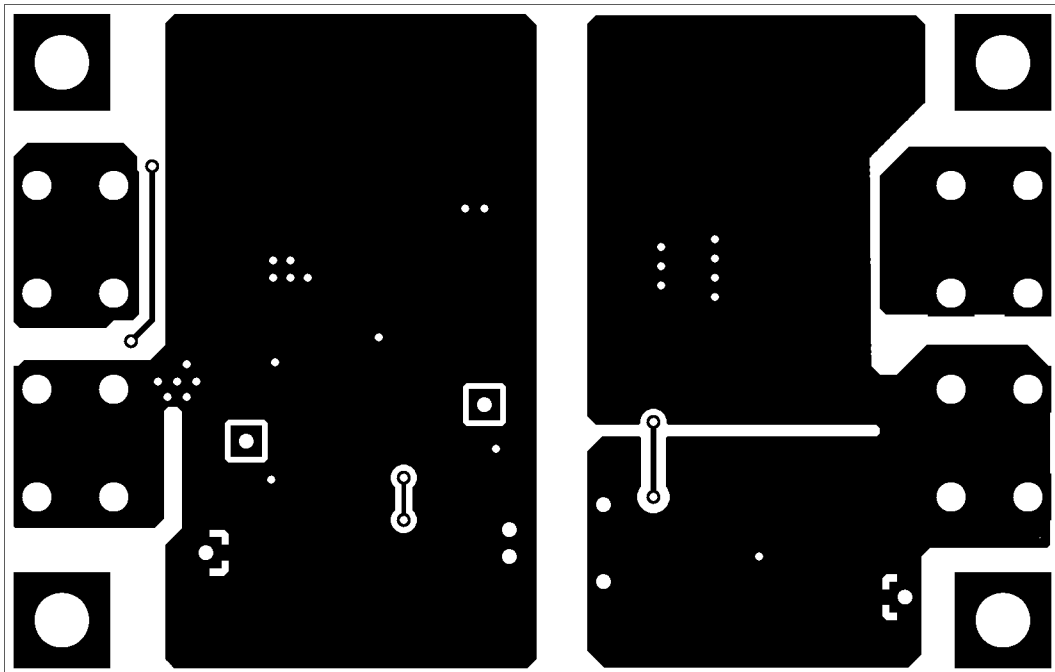


Figure 6. Solder Side

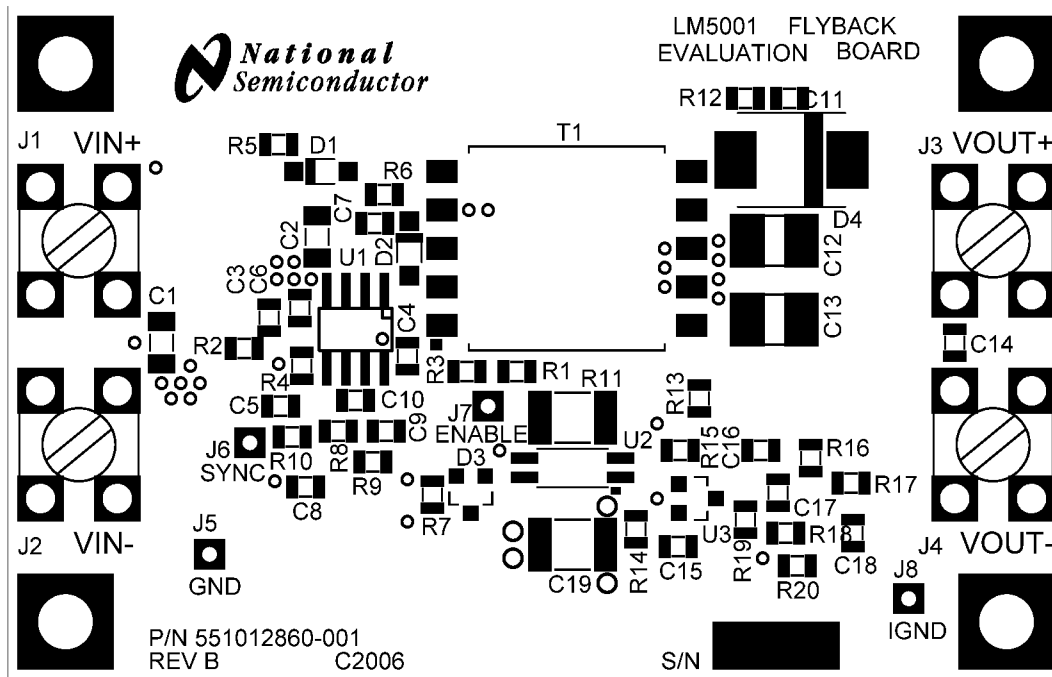


Figure 7. Silkscreen



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