FemtoClock® NG Crystal-to-3.3V, 2.5V Multiple Frequency Clock Generator w/Fanout Buffer

8T49N028

DATA SHEET

General Description

The 8T49N028 is a low RMS phase jitter Clock Synthesizer with selectable internal crystal oscillator or external clock references and eight outputs, configurable as either LVDS, LVPECL or High Impedance.

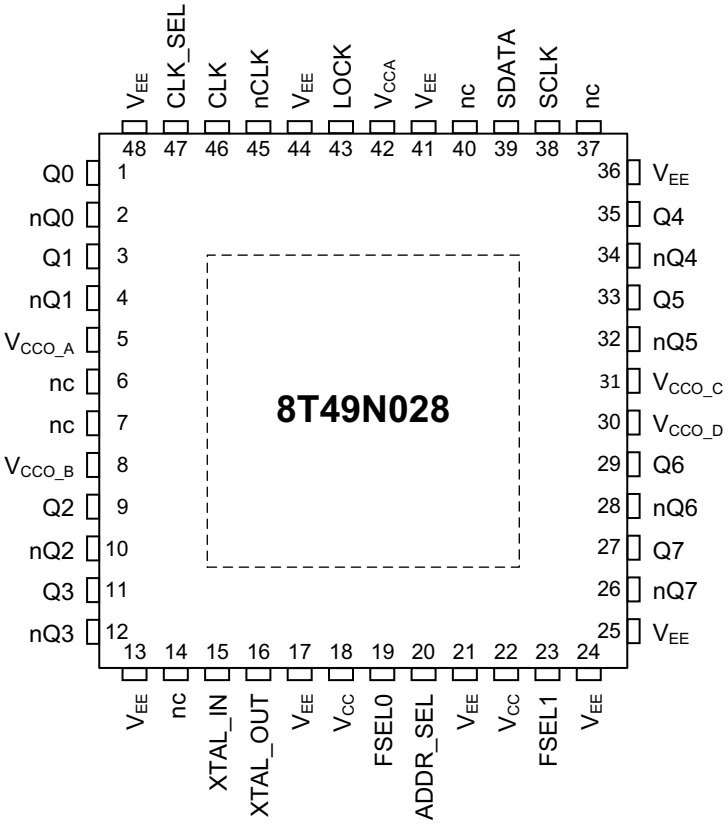
After power up, two frequency select pins determine one of up to four different sets of factory preprogrammed crystal or input frequency and output frequency configurations. From a single input reference, as many as three different output frequencies may be selected for the output banks: two of these frequencies can be generated by the internal crystal oscillator, and/or external clock pre-divider, and/or A output divider, and/or B output divider. The third output frequency is from the B output divider. Device pre-programming can be overwritten through the provided I^2C interface.

Examples of valid frequency configuration setups illustrate this device's flexibility, and are shown in Table 3A. The specific internal register settings for each of the four frequency sets are specified by an IDT order code. Custom codes can be provided by contacting IDT.

Features

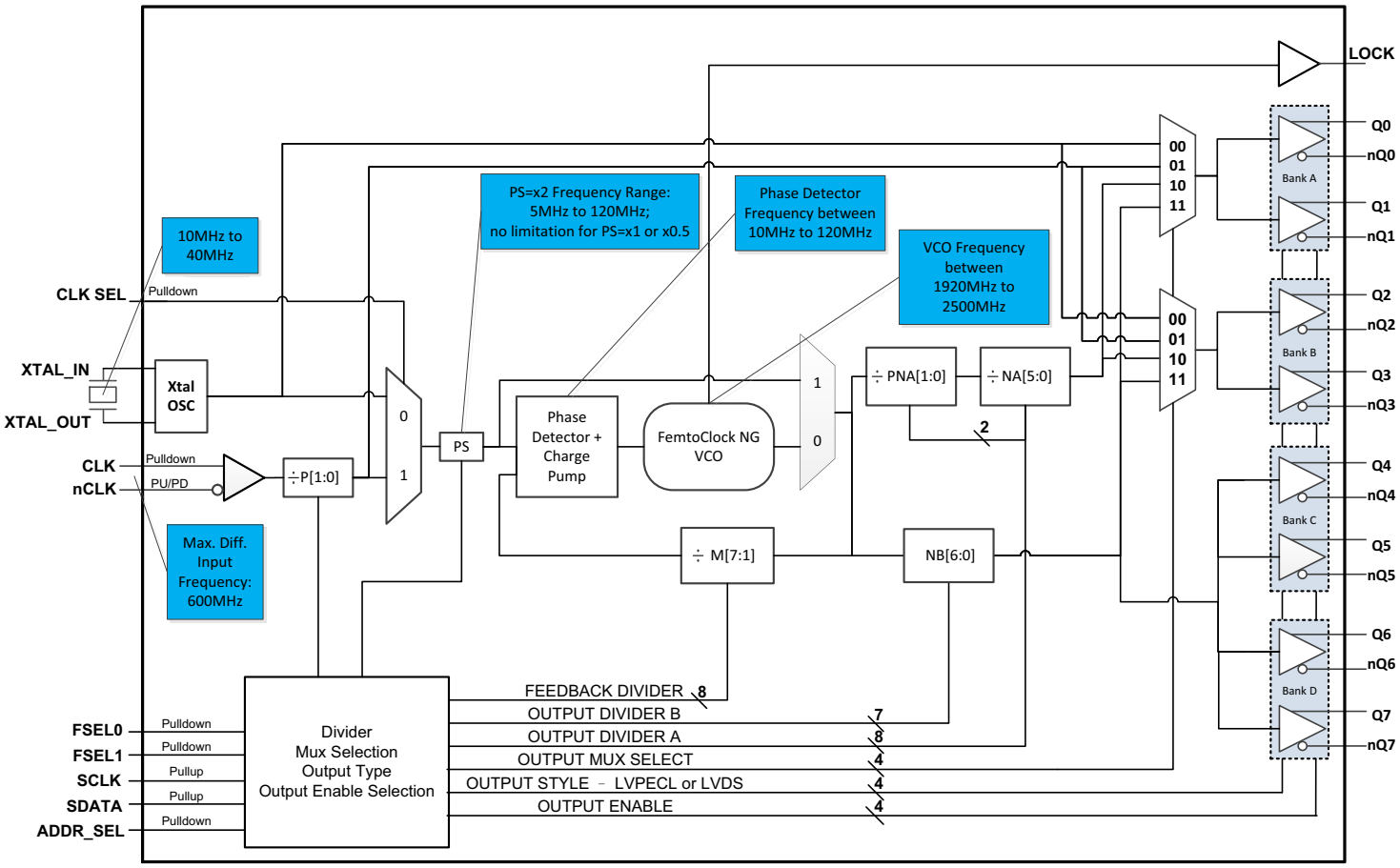
- Fourth Generation FemtoClock NG PLL technology
- Eight selectable LVPECL or LVDS outputs (bank selectable, two output channels per bank)
- CLK, nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- FemtoClock NG VCO Range: 1.92GHz - 2.5GHz
- Bank A and B output frequencies are mux selectable from internal crystal oscillator, reference clock input, output divider A or output divider B
- Clock from OUTPUT DIVIDER A, RMS phase jitter at 156.25MHz (12KHz - 20MHz): 225fs (typical)
- Clock from OUTPUT DIVIDER B, RMS phase jitter at 156.25MHz (12KHz - 20MHz): 219fs (typical)
- Clock from OUTPUT DIVIDER B, RMS phase jitter at 156.25MHz (10kHz - 1MHz): 165fs (typical) Full 2.5V or 3.3V power supply
- Full 2.5V or 3.3V power supply
- I^2C programming interface
- PCI Express (2.5 Gb/S), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) jitter compliant
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Pin Assignment



48-pin, 7mm x 7mm VFQFN Package

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank A)
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank A)
5	V_{CCO_A}	Power		Output supply pins for Bank A
6, 7, 14, 37, 40	nc	Unused		No connect.
8	V_{CCO_B}	Power		Output supply pins for Bank B
9, 10	Q2, nQ2	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank B)
11, 12	Q3, nQ3	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank B)
13, 17, 21, 24, 25, 36, 41, 44, 48	V_{EE} ePAD	Power		Negative supply pins. The Thermal Pad must be connected to V_{EE}.
15, 16	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
18, 22	V_{CC}	Power		Core supply pins.
19, 23	FSEL0, FSEL1	Input	Pulldown	Frequency and configuration. Selects between one of four factory programmable power-up default configurations. The four configurations can have different PLL states, output frequencies, output styles, multiplexer states and output states. These default configurations can be overwritten after power-up via I^2C. LVCMOS/LVTTL interface levels. 00 = Configuration 0 (default) 01 = Configuration 1 10 = Configuration 2 11 = Configuration 3
20	ADDR_SEL	Input	Pulldown	I^2C Address select pin. LVCMOS/LVTTL interface levels.
26, 27	nQ7, Q7	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank D)
28, 29	nQ6, Q6	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank D)
30	V_{CCO_D}	Power		Output supply pins for Bank D.
31	V_{CCO_C}	Power		Output supply pins for Bank C.
32, 33	nQ5, Q5	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank C)
34, 35	nQ4, Q4	Output		Differential output pair. LVPECL or LVDS interface levels. (Bank C)
38	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.
39	SDATA	Input/Output	Pullup	I^2C Data Input. Input: LVCMOS/LVTTL interface levels. Output: Open Drain.
42	V_{CCA}	Power		Analog supply pin.
43	LOCK	Output		PLL Lock Indicator. LVCMOS/LVTTL interface levels.
45	nCLK	Input	Pullup / Pulldown	Inverting differential clock input. Internal resistor bias to $V_{CC}/2$.
46	CLK	Input	Pulldown	Non-inverting differential clock input.
47	CLK_SEL	Input	Pulldown	Input source control pin. LVCMOS/LVTTL interface levels. 0 = XTAL (default) 1 = CLK, nCLK

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	LOCK	$V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_C} = V_{CCO\_D} = 3.465V$		22		Ω
			$V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_C} = V_{CCO\_D} = 2.625V$		27		Ω

Frequency Configuration

Table 3A. Frequency Configuration Examples

divA Frequency (MHz)	divB Frequency (MHz)	Input Frequency (MHz)	Input Clock Divider P	Input Clock Prescaler PS	Feedback Divider M	Output Divider A PNA x NA	Output Divider B NB	VCO Frequency (MHz)
100.00	120.00	25.00	1	x2	48	24	20	2400.00
100.00	125.00	25.00	1	x2	50	25	20	2500.00
100.00	156.25	25.00	1	x2	50	25	16	2500.00
100.00	150.00	25.00	1	x2	48	24	16	2400.00
100.00	250.00	25.00	1	x2	50	25	10	2500.00
100.00	312.50	25.00	1	x2	50	25	8	2500.00
100.00	400.00	25.00	1	x2	48	24	6	2400.00
100.00	500.00	25.00	1	x2	50	25	5	2500.00
100.00	625.00	25.00	1	x2	50	25	4	2500.00
125.00	75.00	25.00	1	x1	90	18	30	2250.00
125.00	156.25	25.00	1	x2	50	20	16	2500.00
125.00	187.50	25.00	1	x1	90	18	12	2250.00
125.00	200.00	25.00	1	x2	40	16	10	2000.00
125.00	250.00	25.00	1	x2	40	16	8	2000.00
125.00	312.50	25.00	1	x2	50	20	8	2500.00
125.00	400.00	25.00	1	x2	40	16	5	2000.00
125.00	500.00	25.00	1	x2	50	20	5	2500.00
125.00	625.00	25.00	1	x2	50	20	4	2500.00
30.72	122.88	19.20	1	x2	64	80	20	2457.60
30.72	153.60	19.20	1	x2	64	80	16	2457.60
122.88	153.60	19.20	1	x2	64	20	16	2457.60
122.88	491.52	19.20	1	x2	64	20	5	2457.60
153.60	491.52	19.20	1	x2	64	16	5	2457.60
155.52	622.08	19.44	1	x2	64	16	4	2488.32
19.20	153.60	30.72	1	x2	40	128	16	2457.60
153.60	491.52	30.72	1	x2	40	16	5	2457.60

NOTE: Each device supports four output frequencies (with related input or crystal value) as selected from this Register Settings Table.
NOTE: XTAL operation: Using divA $f_{OUT} = f_{REF} * PS * [M / (NA \times PNA)]$.
Using divB $f_{OUT} = f_{REF} / P * PS * [M / (NA \times PNA)]$.
Using divB $f_{OUT} = f_{REF} / P * PS * M / NB$.

Table 3B. I²C Register Map

Register	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	0	M0[7]	M0[6]	M0[5]	M0[4]	M0[3]	M0[2]	M0[1]
1	00001	0	M1[7]	M1[6]	M1[5]	M1[4]	M1[3]	M1[2]	M1[1]
2	00010	0	M2[7]	M2[6]	M2[5]	M2[4]	M2[3]	M2[2]	M2[1]
3	00011	0	M3[7]	M3[6]	M3[5]	M3[4]	M3[3]	M3[2]	M3[1]
4	00100	0	NB0[6]	NB0[5]	NB0[4]	NB0[3]	NB0[2]	NB0[1]	NB0[0]
5	00101	0	NB1[6]	NB1[5]	NB1[4]	NB1[3]	NB1[2]	NB1[1]	NB1[0]
6	00110	0	NB2[6]	NB2[5]	NB2[4]	NB2[3]	NB2[2]	NB2[1]	NB2[0]
7	00111	0	NB3[6]	NB3[5]	NB3[4]	NB3[3]	NB3[2]	NB3[1]	NB3[0]
8	01000		BYPASS0	PS0[1]	PS0[0]	P0[1]	P0[0]	CP0[1]	CP0[0]
9	01001		BYPASS1	PS1[1]	PS1[0]	P1[1]	P1[0]	CP1[1]	CP1[0]
10	01010		BYPASS2	PS2[1]	PS2[0]	P2[1]	P2[0]	CP2[1]	CP2[0]
11	01011		BYPASS3	PS3[1]	PS3[0]	P3[1]	P3[0]	CP3[1]	CP3[0]
12	01100	OED0	OEC0	OEB0	OEA0	LVDS_ SELD0	LVDS_ SELC0	LVDS_ SELB0	LVDS_ SELA0
13	01101	OED1	OEC1	OEB1	OEA1	LVDS_ SELD1	LVDS_ SELC1	LVDS_ SELB1	LVDS_ SELA1
14	01110	OED2	OEC2	OEB2	OEA2	LVDS_ SELD2	LVDS_ SELC2	LVDS_ SELB2	LVDS_ SELA2
15	01111	OED3	OEC3	OEB3	OEA3	LVDS_ SELD3	LVDS_ SELC3	LVDS_ SELB3	LVDS_ SELA3
16	10000	0	0	0	0	MUXB0[1]	MUXB0[0]	MUXA0[1]	MUXA0[0]
17	10001	0	0	0	0	MUXB1[1]	MUXB1[0]	MUXA1[1]	MUXA1[0]
18	10010	0	0	0	0	MUXB2[1]	MUXB2[0]	MUXA2[1]	MUXA2[0]
19	10011	0	0	0	0	MUXB3[1]	MUXB3[0]	MUXA3[1]	MUXA3[0]
20	10100	PNA0[1]	PNA0[0]	NA0[5]	NA0[4]	NA0[3]	NA0[2]	NA0[1]	NA0[0]
21	10101	PNA1[1]	PNA1[0]	NA1[5]	NA1[4]	NA1[3]	NA1[2]	NA1[1]	NA1[0]
22	10110	PNA2[1]	PNA2[0]	NA2[5]	NA2[4]	NA2[3]	NA2[2]	NA2[1]	NA2[0]
23	10111	PNA3[1]	PNA3[0]	NA3[5]	NA3[4]	NA3[3]	NA3[2]	NA3[1]	NA3[0]

NOTE: OEx, LVDS_SELx registers control the Output Bank State and not the Individual Output Channel State.

Table 3C. I^2C Function Descriptions

Bits	Name	Function
Mn[7:1]	Integer Feedback Divider Register n (n = 0...3)	Sets the integer feedback divider value. Based on the FemtoClock NG VCO range, the applicable feedback dividers settings are 16 thru 250. Please note the register value presents bits [7:1] of Mn, the LSB of Mn is not in the register. Mn[7:1] bits are programmed with values to support default configuration settings for FSEL[1:0].
NBn[6:0]	Output Divider Register B n (n = 0...3)	Sets the output divider B. The output divider value can range from 2, 3, 4, 5, 6 and 8, 10, 12 to 126 (step: 2). See Table 3I for the output divider coding. NBn[6:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
BYPASSn	PLL Bypass Register n (n = 0...3)	Bypasses PLL Output of the prescaler is routed through the output divider N to the output fanout buffer. Programming a 1 to this bit bypasses the PLL. Programming a 0 to this bit routes the output of the prescaler through the PLL. BYPASSn bits are programmed with values to support default configuration setting for FSEL[1:0]
PSn(1:0)	Input Prescaler Register n (n = 0...3)	Sets the PLL input clock prescaler value. Valid prescaler values are x0.5, x1 or x2. See Table 3E. Set prescaler to x2 for optimum phase noise performance. PSn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
Pn[1:0]	Input Clock Divider Register n (n = 0...3)	Sets the PLL input clock divider. The divider value has the range of 1, 2, 4 and 5. See Table 3E. Pn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
CPn[1:0]	PLL Bandwidth Register n (n = 0...3)	Sets the FemtoClock NG PLL bandwidth by controlling the charge pump current. See Table 3J. CPn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
OEAn OEBn OECn OEDn	Output Enable Register n (n = 0...3)	Sets the outputs to Active or High Impedance. Programming a 0 to this bit sets the outputs to High Impedance. Programming a 1 sets the outputs to active status. OEAn(Bank A), OEBn(Bank B), OECn(Bank C), OEDn(Bank D) bits are programmed with values to support default configuration settings for FSEL[1:0].
LVDS_SELAn LVDS_SELBn LVDS_SELCn LVDS_SELDn	Output Style Register n (n = 0...3)	Sets the differential output style to either LVDS or LVPECL interface levels. Programming a 1 to this bit sets the output styles to LVDS levels. Programming a 0 to this bit sets the output styles to LVPECL levels. LVDS_SELAn(Bank A), LVDS_SELBn(Bank B), LVDS_SELCn (Bank C), LVDS_SELDn(Bank D) bits are programmed with values to support default configuration settings for FSEL[1:0].
MUXAn[1:0] MUXBn[1:0]	MUX Select Register n (n = 0...3)	Sets the multiplexer input to either Crystal Input, Reference Clock Input, Divider A, or Divider B. See Tables 3K and 3L. MUXAn[1:0], MUXBn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
PNAn[1:0]	Output Pre-Divider Register A n (n = 0...3)	Sets the pre output divider A. The output divider value are 2, 3, or 5. See Table 3F for the output divider coding. PNAn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
NAn[5:0]	Output Divider Register A n (n = 0...3)	Sets the output divider A. The output divider value can range from 1 to 63. See Table 3G for the output divider coding. NAn[5:0] bits are programmed with values to support default configuration settings for FSEL[1:0].

Table 3D. PLL Frequency Range Setting

	Frequency Range (MHz)
Phase Detector	10 – 120
x2 Circuitry (PS)	5 – 120

Table 3E. Feedback Divider Mn Coding

Register Bit Mx[8:1]	Feedback Divider Mx
Do Not Use	1 thru 15
00001000	16
00001001	18
00001010	20
00001011	22
…	…
01111100	248
01111101	250

Table 3F. PLL Pre Output Divider PNA Coding

Register Bit PNA_x[1:0]	Pre Output Divider A PNA
00	2
01	3
10	5
11	2

Table 3G. PLL Output Divider NA Coding

Register Bit NA_x[5:0]	Output Divider N
000000	n/a
000001	n/a
000010	2
000011	3
000100	4
000101	5
000110	6
000111	7
001000	8
001001	9
001010	10
001011	11
…	…
111111	63

Table 3H. PLL Output Divider PNA and NA Coding

Register Bit	Register Bit	Output Divider	Output Frequency Range	
PNA_n[1:0]	NA_n[5:0]		f_{OUT_MIN} (MHz)	f_{OUT_MAX} (MHz)
00	000000	n/a	n/a	n/a
00	000001	n/a	n/a	n/a
00	000010	4	480.00	625.00
00	…	NAn * 2	(960 ÷ *NAn*)	(1250 ÷ *NAn*)
00	111111	126	15.24 (approx.)	19.84 (approx.)
01	000000	n/a	n/a	n/a
01	000001	n/a	n/a	n/a
01	000010	6	320.00	416.67
01	…	NAn * 3	(640 ÷ *NAn*)	(833.33 ÷ *NAn*)
01	111111	189	10.16 (approx.)	13.23 (approx.)
10	000000	n/a	n/a	n/a
10	000001	n/a	n/a	n/a
10	000010	10	192.00	250.00
10	…	NAn * 5	(384 ÷ *N*An)	(500 ÷ *NAn*)
10	111111	315	6.10 (approx.)	7.94 (approx.)
11	000000	n/a	n/a	n/a
11	000001	n/a	n/a	n/a
11	000010	4	480.00	625.00
11	…	NAn * 2	(960 ÷ *NAn*)	(1250 ÷ *NAn*)
11	111111	126	15.24 (approx.)	19.84 (approx.)

Table 3I. PLL Output Divider NB Coding

Register Bit	Output Divider N	Output Frequency Range	
NB_n[6:0]		f_{OUT_MIN} (MHz)	f_{OUT_MAX} (MHz)
000000X	n/a	n/a	
0000010	2	960.00	1250.00
0000011	3	640.00	833.33
0000100	4	480.00	625.00
0000101	5	384.00	500.00
000011X	6	320.00	416.67
000100X	8	240.00	312.5
000101X	10	192.00	250.00
000110X	12	160.00	208.33
000111X	14	137.14 (approx.)	178.57 (approx.)
001000X	16	120.00	156.25
…	NB (even integer)	(1920 ÷ *NBn*)	(2500 ÷ *NBn*)
111101X	124	15.48 (approx.)	20.16 (approx.)
111111X	126	15.24 (approx.)	19.84 (approx.)

NOTE: X denotes “don’t care”.

Table 3J. FemtoClock NG PLL Bandwidth Coding

Register Bit		Feedback Divider Value Range (MHz)	
CPn1	CPn0	Minimum	Maximum
0	0	16	48
0	1	48	100
1	0	100	250
1	1	192	250

NOTE: FemtoClock NG PLL stability is only guaranteed over the feedback divider ranges listed is Table 3F, 3G, 3H, 3I and 3J.

Table 3K. MUXAn (n = 0...3) Clock Source

Register Bit		Selected Clock Source
MUXA[1]	MUXA[0]	
0	0	Crystal Input
0	1	CLK, nCLK
1	0	Output Divider A
1	1	Output Divider B

Table 3L. Bank B MUXn Clock Source

Register Bit		Selected Clock Source
MUXB[1]	MUXB[0]	
0	0	Crystal Input
0	1	CLK, nCLK
1	0	Output Divider A
1	1	Output Divider B

Power-up Default Configuration Description

The 8T49N028 supports a variety of options such as different output styles, number of programmed default frequencies, output enable and operating temperature range. The device options and default frequencies must be specified at the time of order and are programmed by IDT prior to shipment. The document, *Programmable FemtoClock® Ordering Product Information* specifies the available order codes, including the device options and default frequency configurations. Example part number: 8T49N028-001NLGI, specifies a quad frequency clock generator with default frequencies of 25MHz, 100MHz, 156.25MHz and 156.25MHz, with four LVPECL outputs that are enabled after power-up, specified over the industrial temperature range and housed in a lead-free (6/6 RoHS) VFQFN package.

Other order codes with respective programmed frequencies are available from IDT upon request. After power-up changes to the output frequencies are controlled by FSEL[1:0] or the I^2C interface. Changes to the output styles and states of outputs (enabled or disabled) can also be controlled with the I^2C interface after power up.

Table 3M. Power-up Default Settings

FSEL1	FSEL0	Frequency Set	PLL State (On or Bypass)	Output State (Active or High Impedance)	Output Style (LVDS or LVPECL)
0 (default)	0 (default)	Frequency Set 0	PLL State 0	Output State 0	Output Style 0
0	1	Frequency Set 1	PLL State 1	Output State 1	Output Style 1
1	0	Frequency Set 2	PLL State 2	Output State 2	Output Style 2
1	1	Frequency Set 3	PLL State 3	Output State 3	Output Style 3

Serial Interface Configuration Description

The 8T49N028 has an I^2C-compatible configuration interface to access any of the internal registers (Table 3B) for frequency and PLL parameter programming. The 8T49N028 acts as a slave device on the I^2C bus and has the address 0b110111x, where x is set by the value on the ADDR_SEL input (see Tables 3N and 3O). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 3B) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Tables 3P, and 3Q). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate the I^2C read or write transfer after accessing byte #23 by sending a stop command.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Table 3N. I^2C Device Slave Address ADDR_SEL = 0 (default)

1	1	0	1	1	1	0	R/W

Table 3O. I^2C Device Slave Address ADDR_SEL = 1

1	1	0	1	1	1	1	R/W

Table 3P. Block Write Operation

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte P	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

Table 3Q. Block Read Operation

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	ACK	Address byte P	ACK	Repeated START	Slave address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_x} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (SDATA)	10mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: V_{CCO_X} denotes V_{CCO_A} + V_{CCO_B} + V_{CCO_C} + V_{CCO_D}.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = V_{CCO_x} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.062	3.3	V_{CC}	V
V_{CCO_x}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current			27	31	mA
I_{EE}	Power Supply Current	LVPECL		250	286	mA
I_{CC}	Power Supply Current	LVDS		164	188	mA
I_{CCO_x}	Output Supply Current	LVDS		140	162	mA

NOTE: V_{CCO_X} denotes V_{CCO_A} + V_{CCO_B} + V_{CCO_C} + V_{CCO_D}.

Table 4B. Power Supply DC Characteristics, V_{CC} = V_{CCO_x} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.054	2.5	V_{CC}	V
V_{CCO_x}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current			23	27	mA
I_{EE}	Power Supply Current	LVPECL		245	276	mA
I_{CC}	Power Supply Current	LVDS		160	180	mA
I_{CCO}	Output Supply Current	LVDS		140	161	mA

NOTE: V_{CCO_X} denotes V_{CCO_A} + V_{CCO_B} + V_{CCO_C} + V_{CCO_D}.

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO\_x} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SCLK, SDATA, FSEL[1:0], CLK_SEL, ADDR_SEL	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	SCLK, SDATA, CLK_SEL, ADDR_SEL	$V_{CC} = 3.3V$	-0.3		0.8	V
			$V_{CC} = 2.5V$	-0.3		0.7	V
		FSEL[1:0],	$V_{CC} = 3.3V$ or $2.5V$	-0.3		0.5	V
I_{IH}	Input High Current	SCLK, SDATA	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	µA
		FSEL[1:0], CLK_SEL, ADDR_SEL	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	SCLK, SDATA	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
		FSEL[1:0], CLK_SEL, ADDR_SEL	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1	LOCK	$V_{CCO\_x} = 3.465V$	2.6			V
			$V_{CCO\_x} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	LOCK	$V_{CCO\_x} = 3.465V$ or $2.625V$			0.7	V

NOTE: V_{CCO_X} denotes $V_{CCO\_A} + V_{CCO\_B} + V_{CCO\_C} + V_{CCO\_D}$.
NOTE 1: Output terminated with 50Ω to $V_{CCO\_x}/2$. See Parameter Measurement Information, *Output Load Test Circuit* diagrams.

Table 4D. Differential DC Characteristics, $V_{CC} = V_{CCO\_x} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	nCLK	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
		CLK	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.2		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE}		$V_{CC} - 1.0$	V

NOTE: V_{CCO_X} denotes $V_{CCO\_A} + V_{CCO\_B} + V_{CCO\_C} + V_{CCO\_D}$.
NOTE 1: Common mode input voltage is at the cross point.

Table 4E. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_x} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO\_x} - 1.1$		$V_{CCO\_x} - 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO\_x} - 2.0$		$V_{CCO\_x} - 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE: V_{CCO_X} denotes $V_{CCO\_A} + V_{CCO\_B} + V_{CCO\_C} + V_{CCO\_D}$.
NOTE 1: Outputs termination with 50Ω to $V_{CCO\_x} - 2V$.

Table 4F. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_x} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO\_x} - 1.2$		$V_{CCO\_x} - 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO\_x} - 2.0$		$V_{CCO\_x} - 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.5		1.0	V

NOTE: V_{CCO_x} denotes $V_{CCO\_A} + V_{CCO\_B} + V_{CCO\_C} + V_{CCO\_D}$.
NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 4G. LVDS DC Characteristics, $V_{CC} = V_{CCO\_x} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	340	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: V_{CCO_x} denotes $V_{CCO\_A} + V_{CCO\_B} + V_{CCO\_C} + V_{CCO\_D}$.

Table 4H. LVDS DC Characteristics, $V_{CC} = V_{CCO\_x} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	335	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: V_{CCO_x} denotes $V_{CCO\_A} + V_{CCO\_B} + V_{CCO\_C} + V_{CCO\_D}$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Load Capacitance (C_L)		12		18	pF
Equivalent Series Resistance (ESR)				50	Ω

AC Electrical Characteristics

Table 6A. PCI Express Jitter Specifications, V_{CC} = V_{CCO_x} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	Output Divider A, f = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		8	12	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	Output Divider A, f = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.8	1.3	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	Output Divider A, f = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.03	0.06	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	Output Divider A, f = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.17	0.32	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.

NOTE: V_{CCO_X} denotes V_{CCO_A} + V_{CCO_B} + V_{CCO_C} + V_{CCO_D}.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 6B. AC Characteristics, V_{CC} = V_{CCO_x} = 3.3V ± 5% or 2.5V ± 5% V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{DIFF_IN}	Differential Input Frequency; NOTE 1					600	MHz
f_{VCO}	VCO Frequency			1920		2500	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2		25MHz Crystal, f_{OUT} = 25MHz, Integration Range: 1kHz – 1MHz		170	209	fs
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2		25MHz Crystal, f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		321	268	fs
*t*jit(Ø)	RMS Phase Jitter, Random; Output Divider A Output Bank A,B NOTE 2		25MHz Crystal, f_{OUT} = 100MHz, Integration Range: 12kHz – 20MHz		299	376	fs
			25MHz Crystal, f_{OUT} = 125MHz, Integration Range: 12kHz – 20MHz		296	390	fs
			25MHz Crystal, f_{OUT} = 156.25MHz, Integration Range: 12kHz – 20MHz		225	301	fs
			25MHz Crystal, f_{OUT} = 156.25MHz, Integration Range: 10kHz – 1MHz		166	189	fs
			25MHz Crystal, f_{OUT} = 250MHz, Integration Range: 12kHz – 20MHz		259	322	fs
			30.72MHz Crystal, f_{OUT} = 491.52MHz, Integration Range: 12kHz – 20MHz		182	234	fs
			19.44MHz Crystal, f_{OUT} = 622.08MHz, Integration Range: 12kHz – 20MHz		330	415	fs
*t*jit(Ø)	RMS Phase Jitter, Random; Output Divider B, Output Bank C,D NOTE 2		25MHz Crystal, f_{OUT} = 100MHz, Integration Range: 12kHz – 20MHz		240	270	fs
			25MHz Crystal, f_{OUT} = 125MHz, Integration Range: 12kHz – 20MHz		228	273	fs
			25MHz Crystal, f_{OUT} = 156.25MHz, Integration Range: 12kHz – 20MHz		219	257	fs
			25MHz Crystal, f_{OUT} = 156.25MHz, Integration Range: 10kHz – 1MHz		165	193	fs
			25MHz Crystal, f_{OUT} = 250MHz, Integration Range: 12kHz – 20MHz		210	251	fs
			30.72MHz Crystal, f_{OUT} = 491.52MHz, Integration Range: 12kHz – 20MHz		171	204	fs
			19.44MHz Crystal, f_{OUT} = 622.08MHz, Integration Range: 12kHz – 20MHz		320	403	fs
tsk(o)	Output Skew; NOTE 3, 4	LVPECL Outputs	LVDS_SEL = 0			130	ps
		LVDS Outputs	LVDS_SEL = 1			100	ps
tsk(b)	Bank Skew	LVPECL Outputs	LVDS_SEL = 0			40	ps
		LVDS Outputs	LVDS_SEL = 1			30	ps

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% - 80%, LVDS_SEL = 0		250	600	ps
		LVDS Outputs	20% - 80%, LVDS_SEL = 1		270	500	ps
odc	Output Duty Cycle		Output Divider N ≠ 3; LVDS_SEL = 0 or 1	47		53	%
			Output Divider N = 3; LVDS_SEL = 0 or 1	45		55	%
t_{LOCK}	PLL Lock Time; NOTE 4, 5	LOCK Output				20	ms
$t_{TRANSITION}$	Transition Time; NOTE 4, 5	LOCK Output				20	ms

NOTE: V_{CCO_X} denotes V_{CCO_A} + V_{CCO_B} + V_{CCO_C} + V_{CCO_D}.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: The input frequency of the differential input is a physical limitation of the device. Follow the PLL setting to insure proper functionality of the device.

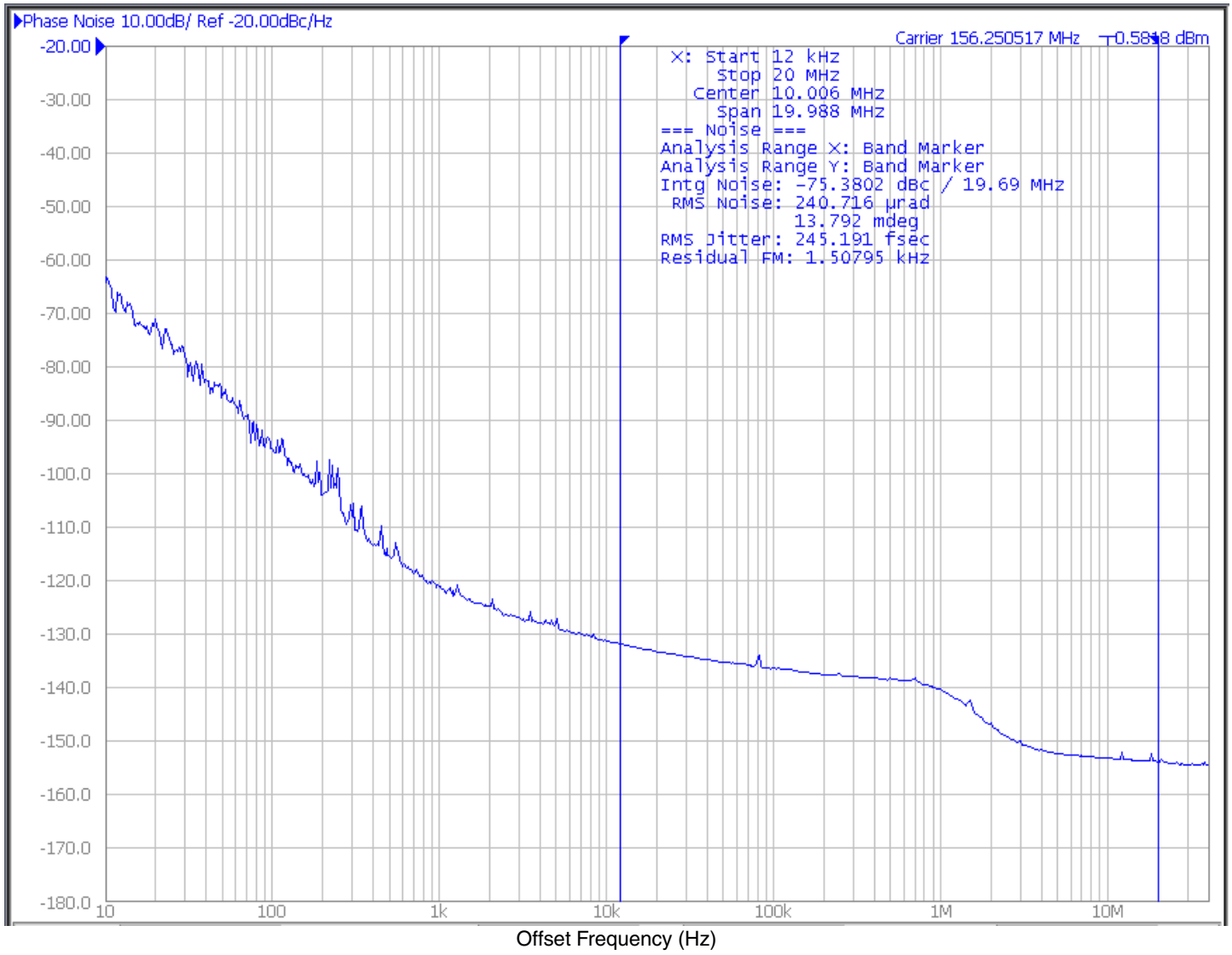
NOTE 2: Refer to Phase Noise Plots.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

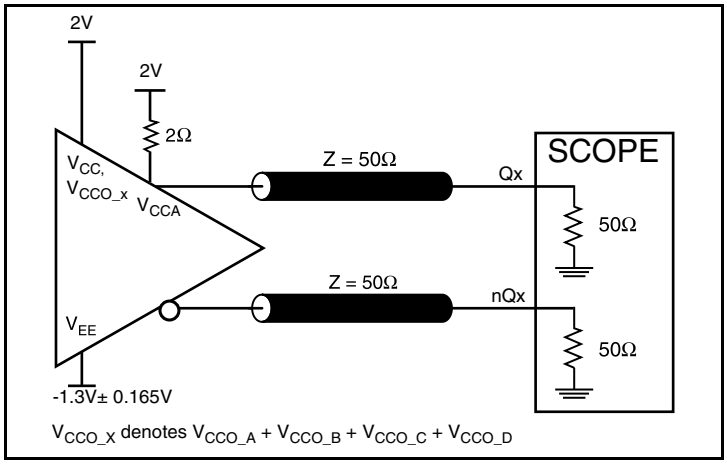
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Refer to t_{LOCK} and $t_{TRANSITION}$ in Parameter Measurement Information.

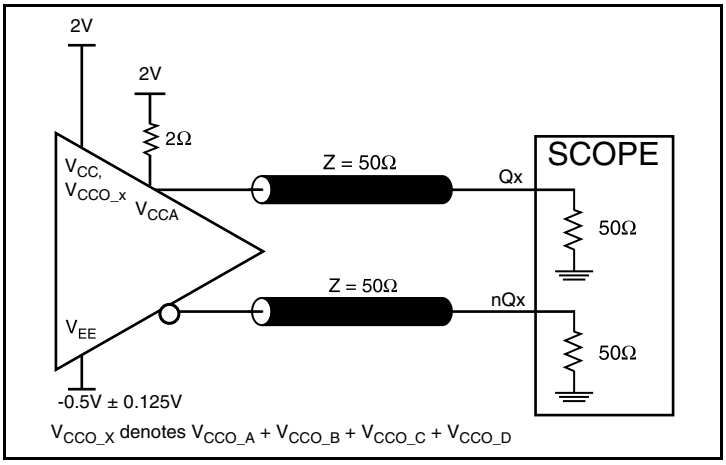
Typical Phase Noise at 156.25MHz



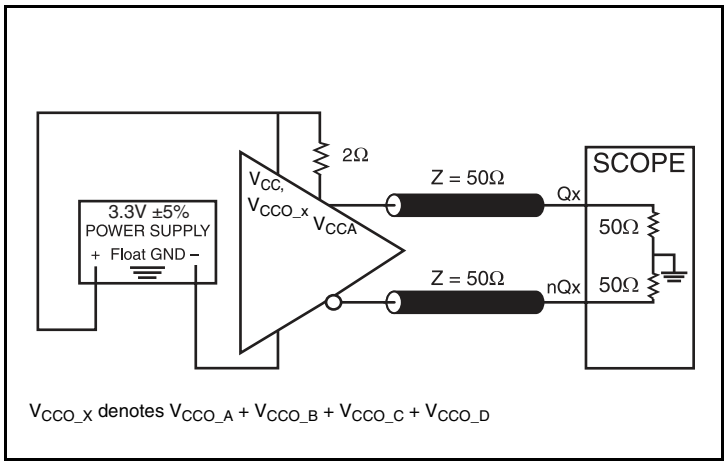
Parameter Measurement Information



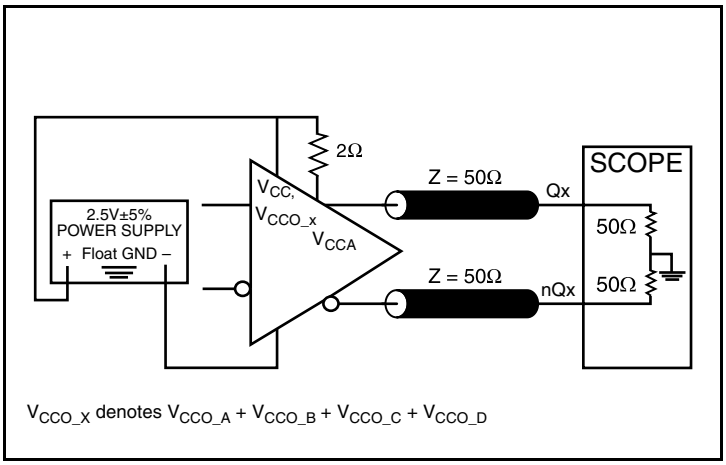
3.3V LVPECL Output Load Test Circuit



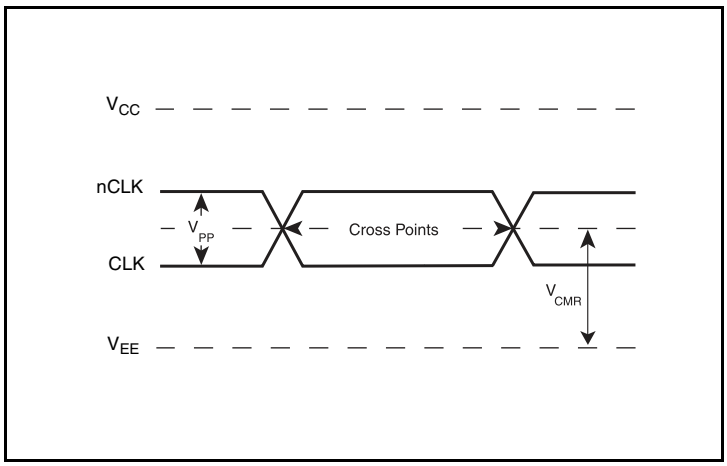
2.5V LVPECL Output Load Test Circuit



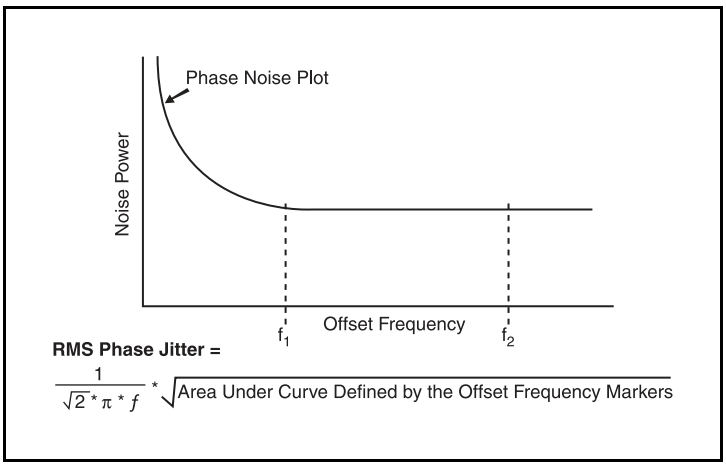
3.3V LVDS Output Load Test Circuit



2.5V LVDS Output Load Test Circuit

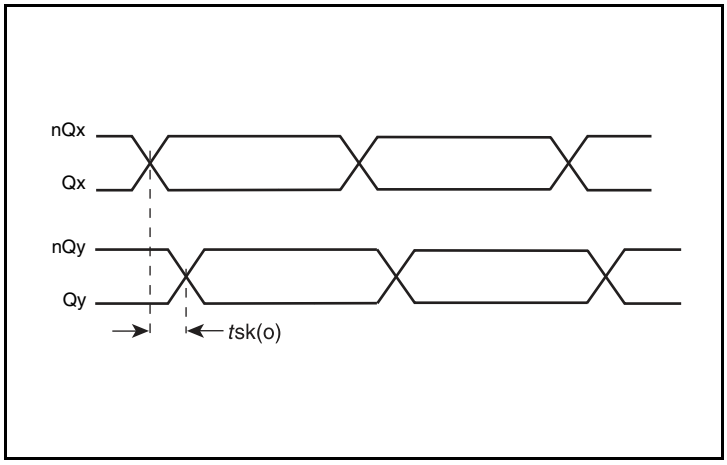


Differential Input Levels

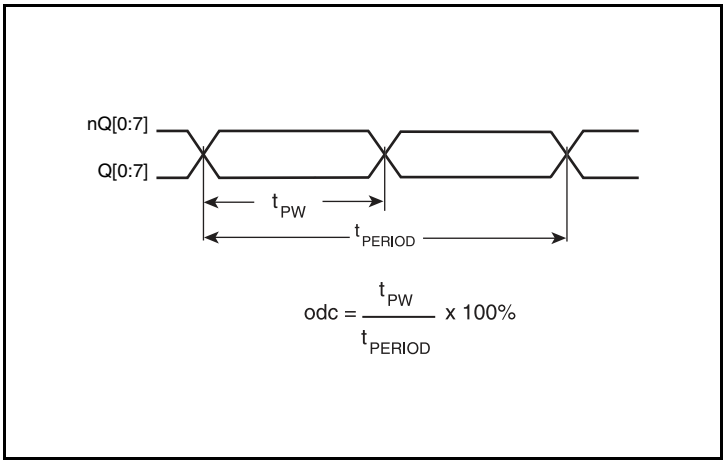


RMS Phase Jitter

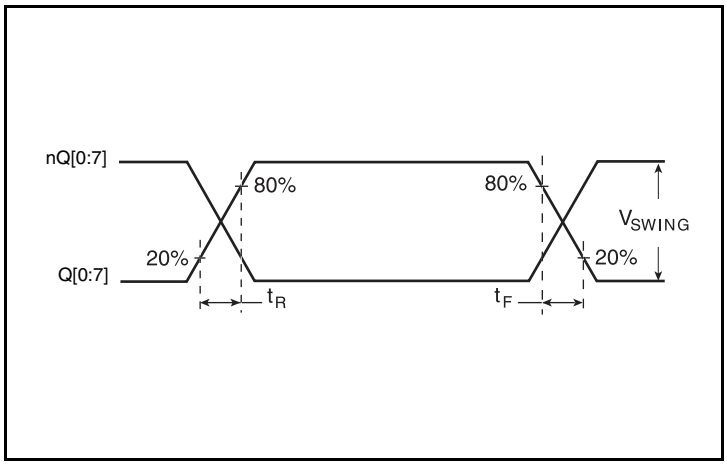
Parameter Measurement Information, continued



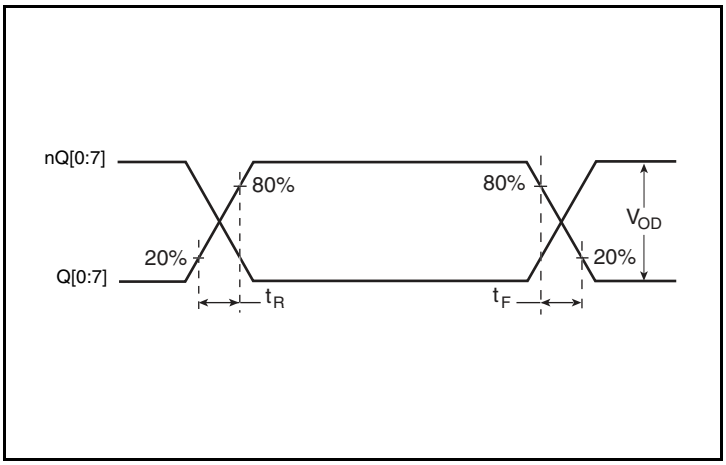
Output Skew



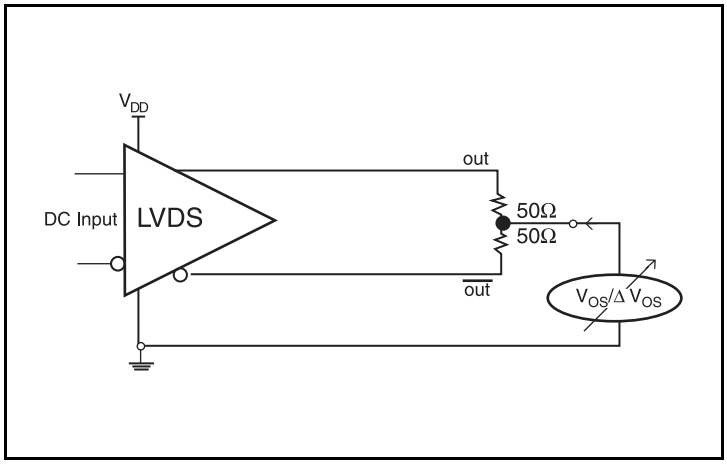
Output Duty Cycle/Pulse Width/Period



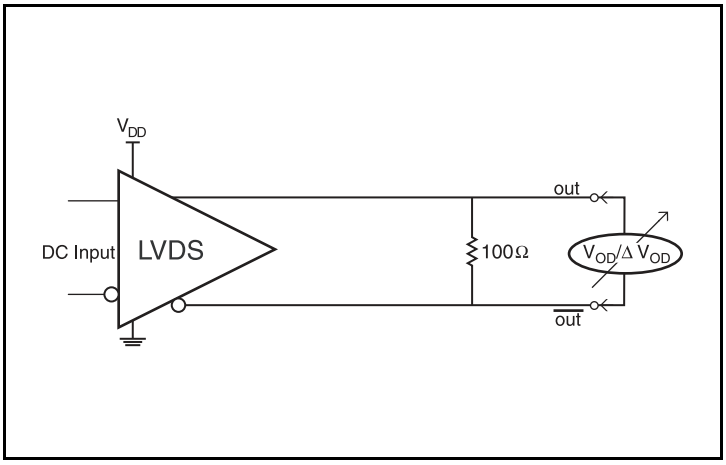
LVPECL Output Rise/Fall Time



LVDS Output Rise/Fall Time

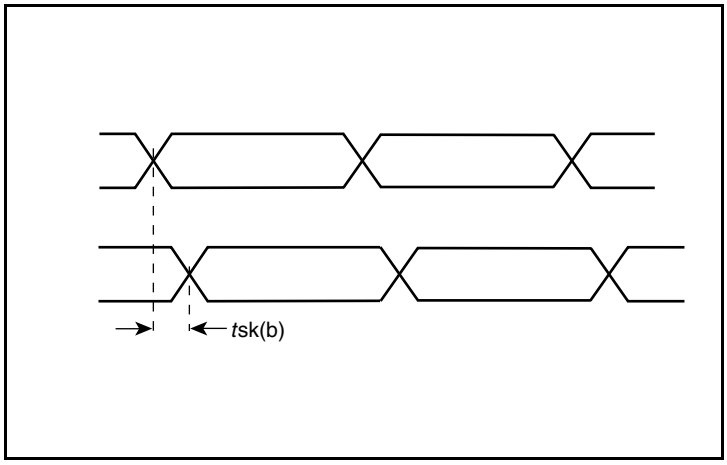


Offset Voltage Setup

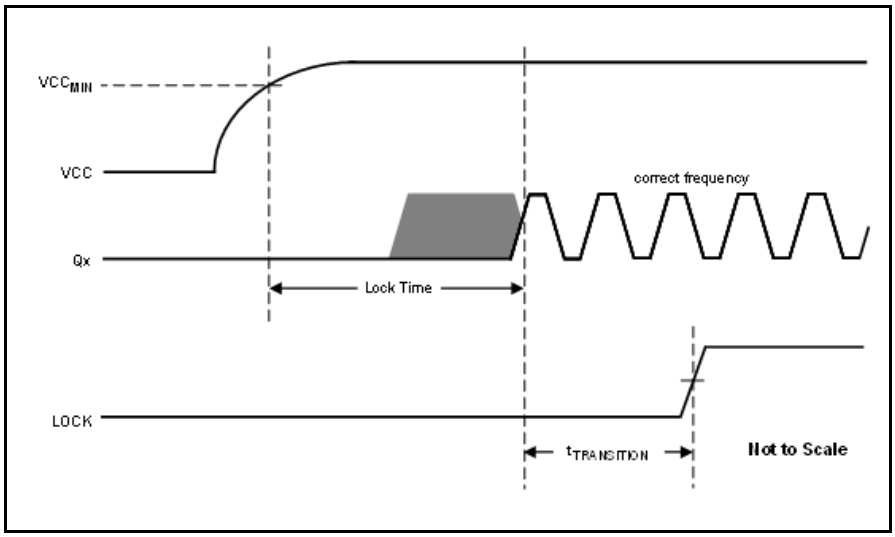


Differential Output Voltage Setup

Parameter Measurement Information, continued



Bank Skew



Lock Time & Transition Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Crystal Input Interface

The 8T49N028 has been characterized with 12pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 12pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

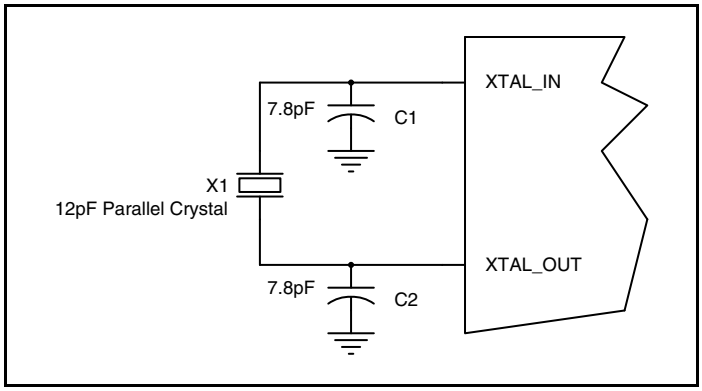


Figure 1. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

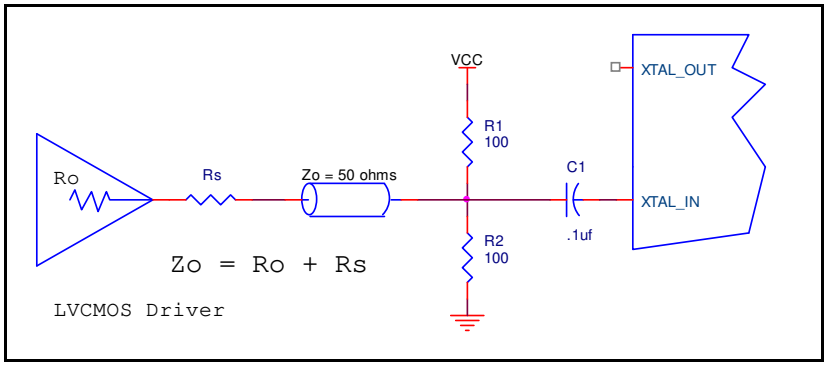


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

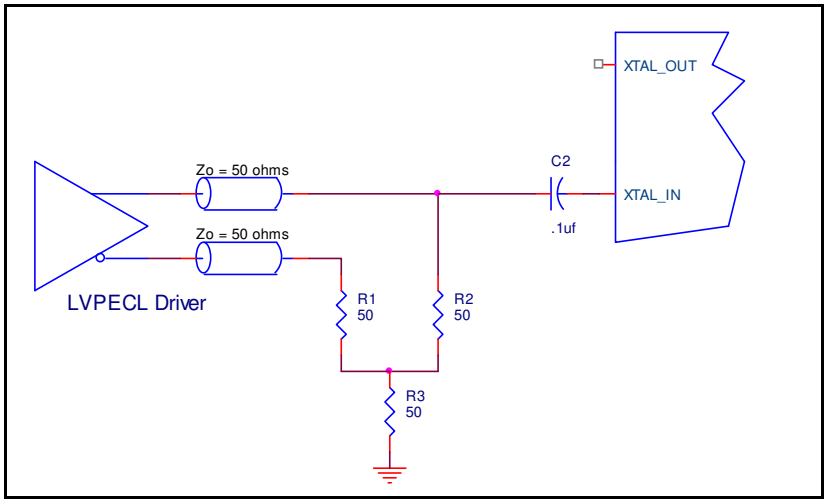


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

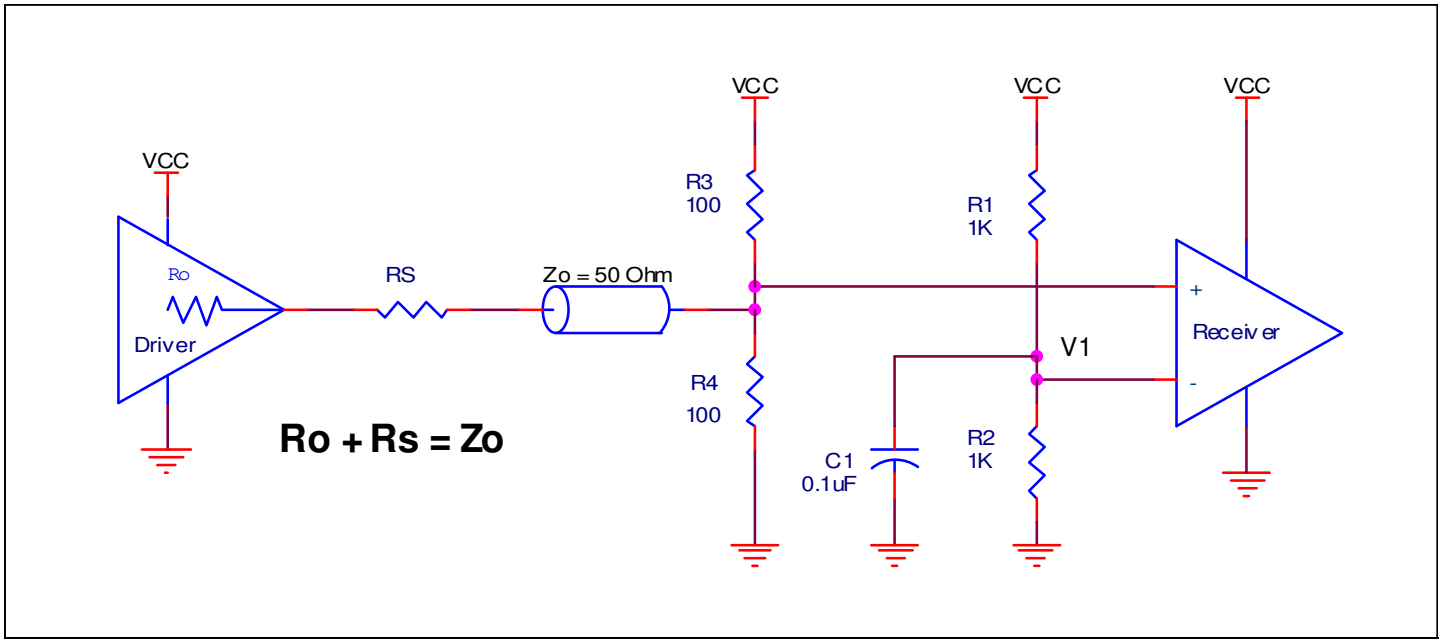


Figure 3. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

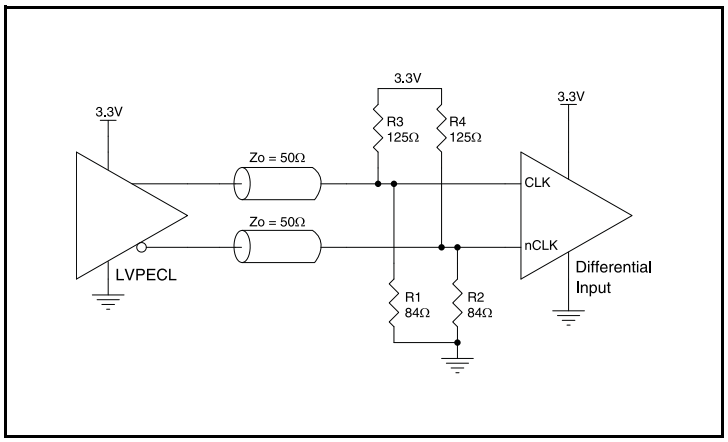


Figure 4A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

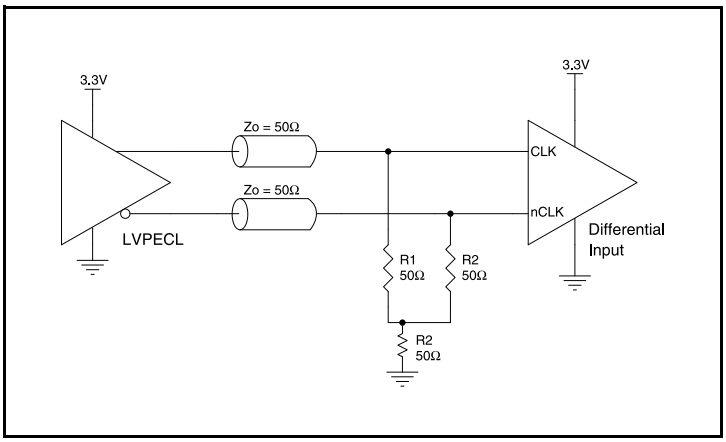


Figure 4B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

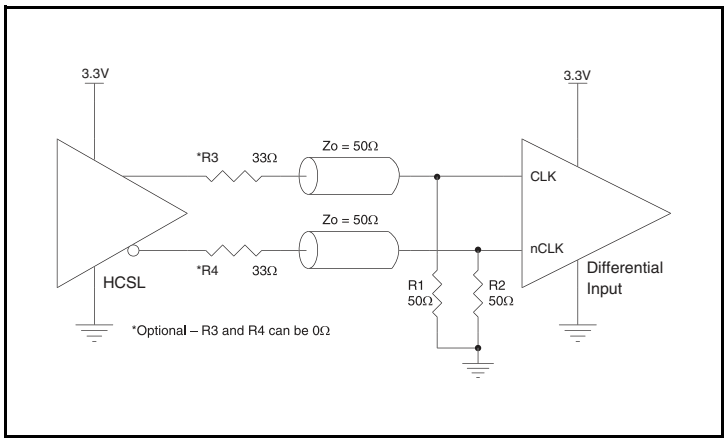


Figure 4C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

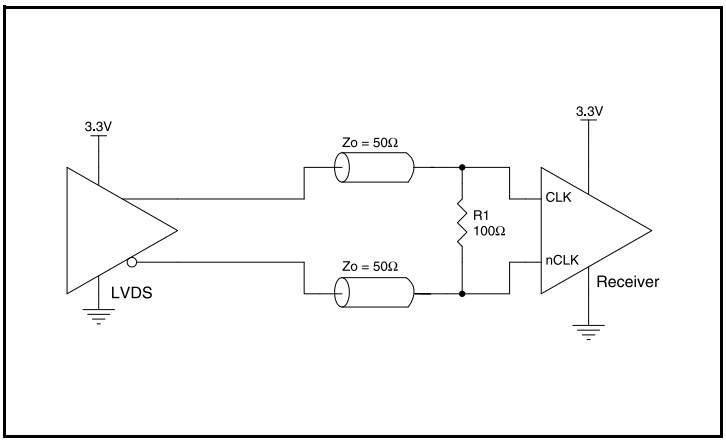


Figure 4D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

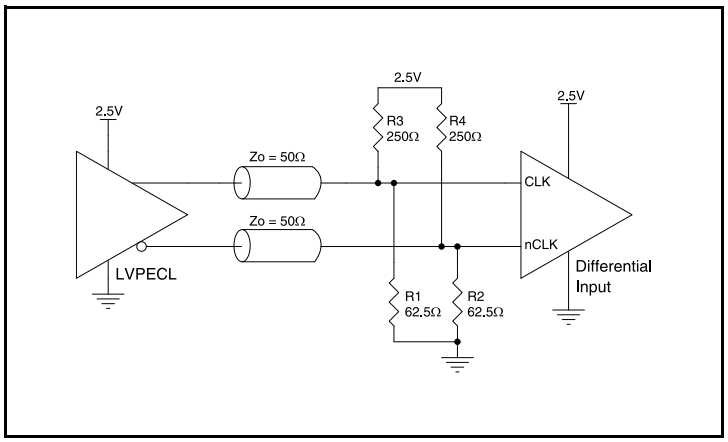


Figure 5A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

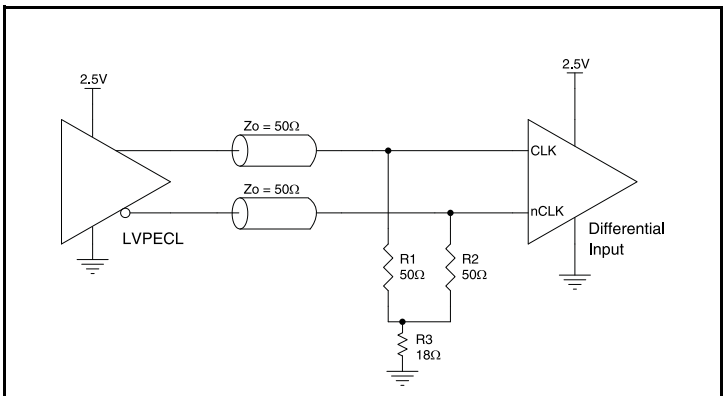


Figure 5B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

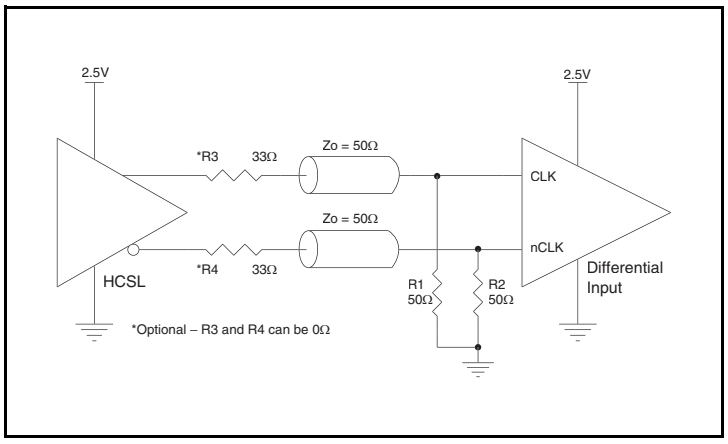


Figure 5C. CLK/nCLK Input Driven by a 2.5V HCSL Driver

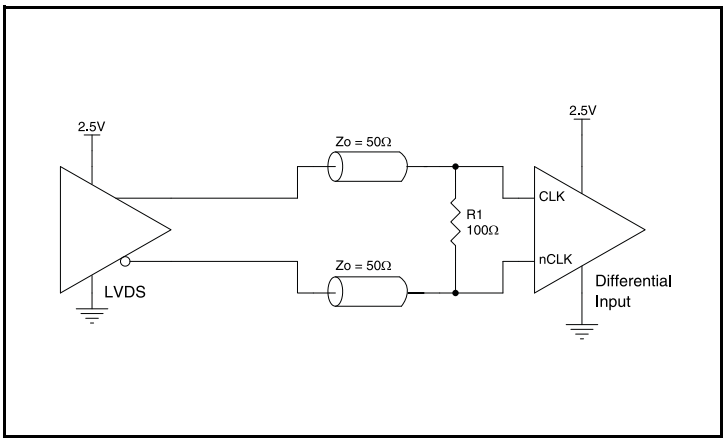


Figure 5D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 6A* can be used with either type of output structure. *Figure 6B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

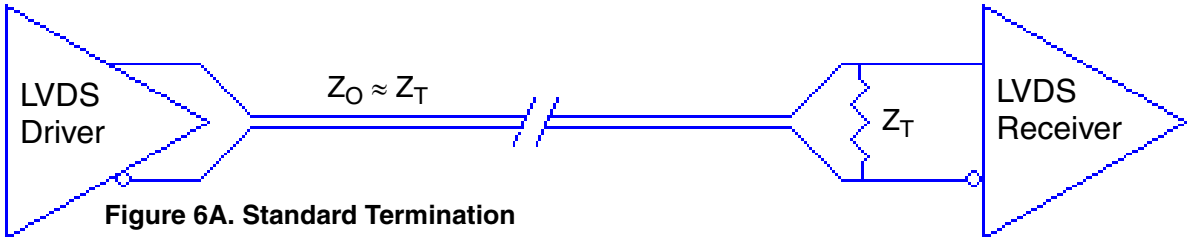


Figure 6A. Standard Termination

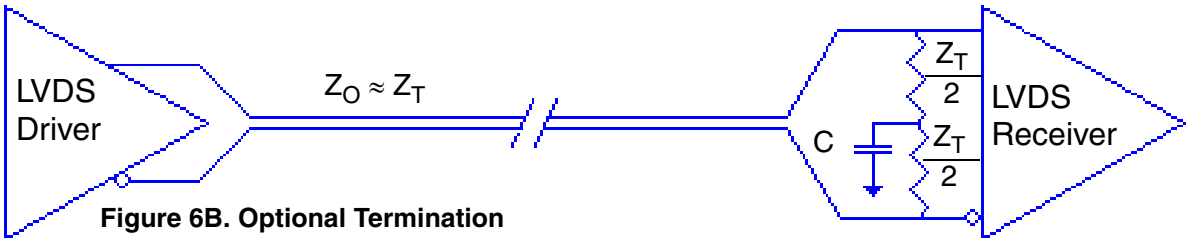


Figure 6B. Optional Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

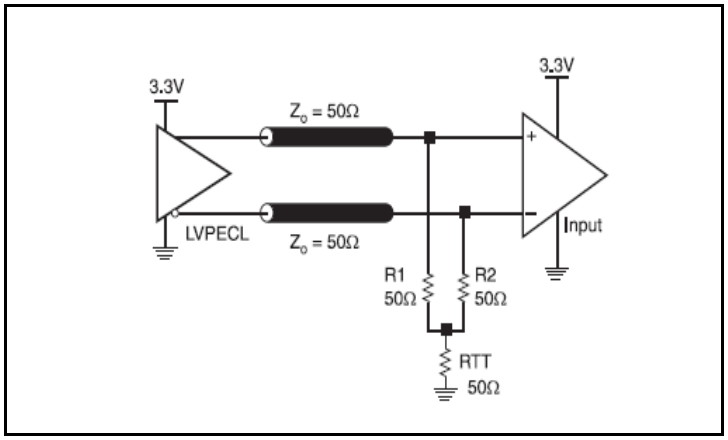


Figure 7A. 3.3V LVPECL Output Termination

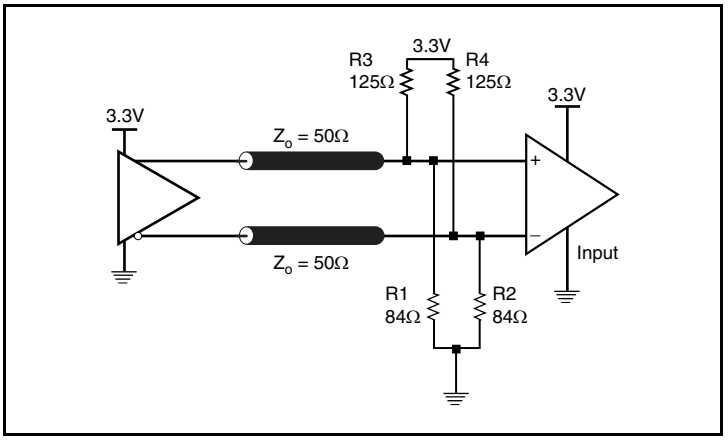


Figure 7B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 8A and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 8B can be eliminated and the termination is shown in *Figure 8C.*

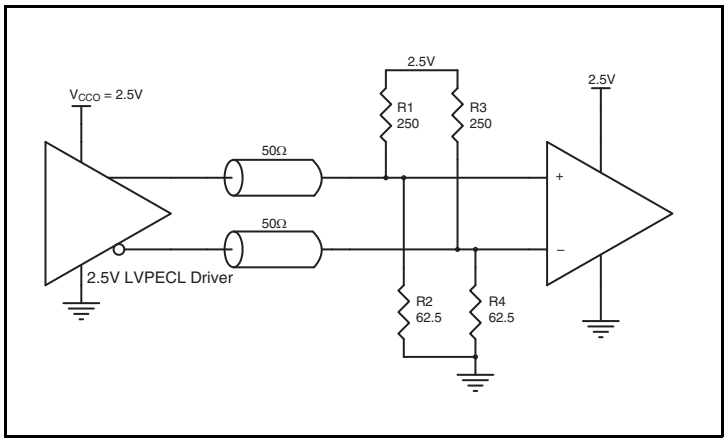


Figure 8A. 2.5V LVPECL Driver Termination Example

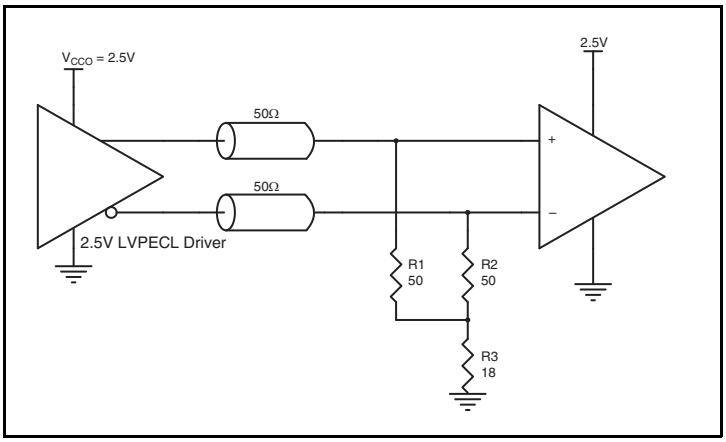


Figure 8B. 2.5V LVPECL Driver Termination Example

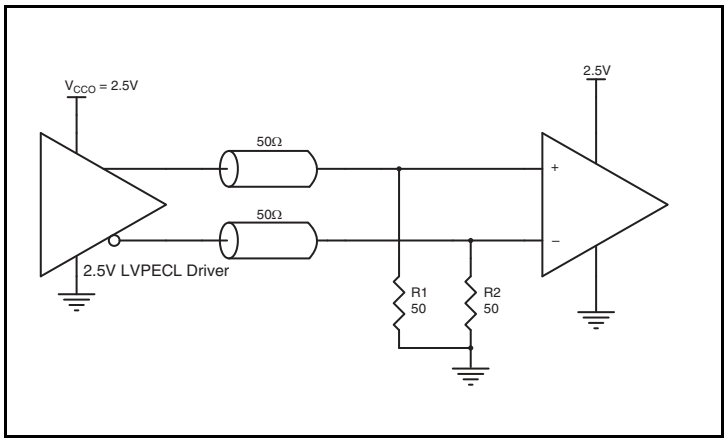


Figure 8C. 2.5V LVPECL Driver Termination Example

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

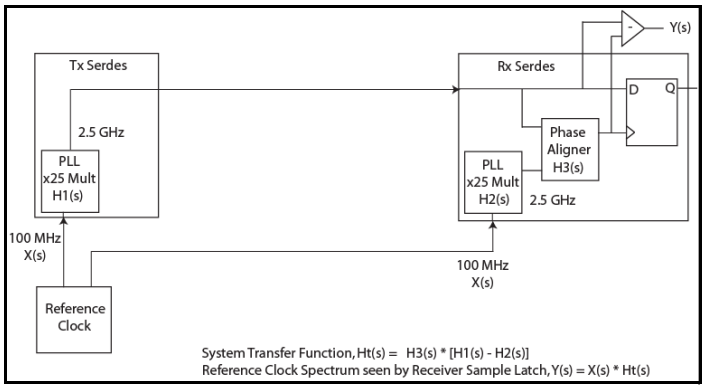
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

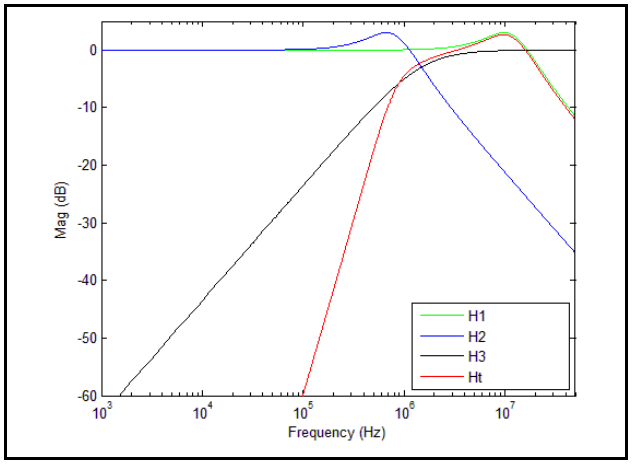
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



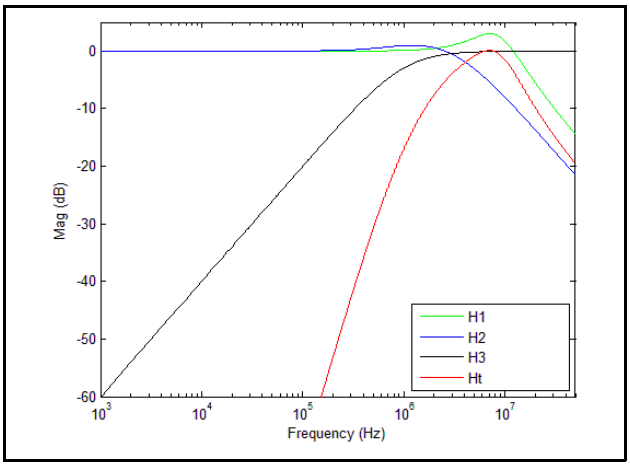
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

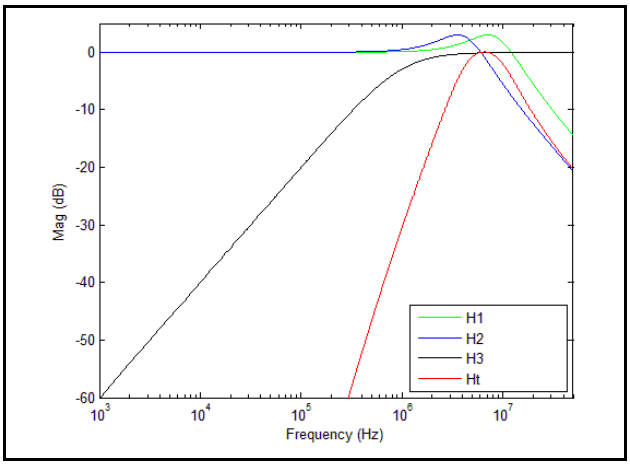


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

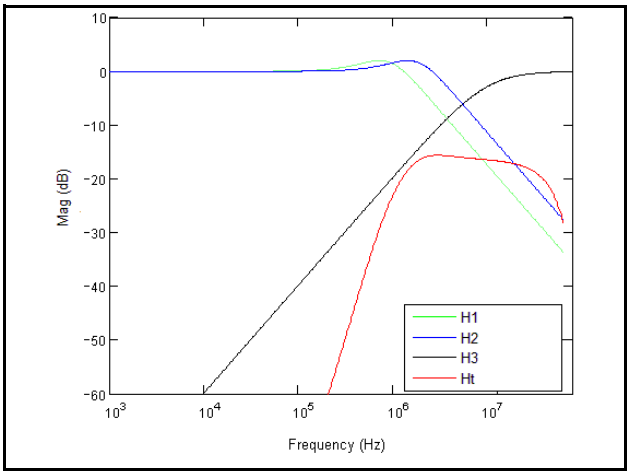


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T49N028. Equations and example calculations are also provided.

LVPECL Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T49N028 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum currents at 85°C is as follows:

I_{EE_MAX} = 286mA

- Power $(core)_{MAX} = I_{EE\_MAX} * V_{CC\_MAX}$ = 3.465V * 286mA = **990.99mW**

- Power $(outputs)_{MAX}$ = **31.55mW/Loaded Output pair**

  If all outputs are loaded, the total power is 8 * 31.55mW = **252.4mW**

Total Power$_{\_MAX}$ = 990.99Mw + 252.4Mw = **1243.39mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 30°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.243W * 31.55°C/W = 122.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	30°C/W	23.1°C/W	19.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 9.*

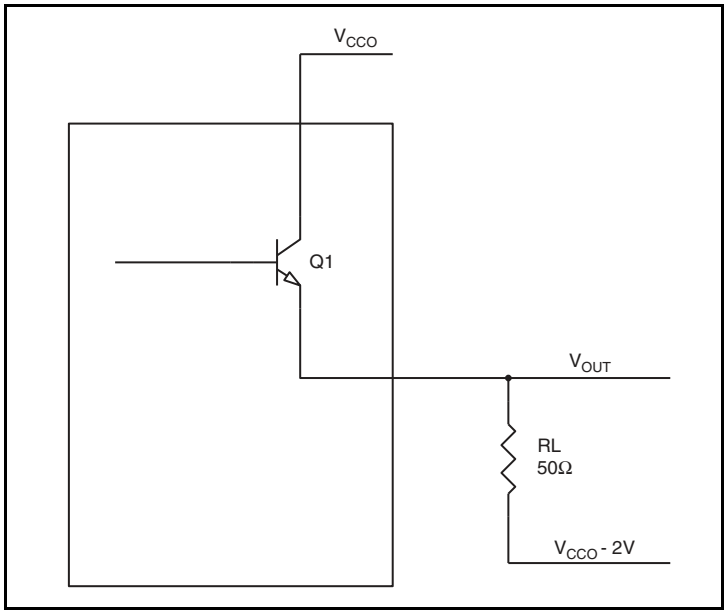


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.75V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.6V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.75V)/50\Omega] * 0.75V =$ **18.75mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.55mW**

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T49N028.
Equations and example calculations are also provided.

LVDS Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T49N028 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum currents at 85°C is as follows:

I_{CC} = 188mA

I_{CCA} = 31mA

I_{CCOX} = 162mA

- Power $(core)_{MAX}$ = $(I_{CC\_MAX} + I_{CCA\_MAX} + I_{CCOX\_MAX}) * V_{DD\_MAX}$
  = (188mA + 31mA + 162mA)*3.465V = **1320.165mW**

Total Power$_{_MAX}$ = 1320.165mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 30°C/W per Table 7.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.320W * 30°C/W = 124.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Reliability Information

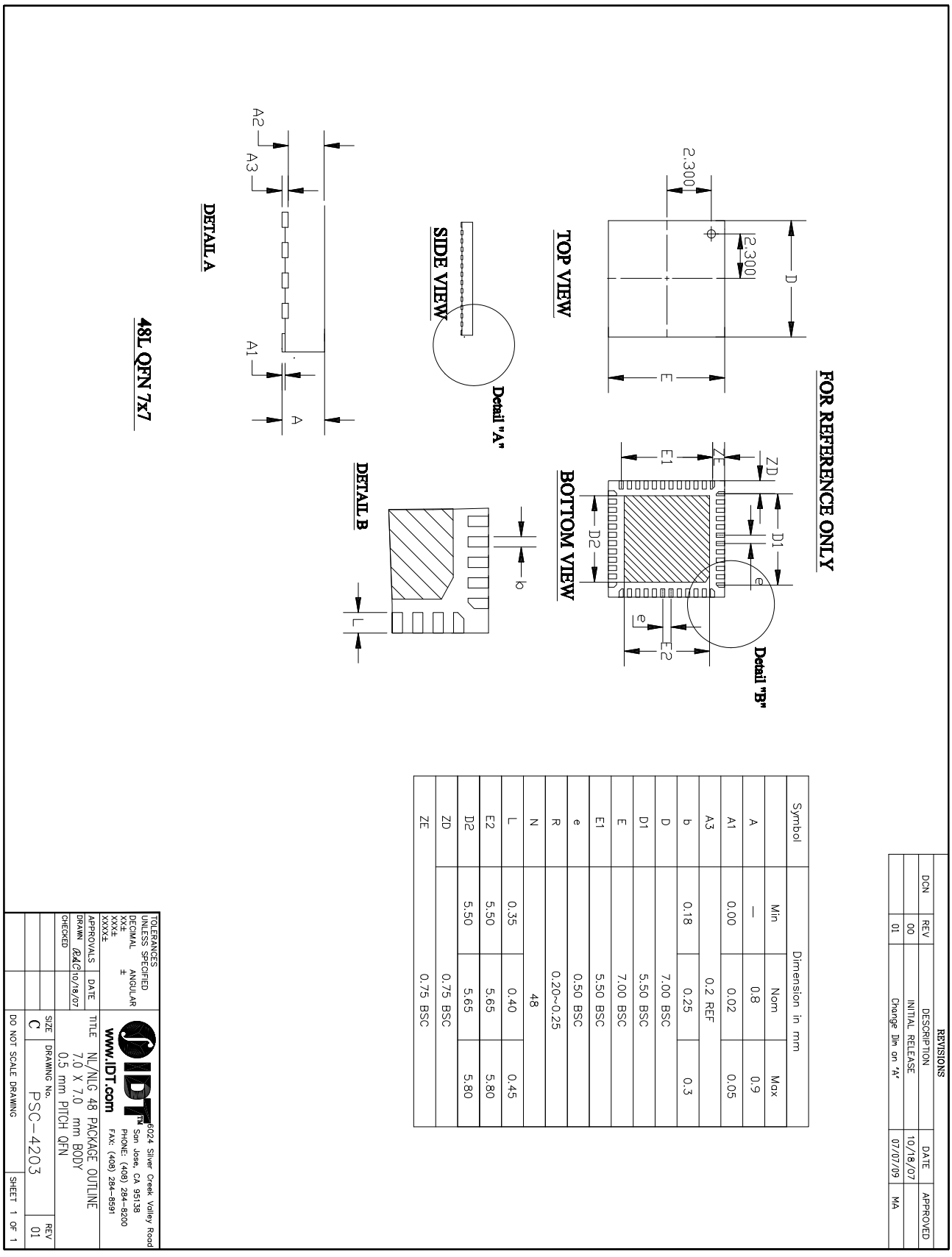
Table 8. θ_{JA} vs. Air Flow Table for a 48-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	30°C/W	23.1°C/W	19.8°C/W

Transistor Count

The transistor count for 8T49N028 is 34,106.

48-Lead VFQFN NL Package Outline and Package Dimensions



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	0.8	0.9
A1	0.00	0.02	0.05
A3		0.2 REF	
b	0.18	0.25	0.3
D		7.00 BSC	
D1		5.50 BSC	
E		7.00 BSC	
E1		5.50 BSC	
e		0.50 BSC	
R		0.20~0.25	
N		48	
L	0.35	0.40	0.45
E2	5.50	5.65	5.80
D2	5.50	5.65	5.80
ZD		0.75 BSC	
ZE		0.75 BSC	

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	10/18/07	
01		Change Dim on 'A'	07/07/09	MA

TOLERANCES UNLESS SPECIFIED
DECIMAL ± ANGULAR ±
XXX±
XXXX±

APPROVALS DATE
DRAWN RAC 10/16/07
CHECKED

IDT™ 6024 Silver Creek Valley Road San Jose, CA 95138
www.IDT.com PHONE: (408) 284-8200 FAX: (408) 284-8591

TITLE NL/NLG 48 PACKAGE OUTLINE 7.0 X 7.0 mm BODY 0.5 mm PITCH QFN

SIZE C | DRAWING No. PSC-4203 | REV 01

DO NOT SCALE DRAWING | SHEET 1 OF 1

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N028-dddNLGI	IDT8T49N028-dddNLGI	“Lead-Free” 48-Lead VFQFN	Tray	-40°C to 85°C
8T49N028-dddNLGI8	IDT8T49N028-dddNLGI	“Lead-Free” 48-Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: For the specific -ddd order codes, refer to *Programmable FemtoClock® Ordering Product Information* document.

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