AMC1035 Evaluation Module

This user's guide describes the characteristics, operation, and use of the AMC1035EVM. A complete circuit description as well as schematic diagram and bill of materials are included.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Table 1. Related Documentation

Device	Literature Number
AMC1035	SBAS837

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1 EVM Overview

1.1 Features

This EVM supports the following features:

- Full-featured Evaluation Board for the AMC1035 single-channel delta-sigma modulator
- ±1-V Input Voltage Range
- Configurable Power Supply Input
- Configurable Clock Input
- Integrated 2.5 V, ±5-mA Reference for Ratiometric Measurements
- Manchester Coded or Uncoded Bitstream Output
- Screw terminals for easy access to analog inputs and outputs

1.2 Introduction

The AMC1035 device is a precision, delta-sigma ($\Delta\Sigma$) modulator that operates from a single 3.0-V to 5.5-V supply and with an externally generated clock signal in the range of 9 MHz to 21 MHz. The differential ±1-V input structure of the device is optimized for use in a noisy environment, as usually found in industrial applications.

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the AMC1035EVM.

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2 Analog Interface

The input to the AMC1035EVM is routed from a two-wire screw terminal at J2. This screw terminal gives the user access to the inputs, AINP and AINN, of the AMC1035 through a low pass filter created by R1, R2, and C2. The input circuit for the AMC1035EVM is shown in Figure 1 below.

3 Power Supply

The AMC1035EVM requires one power rail for V_{DD} . 5 V is a typical value for V_{DD} and V_{DD} can be 3-5.5 V should not exceed 6.5 V. This is connected using pin 1 of J3 referenced to ground, pin 2 of J3.

4 Output Reference

The AMC1035EVM provides an output reference voltage of 2.5 V. This is accessible using pin 1 of J1 and can be seen in the figure below. REFOUT is used to provide excitation for RT1 and the maximum output current is +/-5 mA.

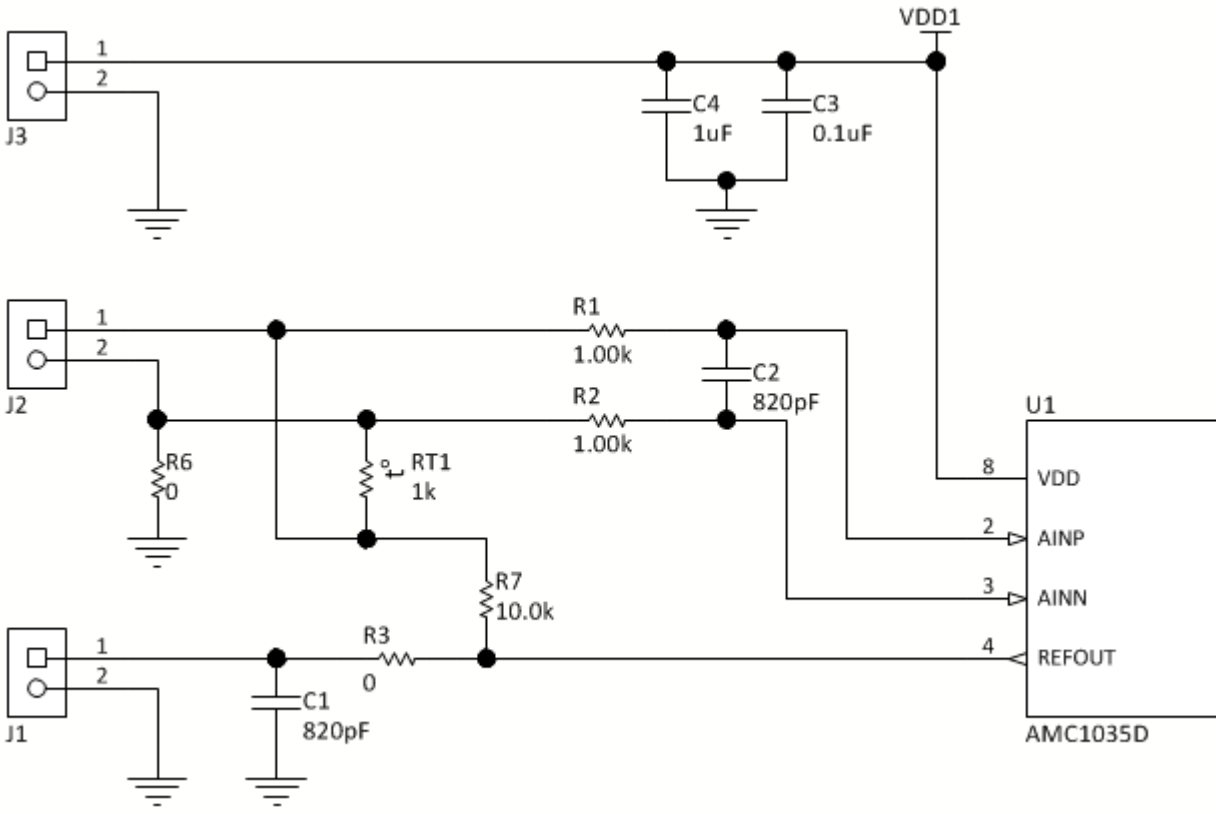

Figure 1. AMC1035EVM Schematic - Analog Interface, Power Supply, Output Reference

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5 Digital Interface

The AMC1035EVM digital input/output interface is composed of two, two terminal screw connectors located at J4 and J5. Pin 1 of J4 is the output data from the modulator and pin 1 of J5 is the clock input for the modulator U1. A 9 MHz to 21 MHz external clock must be applied to pin 1 of J5 referenced to ground, pin 2 of J5. The magnitude of this clocking signal should not exceed V_{DD} +0.5 V.

6 Manchester Coding Enabled

The AMC1035 offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. This feature is enabled by leaving the jumper JP1 installed. To disable the Manchester coding feature, remove JP1.

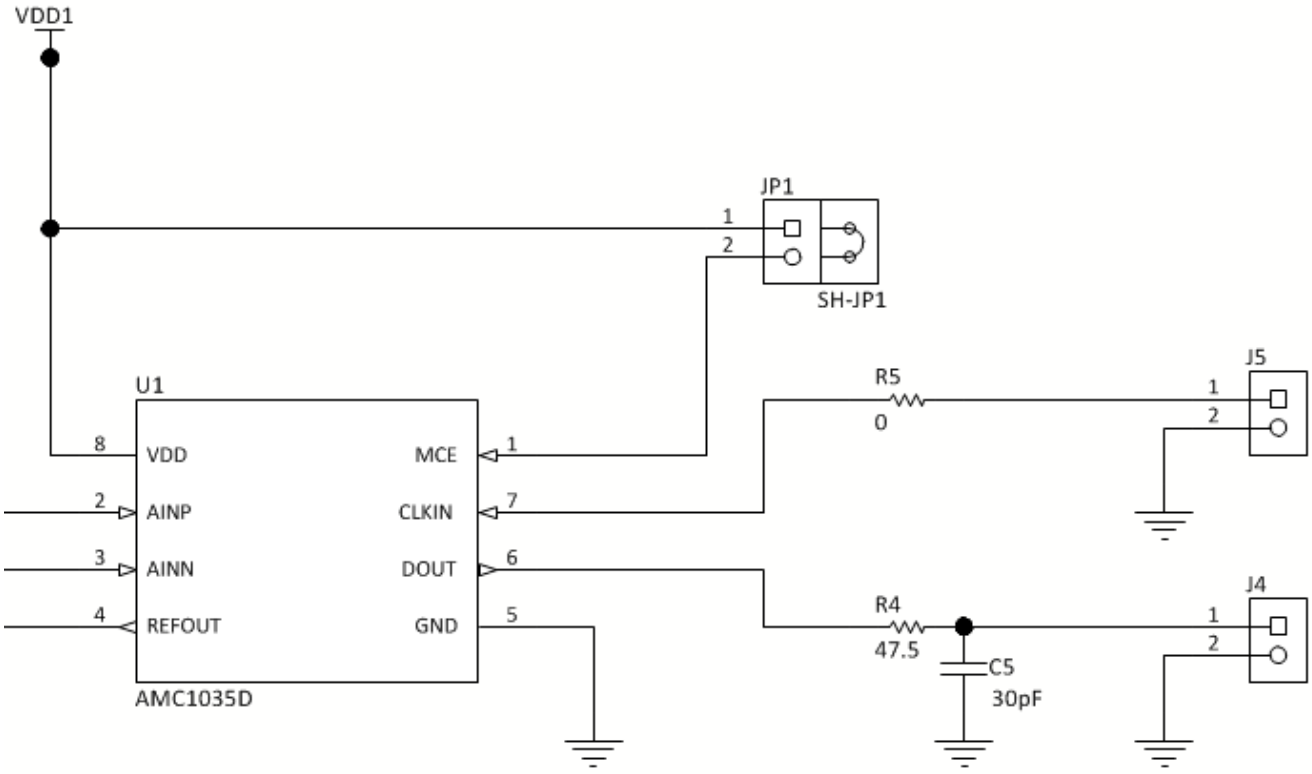

Figure 2. AMC1035EVM Schematic - Digital Interface, Manchester Coding Enabled

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7 General Operation Tables

The following section describes the general operation of the AMC1035EVM

CAUTION

Carefully review the AMC1035 product data sheet for the limitations of the analog input range and ensure that the appropriate analog/digital voltages are applied prior to connecting any analog input to the EVM.

Table 2. J1: REFOUT

Pin Number	Signal	Description
J1.1	REFOUT	2.5 V Output Reference Voltage
J1.2	GND	Ground Reference

Table 3. J2: ANALOG INPUTS

Pin Number	Signal	Description
J2.1	AINP	Non-inverting analog input to the AMC1035
J2.2	AINN	Inverting input to the AMC1035

Table 4. J3: POWER SUPPLY

Pin Number	Signal	Description
J3.1	V_{DD}	Externally supplied power rail. 3 V to 5.5 V, should not exceed 6.5 V
J3.2	GND	Ground Reference

Table 5. J4: DATA OUTPUT

Pin Number	Signal	Description
J4.1	D_{OUT}	Data Output
J4.2	GND	Ground Reference

Table 6. J5: EXTERNAL CLOCK

Pin Number	Signal	Description
J5.1	CLKIN	Externally supplied clocking signal. 9-21 MHz, should not exceed V_{DD} +0.5 V
J5.2	GND	Ground Reference

Table 7. JP1: MANCHESTER CODING ENABLED

Pin Number	Jumper	Description
JP1	INSTALLED	Manchester coding enabled
JP1	UNINSTALLED	Manchester coding disabled

Once the AMC1035EVM is supplied with power and an external clock, the digital outputs become active.

An analog input signal may be applied directly at screw terminal J2. Please see Figure 1 and Table 2 for details. The linear analog input range, AINP to AINN, is +/- 1 V and the full-scale range is +/-1.25 V.

As the input voltage approaches the maximum input level of +1 V, the 1s density of the modulator output will approach 90%. Likewise, when the input voltage approaches the lower limit of -1V the 1s density will be approximately 10%.

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8 BOM, Schematic, and Layout

This section contains the complete bill of materials, schematic diagram and printed circuit board (PCB) layout of the AMC1035EVM.

NOTE: Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing AMC1035EVM PCBs.

8.1 Bill of Materials

Table 8. AMC1035EVM Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C2	CAP, CERM, 820 pF, 50 V, +/- 5%, C0G/NP0, 0805	AVX	08055A821JAT2A
C3	CAP, CERM, 0.1 uF, 100 V, +/- 5%, X7R, 1206	TDK	C3216X7R2E104K160AA
C4	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 1206	AVX	C1206C105K3RACAUTO
C5	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0805	AVX	08051A300JAT2A
J1, J2, J3, J4, J5	Terminal Block, 3.5mm Pitch, 2x1, TH	On-Shore Technology	ED555/2DS
JP1	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S
R1, R2	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Panasonic	ERJ-6ENF1001V
R3, R5, R6	RES, 0, 1%, 0.5 W, 0805	Keystone	5106
R4	RES, 47.5, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW080547R5FKEA
SH-JP1	Shunt, 2mm, Gold plated, Black	Samtec	2SN-BK-G
U1	Delta-Sigma Modulator with Bipolar Input and Reference Output, D0008A (SOIC-8)	Texas Instruments	AMC1035D
C1	CAP, CERM, 820 pF, 50 V, +/- 5%, C0G/NP0, 0805	Not Installed	
R7	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Not Installed	
RT1	Thermistor NTC, 1.0k ohm, 5%, 0805	Not Installed	

8.2 Schematic

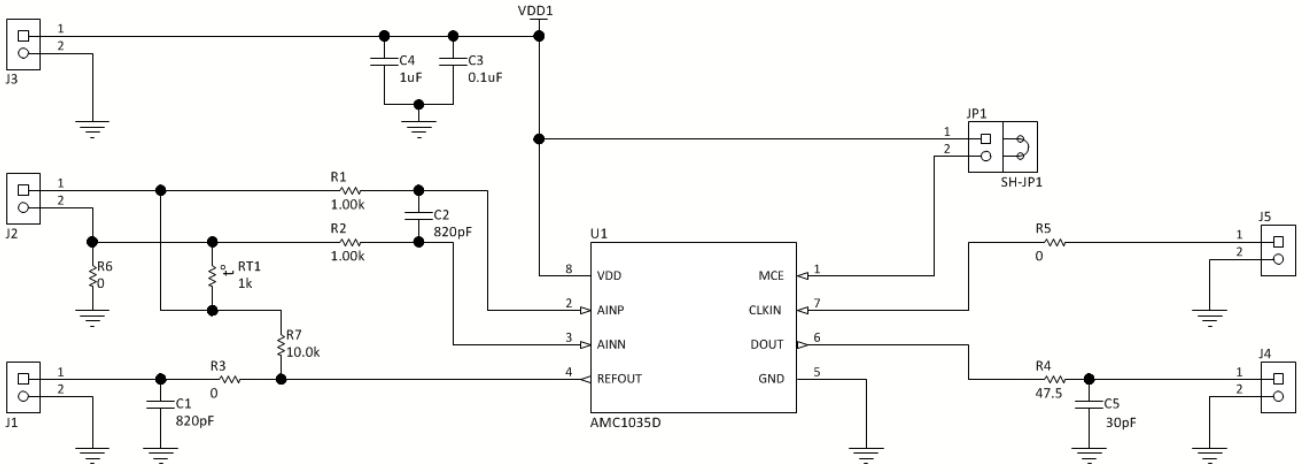

Figure 3. AMC1035EVM Schematic

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8.3 PCB Layout

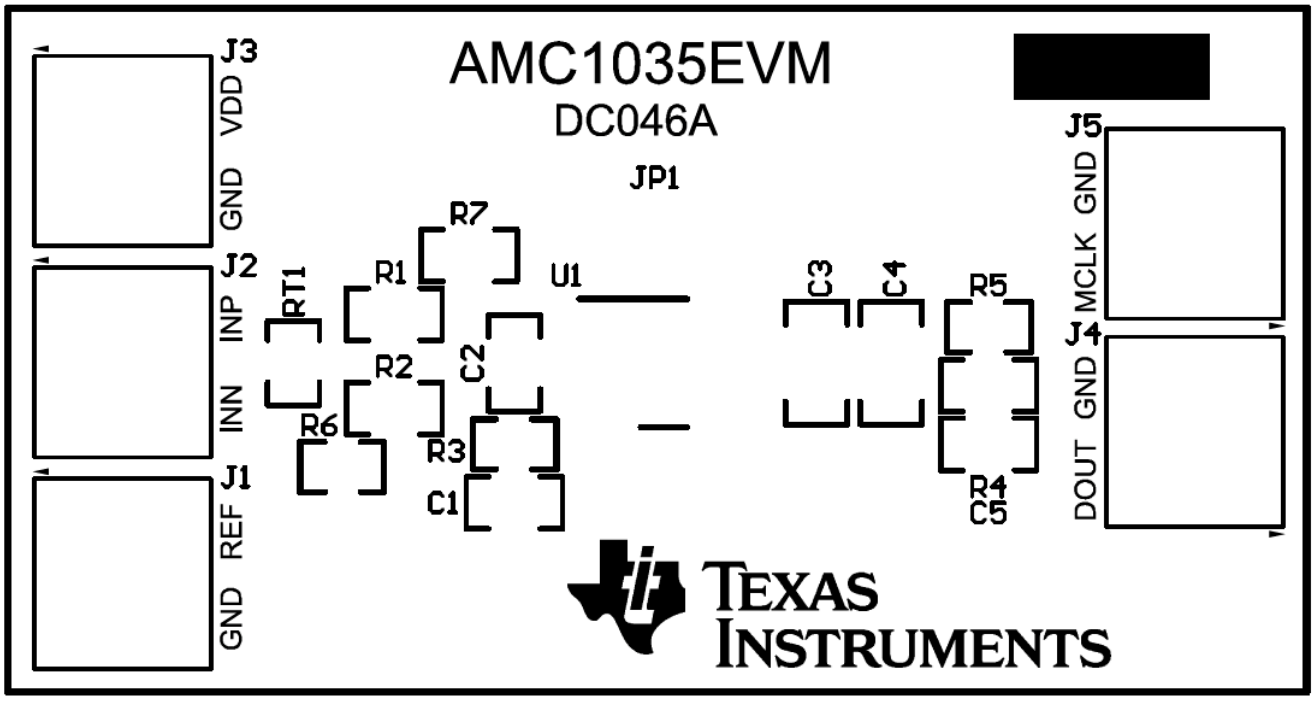

Figure 4. AMC1035EVM - PCB Top Layer Silk Screen

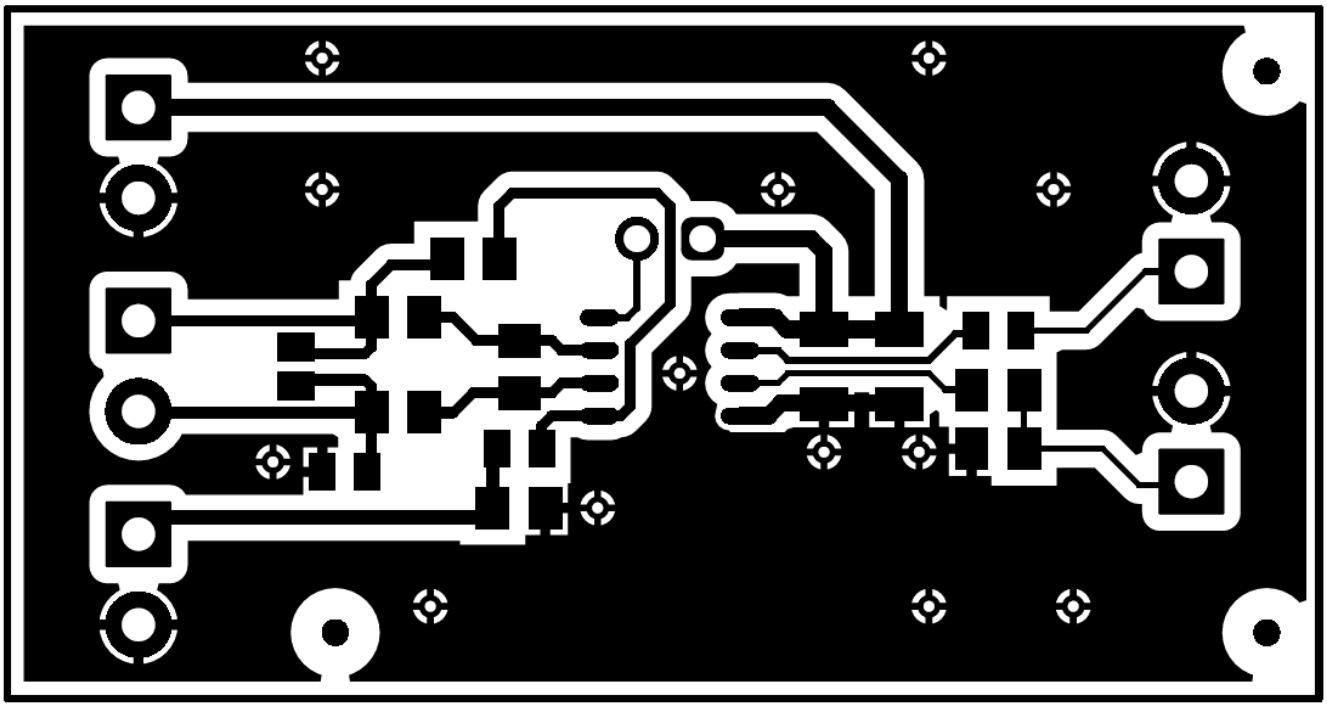

Figure 5. AMC1035EVM - PCB Top Layer Routing

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