TEXAS INSTRUMENTS

THS1206, THS12082, THS10064, THS10082

Evaluation Module

User's Guide

January 2001

AAP Data Conversion

SLAU042B

Preface

Read This First

About This Manual

This user's guide serves as a reference book for the THS1206/THS12082/ THS10064/THS10082 evaluation module. It describes the operation and usage of the 12-bit THS1206/THS12082 and 10-bit THS10064/THS10082 analog-to-digital converter (ADC) evaluation modules.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 EVM Description
- ❏ Chapter 2 Common-Connector Interface
- ❏ Chapter 3 Physical Description
- ❏ Chapter 4 Schematics

Information About Cautions and Warnings

This book contains cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution is provided for your protection. Please read each caution carefully.

Related Documentation From Texas Instruments

Data Sheets:

THS1206 data sheet (literature number SLAS217B) contains electrical specifications, available temperature options, general overview of the device, and application information.

THS12082 data sheet (literature number SLAS216) contains electrical specifications, available temperature options, general overview of the device, and application information.

THS10064 data sheet (literature number SLAS255) contains electrical specifications, available temperature options, general overview of the device, and application information.

THS10082 data sheet (literature number SLAS254) contains electrical specifications, available temperature options, general overview of the device, and application information.

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Chapter 1

EVM Description

This chapter gives a general description and overview of the THS1206/ THS12082/THS10064/THS10082 evaluation module (EVM), and describes the requirements for using this module.

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1.1 Purpose

The evaluation module provides a platform for lab prototype evaluation of the Texas Instruments 12-bit THS1206/THS12082 and the 10-bit THS10064/ THS10082 high-speed analog-to-digital converters. In addition, it provides the interface to Texas Instruments digital signal processor kits or evaluation modules, which provide the *common-connector* interface (C6201, C6701, C6211, C5402).

1.2 Power Supply Requirements

- The EVM is designed to be powered by a lab dc power supply (red and black inputs V_{DD} and AGND). The required supply voltage range is from 6 V to 10 V. It can also be powered by a DSP starter kit or evaluation module, which features the *common-connector* interface. The selection is done with jumpers J1 and J2.

Voltage Limits

Exceeding the 10-V maximum supply voltage range can damage EVM components.

1.3 EVM Basic Function

The EVM allows evaluation of the THS1206, THS12082, THS10064, and THS10082 analog-to-digital converters. Typically, a processor is used for evaluating these devices. The EVM is specifically designed for interfacing to the DSP starter kits or evaluation modules, which feature the common-connector interface (C6201, C6701, C6211, C5402).

The different operation modes for the analog input configuration of the THS1206, THS12082, THS10064, and THS10082 are available on the evaluation module. Any channel selection can be done according to the data sheet of each device.

- **Single-ended analog input**
  The THS1206/THS10064 (THS12082/THS10082) provide up to four (two) single-ended analog input channels. These four (two) single-ended inputs are provided on the EVM via the four BNC connectors, which are labeled AINP, AINM, BINP, and BINM. BNC connectors AINP and AINM do not have any function with the THS12082 and THS10082, which only feature two single-ended analog input channels. The analog input voltage range is from –1 V to 1 V. The analog input is level-shifted into the analog input range of the analog-to-digital converter (1.5 V to 3.5 V) by using an operational amplifier in an inverting configuration. The voltage used for the level shift is generated by the REFOUT (2.5 V) of the analog-to-digital converter. A resistor divider provides the 1.25 V from the 2.5-V output voltage. The analog input signal is dc-coupled.

- **Differential analog input**
  The THS1206/THS10064 (THS12082/THS10082) provide up to two (one) differential analog input channels to the analog-to-digital converter. These two (one) differential inputs are provided on the EVM via the two BNC connectors, which are labeled ADIFF and BDIFF. The BNC connector ADIFF does not have any function with the THS12082 and THS10082, which only feature one differential analog input channel. The analog input voltage range is from –2 V to 2 V. To use the differential mode, a single ended signal is applied to ADIFF or BDIFF. This signal is converted into a differential signal by a transformer, and is therefore ac-coupled. The center tap of the transformer is connected to the common mode output voltage REFOUT of the analog-to-digital converter. As a result, the input signal is shifted to the common-mode voltage REFOUT.

- **Clock circuit**
  An external clock with frequency up to 6 MHz (8 MHz for the THS10082 and THS12082) is required for operation of the analog-to-digital converter in the continuous-conversion mode. The external clock source is required to drive the 50-Ω BNC input EXT-CLK. The clock signal can also be generated from the connected processor. J7 should be set to the appropriate position.

- **Digital output**
  The digital output of the analog-to-digital converter is applied to connector block J9 and is also connected to the data bus of the *common connector* interface. No latch is used between the analog-to-digital converter and J9. The analog-to-digital converter is able to drive up to 30 pF at the data bus D0–D11 (D0–D9 for the THS10064 and THS10082).

1.4 EVM Setup

The EVM provides a platform for lab-prototype evaluation. Typically, it is operated by using a Texas Instruments DSP kit or evaluation module.

- **J1:** selection of the analog supply voltage:

  J1 inserted between 1 and 2: the supply voltage (5 V) is taken from the DSP starter kit or evaluation module with the *common-connector* interface. No external analog supply voltage is required in this configuration.

  J1 inserted between 2 and 3: for use of an external dc power supply (6 V to 10 V). The supply voltage, ranging from 6 V to 10 V, is regulated to 5 V by using the Texas Instruments low-dropout regulator TPS7250.

- **J2**: selection of the digital supply voltage:

  J2 inserted between 1 and 2: the supply voltage (3.3 V) is taken from the DSP starter kit or evaluation module with the *common-connector* interface. No external digital supply voltage is required in this configuration.

  J2 inserted between 2 and 3: for use of an external dc power supply (6 V to 10 V). The supply voltage, ranging from 6 V to 10 V, is regulated to 3.3 V by using the Texas Instruments low-dropout regulator TPS7233.

- **J3**: selection of the analog input configuration:

  J3 inserted between 1 and 4: selection of the differential input ADIFF (in combination with J4 set between 1 and 4)

  J3 inserted between 2 and 5: selection of the single ended input AINP

  J3 inserted between 3 and 6: required for the THS12082 and THS10082, where pin 31 (input AINP of the THS1206) functions as an internal FIFO overflow indicator (OV_FL). This pin can be monitored during data converter software debugging.

- **J4**: selection of the analog input configuration:

  J4 inserted between 1 and 4: selection of the differential input ADIFF (in combination with J3 set between 1 and 4)

  J4 inserted between 2 and 5: selection of the single ended input AINM

  J4 inserted between 3 and 6: required for the THS12082 and THS10082, where the input AINM of the THS1206 functions as RESET input. Pin 3 of J4 is connected to the RESET signal of the common-connector interface.

- **J5**: selection of the analog input configuration;

  J5 inserted between 1 and 2: selection of the single ended input BINP

  J5 inserted between 2 and 3: selection of the differential input BDIFF (in combination with J6 set between 2 and 3)

- **J6**: selection of the analog input configuration:

  J6 inserted between 1 and 2: selection of the single ended input BINM

  J6 inserted between 2 and 3: selection of the differential input BDIFF (in combination with J5 set between 2 and 3)

- **J7**: selection of the clock source:

  J7 inserted between 1 and 2: the clock input of the data converter is connected to the common connector interface. In this case, the DSP should generate the clock signal.

  J7 inserted between 2 and 3: the clock signal should be applied to the BNC connector EXT_CLK in this configuration.

- **J8**: J8 is a connector block where the following digital signals can be monitored:

Pin	Description	Pin	Description
Pin 1	GND	Pin 6	WR/
Pin 2	CLK	Pin 7	GND
Pin 3	GND	Pin 8	OV_FL
Pin 4	DATA_AV	Pin 9	GND
Pin 5	GND	Pin 10	RESET

- **J9**: J9 is a connector block where the following digital signals can be monitored:

Pin	Description	Pin	Description
Pin 1	NC	Pin 21	D3
Pin 2	GND	Pin 22	GND
Pin 3	CS0	Pin 23	D4
Pin 4	GND	Pin 24	GND
Pin 5	NC	Pin 25	D5
Pin 6	GND	Pin 26	GND
Pin 7	DATA_AV	Pin 27	D6
Pin 8	GND	Pin 28	GND
Pin 9	CONV_CLK	Pin 29	D7
Pin 10	GND	Pin 30	GND
Pin 11	CS1	Pin 31	D8
Pin 12	GND	Pin 32	GND
Pin 13	RD	Pin 33	D9
Pin 14	GND	Pin 34	GND
Pin 15	D0	Pin 35	D10/RA0
Pin 16	GND	Pin 36	GND
Pin 17	D1	Pin 37	D11/RA1
Pin 18	GND	Pin 38	GND
Pin 19	D2	Pin 39	NC
Pin 20	GND	Pin 40	GND

- **J10**: generation of chip select with C5000 DSP

  For an interface of the THS1206/THS12082/THS10064/THS10082 EVM to the C5000 DSP starter kit or EVM, J10 should be inserted while J11 is left open.

- **J11**: generation of CS1 with C6000 DSP

  For an interface of the THS1206/THS12082/THS10064/THS10082 EVM to the C6000 DSP starter kit or EVM, J11 should be inserted while J10 is left open.

- **J12**: generation of the write signal

  J12 inserted between 1 and 2: to interface the THS1206/THS12082/THS10064/THS10082 EVM to the C5000 DSP starter kit or EVM, J12 should be inserted between 1 and 2.

  J12 inserted between 2 and 3: to interface the THS1206/THS12082/THS10064/THS10082 EVM to the C6000 DSP starter kit or EVM, J12 should be inserted between 2 and 3.

- **J13**: generation of CS0

  J13 inserted between 1 and 2: to interface the THS1206/THS12082/THS10064/THS10082 EVM to the C6000 DSP starter kit or EVM, J13 should be inserted between 1 and 2.

J13 inserted between 2 and 3: to interface of the THS1206/THS12082/ THS10064/THS10082 EVM to the C5000 DSP starter kit or EVM, J13 should be inserted between 2 and 3.

The EVM provides several test points for the analog and digital grounds. These are labeled TPA and TPD respectively. Two test points for AVDD and DVDD are also provided.

Chapter 2

Common-Connector Interface

This chapter presents the common-connector interface.

Topic **Page**

2.1 Daughtercard Interface

An interface standard is being defined for daughtercards made to function with TMS320C6000 and TMS320C5000 systems. This interface standard is necessary to allow daughtercards to be used on systems from different vendors, and even across devices and DSP platforms. The ‘C6000 daughtercard standard is applicable to all of the ‘C6000 interfaces, and a subset applies to the ‘C5000 platform. Parallel interfaces that can communicate with the daughtercards are the 32-bit external-memory interface (EMIF), the 32-bit expansion bus, and the 16-bit host-port interface (HPI). The ‘C5000 family has a 16-bit EMIF, and 8- and 16-bit HPIs. The specific pinout of the ‘C5000 daughtercards is a subset of the ‘C6000. The pinouts of the J6 connector are described in Table 2–1, and the J7 connector pinouts are described in Table 2–2. Also see *Chapter 4 – Schematics*.

Table 2–1. Jumper J6, Expansion Peripheral Interface Pinout

J1 Pin	Name	Signal Name C5000	Name	Signal Name C6000 (EMIF)	J1 Pin	Name	Signal Name C5000	Name	Signal Name C6000 (EMIF)
1	+5V	Power Supply	+5V	Power Supply	41	3.3V	Power supply	3.3V	Power Supply
2		NC		NC	42		NC		NC
3	X_A19	Address pin	X_A21	Address pin	43		NC		NC
4	X_A18	Address pin	X_A20	Address pin	44		NC		NC
5		NC		NC	45		NC		NC
6		NC		NC	46		NC		NC
7	X_A15	Address pin	X_A17	Address pin	47		NC		NC
8		NC		NC	48		NC		NC
9		NC		NC	49		NC		NC
10		NC		NC	50		NC		NC
11	GND	Ground	GND	Ground	51		NC		NC
12		NC		NC	52		NC		NC
13		NC		NC	53		NC		NC
14		NC		NC	54		NC		NC
15		NC		NC	55		NC		NC
16		NC		NC	56		NC		NC
17		NC		NC	57	X_D11	Data pin	X_D11	Data pin
18		NC		NC	58	X_D10	Data pin	X_D10	Data pin
19		NC		NC	59	X_D9	Data pin	X_D9	Data pin
20		NC		NC	60	X_D8	Data pin	X_D8	Data pin
21		NC		NC	61		NC		NC
22		NC		NC	62		NC		NC
23		NC		NC	63	X_D7	Data pin	X_D7	Data pin
24		NC		NC	64	X_D6	Data pin	X_D6	Data pin
25		NC		NC	65	X_D5	Data pin	X_D5	Data pin
26		NC		NC	66	X_D4	Data pin	X_D4	Data pin
27		NC		NC	67	X_D3	Data pin	X_D3	Data pin
28		NC		NC	68	X_D2	Data pin	X_D2	Data pin
29		NC		NC	69	X_D1	Data pin	X_D1	Data pin
30		NC		NC	70	X_D0	Data pin	X_D0	Data pin
31		NC		NC	71		NC		NC
32		NC		NC	72		NC		NC
33		NC		NC	73	$\overline{\text{X\_RE}}$	Asynchronous read enable	$\overline{\text{ARE}}$	Asynchronous read enable
34		NC		NC	74	$\overline{\text{X\_WE}}$	Asynchronous write enable	$\overline{\text{AWE}}$	Asynchronous read enable
35		NC		NC	75	$\overline{\text{X\_OE}}$	Asynchronous output enable	$\overline{\text{AOE}}$	Asynchronous output enable
36		NC		NC	76		NC		NC
37		NC		NC	77		NC		NC
38		NC		NC	78	$\overline{\text{X\_DS}}$	Data space select	CE0	Chip enable 0
39		NC		NC	79		NC		NC
40		NC		NC	80		NC		NC

Table 2–2. Jumper J7, Expansion Peripheral Interface Pinout

J1 Pin	Name	Signal Name C5000	Name	Signal Name C6000 (EMIF)	J1 Pin	Name	Signal Name C5000	Name	Signal Name C6000 (EMIF)
1		NC		NC	41		NC		NC
2		NC		NC	42		NC		NC
3		NC		NC	43		NC		NC
4		NC		NC	44		NC		NC
5		NC		NC	45	X_TOUT	Timer output	TOUT0	Timer 0 output
6		NC		NC	46		NC		NC
7		NC		NC	47		NC		NC
8		NC		NC	48		NC		NC
9		NC		NC	49		NC		NC
10		NC		NC	50		NC		NC
11		NC		NC	51		NC		NC
12		NC		NC	52		NC		NC
13		NC		NC	53	$\overline{\text{X\_INT0}}$	External interrupt 0	EXT_INT0	External interrupt 0
14		NC		NC	54		NC		NC
15		NC		NC	55		NC		NC
16		NC		NC	56	$\overline{\text{X\_IOSTRB}}$	I/O access strobe	INUM2	Active interrupt number
17		NC		NC	57		NC		NC
18		NC		NC	58		NC		NC
19		NC		NC	59	$\overline{\text{X\_RESET}}$	System reset signal	RESET	System reset signal
20		NC		NC	60		NC		NC
21		NC		NC	61		NC		NC
22		NC		NC	62		NC		NC
23		NC		NC	63		NC		NC
24		NC		NC	64		NC		NC
25		NC		NC	65		NC		NC
26		NC		NC	66		NC		NC
27		NC		NC	67		NC		NC
28		NC		NC	68		NC		NC
29		NC		NC	69		NC		NC
30		NC		NC	70		NC		NC
31		NC		NC	71		NC		NC
32		NC		NC	72		NC		NC
33		NC		NC	73		NC		NC
34		NC		NC	74		NC		NC
35		NC		NC	75	$\overline{\text{DB\_DET}}$	Daughterboard detect	GND	Ground
36		NC		NC	76		NC		NC
37		NC		NC	77	GND	Ground	GND	Ground
38		NC		NC	78		NC		NC
39		NC		NC	79	GND	Ground	GND	Ground
40		NC		NC	80		NC		NC

Chapter 3

Physical Description

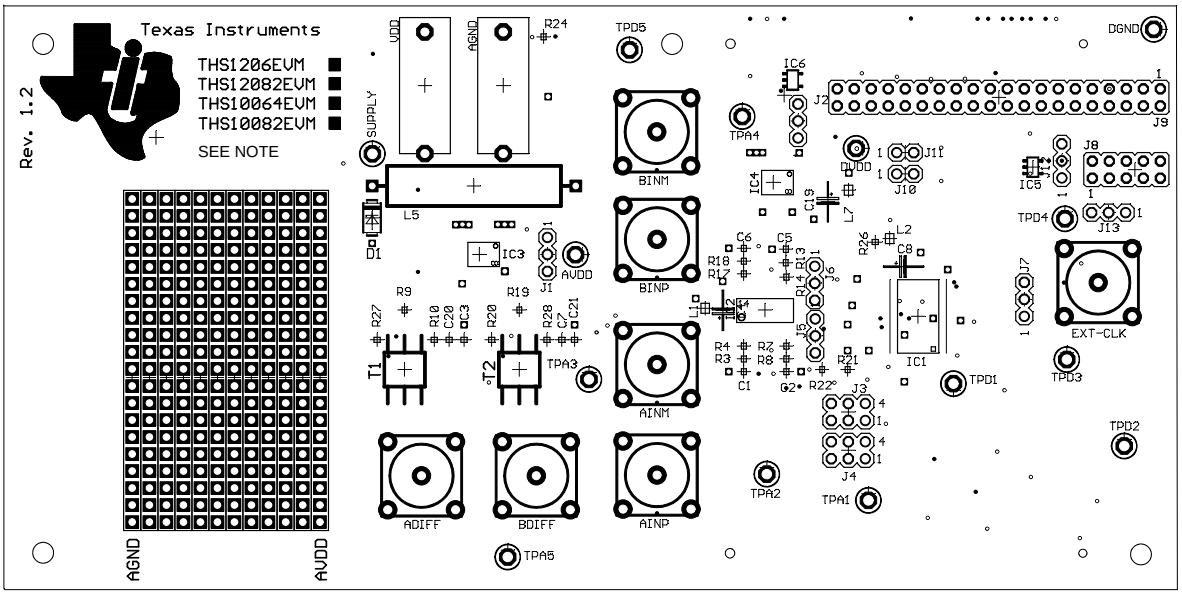
This chapter provides information about the PCB layout, and contains a list of the components used.

Topic **Page**

3.1 Printed-Circuit Board

The following figures show the silkscreen and the four layers of the evaluation module's printed-circuit board.

Figure 3–1. Silkscreen (Top)



Note: Also THS1207 EVM, THS1209 EVM, THS1007 EVM, and THS1009 EVM.

Figure 3–2. Silkscreen (Bottom)

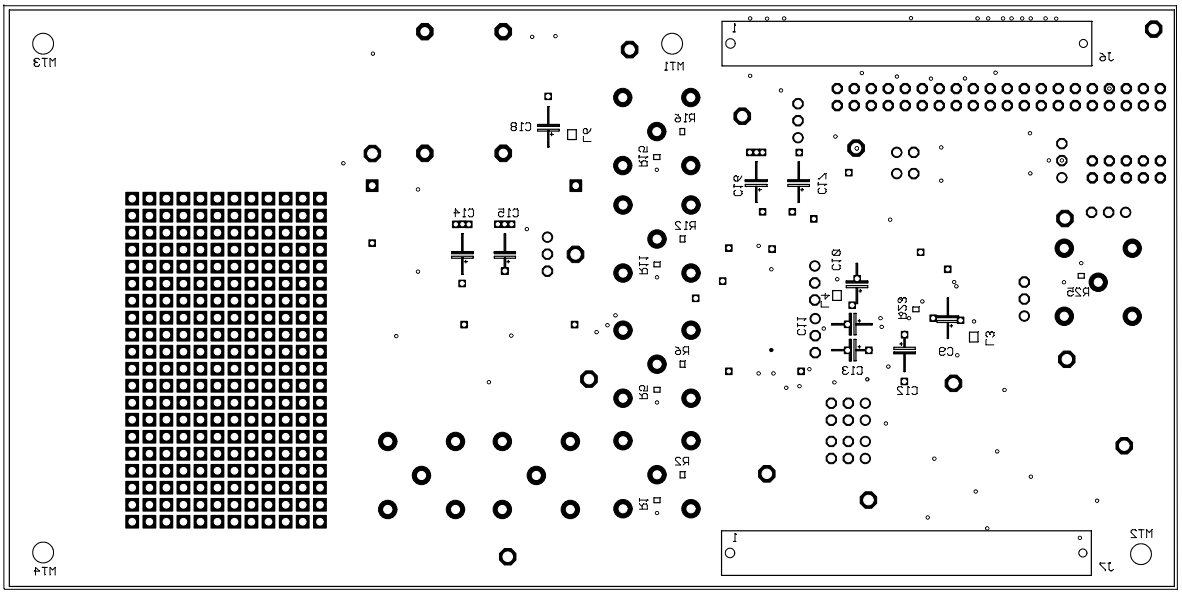


Figure 3–3. Printed-Circuit Board Layer 1

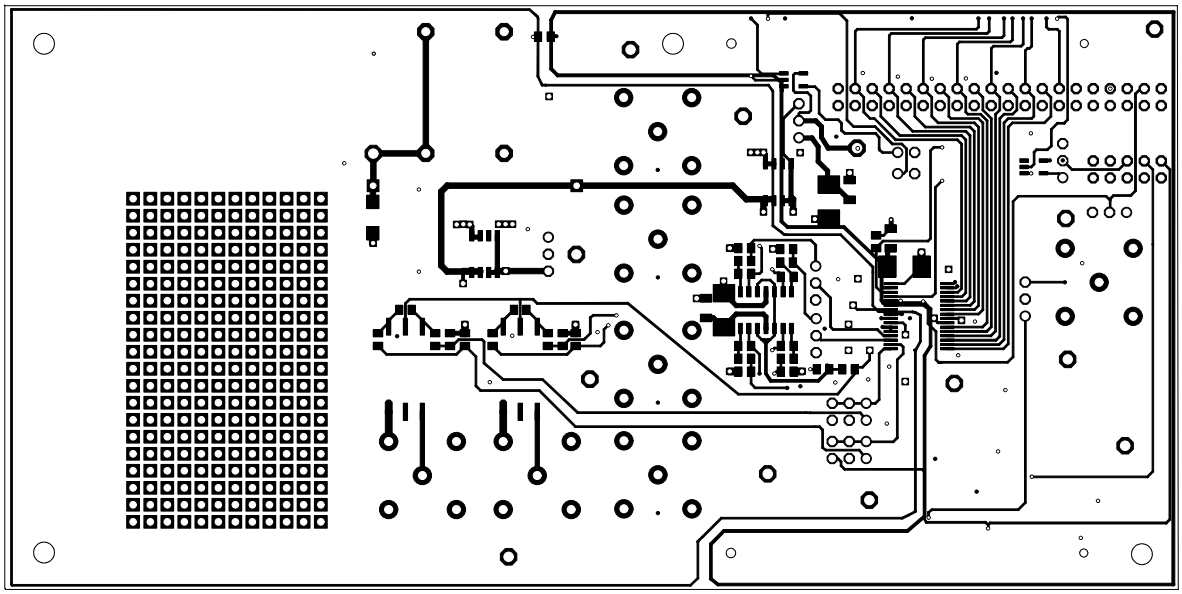


Figure 3–4. Printed-Circuit Board Layer 2

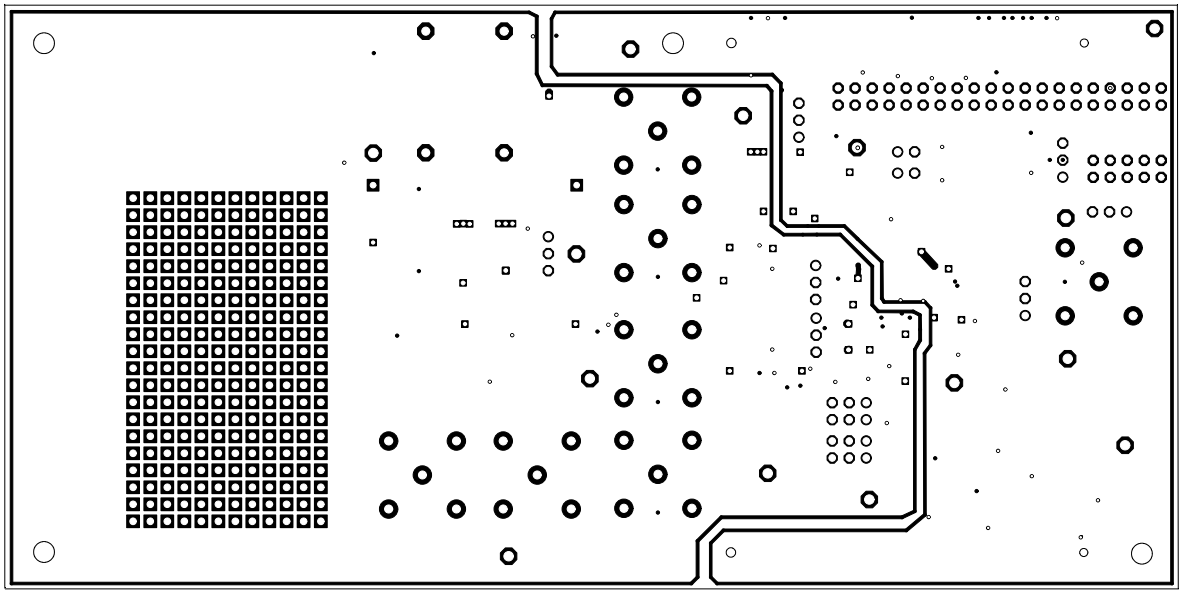


Figure 3–5. Printed-Circuit Board Layer 3

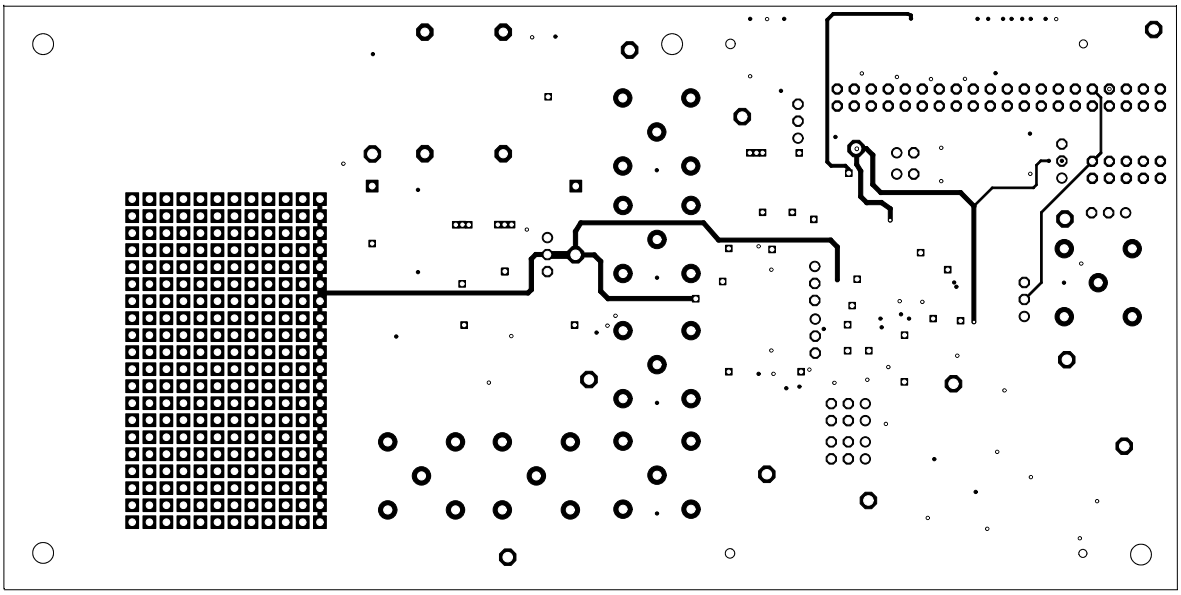
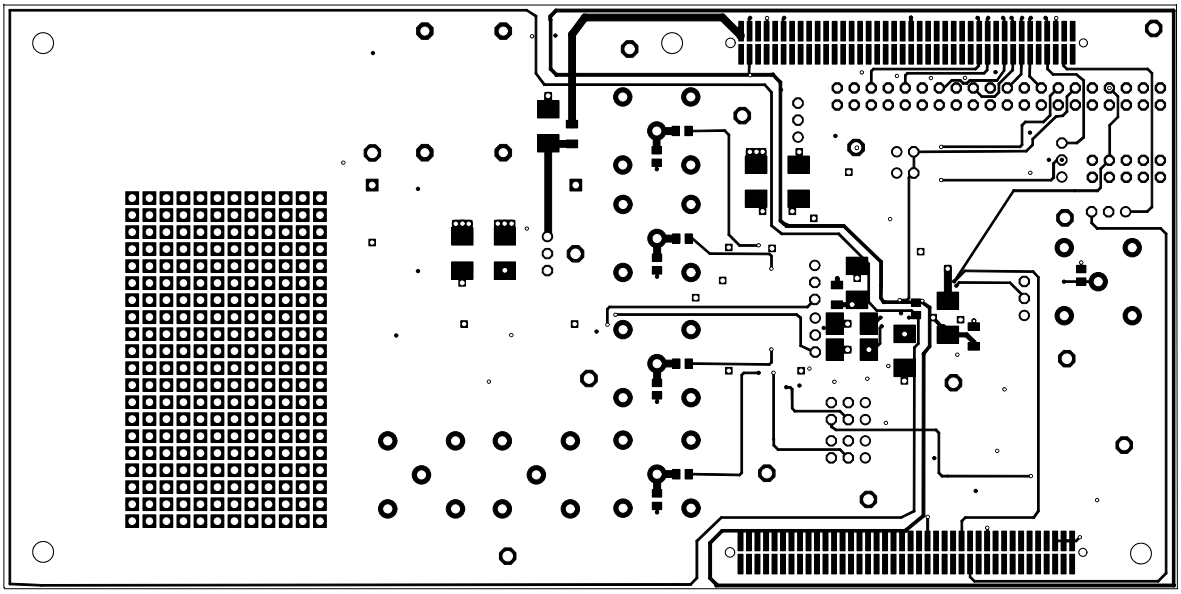


Figure 3–6. Printed-Circuit Board Layer 4



3.2 Bill of Materials

Table 3–1 lists the components used in constructing the EVM.

Table 3–1. Bill of Materials

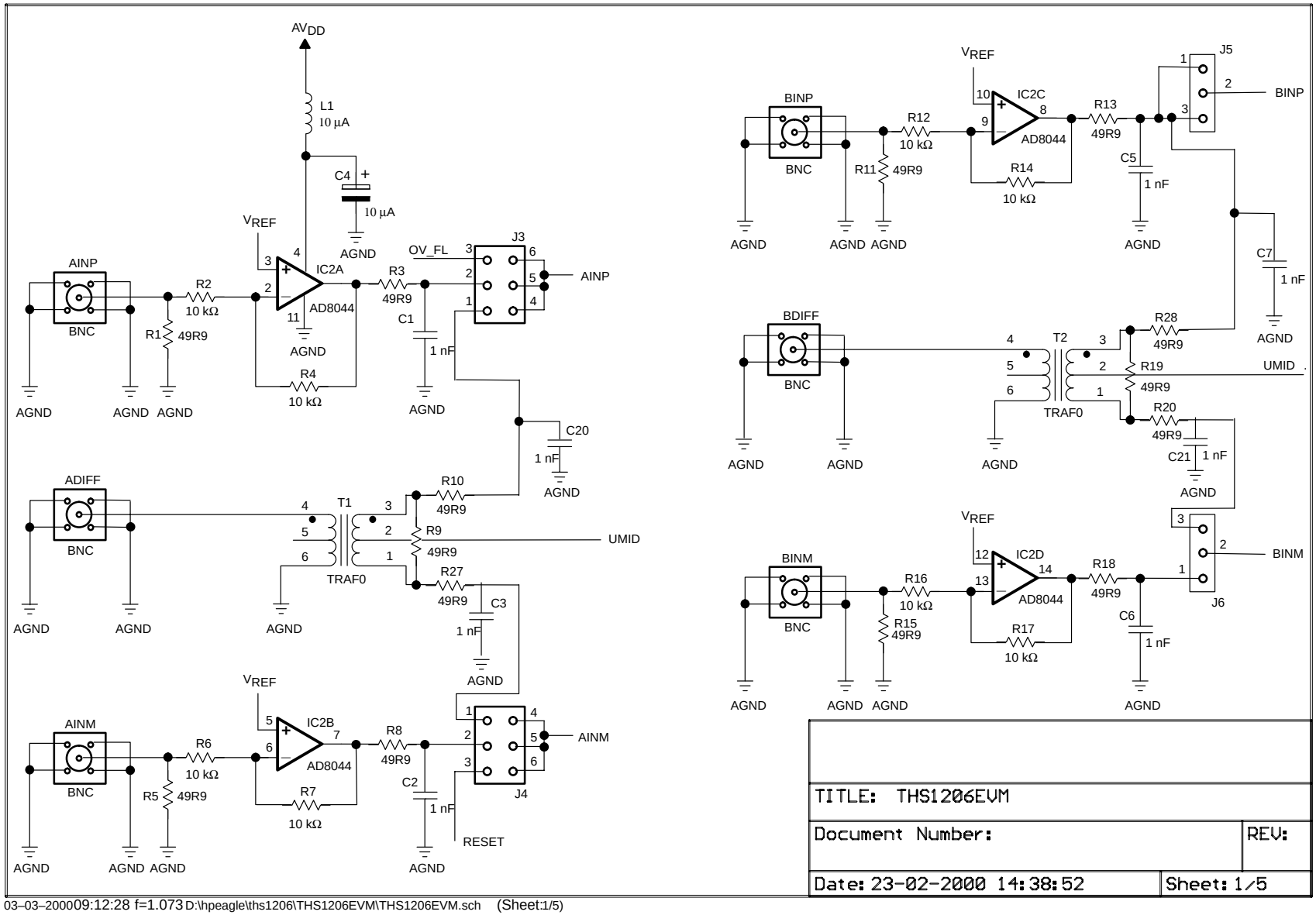
Quantity	Reference	Description	Manufacturer
8	C1–C3, C5–C7, C20–C21	1 nF, SMD, size 0805	MIRA-Electronic:8231/102
13	C4, C8–C19	10 μF Tantalum, C-Case	Bürklin: 25 D 1046
7	L1–L4, L6–L8	10 μH, size 1206	Bürklin: 76 D 470
1	L5	470 μH, size	Bürklin: 74 D 4742
15	R1, R3, R5, R8–R11, R13, R15, R18–R20, R25, R27, R28	49.9 Ω, size 0805	MIRA–Electronic: 8132/49.9
2	R23, R24	0 Ω, size 0805	
11	R2, R4, R6, R7, R12, R14, R16, R17, R21, R22, R26	10 kΩ, size 0805	MIRA-Electronic: 8132/10 k
1	IC1	THS1206CDA†	Bereitstellung von TI
1	IC2	AD8044AR	Spörle
1	IC3	TPS7250QD	Bereitstellung von TI
1	IC4	TPS7233QD	Bereitstellung von TI
1	IC5	SN74AHC1G04DBVR	Bereitstellung von TI
1	IC6	SN74AHC1G02DBVR	Bereitstellung von TI
7	ADIFF, AINM, AINP, BDIFF, BINM, BINP, EXT-CLK	BNC	Bürklin: 78F2475
1	D1	1N4004	Bürklin: 26 S 7950
14	AVDD, DGND, DVDD, SUPPLY, TPA1–TPA5, TPD1–TPD5	Test point	Bürklin: 07 F 810
1	AGND	PB4 black	Bürklin: 35 F 234
1	VDD	PB4 red	Bürklin: 35 F 236
2	T1, T2	Transformer: T1-6T-KK81	Municom
7	J1, J2, J5–J7, J12, J13	Jumper 3 pole	Riebensahm : 0100125112003
2	J10, J11	Jumper 2 pole	Riebensahm : 0100125112002
2	J6, J7 (HD–DSP)	SMD-Connector	Samtec: TFM-140-32-S-D-LC
12	1, 3, J14, J20–J24, J100, J101, J103, TEST	Jumper 2 x 18 pole	
2	J3, J4	Jumper 2 x 3 pole	
1	J8	Jumper 2 x 5 pole	
1	J9	Jumper 2 x 18 pole	

† May be replaced with THS12082, THS10082, THS10064

Chapter 4

Schematics

This chapter contains the evaluation module schematics.


AVDD
L1
10 µA
C4
10 µA
AGND
VREF
AINP
BNC
R2
10 kΩ
R1
49R9
IC2A
AD8044
R3
49R9
C1
1 nF
OV_FL
J3
AINP
R4
10 kΩ
C20
1 nF
ADIFF
T1
TRAF0
R10
49R9
R9
49R9
UMID
R27
49R9
C3
1 nF
AINM
R6
10 kΩ
R5
49R9
IC2B
R8
49R9
J4
AINM
R7
10 kΩ
C2
1 nF
RESET
BINP
R12
10 kΩ
R11
49R9
IC2C
R13
49R9
R14
10 kΩ
C5
1 nF
J5
BINP
C7
1 nF
BDIFF
T2
R28
49R9
R19
49R9
R20
49R9
C21
1 nF
BINM
R16
10 kΩ
R15
49R9
IC2D
R18
49R9
R17
10 kΩ
C6
1 nF
J6
BINM
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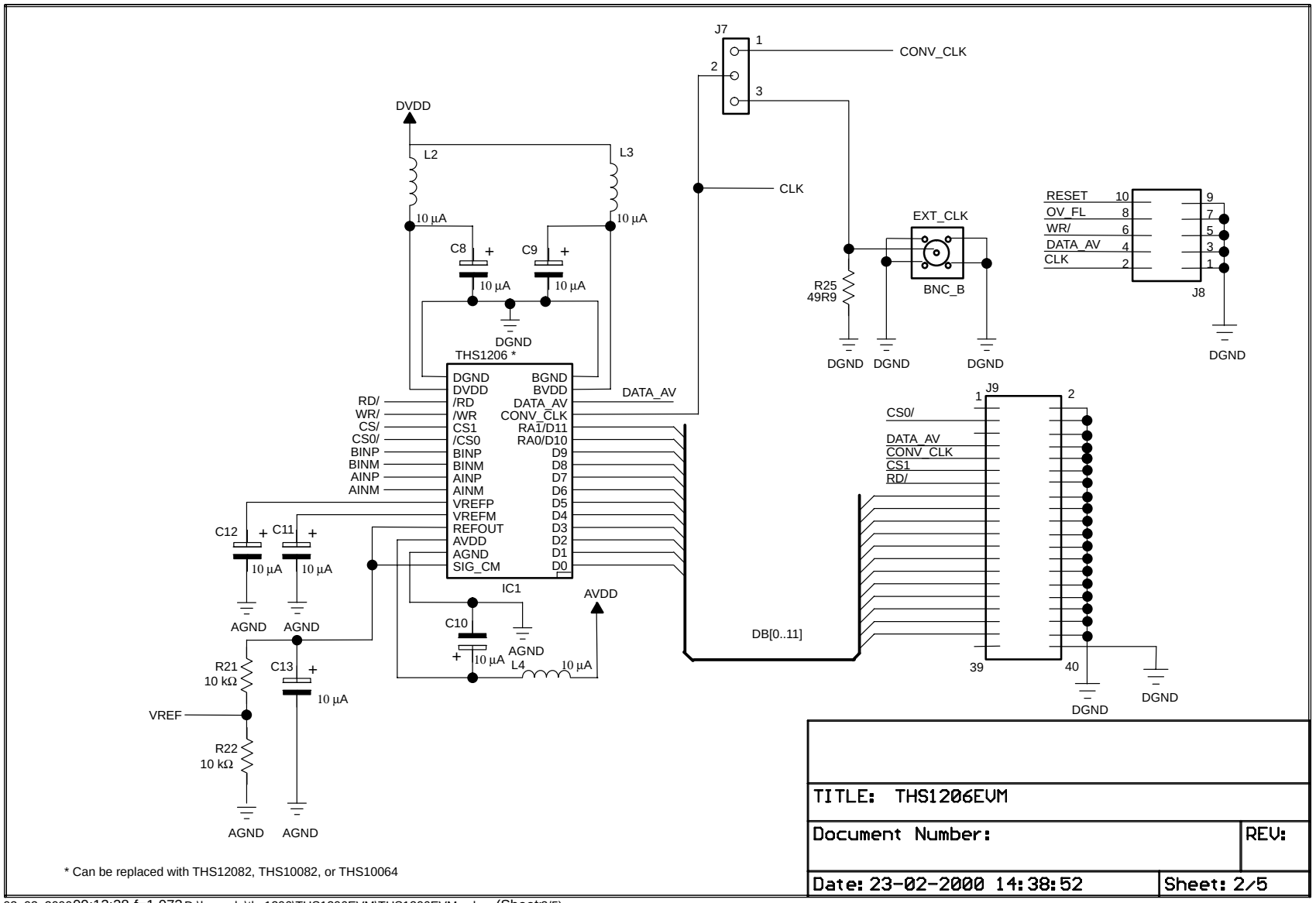
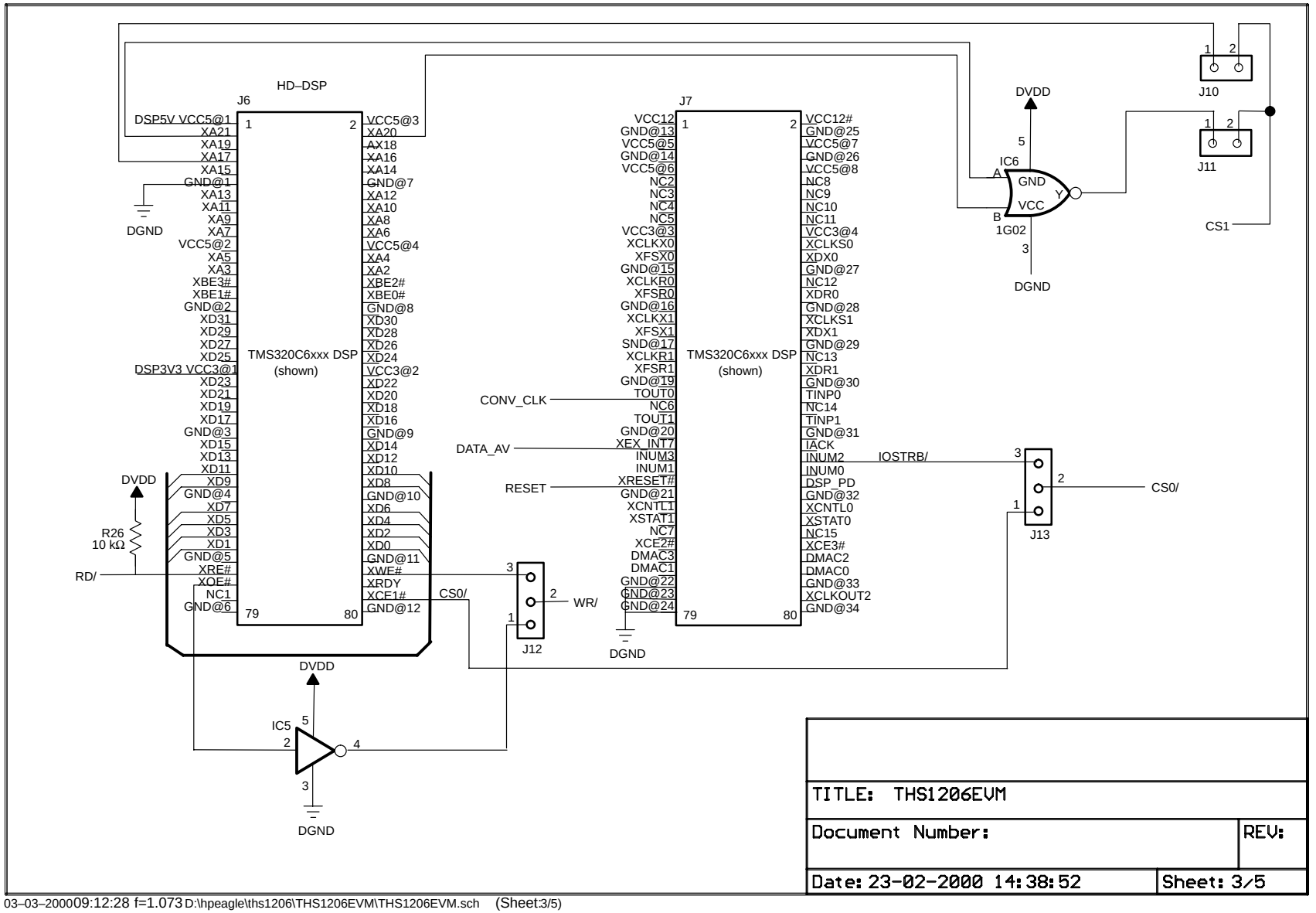
Date: 23-02-2000 14:38:52
Sheet: 1/5



* Can be replaced with THS12082, THS10082, or THS10064


HD–DSP
J6
TMS320C6xxx DSP
(shown)
J7
TMS320C6xxx DSP
(shown)
DVDD
DGND
R26
10 kΩ
RD/
CONV_CLK
DATA_AV
RESET
CS0/
WR/
IOSTRB/
CS1
J10
J11
J12
J13
IC5
IC6
1G02
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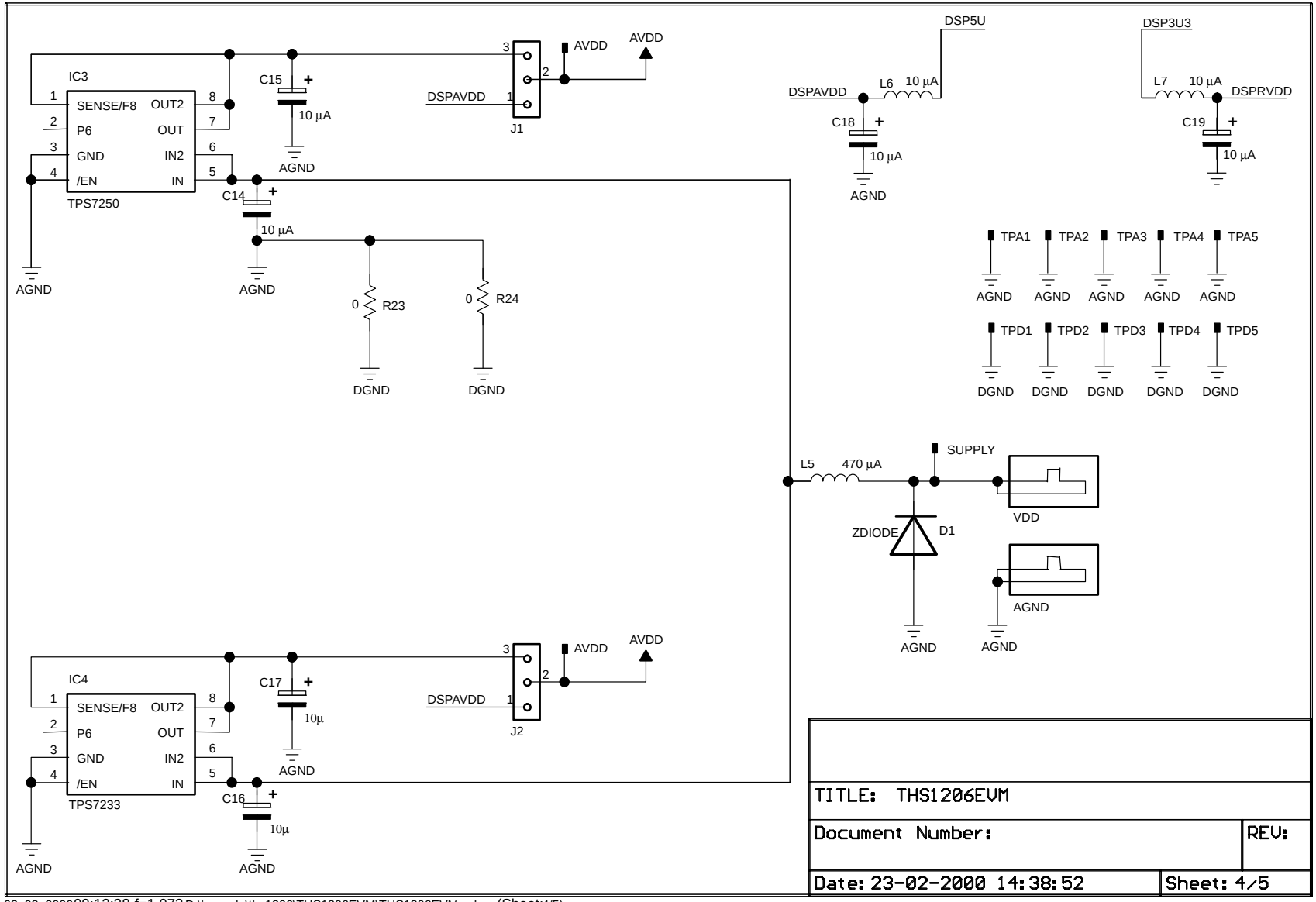
Sheet: 3/5



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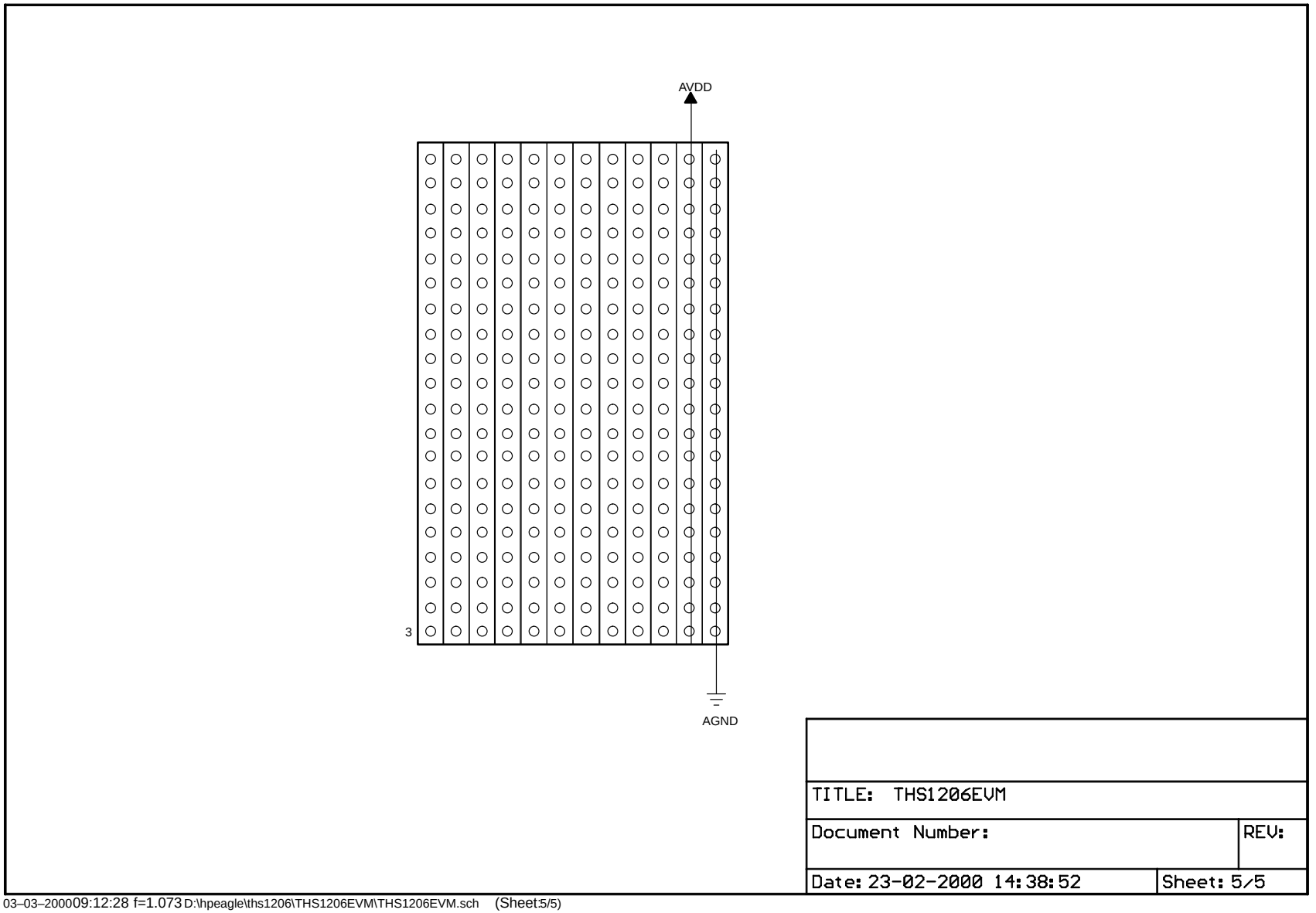

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