



**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



**CY91FV360GA/F362GB/F364G**  
**CY91F365GB/366GA/F366GB**  
**CY91F367GB/F368GB/F369GA/F376G**

## 32-bit Microcontroller FR50 CY91360G Series

The CY91360G series is a standard microcontroller containing a wide range of I/O peripherals and bus control functions. The CY91360G series features a 32-bit RISC CPU (FR50) core and is suitable for embedded control applications requiring high-performance and high-speed CPU processing. Also, Internal memories to improve the execution speed of the CPU.

### Features

#### ■ Execution time: down to 15.6 ns (64 MHz)

#### ■ FR50 CPU: RISC architecture

The CPU has a general-purpose register architecture with improved numeric implementation whereby a wide range of delayed branch instructions reduces losses in execution time due to pipeline breaks.

Bit manipulation instructions and memory access instructions have been enhanced resulting in improved code efficiency and execution speed for control implementation.

- A five-stage pipeline structure provides high-speed processing (one instruction per cycle)
- 32-bit linear address space: 4 Gbytes
- Fixed 16-bit instruction size (basic instructions)
- High-speed multiplication/step division
- High-speed interrupt processing (6 cycles)
- General-purpose registers: 16 × 32 bits

#### ■ External bus interface unit with a wide range of functions

Divides the external memory space into a maximum of eight areas. Chip select signal setting, data bus width selection (8, 16, 32-bit), and area size can be specified for each area.

- Address bus up to 32 bit wide
- Programmable auto-wait function

#### ■ DMAC

Direct memory access (DMA) can be used to perform various types of data transfer without going via the CPU. This improves system performance.

- Eight channels (including up to 3 external channels)
- Four transfer modes supported: single/block, burst, continuous transfer, and fly-by

#### ■ Power consumption control mechanisms

The CY91360G series contains a number of functions for controlling the operating clock to reduce power consumption.

- Software control: Sleep and stop/real time clock functions
- Hardware control: Hardware standby function
- Gear (divider) function: The CPU and peripheral clock frequencies can be set independently.

#### ■ Contains a range of peripheral functions

- UART, U-timer
- Real Time Clock (with optional subclock operation and subclock calibration module)
- Stepper Motor Control
- Sound Generator
- Serial I/O (SIO), SIO-Prescaler
- Power Down Reset
- Alarm Comparator

- I/O-Timer
- I<sup>2</sup>C Interface
- 10-bit D/A Converter
- CAN Interface
- 10-bit A/D converter
- 16-bit reload timer
- 16-bit PWM timer
- Watchdog timer
- Bit search module
- Interrupt controller
- External interrupt inputs
- I/O port function

#### ■ Interrupt levels

“16 maskable interrupt levels”

#### ■ Other

- Power supply voltage
- 5 V power supply used, the internal regulator creates internal supply of 3.3 V
- Package: CY91F362GB is delivered in a QFP208 package, and CY91F369GA in QFP160 package. CY91F364G, CY91F365GB, CY91F366GB, CY91F367GB, CY91F368GB, CY91366GA and CY91F376G will be delivered in an LQFP120 package.  
(See also section [Package Dimensions](#).)

## Contents

<b>Product Lineup</b> .....	<b>3</b>	Interrupt Controller .....	122
<b>Pin Assignments</b> .....	<b>5</b>	External Interrupt/NMI Control Block.....	126
<b>Pin Descriptions</b> .....	<b>13</b>	Delayed Interrupt.....	127
<b>I/O Circuit Type</b> .....	<b>44</b>	Clock Generation.....	127
<b>Handling Devices</b> .....	<b>52</b>	Bus Interface .....	131
Preventing Latch-up .....	52	CAN Controller .....	134
Connecting Unused Pins.....	52	D/A Converter.....	141
External Reset Input.....	52	400 kHz I2C Interface.....	143
Power Supply Pins .....	52	16-bit I/O Timer .....	146
Crystal Oscillator Circuit.....	52	Alarm Comparator .....	149
Using an External Clock.....	53	Power Down Reset.....	150
Mode Pins .....	53	Serial I/O Interface (SIO).....	151
Turning the Power Supply on.....	53	Sound Generator.....	152
A State in Turning Power on .....	53	Stepper Motor Controller.....	155
Note on During Operation of PLL Clock Mode .....	53	Real Time Clock.....	157
The Function of the Watchdog Timer .....	53	Subclock.....	160
<b>Block Diagram</b> .....	<b>54</b>	32 kHz Clock Calibration Unit.....	161
<b>CPU Core</b> .....	<b>55</b>	Flash Memory.....	166
Memory Space .....	55	<b>Flash Memory Mode Signal Assignment</b> .....	<b>186</b>
Dedicated Registers .....	56	<b>Electrical Characteristics</b> .....	<b>191</b>
General-Purpose Registers.....	57	Absolute Maximum Ratings.....	191
<b>Mode Setting</b> .....	<b>58</b>	Recommended Operating Conditions .....	194
Mode Pins .....	58	DC Characteristics .....	195
Mode Register (MODR).....	58	Run Mode Current/Power Consumption .....	198
Fixed Vector .....	58	Clock Settings .....	200
<b>I/O Map</b> .....	<b>59</b>	Converter Characteristics.....	200
How to Read the I/O Map .....	59	A/D Converter Glossary .....	201
<b>CY91F376G Special I/O Map</b> .....	<b>82</b>	Notes on Using A/D Converter .....	203
<b>Interrupt Causes, Interrupt Vectors, and Interrupt Control Register</b> .....	<b>89</b>	Time for Power Supply .....	204
<b>Peripheral Resources</b> .....	<b>92</b>	Flash Memory.....	204
Instruction Cache .....	92	AC Characteristics.....	204
Boot ROM.....	95	<b>Package Thermal Resistance and Max Allowed Power Consumption</b> .....	<b>212</b>
Clock Modulator .....	95	<b>Ordering Information</b> .....	<b>212</b>
I/O Ports .....	96	<b>Package Dimensions</b> .....	<b>213</b>
DMA Controller (DMAC).....	103	<b>Major Changes</b> .....	<b>216</b>
UART.....	106	<b>Document History Page</b> .....	<b>217</b>
U-TIMER (16-bit Timer for UART Baud Rate Generation) .....	109	<b>Sales, Solutions, and Legal Information</b> .....	<b>218</b>
PWM Timer .....	110	Worldwide Sales and Design Support .....	218
16-bit Reload Timer.....	115	Products .....	218
Bit Search Module .....	117	PSoC® Solutions .....	218
10-bit A/D Converter (Successive Approximation Conversion Type).....	119	Cypress Developer Community .....	218
		Technical Support .....	218

## 1. Product Lineup

Table 1-1. CY91FV360GA, CY91F362GB, CY91F364G, CY91F369GA

Resource Channels Memory Size	CY91FV360GA	CY91F362GB	CY91F364G	CY91F369GA
Cache/Instruction RAM	4 KB / 4 KB	- / 4 KB	- / -	- / 4 KB
D-bus RAM	16 KB	12 KB	12 KB	16 KB
F-bus RAM	16 KB	4 KB	4 KB	16 KB
Flash/ROM (F-bus)	512 KB Fast Flash	512 KB Normal Flash	256 KB Fast Flash	512 KB Fast Flash
Boot ROM	2 KB	2 KB	2 KB	2 KB
EDSU	-	-	1	-
CAN	4 ch	3 ch	1 ch	2 ch
Stepper Motor Control	4 ch	4 ch	-	-
Sound Generator	1 ch	1 ch	-	1 ch
PPG	8 ch	8 ch	4 ch	4 ch
Input Capture	4 ch	4 ch	4 ch	-
Output Compare	4 ch	4 ch	4 ch	-
Free Running Timer	2 ch	2 ch	2 ch	-
D/A Converter	2 ch	2 ch	2 ch	-
A/D Converter	16 ch	16 ch	12 ch	10 ch
400 kHz I <sup>2</sup> C interface	1 ch	1 ch	1 ch	1 ch
Alarm Comparator	1 ch	1 ch	-	1 ch
SIO/SIO Prescaler	2 ch	2 ch	1 ch	2 ch
UART/U-Timer	3 ch	3 ch	1 ch	1 ch
USART with LIN Function	-	-	2 ch	-
16-bit Reload Timer	6 ch	6 ch	3 ch	6 ch
Ext. Interrupt	8 ch	8 ch	8 ch	8 ch
Non Maskable Interrupt	1	-	1	-
Real Time Clock	1	1	1	1
32 kHz Subclock Option for RTC	yes	no	yes	no
Subclock Calibration	yes	no	yes	no
LED Port	8 bit	8 bit	8 bit	-
Power Down Reset	1	1	-	1
Bit Search Module	1	1	1	1
Watchdog Timer	1	1	1	1
Ext. Address Bus	32 bit	21 bit	-	up to 24 bit
Ext. Data Bus	32 bit	32 bit	-	32 bit
Ext. DMA	3 ch	1 ch	-	1 ch
Max Operating Frequency	64 MHz	64 MHz	64 MHz	64 MHz

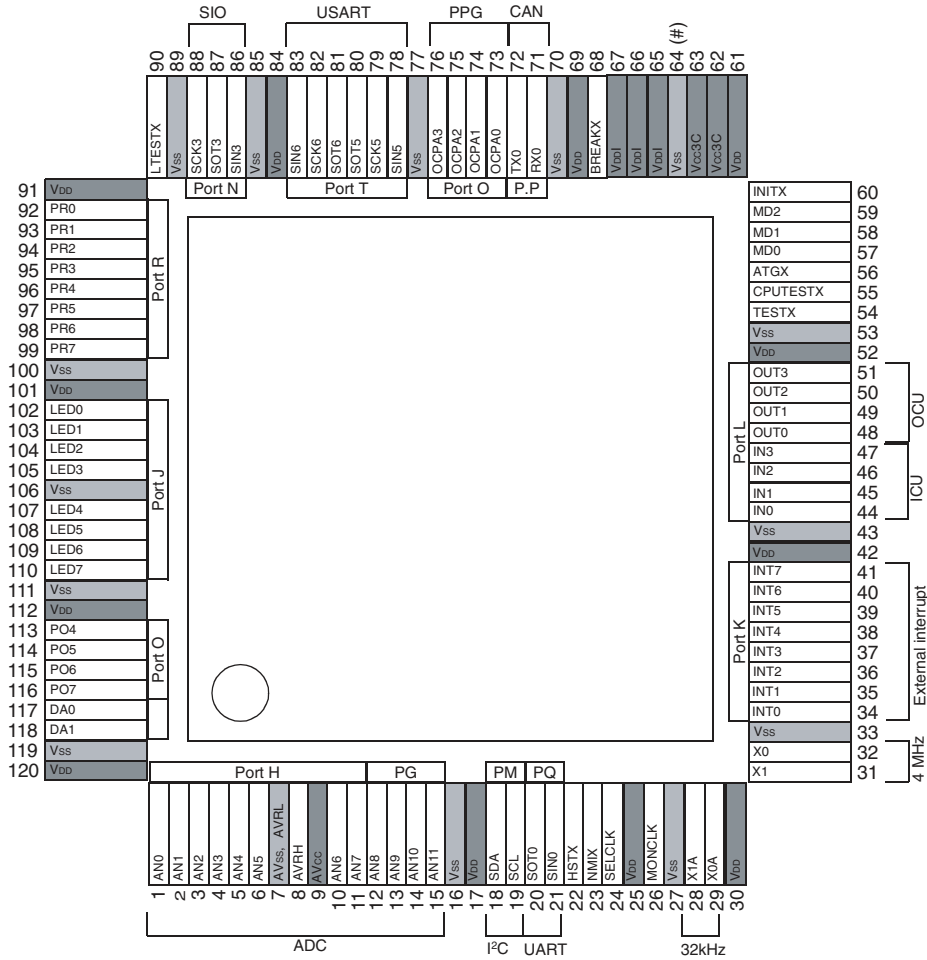
**Table 1-2. CY91F365GB, CY91F366GB, CY91366GA, CY91F367GB, CY91F368GB**

Resource Channels Memory Size	CY91F365GB	CY91F366GB CY91366GA	CY91F367GB	CY91F368GB	CY91F376G
Cache/Instruction RAM	- / 4 KB	- / 4 KB	- / 4 KB	- / 4 KB	- / 4 KB
D-bus RAM	16 KB	16 KB	16 KB	16 KB	16 KB
F-bus RAM	16 KB	16 KB	16 KB	16 KB	16 KB
Flash/ROM (F-bus)	512 KB Fast Flash	512 KB Normal Flash	512 KB Fast Flash	512 KB Fast Flash	768 KB Fast Flash
Boot ROM	2 KB	2 KB	2 KB	2 KB	2 KB
EDSU	-	-	-	-	-
CAN	2 ch	2 ch	2 ch	2 ch	2 ch
Stepper Motor Control	4 ch	4 ch	-	-	4 ch
Sound Generator	1 ch	1 ch	-	-	1 ch
PPG	8 ch	8 ch	4 ch	4 ch	8 ch
Input Capture	4 ch	4 ch	4 ch	4 ch	4 ch
Output Compare	2 ch	2 ch	2 ch	2 ch	2 ch
Free Running Timer	2 ch	2 ch	2 ch	2 ch	2 ch
D/A Converter	2 ch	-	-	-	-
A/D Converter	8 ch	8 ch	8 ch	8 ch	8 ch
I <sup>2</sup> C 400kHz	1 ch	1 ch	1 ch	1 ch	1 ch
Alarm Comparator	1 ch	1 ch	1 ch	1 ch	1 ch
SIO/SIO Prescaler	2 ch	2 ch	2 ch	2 ch	2 ch
UART/U-Timer	2 ch	2 ch	1 ch	1 ch	2 ch
USART with LIN function	-	-	-	-	-
16-bit Reload Timer	6 ch	6 ch	3 ch	3 ch	6 ch
Ext. Interrupt	8 ch	8 ch	8 ch	8 ch	8 ch
Non Maskable Interrupt	-	-	-	-	-
Real Time Clock	1	1	1	1	1
32 kHz Subclock Option for RTC	no	yes	no	yes	yes
Subclock Calibration	no	yes	no	yes	yes
LED Port	-	-	-	-	-
Power Down Reset	1	1	1	1	1
Bit Search Module	1	1	1	1	1
Watchdog Timer	1	1	1	1	1
Ext. Address Bus	-	-	-	-	-
Ext. Data Bus	-	-	-	-	-
Ext. DMA	-	-	-	-	-
Max Operating Frequency	64 MHz	64 MHz	64 MHz	64 MHz	64 MHz



Figure 2-2. CY91F364G

(Top View)



(LQM120)

Figure 2-3. CY91F369GA

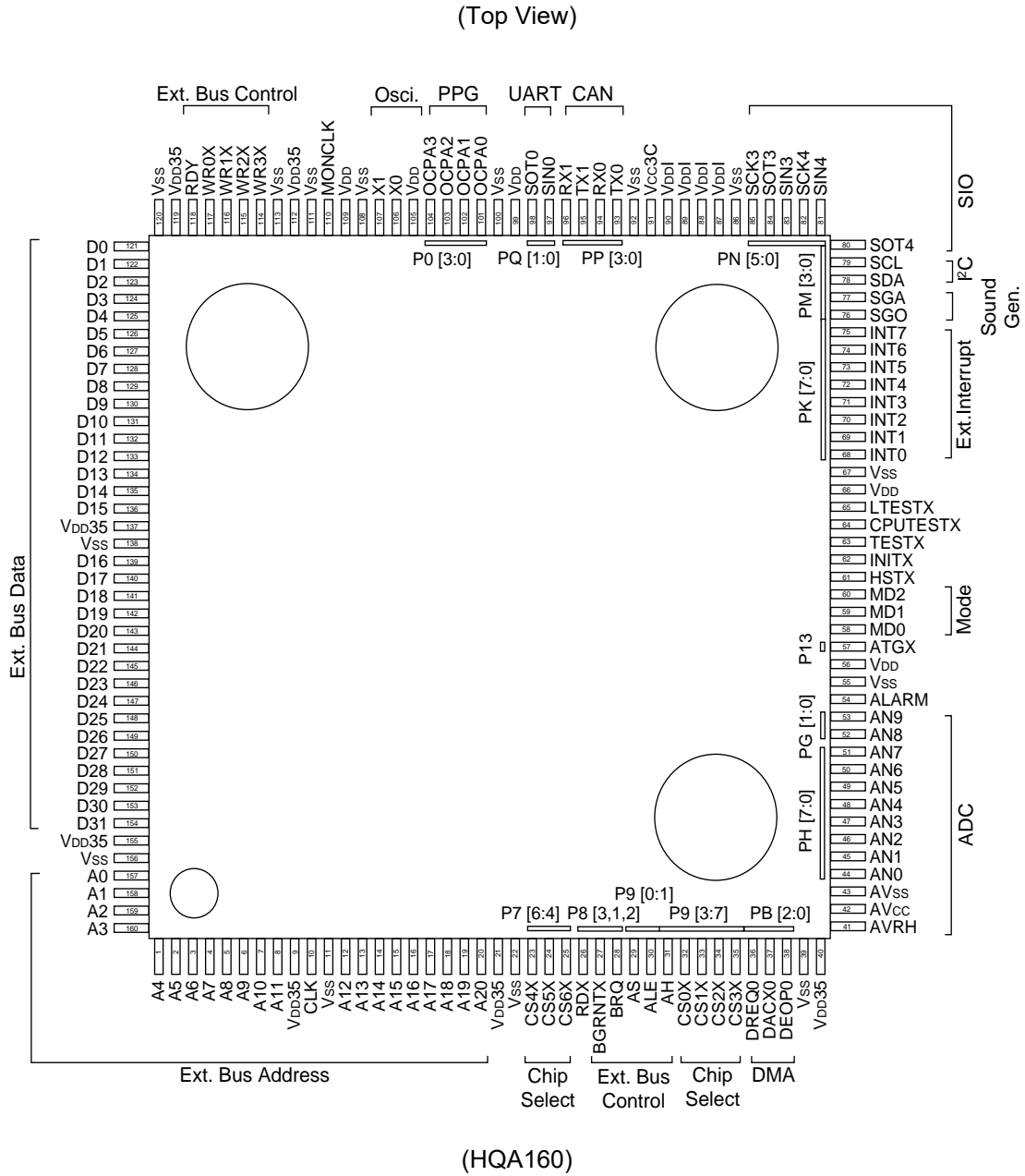
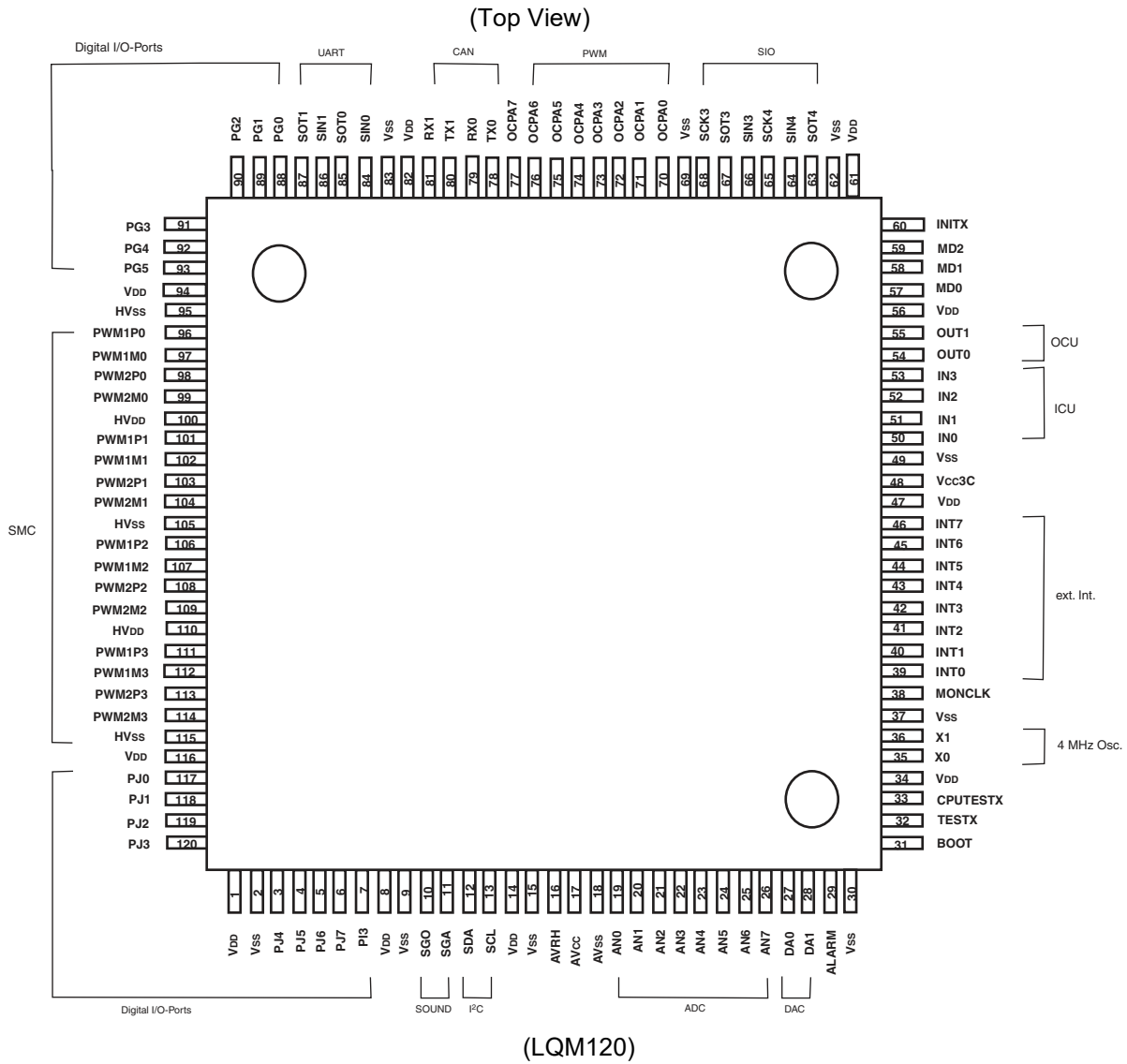




Figure 2-4. CY91F365GB



**Figure 2-5. CY91F366GB/CY91F376G**

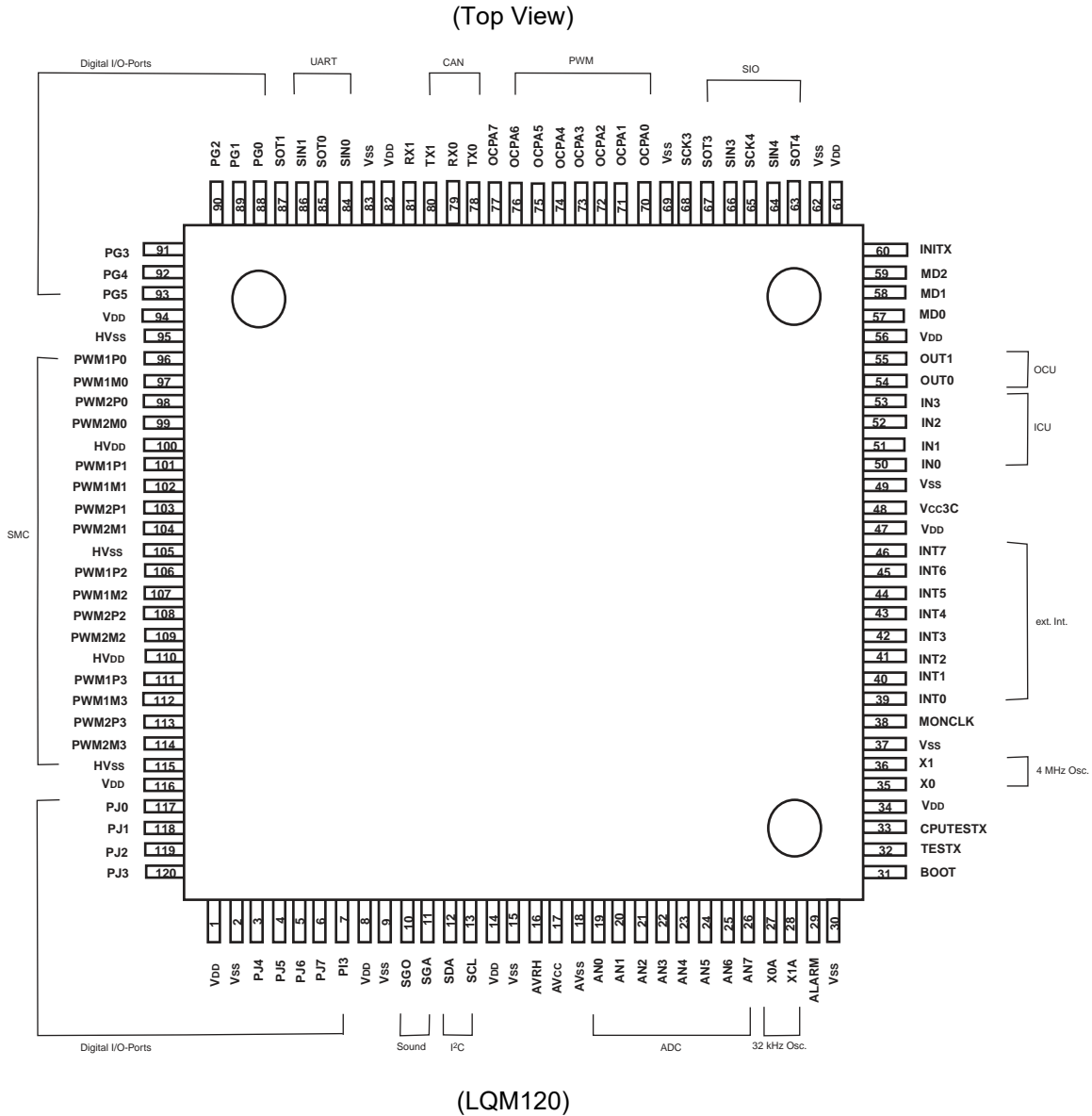


Figure 2-6. CY91F367GB

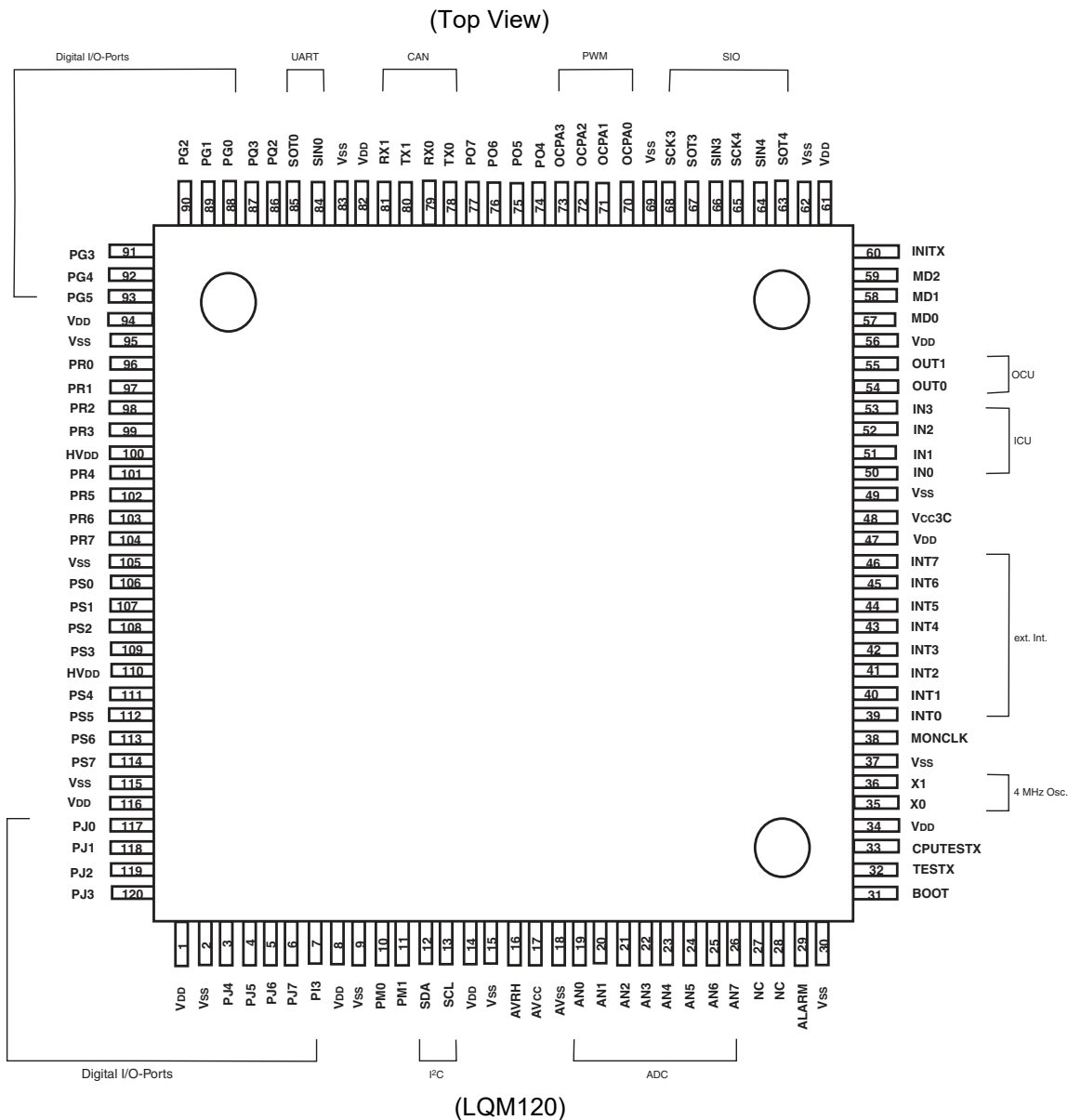


Figure 2-7. CY91F368GB

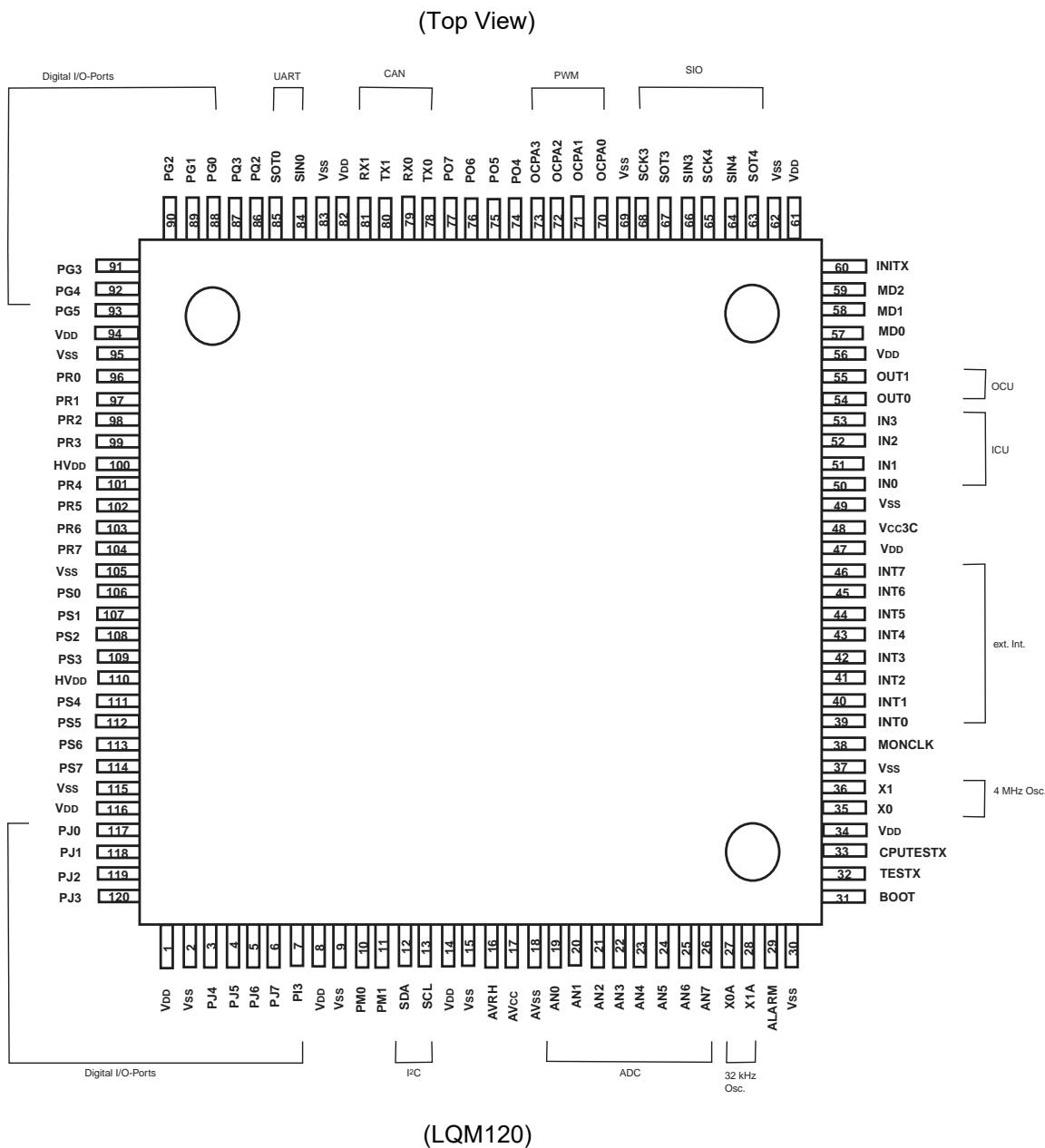
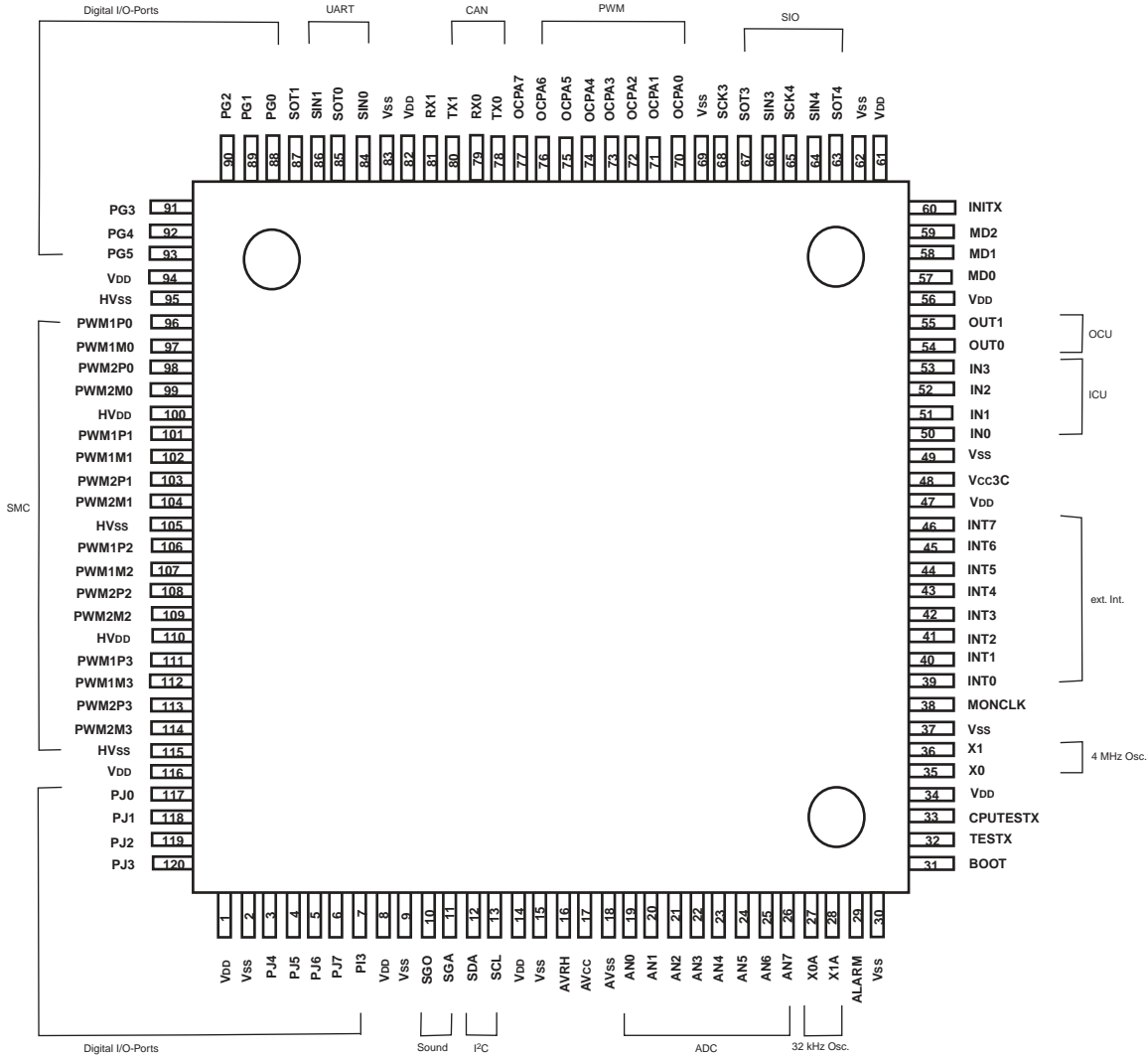


Figure 2-8. CY91366GA

(Top View)



(LQM120)

### 3. Pin Descriptions

Table 3-1. CY91FV360GA I/O Pins and their Functions

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	D18	I/O	–	Q	Ext. Bus Data Bit 18
2	D11	I/O	–	Q	Ext. Bus Data Bit 11
3	D2	I/O	–	Q	Ext. Bus Data Bit 2
4	Not Connected				
5	HV <sub>SS</sub>	–	–	–	–
6	HV <sub>DD5B</sub>	–	–	–	–
7	PWM2M1	I/O	PR7	M	SMC 1
8	PWM1M1	I/O	PR5	K	SMC 1
9	PWM1P0	I/O	PR0	K	SMC 0
10	V <sub>DD5R</sub>	–	–	–	–
11	V <sub>DD5P</sub>	–	–	–	–
12	SCK4	I/O	PN2	A	SIO Clock
13	V <sub>DD5J</sub>	–	–	–	–
14	EXRAM	I	–	P	Trace Control
15	TWRX	O	–	X	Trace Control
16	TAD9	O	–	X	Trace Address
17	TAD5	O	–	X	Trace Address
18	TAD3	O	–	X	Trace Address
19	TDT68	I/O	–	W	Trace Data
20	TDT63	I/O	–	W	Trace Data
21	TDT57	I/O	–	W	Trace Data
22	TDT49	I/O	–	W	Trace Data
23	TDT23	I/O	–	W	Trace Data
24	TDT16	I/O	–	W	Trace Data
25	TDT7	I/O	–	W	Trace Data
26	TDT2	I/O	–	W	Trace Data
27	ICD0	I/O	–	N	ICE Data
28	ICLK	I/O	–	L	ICE Clock
29	X0	I	–	H	4 MHz Oscillator Pin
30	INTX	I	–	U	Initial Pin
31	MD1	I	–	T	Mode Pin 1
32	IN3	I/O	PL3	A	ICU Input 3
33	INT3	I/O	PK3	A	Ext. Interrupt 3
34	AN3	I/O	PH3	B	ADC Input 3
35	DACK2	I/O	PB6	A	DMA Acknowledge 2
36	AN13	I/O	PG5	B	ADC Input 13
37	AN8	I/O	PG0	B	ADC Input 8
38	ALE	I/O	P91	A	Ext. Bus Control

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
39	WR1X	I/O	P85	S	Ext. Bus Control
40	RDX	I/O	P83	S	Ext. Bus Control
41	CS7X	I/O	–	A	Chip Select 7 (CAN)
42	A26	I/O	–	Q	Ext. Bus Address Bit 26
43	A20	I/O	–	Q	Ext. Bus Address Bit 20
44	A12	I/O	–	Q	Ext. Bus Address Bit 12
45	D21	I/O	–	Q	Ext. Bus Data Bit 21
46	D16	I/O	–	Q	Ext. Bus Data Bit 16
47	D13	I/O	–	Q	Ext. Bus Data Bit 13
48	D7	I/O	–	Q	Ext. Bus Data Bit 7
49	D3	I/O	–	Q	Ext. Bus Data Bit 3
50	V <sub>SS</sub>	–	–	–	–
51	PWM2P2	I/O	PS2	K	SMC 2
52	PWM2P1	I/O	PR6	K	SMC 1
53	PWM1P1	I/O	PR4	K	SMC 1
54	Not Connected				
55	SIN1	I/O	PQ2	A	UART 1 Input
56	TX3	I/O	PP6	Q	CAN 3 TX
57	SOT3	I/O	PN4	A	SIO Output
58	SOT4	I/O	PN0	A	SIO Output
59	Not Connected				
60	Not Connected				
61	SGO	I/O	PM0	A	Sound Generator SGO
62	TOEX	O	–	X	Trace Control
63	TAD8	O	–	X	Trace Address
64	TAD2	O	–	X	Trace Address
65	TDT67	I/O	–	W	Trace Data
66	TDT60	I/O	–	W	Trace Data
67	TDT54	I/O	–	W	Trace Data
68	TDT48	I/O	–	W	Trace Data
69	TDT26	I/O	–	W	Trace Data
70	TDT21	I/O	–	W	Trace Data
71	TDT18	I/O	–	W	Trace Data
72	TDT12	I/O	–	W	Trace Data
73	TDT8	I/O	–	W	Trace Data
74	TDT3	I/O	–	W	Trace Data
75	ICS2	O	–	G	ICE Status
76	V <sub>DD5F</sub>	–	–	–	–
77	RSTX	I	–	E	Reset Pin

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
78	OUT2	I/O	PL6	A	OCU Output 2
79	IN0	I/O	PL0	A	ICU Input 0
80	INT2	I/O	PK2	A	Ext. Interrupt 2
81	AN6	I/O	PH6	B	ADC Input 6
82	AN1	I/O	PH1	B	ADC Input 1
83	AV <sub>cc</sub>	–	–	–	Analog V <sub>cc</sub>
84	DEOP0	I/O	PB2	A	DMA EOP 0
85	AN14	I/O	PG6	B	ADC Input 14
86	AN9	I/O	PG1	B	ADC Input 9
87	AS	I/O	P90	A	Ext. Bus Control
88	BRQ	I/O	P82	A	Ext. Bus Control
89	CS6X	I/O	P76	A	Chip Select 6
90	A23	I/O	–	Q	Ext. Bus Address Bit 23
91	A17	I/O	–	Q	Ext. Bus Address Bit 17
92	A11	I/O	–	Q	Ext. Bus Address Bit 11
93	D27	I/O	–	Q	Ext. Bus Data Bit 27
94	D22	I/O	–	Q	Ext. Bus Data Bit 22
95	D17	I/O	–	Q	Ext. Bus Data Bit 17
96	D6	I/O	–	Q	Ext. Bus Data Bit 16
97	V <sub>DD5S</sub>	–	–	–	–
98	PWM1M3	I/O	PS5	K	SMC 3
99	PWM2M3	I/O	PS7	M	SMC 3
100	HV <sub>DD5A</sub>	–	–	–	–
101	PWM2P0	I/O	PR2	K	SMC0
102	V <sub>CC3C</sub>	–	–	C	Bypass Capacitor Pin
103	SOT1	I/O	PQ3	A	UART 1 Output
104	SIN0	I/O	PQ0	A	UART 0 Input
105	TX1	I/O	PP2	Q	CAN 1 TX
106	OCPA2	I/O	PO2	A	PPG Output
107	SCK3	I/O	PN5	A	SIO Clock
108	SIN4	I/O	PN1	A	SIO Input
109	SCL	I/O	PM3	Y	I <sup>2</sup> C SCL
110	TCLK	I/O	–	W	Trace Control
111	TAD12	O	–	X	Trace Address
112	TAD15	O	–	X	Trace Address
113	TAD1	O	–	X	Trace Address
114	TDT65	I/O	–	W	Trace Data
115	TDT59	I/O	–	W	Trace Data
116	TDT55	I/O	–	W	Trace Data



**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
117	TDT51	I/O	–	W	Trace Data
118	TDT42	I/O	–	W	Trace Data
119	TDT32	I/O	–	W	Trace Data
120	TDT27	I/O	–	W	Trace Data
121	TDT22	I/O	–	W	Trace Data
122	TDT11	I/O	–	W	Trace Data
123	TDT4	I/O	–	W	Trace Data
124	ICD3	I/O	–	N	ICE Data
125	TDT1	I/O	–	W	Trace Data
126	SELCLK	I	–	F	Clock Selection
127	NMIX	I	–	E	Non maskable Interrupt
128	OUT1	I/O	PL5	A	OCU Output 1
129	IN1	I/O	PL1	A	ICU Input 1
130	INT5	I/O	PK5	A	Ext. Interrupt 5
131	LED4	I/O	PJ4	J	LED Port 4
132	ALARM	I	–	D	Alarm Comparator Input
133	AN7	I/O	PH7	B	ADC Input 7
134	AN2	I/O	PH2	B	ADC Input 2
135	DACK0	I/O	PB1	A	DMA acknowledge 0
136	AN10	I/O	PG2	B	ADC Input 10
137	CS0X	I/O	P94	A	Chip select 0
138	CS3X	I/O	P97	A	Chip select 3
139	BGRNTX	I/O	P81	A	Ext. Bus Control
140	CS4X	I/O	P74	A	Chip select 4
141	A22	I/O	–	Q	Ext. Bus Address Bit 22
142	A18	I/O	–	Q	Ext. Bus Address Bit 18
143	A14	I/O	–	Q	Ext. Bus Address Bit 14
144	A5	I/O	–	Q	Ext. Bus Address Bit 5
145	INDEX	–	–	–	Index Pin
146	D30	I/O	–	Q	Ext. Bus Data Bit 30
147	D26	I/O	–	Q	Ext. Bus Data Bit 26
148	D19	I/O	–	Q	Ext. Bus Data Bit 19
149	D10	I/O	–	Q	Ext. Bus Data Bit 10
150	D9	I/O	–	Q	Ext. Bus Data Bit 9
151	D5	I/O	–	Q	Ext. Bus Data Bit 5
152	PWM2M2	I/O	PS3	M	SMC 2
153	PWM1P3	I/O	PS4	K	SMC 3
154	PWM2M0	I/O	PR3	M	SMC 0
155	V <sub>SS</sub>	–	–	–	–

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
156	SOT2	I/O	PQ5	A	UART 2 Output
157	SOT0	I/O	PQ1	A	UART 0 Output
158	V <sub>DD</sub> 50	–	–	–	–
159	OCPA7	I/O	PO7	A	PPG Output
160	OCPA5	I/O	PO5	A	PPG Output
161	OCPA1	I/O	PO1	A	PPG Output
162	V <sub>DD</sub> 5K	–	–	–	–
163	X1A	O	–	I	32 kHz Oscillator Pin
164	X0A	I	–	I	32 kHz Oscillator Pin
165	SDA	I/O	PM2	Y	I <sup>2</sup> C SDA
166	TAD10	O	–	X	Trace Address
167	TAD11	O	–	X	Trace Address
168	TDT66	I/O	–	W	Trace Data
169	TDT61	I/O	–	W	Trace Data
170	TDT58	I/O	–	W	Trace Data
171	TDT52	I/O	–	W	Trace Data
172	TDT45	I/O	–	W	Trace Data
173	TDT39	I/O	–	W	Trace Data
174	TDT35	I/O	–	W	Trace Data
175	TDT31	I/O	–	W	Trace Data
176	TDT24	I/O	–	W	Trace Data
177	TDT15	I/O	–	W	Trace Data
178	TDT14	I/O	–	W	Trace Data
179	TDT10	I/O	–	W	Trace Data
180	ICD1	I/O	–	N	ICE Data
181	ICD2	I/O	–	N	ICE Data
182	HSTX	I	–	E	Hardware Standby
183	OUT3	I/O	PL7	A	OCU Output 3
184	OUT0	I/O	PL4	A	OCU Output 0
185	INT6	I/O	PK6	A	Ext. Interrupt 6
186	LED7	I/O	PJ7	J	LED Port 7
187	LED1	I/O	PJ1	J	LED Port 1
188	CPUTESTX	I	–	E	Test Input
189	DA1	O	–	C	DAC Output
190	AN4	I/O	PH4	B	ADC Input 4
191	DEOP1	I/O	PB5	A	DMA EOP 1
192	DACK1	I/O	PB4	A	DMA Acknowledge 1
193	DREQ0	I/O	PB0	A	DMA Request 0
194	CLK	I/O	P92	A	Ext. Bus Clock

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
195	AH/BOOT	I/O	P93	A	Ext. Bus Control/Boot Signal
196	CS5X	I/O	P75	A	Chip Select 5
197	A24	I/O	–	Q	Ext. Bus Address Bit 24
198	A21	I/O	–	Q	Ext. Bus Address Bit 21
199	A15	I/O	–	Q	Ext. Bus Address Bit 15
200	A8	I/O	–	Q	Ext. Bus Address Bit 8
201	A2	I/O	–	Q	Ext. Bus Address Bit 2
202	A0	I/O	–	Q	Ext. Bus Address Bit 0
203	D29	I/O	–	Q	Ext. Bus Address Bit 29
204	D25	I/O	–	Q	Ext. Bus Address Bit 25
205	D20	I/O	–	Q	Ext. Bus Address Bit 20
206	D15	I/O	–	Q	Ext. Bus Address Bit 15
207	D4	I/O	–	Q	Ext. Bus Address Bit 4
208	HV <sub>DD5C</sub>	–	–	–	–
209	PWM1M2	I/O	PS1	K	SMC2
210	PWM1P2	I/O	PS0	K	SMC2
211	PWM1M0	I/O	PR1	K	SMC0
212	SIN2	I/O	PQ4	A	UART 2 Input
213	RX3	I/O	PP7	Q	CAN 3 RX
214	V <sub>SS</sub>	–	–	–	–
215	RX0	I/O	PP1	Q	CAN 0 RX
216	V <sub>DD5N</sub>	–	–	–	–
217	OCPA4	I/O	PO4	A	PPG Output
218	OCPA0	I/O	PO0	A	PPG Output
219	SIN3	I/O	PN3	A	SIO Input
220	V <sub>SS</sub>	–	–	–	–
221	SGA	I/O	PM1	A	Sound Generator SGA
222	TAD13	O	–	X	Trace Address
223	TAD7	O	–	X	Trace Address
224	TAD6	O	–	X	Trace Address
225	TDT64	I/O	–	W	Trace Data
226	TDT56	I/O	–	W	Trace Data
227	TDT50	I/O	–	W	Trace Data
228	TDT44	I/O	–	W	Trace Data
229	TDT41	I/O	–	W	Trace Data
230	TDT37	I/O	–	W	Trace Data
231	TDT34	I/O	–	W	Trace Data
232	TDT30	I/O	–	W	Trace Data
233	TDT25	I/O	–	W	Trace Data

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
234	TDT20	I/O	–	W	Trace Data
235	TDT9	I/O	–	W	Trace Data
236	BREAK	I	–	O	ICE Break
237	ICS1	O	–	G	ICE Status
238	ICS0	O	–	G	ICE Status
239	MD2	I	–	T	Mode Pin 2
240	IN2	I/O	PL2	A	ICU Input 2
241	INT4	I/O	PK4	A	Ext. Interrupt 4
242	LED6	I/O	PJ6	J	LED Port 6
243	LED3	I/O	PJ3	J	LED Port 3
244	Not Connected				
245	TESTX	I	–	E	Test Input
246	DA0	O	–	C	DAC Output
247	AN5	I/O	PH5	B	ADC Input 5
248	AN0	I/O	PH0	B	ADC Input 0
249	AN15	I/O	PG7	B	ADC Input 15
250	CS1X	I/O	P95	A	Chip select 1
251	WR3X	I/O	P87	S	Ext. Bus Control
252	WR2X	I/O	P86	S	Ext. Bus Control
253	DREQ2	I/O	P73	A	DMA Request 2
254	A19	I/O	–	Q	Ext. Bus Address Bit 19
255	A13	I/O	–	Q	Ext. Bus Address Bit 13
256	A7	I/O	–	Q	Ext. Bus Address Bit 7
257	A4	I/O	–	Q	Ext. Bus Address Bit 4
258	D31	I/O	–	Q	Ext. Bus Data Bit 31
259	D28	I/O	–	Q	Ext. Bus Data Bit 28
260	D23	I/O	–	Q	Ext. Bus Data Bit 23
261	D14	I/O	–	Q	Ext. Bus Data Bit 14
262	D8	I/O	–	Q	Ext. Bus Data Bit 8
263	D1	I/O	–	Q	Ext. Bus Data Bit 1
264	D0	I/O	–	Q	Ext. Bus Data Bit 0
265	Not Connected				
266	HV <sub>SS</sub>	–	–	–	–
267	Not Connected				
268	V <sub>SS</sub>	–	–	–	–
269	RX2	I/O	PP5	Q	CAN 2 RX
270	RX1	I/O	PP3	Q	CAN 1 RX
271	V <sub>SS</sub>	–	–	–	–
272	OCPA3	I/O	PO3	A	PPG Output

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
273	V <sub>SS</sub>	–	–	–	–
274	Not Connected				
275	V <sub>DD5I</sub>	–	–	–	–
276	TADSCX	O	–	X	Trace Control
277	TCE1X	O	–	X	Trace Control
278	TAD4	O	–	X	Trace Address
279	TAD0	O	–	X	Trace Address
280	TDT62	I/O	–	W	Trace Data
281	TDT53	I/O	–	W	Trace Data
282	TDT47	I/O	–	W	Trace Data
283	TDT43	I/O	–	W	Trace Data
284	TDT36	I/O	–	W	Trace Data
285	TDT33	I/O	–	W	Trace Data
286	TDT28	I/O	–	W	Trace Data
287	TDT19	I/O	–	W	Trace Data
288	TDT13	I/O	–	W	Trace Data
289	TDT6	I/O	–	W	Trace Data
290	TDT5	I/O	–	W	Trace Data
291	X1	O	–	H	4 MHz Oscillator Pin
292	MONCLK	O	–	G	Clock Output for test purposes
293	MD0	I	–	T	Mode Pin 0
294	INT7	I/O	PK7	A	Ext. Interrupt 7
295	INT1	I/O	PK1	A	Ext. Interrupt 1
296	LED5	I/O	PJ5	J	LED Port 5
297	LTESTX	I	–	E	Test Input
298	ATGX	I/O	PI3	A	Analog Reference Low
299	AVRL	–	–	R	Analog Reference High
300	AVRH	–	–	R	DMA Request 1
301	DREQ1	I/O	PB3	A	ADC Input 12
302	AN12	I/O	PG4	B	ADC Input 11
303	AN11	I/O	PG3	B	Ext. Bus Control
304	WROX	I/O	P84	S	Ext. Bus Control
305	RDY	I/O	–	S	Ext. Bus Control
306	A25	I/O	–	Q	Ext. Bus Address Bit 25
307	A16	I/O	–	Q	Ext. Bus Address Bit 16
308	A10	I/O	–	Q	Ext. Bus Address Bit 10
309	A6	I/O	–	Q	Ext. Bus Address Bit 6
310	A1	I/O	–	Q	Ext. Bus Address Bit 1
311	Not Connected				

**Table 3-1. CY91FV360GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
312	D24	I/O	–	Q	Ext. Bus Data Bit 24
313	D12	I/O	–	Q	Ext. Bus Data Bit 12
314	Not Connected				
315	PWM2P3	I/O	PS6	K	SMC 3
316	HV <sub>SS</sub>	–	–	–	–
317	HV <sub>SS</sub>	–	–	–	–
318	Not Connected				
319	V <sub>DD5Q</sub>	–	–	–	–
320	TX2	I/O	PP4	Q	CAN 2 TX
321	TX0	I/O	PP0	Q	CAN 0 TX
322	OCPA6	I/O	PO6	A	PPG Output
323	V <sub>DD5M</sub>	–	–	–	–
324	V <sub>DD5L</sub>	–	–	–	–
325	Not Connected				
326	V <sub>DD5H</sub>	–	–	–	–
327	TAD14	O	–	X	Trace Address
328	V <sub>SS3</sub>	–	–	–	–
329	V <sub>SS3</sub>	–	–	–	–
330	Not Connected				
331	V <sub>DD3C</sub>	–	–	–	–
332	TDT46	I/O	–	W	Trace Data
333	TDT40	I/O	–	W	Trace Data
334	TDT38	I/O	–	W	Trace Data
335	V <sub>DD3B</sub>	–	–	–	–
336	TDT29	I/O	–	W	Trace Data
337	TDT17	I/O	–	W	Trace Data
338	V <sub>DD3A</sub>	–	–	–	–
339	TDT0	I/O	–	W	Trace Data
340	V <sub>SS</sub>	–	–	–	–
341	V <sub>SS</sub>	–	–	–	–
342	Not Connected				
343	V <sub>DD5E</sub>	–	–	–	–
344	INT0	I/O	PK0	A	Ext. Interrupt 0
345	LED2	I/O	PJ2	J	LED Port 2
346	LED0	I/O	PJ0	J	LED Port 0
347	V <sub>DD5D</sub>	–	–	–	–
348	AV <sub>SS</sub>	–	–	–	Analog V <sub>SS</sub>
349	DEOP2	I/O	PB7	A	DMA EOP 2
350	V <sub>DD5C</sub>	–	–	–	–

**Table 3-1. CY91FV360GA I/O Pins and their Functions** *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
351	CS2X	I/O	P96	A	Chip Select 2
352	V <sub>SS</sub>	–	–	–	–
353	V <sub>SS</sub>	–	–	–	–
354	V <sub>DD5B</sub>	–	–	–	–
355	Not Connected				
356	A9	I/O	–	Q	Ext. Bus Address Bit 9
357	A3	I/O	–	Q	Ext. Bus Address Bit 3
358	V <sub>SS</sub>	–	–	–	–
359	V <sub>SS</sub>	–	–	–	–
360	V <sub>DD5T</sub>	–	–	–	–
361	V <sub>SS</sub>	–	–	–	–
362	V <sub>SS</sub>	–	–	–	–
363	V <sub>SS</sub>	–	–	–	–
364	Not Connected				
365	HV <sub>SS</sub>	–	–	–	–
366	V <sub>SS</sub>	–	–	–	–
367	V <sub>SS</sub>	–	–	–	–
368	Not Connected				
369	V <sub>SS</sub>	–	–	–	–
370	V <sub>SS</sub>	–	–	–	–
371	Not Connected				
372	V <sub>SS</sub>	–	–	–	–
373	V <sub>SS</sub>	–	–	–	–
374	V <sub>SS</sub>	–	–	–	–
375	V <sub>DD3D</sub>	–	–	–	–
376	V <sub>SS3</sub>	–	–	–	–
377	V <sub>SS3</sub>	–	–	–	–
378	V <sub>SS3</sub>	–	–	–	–
379	Not Connected				
380	V <sub>SS3</sub>	–	–	–	–
381	V <sub>SS3</sub>	–	–	–	–
382	Not Connected				
383	V <sub>SS3</sub>	–	–	–	–
384	V <sub>SS3</sub>	–	–	–	–
385	V <sub>SS3</sub>	–	–	–	–
386	V <sub>DD5G</sub>	–	–	–	–
387	V <sub>SS</sub>	–	–	–	–
388	V <sub>SS</sub>	–	–	–	–
389	V <sub>SS</sub>	–	–	–	–

**Table 3-1. CY91FV360GA I/O Pins and their Functions** *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
390	Not Connected				
391	V <sub>SS</sub>	–	–	–	–
392	V <sub>SS</sub>	–	–	–	–
393	Not Connected				
394	V <sub>SS</sub>	–	–	–	–
395	V <sub>SS</sub>	–	–	–	–
396	V <sub>SS</sub>	–	–	–	–
397	Not Connected				
398	V <sub>SS</sub>	–	–	–	–
399	V <sub>SS</sub>	–	–	–	–
400	V <sub>SS</sub>	–	–	–	–
401	V <sub>DD5A</sub>	–	–	–	–

**Table 3-2. CY91FV362GB I/O Pins and their Functions**

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	D24	I/O	–	Q	Ext. Bus Data Bit 24
2	D25	I/O	–	Q	Ext. Bus Data Bit 25
3	D26	I/O	–	Q	Ext. Bus Data Bit 26
4	D27	I/O	–	Q	Ext. Bus Data Bit 27
5	D28	I/O	–	Q	Ext. Bus Data Bit 28
6	D29	I/O	–	Q	Ext. Bus Data Bit 29
7	D30	I/O	–	Q	Ext. Bus Data Bit 30
8	D31	I/O	–	Q	Ext. Bus Data Bit 31
9	A0	I/O	–	Q	Ext. Bus Address Bit 0
10	A1	I/O	–	Q	Ext. Bus Address Bit 1
11	A2	I/O	–	Q	Ext. Bus Address Bit 2
12	A3	I/O	–	Q	Ext. Bus Address Bit 3
13	A4	I/O	–	Q	Ext. Bus Address Bit 4
14	A5	I/O	–	Q	Ext. Bus Address Bit 5
15	A6	I/O	–	Q	Ext. Bus Address Bit 6
16	A7	I/O	–	Q	Ext. Bus Address Bit 7
17	A8	I/O	–	Q	Ext. Bus Address Bit 8
18	A9	I/O	–	Q	Ext. Bus Address Bit 9
19	A10	I/O	–	Q	Ext. Bus Address Bit 10
20	A11	I/O	–	Q	Ext. Bus Address Bit 11
21	A12	I/O	–	Q	Ext. Bus Address Bit 12
22	A13	I/O	–	Q	Ext. Bus Address Bit 13
23	A14	I/O	–	Q	Ext. Bus Address Bit 14



**Table 3-2. CY91FV362GB I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
24	A15	I/O	–	Q	Ext. Bus Address Bit 15
25	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus VDD, 3.3 V or 5.0 V
26	V <sub>SS</sub>	–	–	–	–
27	A16	I/O	–	Q	Ext. Bus Address Bit 16
28	A17	I/O	–	Q	Ext. Bus Address Bit 17
29	A18	I/O	–	Q	Ext. Bus Address Bit 18
30	A19	I/O	–	Q	Ext. Bus Address Bit 19
31	A20	I/O	–	Q	Ext. Bus Address Bit 20
32	CS4X	I/O	P74	A	Chip Select 4
33	CS5X	I/O	P75	A	Chip Select 5
34	CS6X	I/O	P76	A	Chip Select 6
35	RDY	I/O	–	S	Ext. Bus Control
36	BGRNT	I/O	P81	A	Ext. Bus Control
37	BRQ	I/O	P82	A	Ext. Bus Control
38	RDX	I/O	–	S	Ext. Bus Control
39	WROX	I/O	–	S	Ext. Bus Control
40	WR1X	I/O	–	S	Ext. Bus Control
41	WR2X	I/O	–	S	Ext. Bus Control
42	WR3X	I/O	–	S	Ext. Bus Control
43	AS	I/O	P90	A	Ext. Bus Control
44	ALE	I/O	P91	A	Ext. Bus Control
45	CLK	I/O	–	A	Ext. Bus Clock
46	AH	I/O	P93	A	Ext. Bus Control Signal
47	CS0X	I/O	P94	A	Chip select 0
48	CS1X	I/O	P95	A	Chip select 1
49	CS2X	I/O	P96	A	Chip select 2
50	CS3X	I/O	P97	A	Chip select 3
51	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
52	V <sub>SS</sub>	–	–	–	–
53	AN8	I/O	PG0	B	ADC Input 8
54	AN9	I/O	PG1	B	ADC Input 9
55	AN10	I/O	PG2	B	ADC Input 10
56	AN11	I/O	PG3	B	ADC Input 11
57	AN12	I/O	PG4	B	ADC Input 12
58	AN13	I/O	PG5	B	ADC Input 13
59	AN14	I/O	PG6	B	ADC Input 14
60	AN15	I/O	PG7	B	ADC Input 15
61	DREQ0	I/O	PB0	A	DMR Request 0
62	DACK0	I/O	PB1	A	DMA Acknowledge 0

**Table 3-2. CY91FV362GB I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
63	DEOP0	I/O	PB2	A	DMA EOP 0
64	A	–	–	–	Analog V <sub>cc</sub>
65	AVRH	–	–	R	Analog Reference High
66	AN0	I/O	PH0	B	ADC Input 0
67	AN1	I/O	PH1	B	ADC Input 1
68	AN2	I/O	PH2	B	ADC Input 2
69	AN3	I/O	PH3	B	ADC Input 3
70	AN4	I/O	PH4	B	ADC Input 4
71	AN5	I/O	PH5	B	ADC Input 5
72	AN6	I/O	PH6	B	ADC Input 6
73	AN7	I/O	PH7	B	ADC Input 7
74	AV <sub>ss</sub>	–	–	–	Analog V <sub>ss</sub> , Analog Reference Low
75	DA0	O	–	C	DAC Output
76	DA1	O	–	C	DAC Output
77	ALARM	I	–	D	Alarm Comparator Input
78	V <sub>ss</sub>	–	–	–	–
79	V <sub>DD</sub>	–	–	–	–
80	ATGX	I/O	PI3	A	ADC Trigger Input
81	TESTX	I	–	E	Test Input (should be connected to V <sub>DD</sub> )
82	CPUTESTX	I	–	E	Test Input (should be connected to V <sub>DD</sub> )
83	LTESTX	I	–	E	Test Input (should be connected to V <sub>DD</sub> )
84	LED0	I/O	PJ0	J	LED Port 0
85	LED1	I/O	PJ1	J	LED Port 1
86	LED2	I/O	PJ2	J	LED Port 2
87	LED3	I/O	PJ3	J	LED Port 3
88	LED4	I/O	PJ4	J	LED Port 4
89	LED5	I/O	PJ5	J	LED Port 5
90	LED6	I/O	PJ6	J	LED Port 6
91	LED7	I/O	PJ7	J	LED Port 7
92	V <sub>DD</sub>	–	–	–	–
93	V <sub>ss</sub>	–	–	–	–
94	INT0	I/O	PK0	A	Ext. Interrupt 0
95	INT1	I/O	PK1	A	Ext. Interrupt 1
96	INT2	I/O	PK2	A	Ext. Interrupt 2
97	INT3	I/O	PK3	A	Ext. Interrupt 3
98	INT4	I/O	PK4	A	Ext. Interrupt 4
99	INT5	I/O	PK5	A	Ext. Interrupt 5

**Table 3-2. CY91FV362GB I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
100	INT6	I/O	PK6	A	Ext. Interrupt 6
101	INT7	I/O	PK7	A	Ext. Interrupt 7
102	IN0	I/O	PL0	A	ICU Input 0
103	IN1	I/O	PL1	A	ICU Input 1
104	IN2	I/O	PL2	A	ICU Input 2
105	IN3	I/O	PL3	A	ICU Input 3
106	OUT0	I/O	PL4	A	OCU Output 0
107	OUT1	I/O	PL5	A	OCU Output 1
108	OUT2	I/O	PL6	A	OCU Output 2
109	OUT3	I/O	PL7	A	OCU Output 3
110	V <sub>SS</sub>	–	–	–	–
111	MD0	I	–	T	Mode Pin 0
112	MD1	I	–	T	Mode Pin 1
113	MD2	I	–	T	Mode Pin 2
114	HSTX	I	–	E	Hardware Standby
115	INITX	I	–	U	Initial Pin
116	MONCLK	O	–	G	System Clock Output for Evaluation Purposes
117	SELCLK	I	–	F	Clock Selection, must be connected to V <sub>DD</sub>
118	V <sub>DD</sub>	–	–	–	–
119	X0	I	–	H	4 MHz Oscillator Pin
120	X1	O	–	H	4 MHz Oscillator Pin
121	X0A	I	–	I	Reserved-must be connected to V <sub>SS</sub>
122	X1A	O	–	I	Reserved-should be left open
123	V <sub>SS</sub>	–	–	–	–
124	CPO	–	–	C	Reserved-should be left open
125	VCI	–	–	D	Reserved-must be connected to V <sub>SS</sub>
126	SGO	I/O	PM0	A	Sound Generator SGO
127	SGA	I/O	PM1	A	Sound Generator SGA
128	SDA	I/O	PM2	Y	I <sup>2</sup> C SDA
129	SCL	I/O	PM3	Y	I <sup>2</sup> C SCL
130	SOT4	I/O	PN0	A	SIO Output
131	SIN4	I/O	PN1	A	SIO Input
132	SCK4	I/O	PN2	A	SIO Clock
133	SIN3	I/O	PN3	A	SIO Input
134	SOT3	I/O	PN4	A	SIO Output
135	SCK3	I/O	PN5	A	SIO Clock
136	OCPA 0	I/O	PO0	A	PPG Output
137	OCPA 1	I/O	PO1	A	PPG Output

**Table 3-2. CY91FV362GB I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
138	OCPA 2	I/O	PO2	A	PPG Output
139	OCPA 3	I/O	PO3	A	PPG Output
140	OCPA 4	I/O	PO4	A	PPG Output
141	OCPA 5	I/O	PO5	A	PPG Output
142	OCPA 6	I/O	PO6	A	PPG Output
143	OCPA 7	I/O	PO7	A	PPG Output
144	V <sub>DD</sub>	–	–	–	–
145	V <sub>SS</sub>	–	–	–	–
146	TX0	I/O	PP0	Q	CAN 0 TX
147	RX0	I/O	PP1	Q	CAN 0 RX
148	TX1	I/O	PP2	Q	CAN 1 TX
149	RX1	I/O	PP3	Q	CAN 1 RX
150	TX2	I/O	PP4	Q	CAN 2 TX
151	RX2	I/O	PP5	Q	CAN 2 RX
152	SIN0	I/O	PQ0	A	UART 0 Input
153	SOT0	I/O	PQ1	A	UART 0 Output
154	SIN1	I/O	PQ2	A	UART 1 Input
155	SOT1	I/O	PQ3	A	UART 1 Output
156	SIN2	I/O	PQ4	A	UART 2 Input
157	SOT2	I/O	PQ5	A	UART 2 Output
158	V <sub>SS</sub>	–	–	–	–
159	V <sub>CC3C</sub>	–	–	C	Bypass Capacitor Pin
160	V <sub>DD</sub>	–	–	–	–
161	HV <sub>SS</sub>	–	–	–	–
162	PWM1P0	I/O	PR0	K	SMC 0
163	PWM1M0	I/O	PR1	K	SMC 0
164	PWM2P0	I/O	PR2	K	SMC 0
165	PWM2M0	I/O	PR3	M	SMC 0
166	HV <sub>DD</sub>	–	–	–	–
167	PWM1P1	I/O	PR4	K	SMC 1
168	PWM1M1	I/O	PR5	K	SMC 1
169	PWM2P1	I/O	PR6	K	SMC 1
170	PWM2M1	I/O	PR7	M	SMC 1
171	HV <sub>SS</sub>	–	–	–	–
172	PWM1P2	I/O	PS0	K	SMC 2
173	PWM1M2	I/O	PS1	K	SMC 2
174	PWM2P2	I/O	PS2	K	SMC 2
175	PWM2M2	I/O	PS3	M	SMC 2
176	HV <sub>DD</sub>	–	–	–	–

**Table 3-2. CY91FV362GB I/O Pins and their Functions** *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
177	PWM1P3	I/O	PS4	K	SMC 3
178	PWM1M3	I/O	PS5	K	SMC 3
179	PWM2P3	I/O	PS6	K	SMC 3
180	PWM2M3	I/O	PS7	M	SMC 3
181	HV <sub>SS</sub>	–	–	–	–
182	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
183	D0	I/O	–	Q	Ext. Bus Data Bit 0
184	D1	I/O	–	Q	Ext. Bus Data Bit 1
185	D2	I/O	–	Q	Ext. Bus Data Bit 2
186	D3	I/O	–	Q	Ext. Bus Data Bit 3
187	D4	I/O	–	Q	Ext. Bus Data Bit 4
188	D5	I/O	–	Q	Ext. Bus Data Bit 5
189	D6	I/O	–	Q	Ext. Bus Data Bit 6
190	D7	I/O	–	Q	Ext. Bus Data Bit 7
191	D8	I/O	–	Q	Ext. Bus Data Bit 8
192	D9	I/O	–	Q	Ext. Bus Data Bit 9
193	D10	I/O	–	Q	Ext. Bus Data Bit 10
194	D11	I/O	–	Q	Ext. Bus Data Bit 11
195	D12	I/O	–	Q	Ext. Bus Data Bit 12
196	D13	I/O	–	Q	Ext. Bus Data Bit 13
197	D14	I/O	–	Q	Ext. Bus Data Bit 14
198	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
199	V <sub>SS</sub>	–	–	–	–
200	D15	I/O	–	Q	Ext. Bus Data Bit 15
201	D16	I/O	–	Q	Ext. Bus Data Bit 16
202	D17	I/O	–	Q	Ext. Bus Data Bit 17
203	D18	I/O	–	Q	Ext. Bus Data Bit 18
204	D19	I/O	–	Q	Ext. Bus Data Bit 19
205	D20	I/O	–	Q	Ext. Bus Data Bit 20
206	D21	I/O	–	Q	Ext. Bus Data Bit 21
207	D22	I/O	–	Q	Ext. Bus Data Bit 22
208	D23	I/O	–	Q	Ext. Bus Data Bit 23

Note: If pins V<sub>DD35</sub> (25, 51, 182, 198) are connected to 3.3 V then the external bus interface (pins 1-52, 182-208) can be operated at 3.3 V levels.

**Table 3-3. CY91F364G I/O Pins and their Functions**

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	AN0	I/O	PH0	B	ADC Input 0
2	AN1	I/O	PH1	B	ADC Input 1
3	AN2	I/O	PH2	B	ADC Input 2
4	AN3	I/O	PH3	B	ADC Input 3
5	AN4	I/O	PH4	B	ADC Input 4
6	AN5	I/O	PH5	B	ADC Input 5
7	AV <sub>ss</sub> , AVRL	–	–	–	AV <sub>ss</sub> , Analog Reference Low
8	AVRH	–	–	R	Analog Reference High
9	AV <sub>cc</sub>	–	–	–	AV <sub>cc</sub>
10	AN6	I/O	PH6	B	ADC Input 6
11	AN7	I/O	PH7	B	ADC Input 7
12	AN8	I/O	PG0	B	ADC Input 8
13	AN9	I/O	PG1	B	ADC Input 9
14	AN10	I/O	PG2	B	ADC Input 10
15	AN11	I/O	PG3	B	ADC Input 11
16	V <sub>ss</sub>	–	–	–	–
17	V <sub>DD</sub>	–	–	–	–
18	SDA	I/O	PM2	YA	I <sup>2</sup> C SDA
19	SCL	I/O	PM3	YA	I <sup>2</sup> C SCL
20	SOT0	I/O	PQ1	A	UART 0 SOT
21	SIN0	I/O	PQ0	A	UART 0 SIN
22	HSTX	I	–	F	Hardware Standby
23	NMIX	I	–	E	Non Maskable Interrupt
24	SELCLK	I	–	F	Select RTC Clock
25	V <sub>DD</sub>	–	–	–	–
26	MONCLK	O	–	Q1	Modulated Clock Output
27	V <sub>ss</sub>	–	–	–	–
28	X1A	O	–	I	32 kHz Oscillator Pin
29	X0A	I	–	I	32 kHz Oscillator Pin
30	V <sub>DD</sub>	–	–	–	–
31	X1	O	–	H	4 MHz Oscillator Pin
32	X0	I	–	H	4 MHz Oscillator Pin
33	V <sub>ss</sub>	–	–	–	–
34	INT0	I/O	PK0	B	External Interrupt 0
35	INT1	I/O	PK1	B	External Interrupt 1
36	INT2	I/O	PK2	B	External Interrupt 2
37	INT3	I/O	PK3	B	External Interrupt 3

**Table 3-3. CY91F364G I/O Pins and their Functions** (continued)

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
38	INT4	I/O	PK4	B	External Interrupt 4
39	INT5	I/O	PK5	B	External Interrupt 5
40	INT6	I/O	PK6	B	External Interrupt 6
41	INT7	I/O	PK7	B	External Interrupt 7
42	V <sub>DD</sub>	–	–	–	–
43	V <sub>SS</sub>	–	–	–	–
44	IN0	I/O	PL0	B	ICU Input 0 <sup>a</sup>
45	IN1	I/O	PL1	B	ICU Input 1 <sup>a</sup>
46	IN2	I/O	PL2	B	ICU Input 2 <sup>a</sup>
47	IN3	I/O	PL3	B	ICU Input 3 <sup>a</sup>
48	OUT0	I/O	PL4	B	OCU Output 0
49	OUT1	I/O	PL5	B	OCU Output 1
50	OUT2	I/O	PL6	B	OCU Output 2
51	OUT3	I/O	PL7	B	OCU Output 3
52	V <sub>DD</sub>	–	–	–	–
53	V <sub>SS</sub>	–	–	–	–
54	TESTX	I	–	E	Test Input
55	CPUTESTX	I	–	E	Test Input
56	ATGX	I/O	PI3	A	ADC Trigger
57	MD0	I	–	T	Mode Pin 0
58	MD1	I	–	T	Mode Pin 1
59	MD2	I	–	T	Mode Pin 2
60	INITX	I	–	U	Initial Pin
61	V <sub>DD</sub>	–	–	–	–
62	V <sub>CC3C</sub>	–	–	–	Pins for power supply capacitor or for external power supply of core voltage
63	V <sub>CC3C</sub>	–	–	–	
64	V <sub>SS</sub> (#)	–	–	–	
65	V <sub>DDL</sub>	–	–	–	Separate Core Power Supply
66	V <sub>DDL</sub>	–	–	–	
67	V <sub>DDL</sub>	–	–	–	
68	BREAKX	I	BREAKX	E	EDSU Break Pin
69	V <sub>DD</sub>	–	–	–	–
70	V <sub>SS</sub>	–	–	–	–
71	RX0	I/O	PP1	Q	CAN RX
72	TX0	I/O	PP0	Q	CAN TX
73	OCPA0	I/O	PO0	A	PPG Output 0
74	OCPA1	I/O	PO1	A	PPG Output 1
75	OCPA2	I/O	PO2	A	PPG Output 2

**Table 3-3. CY91F364G I/O Pins and their Functions** *(continued)*

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
76	OCPA3	I/O	PO3	A	PPG Output 3
77	V <sub>SS</sub>	–	–	–	–
78	SIN5	I/O	PT0	A	USART 5 SIN
79	SCK5	I/O	PT1	A	USART 5 SCK
80	SOT5	I/O	PT2	A	USART 5 SOT
81	SOT6	I/O	PT3	A	USART 6 SOT
82	SCK6	I/O	PT4	A	USART 6 SCK
83	SIN6	I/O	PT5	A	USART 6 SIN
84	V <sub>DD</sub>	–	–	–	–
85	V <sub>SS</sub>	–	–	–	–
86	SIN3	I/O	PN3	A	SIO SIN
87	SOT3	I/O	PN4	A	SIO SOT
88	SCK3	I/O	PN5	A	SIO SCK
89	V <sub>SS</sub>	–	–	–	–
90	LTESTX	I	LTESTX	E	Test Pin
91	V <sub>DD</sub>	–	–	–	–
92	PR0	I/O	PR0	A	Port R 0
93	PR1	I/O	PR1	A	Port R 1
94	PR2	I/O	PR2	A	Port R 2
95	PR3	I/O	PR3	A	Port R 3
96	PR4	I/O	PR4	A	Port R 4
97	PR5	I/O	PR5	A	Port R 5
98	PR6	I/O	PR6	A	Port R 6
99	PR7	I/O	PR7	A	Port R 7
100	V <sub>SS</sub>	–	–	–	–
101	V <sub>DD</sub>	–	–	–	–
102	LED0	I/O	PJ0	J	LED Port 0
103	LED1	I/O	PJ1	J	LED Port 1
104	LED2	I/O	PJ2	J	LED Port 2
105	LED3	I/O	PJ3	J	LED Port 3
106	V <sub>SS</sub>	–	–	–	–
107	LED4	I/O	PJ4	J	LED Port 4
108	LED5	I/O	PJ5	J	LED Port 5
109	LED6	I/O	PJ6	J	LED Port 6
110	LED7	I/O	PJ7	J	LED Port 7
111	V <sub>SS</sub>	–	–	–	–
112	V <sub>DD</sub>	–	–	–	–
113	PO4	I/O	PO4	A	Port O 4



**Table 3-3. CY91F364G I/O Pins and their Functions** (continued)

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
114	PO5	I/O	PO5	A	Port O 5
115	PO6	I/O	PO6	A	Port O 6
116	PO7	I/O	PO7	A	Port O 7
117	DA0	O	–	C	<sup>c</sup>
118	DA1	O	–	C	<sup>c</sup>
119	V <sub>SS</sub>	–	–	–	–
120	V <sub>DD</sub>	–	–	–	–

- a. If the port L function register bits are cleared, the ICU input lines are connected with the LSYNC outputs of the LIN-USARTs.  
b. Pin 064 (V<sub>SS</sub>) will be available after redesign.  
c. The pins DA1 and DA0 are also used for digital test functions. To ensure proper system function, always write “0” to port P R-bus port data direction register DDRP [3:2] and port P R-bus port function register PFRP [3:2].

**Table 3-4. CY91F369GA I/O Pins and their Functions**

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	A4	I/O	–	Q	Ext. Bus Address Bit 4
2	A5	I/O	–	Q	Ext. Bus Address Bit 5
3	A6	I/O	–	Q	Ext. Bus Address Bit 6
4	A7	I/O	–	Q	Ext. Bus Address Bit 7
5	A8	I/O	–	Q	Ext. Bus Address Bit 8
6	A9	I/O	–	Q	Ext. Bus Address Bit 9
7	A10	I/O	–	Q	Ext. Bus Address Bit 10
8	A11	I/O	–	Q	Ext. Bus Address Bit 11
9	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
10	CLK	I/O	–	A	Ext. Bus Clock
11	V <sub>SS</sub>	–	–	–	–
12	A12	I/O	–	Q	Ext. Bus Address Bit 12
13	A13	I/O	–	Q	Ext. Bus Address Bit 13
14	A14	I/O	–	Q	Ext. Bus Address Bit 14
15	A15	I/O	–	Q	Ext. Bus Address Bit 15
16	A16	I/O	–	Q	Ext. Bus Address Bit 16
17	A17	I/O	–	Q	Ext. Bus Address Bit 17
18	A18	I/O	–	Q	Ext. Bus Address Bit 18
19	A19	I/O	–	Q	Ext. Bus Address Bit 19
20	A20	I/O	–	Q	Ext. Bus Address Bit 20
21	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
22	V <sub>SS</sub>	–	–	–	–
23	CS4X	I/O	P74	A	Chip Select 4
24	CS5X	I/O	P75	A	Chip Select 5
25	CS6X	I/O	P76	A	Chip Select 6

**Table 3-4. CY91F369GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
26	RDX	I/O	–	S	Ext. Bus Control
27	BGRNTX	I/O	P81	A	Ext. Bus Control
28	BRQ	I/O	P82	A	Ext. Bus Control
29	AS	I/O	P90	A	Ext. Bus Control
30	ALE	I/O	P91	A	Ext. Bus Control
31	AH	I/O	P93	A	Ext. Bus Control Signal
32	CS0X	I/O	P94	A	Chip select 0
33	CS1X	I/O	P95	A	Chip select 1
34	CS2X	I/O	P96	A	Chip select 2
35	CS3X	I/O	P97	A	Chip select 3
36	DREQ0	I/O	PB0	A	DMA Request 0
37	DACK0	I/O	PB1	A	DMA Acknowledge 0
38	DEOP0	I/O	PB2	A	DMA EOP 0
39	V <sub>SS</sub>	–	–	–	–
40	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
41	AVRH	–	–	R	Analog Reference High
42	AV <sub>CC</sub>	–	–	–	Analog V <sub>CC</sub>
43	AV <sub>SS</sub>	–	–	–	Analog V <sub>SS</sub> , Analog Reference Low
44	AN0	I/O	PH0	B	ADC Input 0
45	AN1	I/O	PH1	B	ADC Input 1
46	AN2	I/O	PH2	B	ADC Input 2
47	AN3	I/O	PH3	B	ADC Input 3
48	AN4	I/O	PH4	B	ADC Input 4
49	AN5	I/O	PH5	B	ADC Input 5
50	AN6	I/O	PH6	B	ADC Input 6
51	AN7	I/O	PH7	B	ADC Input 7
52	AN8	I/O	PG0	B	ADC Input 8
53	AN9	I/O	PG1	B	ADC Input 9
54	ALARM	I	–	D	Alarm Comparator Input
55	V <sub>SS</sub>	–	–	–	–
56	V <sub>DD</sub>	–	–	–	–
57	ATGX	I/O	P13	A	ADC Trigger Input
58	MD0	I	–	T	Mode Pin 0
59	MD1	I	–	T	Mode Pin 1
60	MD2	I	–	T	Mode Pin 2
61	HSTX	I	–	E	Hardware Standby
62	INITX	I	–	U	Initial Pin
63	TESTX	I	–	E	Test Input (should be connected to V <sub>DD</sub> )

**Table 3-4. CY91F369GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
64	CPUTESTX	I	–	E	Test Input (should be connected to V <sub>DD</sub> )
65	LTESTX	I	–	E	Test Input (should be connected to V <sub>DD</sub> )
66	V <sub>DD</sub>	–	–	–	–
67	V <sub>SS</sub>	–	–	–	–
68	INT0	I/O	PK0	A	Ext. Interrupt 0
69	INT1	I/O	PK1	A	Ext. Interrupt 1
70	INT2	I/O	PK2	A	Ext. Interrupt 2
71	INT3	I/O	PK3	A	Ext. Interrupt 3
72	INT4	I/O	PK4	A	Ext. Interrupt 4
73	INT5	I/O	PK5	A	Ext. Interrupt 5
74	INT6	I/O	PK6	A	Ext. Interrupt 6
75	INT7	I/O	PK7	A	Ext. Interrupt 7
76	SGO	I/O	PM0	A	Sound Generator SGO
77	SGA	I/O	PM1	A	Sound Generator SGA
78	SDA	I/O	PM2	Y	I <sup>2</sup> C SDA
79	SCL	I/O	PM3	Y	I <sup>2</sup> C SCL
80	SOT4	I/O	PN0	A	SIO Output
81	SIN4	I/O	PN1	A	SIO Input
82	SCK4	I/O	PN2	A	SIO Clock
83	SIN3	I/O	PN3	A	SIO Input
84	SOT3	I/O	PN4	A	SIO Output
85	SCK3	I/O	PN5	A	SIO Clock
86	V <sub>SS</sub>	–	–	–	–
87	V <sub>DDI</sub>	–	–	–	Supply Voltage for Internal Regulator
88	V <sub>DDI</sub>	–	–	–	Supply Voltage for Internal Regulator
89	V <sub>DDI</sub>	–	–	–	Supply Voltage for Internal Regulator
90	V <sub>DDI</sub>	–	–	–	Supply Voltage for Internal Regulator
91	V <sub>CC3C</sub>	–	–	–	Capacitor Pin for Internal Regulator
92	V <sub>SS</sub>	–	–	–	–
93	TX0	I/O	PP0	Q	CAN 0 TX
94	RX0	I/O	PP1	Q	CAN 0 RX
95	TX1	I/O	PP2	Q	CAN 1 TX
96	RX1	I/O	PP3	Q	CAN 1 RX
97	SIN0	I/O	PQ0	A	UART 0 Input
98	SOT0	I/O	PQ1	A	UART 0 Output
99	V <sub>DD</sub>	–	–	–	–
100	V <sub>SS</sub>	–	–	–	–
101	OCPA0	I/O	PO0	A	PPG Output

**Table 3-4. CY91F369GA I/O Pins and their Functions** *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
102	OCPA1	I/O	PO1	A	PPG Output
103	OCPA2	I/O	PO2	A	PPG Output
104	OCPA3	I/O	PO3	A	PPG Output
105	V <sub>DD</sub>	–	–	–	–
106	X0	I	–	H	4 MHz Oscillator Pin
107	X1	O	–	H	4 MHz Oscillator Pin
108	V <sub>SS</sub>	–	–	–	–
109	V <sub>DD</sub>	–	–	–	–
110	MONCLK	O	–	Q1	System Clock Output
111	V <sub>SS</sub>	–	–	–	–
112	V <sub>DD</sub> 35	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
113	V <sub>SS</sub>	–	–	–	–
114	WR3X	I/O	–	S	Ext. Bus Control
115	WR2X	I/O	–	S	Ext. Bus Control
116	WR1X	I/O	–	S	Ext. Bus Control
117	WROX	I/O	–	S	Ext. Bus Control
118	RDY	I/O	–	S	Ext. Bus Control
119	V <sub>DD</sub> 35	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
120	V <sub>SS</sub>	–	–	–	–
121	D0	I/O	–	Q	Ext. Bus Data Bit 0
122	D1	I/O	–	Q	Ext. Bus Data Bit 1
123	D2	I/O	–	Q	Ext. Bus Data Bit 2
124	D3	I/O	–	Q	Ext. Bus Data Bit 3
125	D4	I/O	–	Q	Ext. Bus Data Bit 4
126	D5	I/O	–	Q	Ext. Bus Data Bit 5
127	D6	I/O	–	Q	Ext. Bus Data Bit 6
128	D7	I/O	–	Q	Ext. Bus Data Bit 7
129	D8	I/O	–	Q	Ext. Bus Data Bit 8
130	D9	I/O	–	Q	Ext. Bus Data Bit 9
131	D10	I/O	–	Q	Ext. Bus Data Bit 10
132	D11	I/O	–	Q	Ext. Bus Data Bit 11
133	D12	I/O	–	Q	Ext. Bus Data Bit 12
134	D13	I/O	–	Q	Ext. Bus Data Bit 13
135	D14	I/O	–	Q	Ext. Bus Data Bit 14
136	D15	I/O	–	Q	Ext. Bus Data Bit 15
137	V <sub>DD</sub> 35	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
138	V <sub>SS</sub>	–	–	–	–
139	D16	I/O	–	Q	Ext. Bus Data Bit 16
140	D17	I/O	–	Q	Ext. Bus Data Bit 17

**Table 3-4. CY91F369GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
141	D18	I/O	–	Q	Ext. Bus Data Bit 18
142	D19	I/O	–	Q	Ext. Bus Data Bit 19
143	D20	I/O	–	Q	Ext. Bus Data Bit 20
144	D21	I/O	–	Q	Ext. Bus Data Bit 21
145	D22	I/O	–	Q	Ext. Bus Data Bit 22
146	D23	I/O	–	Q	Ext. Bus Data Bit 23
147	D24	I/O	–	Q	Ext. Bus Data Bit 24
148	D25	I/O	–	Q	Ext. Bus Data Bit 25
149	D26	I/O	–	Q	Ext. Bus Data Bit 26
150	D27	I/O	–	Q	Ext. Bus Data Bit 27
151	D28	I/O	–	Q	Ext. Bus Data Bit 28
152	D29	I/O	–	Q	Ext. Bus Data Bit 29
153	D30	I/O	–	Q	Ext. Bus Data Bit 30
154	D31	I/O	–	Q	Ext. Bus Data Bit 31
155	V <sub>DD35</sub>	–	–	–	Separated Ext. Bus V <sub>DD</sub> , 3.3 or 5.0 V
156	V <sub>SS</sub>	–	–	–	–
157	A0	I/O	–	Q	Ext. Bus Address Bit 0
158	A1	I/O	–	Q	Ext. Bus Address Bit 1
159	A2	I/O	–	Q	Ext. Bus Address Bit 2
160	A3	I/O	–	Q	Ext. Bus Address Bit 3

Note: If pins V<sub>DD35</sub> (9, 21, 40, 112, 119, 137, 155) are connected to a 3.3 V supply the external bus interface (pins 1-40, 112-160) can be operated at 3.3 V levels.

**Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions**

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
1	V <sub>DD</sub>	–	–	–	–	–
2	V <sub>SS</sub>	–	–	–	–	–
3	PJ4	I/O	PJ4	A	A	Digital I/O-Port
4	PJ5	I/O	PJ5	A	A	Digital I/O-Port
5	PJ6	I/O	PJ6	A	A	Digital I/O-Port
6	PJ7	I/O	PJ7	A	A	Digital I/O-Port
7	PI3	I/O	PI3	A	A	Digital I/O-Port
8	V <sub>DD</sub>	–	–	–	–	–
9	V <sub>SS</sub>	–	–	–	–	–
10	SGO	I/O	PM0	A	A	Sound Gen. SGO
11	SGA	I/O	PM1	A	A	Sound Gen. SGA
12	SDA	I/O	PM2	Y	Y	I <sup>2</sup> C SDA (no internal pull-up)
13	SCL	I/O	PM3	Y	Y	I <sup>2</sup> C SCL (no internal pull-up)

**Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
14	V <sub>DD</sub>	–	–	–	–	–
15	V <sub>SS</sub>	–	–	–	–	–
16	AVRH	–	–	R	R	Analog Ref. High
17	AV <sub>CC</sub>	–	–	–	–	Analog V <sub>CC</sub>
18	AV <sub>SS</sub>	–	–	–	–	Analog Ref. Low/Analog V <sub>SS</sub>
19	AN0	I/O	PH0	B	B	ADC Input
20	AN1	I/O	PH1	B	B	ADC Input
21	AN2	I/O	PH2	B	B	ADC Input
22	AN3	I/O	PH3	B	B	ADC Input
23	AN4	I/O	PH4	B	B	ADC Input
24	AN5	I/O	PH5	B	B	ADC Input
25	AN6	I/O	PH6	B	B	ADC Input
26	AN7	I/O	PH7	B	B	ADC Input
27	DA0	O	–	C	C	DAC Output (CY91F365GB)
	X0A	I	–	I	I	32 kHz Osc. Pin (CY91F366GB/366GA/ CY91F376G)
28	DA1	O	–	C	C	DAC Output (CY91F365GB)
	X1A	O	–	I	I	32 kHz Osc. Pin (CY91F366GB/366GA/ CY91F376G)
29	ALARM	I	–	D	D	Alarm Comparator Input
30	V <sub>SS</sub>	–	–	–	–	–
31	BOOT	I/O	P93	A	A	BOOT Pin (see note)
32	TESTX	I	–	E	E	Test Mode Pin
33	CPUTESTX	I	–	E	E	Test Mode Pin
34	V <sub>DD</sub>	–	–	–	–	–
35	X0	I	–	H	H	4 MHz Oscillator Pin
36	X1	O	–	H	H	4 MHz Oscillator Pin
37	V <sub>SS</sub>	–	–	–	–	–
38	MONCLK	O	–	G	G	Clock Output
39	INT0	I/O	PK0	A	A	Ext. Interrupt
40	INT1	I/O	PK1	A	A	Ext. Interrupt
41	INT2	I/O	PK2	A	A	Ext. Interrupt
42	INT3	I/O	PK3	A	A	Ext. Interrupt
43	INT4	I/O	PK4	A	A	Ext. Interrupt
44	INT5	I/O	PK5	A	A	Ext. Interrupt
45	INT6	I/O	PK6	A	A	Ext. Interrupt
46	INT7	I/O	PK7	A	A	Ext. Interrupt
47	V <sub>DD</sub>	–	–	–	–	Internal Power Supply Voltage pin
48	V <sub>CC3C</sub>	–	–	–	–	Capacitor Pin for Internal Power Supply.

**Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions (continued)**

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
49	V <sub>SS</sub>	–	–	–	–	–
50	IN0	I/O	PL0	A	A	ICU Input
51	IN1	I/O	PL1	A	A	ICU Input
52	IN2	I/O	PL2	A	A	ICU Input
53	IN3	I/O	PL3	A	A	ICU Input
54	OUT0	I/O	PL4	A	A	OCU Output
55	OUT1	I/O	PL5	A	A	OCU Output
56	V <sub>DD</sub>	–	–	–	–	Internal Power Supply Voltage pin
57	MD0	I	–	T	F	Mode Pin
58	MD1	I	–	T	F	Mode Pin
59	MD2	I	–	T	F	Mode Pin
60	INITX	I	–	U	U	Initial Pin
61	V <sub>DD</sub>	–	–	–	–	Internal Power Supply Voltage pin
62	V <sub>SS</sub>	–	–	–	–	–
63	SOT4	I/O	PN0	A	A	SIO Output
64	SIN4	I/O	PN1	A	A	SIO Input
65	SCK4	I/O	PN2	A	A	SIO Clock
66	SIN3	I/O	PN3	A	A	SIO Input
67	SOT3	I/O	PN4	A	A	SIO Output
68	SCK3	I/O	PN5	A	A	SIO Clock
69	V <sub>SS</sub>	–	–	–	–	–
70	OCPA0	I/O	PO0	A	A	PPG Output
71	OCPA1	I/O	PO1	A	A	PPG Output
72	OCPA2	I/O	PO2	A	A	PPG Output
73	OCPA3	I/O	PO3	A	A	PPG Output
74	OCPA4	I/O	PO4	A	A	PPG Output
75	OCPA5	I/O	PO5	A	A	PPG Output
76	OCPA6	I/O	PO6	A	A	PPG Output
77	OCPA7	I/O	PO7	A	A	PPG Output
78	TX0	I/O	PP0	Q	Q	CAN TX Output
79	RX0	I/O	PP1	Q	Q	CAN RX Output
80	TX1	I/O	PP2	Q	Q	CAN TX Output
81	RX1	I/O	PP3	Q	Q	CAN RX Output
82	V <sub>DD</sub>	–	–	–	–	–
83	V <sub>SS</sub>	–	–	–	–	–
84	SIN0	I/O	PQ0	A	A	UART Input
85	SOT0	I/O	PQ1	A	A	UART Output
86	SIN1	I/O	PQ2	A	A	UART Input

**Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions (continued)**

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
87	SOT1	I/O	PQ3	A	A	UART Output
88	PG0	I/O	PG0	A	A	Digital I/O-Port
89	PG1	I/O	PG1	A	A	Digital I/O-Port
90	PG2	I/O	PG2	A	A	Digital I/O-Port
91	PG3	I/O	PG3	A	A	Digital I/O-Port
92	PG4	I/O	PG4	A	A	Digital I/O-Port
93	PG5	I/O	PG5	A	A	Digital I/O-Port
94	V <sub>DD</sub>	–	–	–	–	–
95	HV <sub>SS</sub>	–	–	–	–	SMC V <sub>SS</sub>
96	PWM1P0	I/O	PR0	K	K	SMC 0
97	PWM1M0	I/O	PR1	K	K	SMC 0
98	PWM2P0	I/O	PR2	K	K	SMC 0
99	PWM2M0	I/O	PR3	M	M	SMC 0
100	HV <sub>DD</sub>	–	–	–	–	SMC V <sub>DD</sub>
101	PWM1P1	I/O	PR4	K	K	SMC 1
102	PWM1M1	I/O	PR5	K	K	SMC 1
103	PWM2P1	I/O	PR6	K	K	SMC 1
104	PWM2M1	I/O	PR7	M	M	SMC 1
105	HV <sub>SS</sub>	–	–	–	–	SMC V <sub>SS</sub>
106	PWM1P2	I/O	PS0	K	K	SMC 2
107	PWM1M2	I/O	PS1	K	K	SMC 2
108	PWM2P2	I/O	PS2	K	K	SMC 2
109	PWM2M2	I/O	PS3	M	M	SMC 2
110	HV <sub>DD</sub>	–	–	–	–	SMC V <sub>DD</sub>
111	PWM1P3	I/O	PS4	K	K	SMC 3
112	PWM1M3	I/O	PS5	K	K	SMC 3
113	PWM2P3	I/O	PS6	K	K	SMC 3
114	PWM2M3	I/O	PS7	M	M	SMC 3
115	HV <sub>SS</sub>	–	–	–	–	–
116	V <sub>DD</sub>	–	–	–	–	–
117	PJ0	I/O	PJ0	A	A	Digital I/O-Port
118	PJ1	I/O	PJ1	A	A	Digital I/O-Port
119	PJ2	I/O	PJ2	A	A	Digital I/O-Port
120	PJ3	I/O	PJ3	A	A	Digital I/O-Port

Note: Pin 31 (BOOT) should be low by default (pull down resistor). To avoid disturbances in case of reset/boot, it should preferably only be used as output by any application.



**Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions**

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	V <sub>DD</sub>	–	–	–	–
2	V <sub>SS</sub>	–	–	–	–
3	PJ4	I/O	PJ4	A	Digital I/O-Port
4	PJ5	I/O	PJ5	A	Digital I/O-Port
5	PJ6	I/O	PJ6	A	Digital I/O-Port
6	PJ7	I/O	PJ7	A	Digital I/O-Port
7	PI3	I/O	PI3	A	Digital I/O-Port
8	V <sub>DD</sub>	–	–	–	–
9	V <sub>SS</sub>	–	–	–	–
10	PM0	I/O	PM0	A	Digital I/O-Port
11	PM1	I/O	PM1	A	Digital I/O-Port
12	SDA	I/O	PM2	Y	I <sup>2</sup> C SDA (no internal pull-up)
13	SCL	I/O	PM3	Y	I <sup>2</sup> C SCL (no internal pull-up)
14	V <sub>DD</sub>	–	–	–	–
15	V <sub>SS</sub>	–	–	–	–
16	AVRH	–	–	R	Analog Ref. High
17	AV <sub>CC</sub>	–	–	–	Analog V <sub>CC</sub>
18	AV <sub>SS</sub>	–	–	–	Analog Ref. Low/Analog V <sub>SS</sub>
19	AN0	I/O	PH0	B	ADC Input
20	AN1	I/O	PH1	B	ADC Input
21	AN2	I/O	PH2	B	ADC Input
22	AN3	I/O	PH3	B	ADC Input
23	AN4	I/O	PH4	B	ADC Input
24	AN5	I/O	PH5	B	ADC Input
25	AN6	I/O	PH6	B	ADC Input
26	AN7	I/O	PH7	B	ADC Input
27	X0A	I	–	I	32 kHz Oscillator Pin (CY91F368GB)
	N.C.	–	–	–	Not Connected (CY91F367GB)
28	X1A	O	–	I	32 kHz Oscillator Pin (CY91F368GB)
	N.C.	–	–	–	Not Connected (CY91F367GB)
29	ALARM	I	–	D	Alarm Comparator Input
30	V <sub>SS</sub>	–	–	–	–
31	BOOT	I/O	P93	A	BOOT Pin <sup>a</sup>
32	TESTX	I	–	E	Test mode pin
33	CPUTESTX	I	–	E	Test mode pin
34	V <sub>DD</sub>	–	–	–	–
35	X0	I	–	H	4 MHz Oscillator Pin

**Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
36	X1	O	–	H	4 MHz Oscillator Pin
37	V <sub>SS</sub>	–	–	–	–
38	MONCLK	O	–	G	Clock output
39	INT0	I/O	PK0	A	Ext. Interrupt
40	INT1	I/O	PK1	A	Ext. Interrupt
41	INT2	I/O	PK2	A	Ext. Interrupt
42	INT3	I/O	PK3	A	Ext. Interrupt
43	INT4	I/O	PK4	A	Ext. Interrupt
44	INT5	I/O	PK5	A	Ext. Interrupt
45	INT6	I/O	PK6	A	Ext. Interrupt
46	INT7	I/O	PK7	A	Ext. Interrupt
47	V <sub>DD</sub>	–	–	–	Internal Power Supply Voltage pin
48	V <sub>CC3C</sub>	–	–	–	Capacitor Pin for Internal Power Supply
49	V <sub>SS</sub>	–	–	–	–
50	IN0	I/O	PL0	A	ICU Input
51	IN1	I/O	PL1	A	ICU Input
52	IN2	I/O	PL2	A	ICU Input
53	IN3	I/O	PL3	A	ICU Input
54	OUT0	I/O	PL4	A	OCU Output
55	OUT1	I/O	PL5	A	OCU Output
56	V <sub>DD</sub>	–	–	–	Internal Power Supply Voltage pin
57	MD0	I	–	T	Mode Pin
58	MD1	I	–	T	Mode Pin
59	MD2	I	–	T	Mode Pin
60	INITX	I	–	U	Initial Pin
61	V <sub>DD</sub>	–	–	–	Internal Power Supply Voltage pin
62	V <sub>SS</sub>	–	–	–	–
63	SOT4	I/O	PN0	A	SIO Output
64	SIN4	I/O	PN1	A	SIO Input
65	SCK4	I/O	PN2	A	SIO Clock
66	SIN3	I/O	PN3	A	SIO Input
67	SOT3	I/O	PN4	A	SIO Output
68	SCK3	I/O	PN5	A	SIO Clock
69	V <sub>SS</sub>	–	–	–	–
70	OCPA0	I/O	PO0	A	PPG Output
71	OCPA1	I/O	PO1	A	PPG Output
72	OCPA2	I/O	PO2	A	PPG Output
73	OCPA3	I/O	PO3	A	PPG Output

**Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions** (continued)

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
74	PO4	I/O	PO4	A	Digital I/O-Port
75	PO5	I/O	PO5	A	Digital I/O-Port
76	PO6	I/O	PO6	A	Digital I/O-Port
77	PO7	I/O	PO7	A	Digital I/O-Port
78	TX0	I/O	PP0	Q	CAN TX Output
79	RX0	I/O	PP1	Q	CAN RX Output
80	TX1	I/O	PP2	Q	CAN TX Output
81	RX1	I/O	PP3	Q	CAN RX Output
82	V <sub>DD</sub>	–	–	–	–
83	V <sub>SS</sub>	–	–	–	–
84	SIN0	I/O	PQ0	A	UART Input
85	SOT0	I/O	PQ1	A	UART Output
86	PQ2	I/O	PQ2	A	Digital I/O-Port
87	PQ3	I/O	PQ3	A	Digital I/O-Port
88	PG0	I/O	PG0	A	Digital I/O-Port
89	PG1	I/O	PG1	A	Digital I/O-Port
90	PG2	I/O	PG2	A	Digital I/O-Port
91	PG3	I/O	PG3	A	Digital I/O-Port
92	PG4	I/O	PG4	A	Digital I/O-Port
93	PG5	I/O	PG5	A	Digital I/O-Port
94	V <sub>DD</sub>	–	–	–	–
95	V <sub>SS</sub>	–	–	–	–
96	PR0	I/O	PR0	K	Digital I/O-Port
97	PR1	I/O	PR1	K	Digital I/O-Port
98	PR2	I/O	PR2	K	Digital I/O-Port
99	PR3	I/O	PR3	M	Digital I/O-Port
100	HV <sub>DD</sub>	–	–	–	V <sub>DD</sub> for Ports R and S
101	PR4	I/O	PR4	K	Digital I/O-Port
102	PR5	I/O	PR5	K	Digital I/O-Port
103	PR6	I/O	PR6	K	Digital I/O-Port
104	PR7	I/O	PR7	M	Digital I/O-Port
105	V <sub>SS</sub>	–	–	–	–
106	PS0	I/O	PS0	K	Digital I/O-Port
107	PS1	I/O	PS1	K	Digital I/O-Port
108	PS2	I/O	PS2	K	Digital I/O-Port
109	PS3	I/O	PS3	M	Digital I/O-Port
110	HV <sub>DD</sub>	–	–	–	V <sub>DD</sub> for Ports R and S
111	PS4	I/O	PS4	K	Digital I/O-Port

**Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions** *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
112	PS5	I/O	PS5	K	Digital I/O-Port
113	PS6	I/O	PS6	K	Digital I/O-Port
114	PS7	I/O	PS7	M	Digital I/O-Port
115	V <sub>SS</sub>	–	–	–	–
116	V <sub>DD</sub>	–	–	–	–
117	PJ0	I/O	PJ0	A	Digital I/O-Port
118	PJ1	I/O	PJ1	A	Digital I/O-Port
119	PJ2	I/O	PJ2	A	Digital I/O-Port
120	PJ3	I/O	PJ3	A	Digital I/O-Port

- a. Pin 31 (BOOT) should be low by default (pull down resistor). To avoid disturbances in case of reset/boot, it should preferably only be used as output by any application.



#### 4. I/O Circuit Type

Type	Circuit Type	Remarks
A		<ul style="list-style-type: none"> <li>■ CMOS Automotive level Schmitt-Trigger Input</li> <li>■ STOP control</li> <li>■ <math>I_{OH} = 4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
B		<ul style="list-style-type: none"> <li>■ CMOS Automotive level Schmitt-Trigger Input</li> <li>■ Analog Input</li> <li>■ STOP control</li> <li>■ <math>I_{OH} = 4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
C		<ul style="list-style-type: none"> <li>■ Analog output</li> </ul>
D		<ul style="list-style-type: none"> <li>■ Analog Input</li> </ul>



Type	Circuit Type	Remarks
E		<ul style="list-style-type: none"> <li>■ CMOS Schmitt-Trigger Input</li> <li>■ Pullup Resistor: 50 kΩ</li> </ul>
F		<ul style="list-style-type: none"> <li>■ CMOS Schmitt-Trigger Input</li> </ul>
G		<ul style="list-style-type: none"> <li>■ Tristate Output</li> <li>■ <math>I_{OH} = 4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
H		<ul style="list-style-type: none"> <li>■ 4 MHz Oscillator Pin</li> </ul>



Type	Circuit Type	Remarks
I		<ul style="list-style-type: none"> <li>■ 32 kHz Oscillator Pin</li> </ul>
J		<ul style="list-style-type: none"> <li>■ CMOS Automotive level Schmitt-Trigger Input</li> <li>■ STOP control (LED)</li> <li>■ <math>I_{OH} = 14 \text{ mA}</math>, <math>I_{OL} = 24 \text{ mA}</math></li> </ul>
K		<ul style="list-style-type: none"> <li>■ CMOS Automotive level Schmitt-Trigger Input</li> <li>■ STOP control (SMC)</li> <li>■ <math>I_{OH} = 30 \text{ mA}</math>, <math>I_{OL} = 30 \text{ mA}</math></li> <li>■ Typ slew rate of 40 ns</li> </ul>
L		<ul style="list-style-type: none"> <li>■ CMOS Input</li> <li>■ 5 V or 3 V input</li> <li>■ <math>I_{OH} = 4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>



Type	Circuit Type	Remarks
M		<ul style="list-style-type: none"> <li>■ CMOS Automotive level Schmitt-Trigger Input</li> <li>■ Analog Input</li> <li>■ STOP control (SMC)</li> <li>■ <math>I_{OH} = 30\text{ mA}</math>, <math>I_{OL} = 30\text{ mA}</math></li> <li>■ Typ slew rate of 40 ns</li> </ul>
N		<ul style="list-style-type: none"> <li>■ CMOS Input</li> <li>■ Pulldown Resistor: 50 k<math>\Omega</math></li> <li>■ 5 V or 3 V input</li> <li>■ <math>I_{OH} = 4\text{ mA}</math>, <math>I_{OL} = 4\text{ mA}</math></li> </ul>
O		<ul style="list-style-type: none"> <li>■ CMOS Input</li> <li>■ Pulldown Resistor: 50 k<math>\Omega</math></li> <li>■ 5 V or 3 V input</li> </ul>
P		<ul style="list-style-type: none"> <li>■ CMOS Input</li> <li>■ 3 V input</li> </ul>





Type	Circuit Type	Remarks
Q/Q1		<ul style="list-style-type: none"> <li>■ Q: CMOS Input, STOP control, <math>I_{OH} = 4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>■ Q1: CMOS Input, STOP control, <math>I_{OH} = 8 \text{ mA}</math>, <math>I_{OL} = 8 \text{ mA}</math></li> </ul>
S		<ul style="list-style-type: none"> <li>■ CMOS Schmitt-Trigger Input</li> <li>■ STOP control</li> <li>■ Pullup Resistor: 10 kΩ</li> <li>■ <math>I_{OH} = 4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
T		<ul style="list-style-type: none"> <li>■ CMOS Input</li> <li>■ Can withstand high <math>V_{ID}</math> for flash programming</li> </ul>
U		<ul style="list-style-type: none"> <li>■ CMOS Schmitt-Trigger Input</li> <li>■ Pullup Resistor to the core: 50 kΩ</li> <li>■ 3 V and 5 V input</li> </ul>



Type	Circuit Type	Remarks
V		<ul style="list-style-type: none"> <li>■ CMOS Schmitt-Trigger Input</li> <li>■ STOP control</li> <li>■ Pullup Resistor: 50 kΩ</li> <li>■ I<sub>OH</sub> = 4 mA, I<sub>OL</sub> = 4 mA</li> </ul>
W		<ul style="list-style-type: none"> <li>■ CMOS Input</li> <li>■ 3 V input</li> </ul>
X		<ul style="list-style-type: none"> <li>■ Tristate Output, 3 V</li> </ul>
Y		<ul style="list-style-type: none"> <li>■ CMOS Input in I<sup>2</sup>C mode operating as open drain outputs</li> <li>■ STOP control</li> <li>■ I<sub>OH</sub> = 3 mA, I<sub>OL</sub> = 3 mA</li> </ul>



Type	Circuit Type	Remarks
YA		<ul style="list-style-type: none"> <li>■ I/O in I<sup>2</sup>C mode operating as open drain outputs</li> <li>■ CMOS Schmitt-Trigger Input</li> <li>■ STOP control</li> <li>■ I<sub>OH</sub> = 3 mA, I<sub>OL</sub> = 3 mA</li> </ul>

Note: Symbols used in circuit types (Common to all circuit diagrams)

- P: P channel transistor
- N: N channel transistor
- R: Diffusion resistor

Circuit Type	Description
A	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Automotive Schmitt-Trigger Input, STOP control
B	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control
C	Analog Output
D	Analog Input
E	CMOS Schmitt-Trigger Input, Pull-up Resistor: $50 \text{ k}\Omega$ ,
F	CMOS Schmitt-Trigger Input
G	Tristate Output, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$
H	4 MHz Oscillator Pin
I	32 kHz Oscillator pin
J	I/O, $I_{OH} = 14 \text{ mA}$ / $I_{OL} = 24 \text{ mA}$ , CMOS Automotive Schmitt-Trigger Input, STOP control (LED)
K	I/O, $I_{OH} = 30 \text{ mA}$ / $I_{OL} = 30 \text{ mA}$ , CMOS Automotive Schmitt-Trigger Input, STOP control, slew rate improved for EMC (SMC)
L	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Input: 5 V or 3 V input
M	I/O, $I_{OH} = 30 \text{ mA}$ / $I_{OL} = 30 \text{ mA}$ , CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control, slew rate improved for EMC (SMC)
N	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Input: 5 V or 3 V input, Pulldown Resistor: $50 \text{ k}\Omega$
O	CMOS Input: 5 V or 3 V input, Pulldown Resistor: $50 \text{ k}\Omega$
P	CMOS Input: 3 V input
Q	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Input, STOP control
Q1	I/O, $I_{OH} = 8 \text{ mA}$ / $I_{OL} = 8 \text{ mA}$ , CMOS Input, STOP control
R	AVRL / AVRH Input
S	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Input, STOP control, Pull-up Resistor: $10 \text{ k}\Omega$ ,
T	CMOS Input, can withstand $V_{ID}$ for flash programming
U	CMOS Schmitt-Trigger Input, Pull-up Resistor: $50 \text{ k}\Omega$ , 3.3 V and 5 V inputs to core
W	I/O, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , CMOS Input: 3 V input
X	Tristate Output, $I_{OH} = 4 \text{ mA}$ / $I_{OL} = 4 \text{ mA}$ , 3 V
Y	I/O, $I_{OH} = 3 \text{ mA}$ / $I_{OL} = 3 \text{ mA}$ (I <sup>2</sup> C), CMOS Input, STOP control
YA	I/O, $I_{OH} = 3 \text{ mA}$ / $I_{OL} = 3 \text{ mA}$ (I <sup>2</sup> C), CMOS Schmitt-Trigger Input, STOP control

## 5. Handling Devices

### 5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than  $V_{DD}$  or less than  $V_{SS}$  is applied to an input or output pin or if the voltage applied between  $V_{DD}$  and  $V_{SS}$  exceeds the rating. If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.

### 5.2 Connecting Unused Pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be tied to  $V_{DD}$  or  $V_{SS}$  through resistors. In this case those resistors should be more than 2 k $\Omega$ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

The resistor of more than 2 k $\Omega$  is used to limit currents through the protection diodes. In case of voltages at the not used pin of 0.3 V or more below  $V_{SS}$  or 0.3 V or more above  $V_{DD}$  currents which could cause latch-up will flow through those diodes.

### 5.3 External Reset Input

When inputting an "L" level to the INITX pin, hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

### 5.4 Power Supply Pins

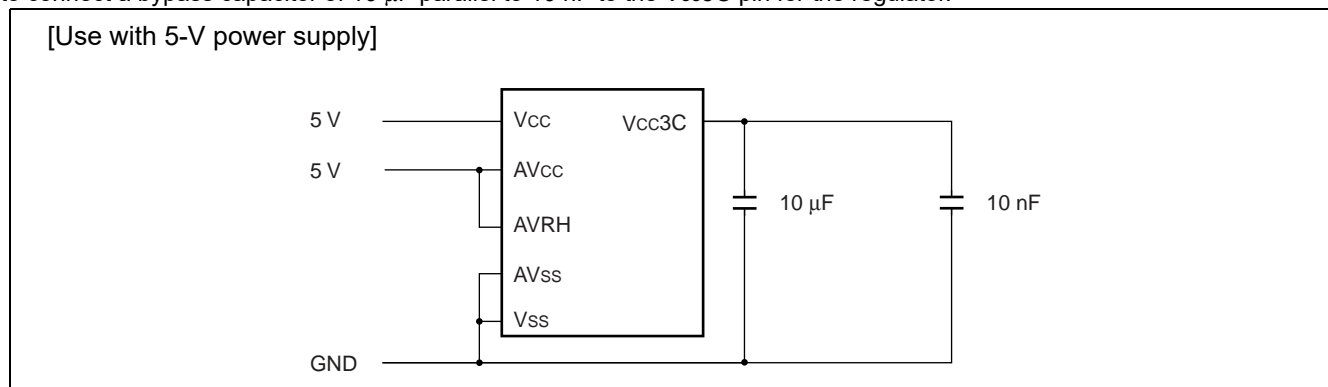
All  $V_{DD}$  pins should be connected to the same potential (exception can be the external bus interface on F362GB and F369GA). The analogue supply voltage ( $AV_{CC}$ ) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V this voltage also must not be turned on before the 5 V digital voltage has been switched on. If the supply voltage to the external bus interface is switched off (it may not be tristate but should be pulled low) it must be made sure that all related signals do not have a voltage higher than this pulled down supply.

When multiple  $V_{DD}$  and  $V_{SS}$  pins are provided, be sure to connect all  $V_{DD}$  and  $V_{SS}$  pins to the power supply or ground externally. Although pins at the same potential are connected together in the internal device design so as to prevent malfunctions such as latch-up, connecting all  $V_{DD}$  and  $V_{SS}$  pins appropriately minimizes unwanted radiation, prevents malfunction of strobe signals due to increases in the ground level, and keeps the overall output current rating.

Also, take care to connect  $V_{DD}$  and  $V_{SS}$  to current source in the lowest possible impedance.

Connection of a ceramic bypass capacitor of approximately 0.1  $\mu\text{F}$  between  $V_{DD}$  and  $V_{SS}$  close to the device is recommended.

The CY91360G series contains a regulator. To use the device with the 5-V power supply, supply 5-V power to the  $V_{CC}$  pins and be sure to connect a bypass capacitor of 10  $\mu\text{F}$  parallel to 10 nF to the  $V_{CC3C}$  pin for the regulator.



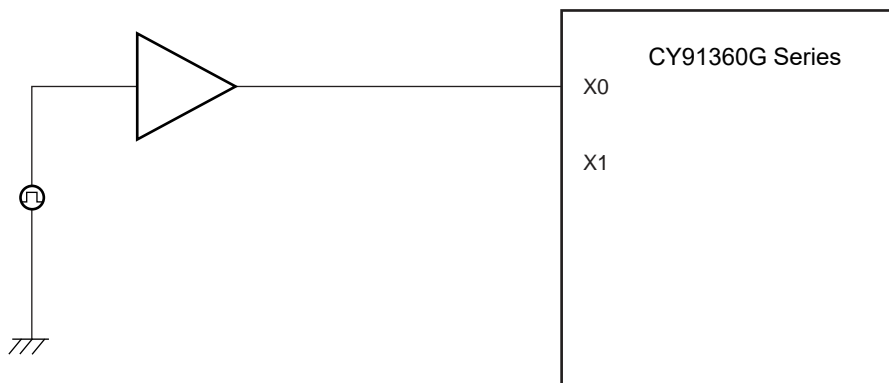
### 5.5 Crystal Oscillator Circuit

Noise in the vicinity of the X0 and X1 pins can be a cause of device malfunction. Design the circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

A printed circuit board design that surrounds the X0 and X1 pins with ground provides for stable operation and is strongly recommended.

## 5.6 Using an External Clock

To use an external clock, drive X0 pin only and leave X1 pin open. Below is a diagram of how to use external clock.



## 5.7 Mode Pins

Connect the mode pins (MD0 to MD2) directly to VDD or Vss.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to VDD or Vss and to provide a low-impedance connection.

## 5.8 Turning the Power Supply on

Immediately after power on always execute INIT at the INITX pin (start with a low level at the INITX pin). Hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

The analogue supply voltage (AV<sub>CC</sub>) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V this voltage also must not be turned on before the 5 V digital voltage has been switched on.

## 5.9 A State in Turning Power on

As long as the minimum operating voltage has not been reached during power-on the output pin levels are not guaranteed.

## 5.10 Note on During Operation of PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempts to be working with the self-frequency of the self-oscillating circuit within the PLL even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 5.11 The Function of the Watchdog Timer

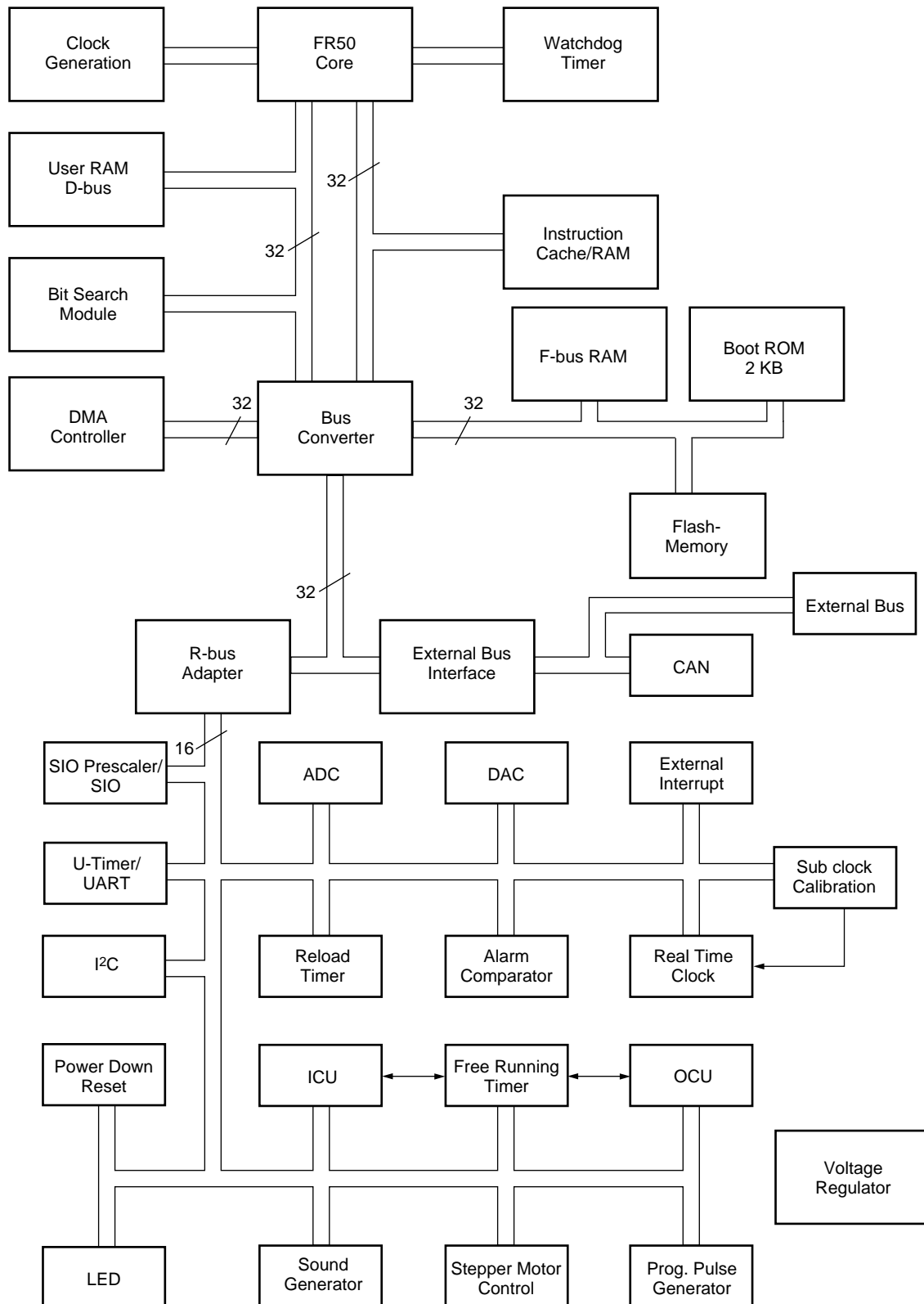
The watchdog timer in this model has the functions watching that the program performs the delay of reset within a fixed period and resetting the CPU when the delay of reset is not performed because of the program malfunction.

Therefore, once the function of the watchdog timer is enabled, the watchdog timer keeps on operating until the reset operation. As an exceptional processing, the watchdog timer performs the delay of reset automatically under the condition in which the CPU program operation is stopped. Please refer to the explanation item of the function of the watchdog timer about the exceptional condition.

By the way, if above condition will be issued by the system program or hardware malfunction, a watchdog reset may be not performed. In this case please perform the reset operation (INIT) by using the external INITX pin.

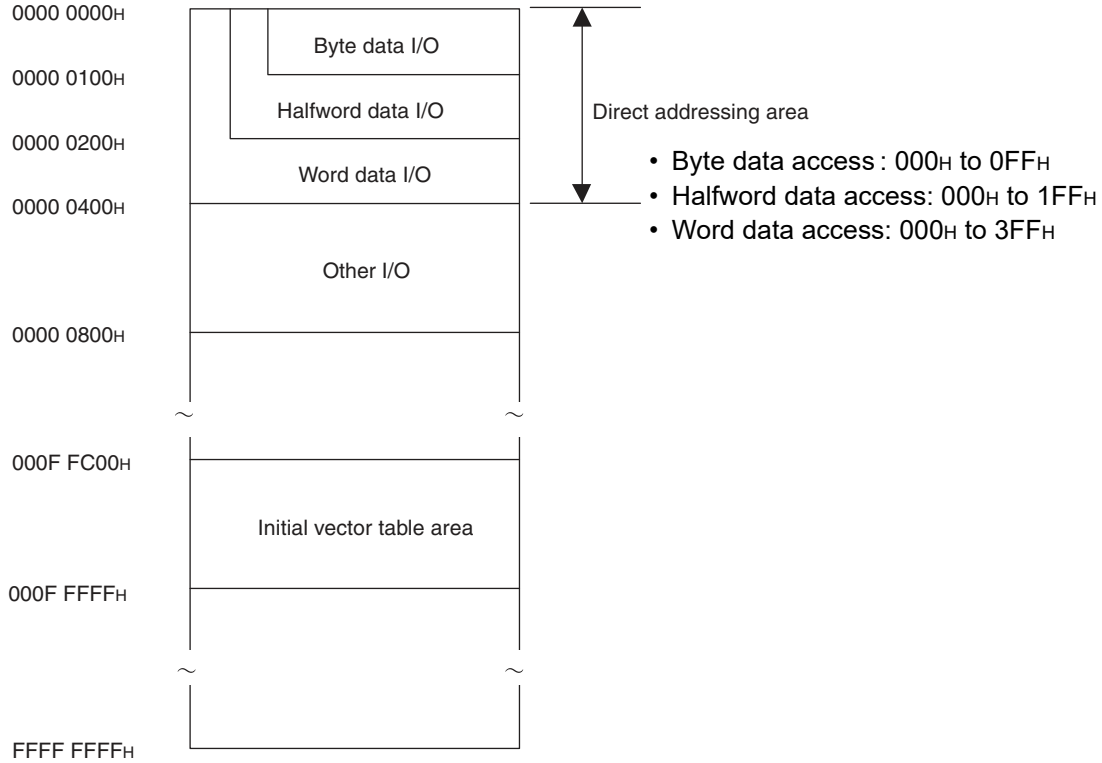


## 6. Block Diagram



## 7. CPU Core

### 7.1 Memory Space



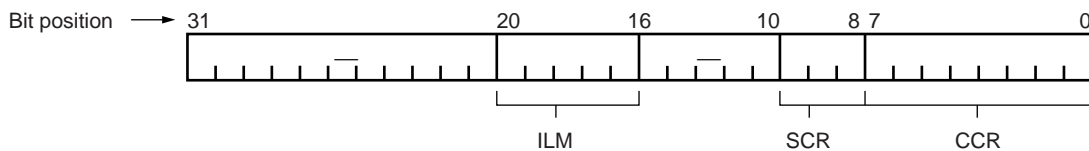


## 7.2 Dedicated Registers

Each of the dedicated registers is used for a particular purpose. The dedicated registers consist of the program counter (PC), program status (PS), table base register (TBR), return pointer (RP), system stack pointer (SSP), user stack pointer (USP), and multiplication and division result registers (MDH/MDL).

	← 32 bits →	Initial value
Program counter	PC	XXXX XXXXH (Indeterminate)
Program status	PS	
Table base register	TBR	000F FC00H
Return pointer	RP	XXXX XXXXH (Indeterminate)
System stack pointer	SSP	0000 0000H
User stack pointer	USP	XXXX XXXXH (Indeterminate)
Multiplication and division results registers	MDH	XXXX XXXXH (Indeterminate)
	MDL	XXXX XXXXH (Indeterminate)

### 7.2.1 Program Status (PS)

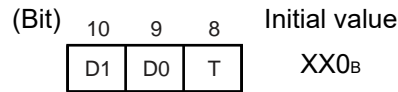


CCR: Condition Code Register  
SCR: System Condition Code Register  
ILM: Interrupt Level Mask

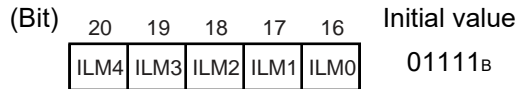
### 7.2.2 Condition Code Register (CCR)

(Bit)	7	6	5	4	3	2	1	0	Initial value
	—	—	S	I	N	Z	V	C	--00XXXX <sub>B</sub>

7.2.3 System Condition Code Register (SCR)



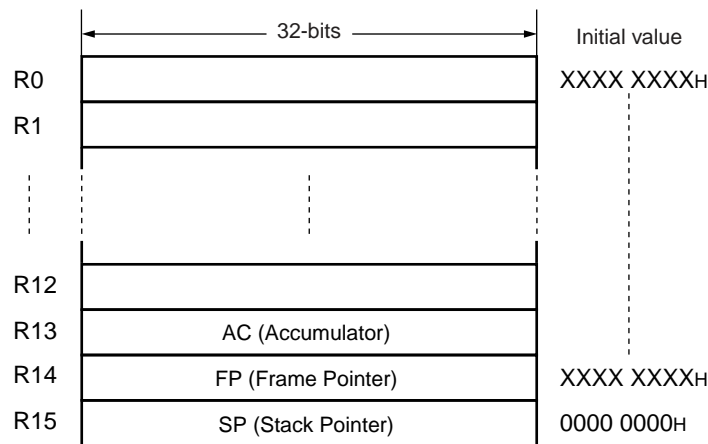
7.2.4 Interrupt Level Mask Register (ILM)



**7.3 General-Purpose Registers**

The general-purpose registers are CPU registers R0 to R15. The register are used as the accumulator for operations and as pointers (a field indicating an address) for memory access. The user can specify the purpose for which the general-purpose registers are used.

**Register Bank Structure**



Among 16 general-purpose registers, the following registers assume a special purpose. This enhances some instructions.

- R13 : Virtual accumulator (AC)
- R14 : Frame pointer (FP)
- R15 : Stack pointer (SP)

The initial value of R0 to R14 after a reset is indeterminate. The initial value of R15 is 00000000<sub>H</sub> (SSP value).

## 8. Mode Setting

The FR50 of devices uses mode pins (MD2 to MD0) and a mode register (MODR) to set the operation mode.

### 8.1 Mode Pins

Three mode pins (MD2 to MD0) are used to specify the reset mode vector access area.

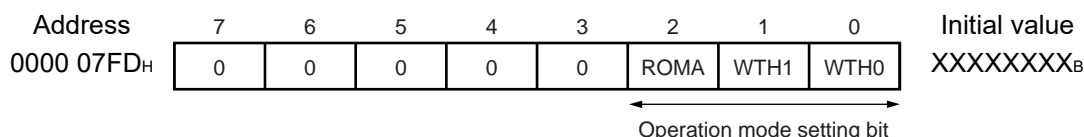
Mode Pins			Mode Name	Reset Vector Access Area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	The mode register is used to set the bus width.
remaining settings			-	-	Reserved

### 8.2 Mode Register (MODR)

The data to be written to 0000 07FD<sub>H</sub> using mode vector fetch is called mode data.

MODR is located at 0000 07FD<sub>H</sub>. After an operation mode has been set in MODR, the device operates in this operation mode. MODR is set only when a reset factor (INIT level) occurs. User programs cannot write data to MODR.

< Mode Register (MODR) >



[Bits 7 to 3]: (Reserved bits)

Always set 00000 at bits 7 to 3. Operation is not guaranteed when other values are set.

[Bit 2]: ROMA (internal ROM enable bit)

The ROMA bit is used to set whether to validate the internal ROM area (F-bus memory area).

ROMA	Function	Remarks
0	External ROM mode	Access to the F-bus area is external.
1	Internal ROM mode	

[Bits 1 and 0]: WTH1 and WTH0 (bus width/single chip mode specifying bits)

The WTH1 and WTH0 bits are used to set the bus width (valid when operation mode is external bus mode) and the single chip mode. When the operation mode is the external bus mode, this value is set at the BW1 and BW0 bits of AMD0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	32-bit bus width	External bus mode
1	1	Single chip mode	

### 8.3 Fixed Vector

If CY91360 series devices are started in mode MD[2:0] = 000, the internal fixed mode vector (FMV = 0x06) and the fixed reset vector are used. The fixed reset vector points to the start address of the internal Boot ROM.

This enables access to the F-bus area, to the internal CAN modules and the internal flash memory.

See also section Boot ROM.

## 9. I/O Map

### 9.1 How to Read the I/O Map

Address	Register				Internal peripheral circuit
	+0	+1	+2	+3	
000014 <sub>H</sub>	PDRG [R/W] ↑XXXXXXXX --	PDRH [R/W] XXXXXXXXXX	PDRI [R/W] ----XXXX	-	Port data register

Read/write attribute

Register initial value after a reset (bit initial values)  
 "1": initial value "1", "0": initial value "0",  
 "x": initial value "X" (Undefined)

"-" indicates non-existent bits

Register name (The register in column 1 is at address 4n, the register in column 2 at 4n + 1, and so on.)

Address of far left of register (+0), +1, +2, and +3 each increment the address by one. When performing word access, the register in column 1 is placed at the MSB end of the data.

Note: Do not use RMW instructions on registers containing write-only (W) bits.

RMW instructions (RMW: read-modify-write):

```

AND   Rj, @Ri  OR   Rj, @Ri  EOR   Rj, @Ri
ANDH  Rj, @Ri  ORH  Rj, @Ri  EORH  Rj, @Ri
ANDB  Rj, @Ri  ORB  Rj, @Ri  EORB  Rj, @Ri
BANDL #u4, @Ri BORL #u4, @Ri BEORL #u4, @Ri
BANDH #u4, @Ri BORH #u4, @Ri BEORH #u4, @Ri
  
```

The data in reserved areas and areas marked "-" is indeterminate.

Do not use those areas.

Address	Register				Block
	+0	+1	+2	+3	
000000 <sub>H</sub>	Reserved	Reserved	Reserved	Reserved	T-unit Port Data Register
000004 <sub>H</sub>	Reserved	Reserved	Reserved	PDR7 [R/W] 1111XXXX	
000008 <sub>H</sub>	PDR8 [R/W] XXXXXXXXXX	PDR9 [R/W] XXXXXXXXX1	-	PDRB [R/W] XXXXXXXXXX	
00000C <sub>H</sub>	-				
000010 <sub>H</sub>	PDRG [R/W] XXXXXXXXXX	PDRH [R/W] XXXXXXXXXX	PDRI [R/W] X --- X ---	PDRJ [R/W] XXXXXXXXXX	R-bus Port Data Register
000014 <sub>H</sub>	PDRK [R/W] XXXXXXXXXX	PDRL [R/W] XXXXXXXXXX	PDRM [R/W] ---- XXXX	PDRN [R/W] -- XXXXXX	
000018 <sub>H</sub>	PDRO [R/W] XXXXXXXXXX	PDRP [R/W] XXXXXXXXXX	PDRQ [R/W] -- XXXXXX	PDRR [R/W] XXXXXXXXXX	
00001C <sub>H</sub>	PDRS [R/W] XXXXXXXXXX	-	-	-	

Address	Register				Block
	+0	+1	+2	+3	
000020H to 00003CH	-				Reserved
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext int/NMI
000044H	DICR [R/W] ----- 0	HRCL [R/W, R] 0 -- 11111	CLKR2 [R/W] ----- 000	reserved	DLYI/I-unit RTC
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	-		TMCSR0 [R/W] ---- 0000 --- 00000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	-		TMCSR1 [R/W] ---- 0000 --- 00000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	-		TMCSR2 [R/W] ---- 0000 --- 00000		
000060H	SSR0 [R/W] 00001 - 00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W, W] 00000100	SMR0 [R/W, W] 00 -- 0 - 00	UART0
000064H	ULS0 [R/W] ---- 0000	-	-	-	
000068H	UTIM0/UTIMR0 [R/W] 00000000 00000000		DRCL0 [W] -----	UTIMC0 [R/W] 0 --- 0001	U-TIMER 0
00006CH	SSR1 [R/W, R] 00001 - 00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W, W] 00000100	SMR1 [R/W, W] 00 -- 0 - 00	UART1
000070H	ULS1 [R/W] ---- 0000	-	-	-	
000074H	UTIM1/UTIMR1 [R/W] 00000000 00000000		DRCL1 [W] -----	UTIMC1 [R/W] 0 --- 0001	U-TIMER 1
000078H	SSR2 [R/W, R] 00001 - 00	SIDR2 [R/W] XXXXXXXX	SCR2 [R/W, W] 00000100	SMR2 [R/W, W] 00 -- 0 - 00	UART2
00007CH	ULS2 [R/W] ---- 0000	-	-	-	
000080H	UTIM2/UTIMR2 [R/W] 00000000 00000000		DRCL2 [W] -----	UTIMC2 [R/W] 0 --- 0001	U-TIMER2
000084H	SMCS0 [R/W, R] 00000010 ---- 00-0		SES0 [R/W] ----- 00	SDR0 [R/W] 00000000	SIO 0
000088H	SMCS1 [R/W, R] 00000010 ---- 00-0		SES1 [R/W] ----- 00	SDR1 [R/W] 00000000	SIO 1
00008CH	CDCR0 [R/W] 0 --- 1111	Reserved	CDCR1 [R/W] 0 --- 1111	Reserved	SIO 0/1 Prescaler
000090H	-				Reserved
000094H	-	-	-	-	Reserved
000098H	-	-	-	-	

Address	Register				Block
	+0	+1	+2	+3	
00009C <sub>H</sub>	ADMD [R/W, W] ---X0000	ADCH [R/W] 00000000	-	ADCS [R/W, W] 0000 -- 00	A/D Converter
0000A0 <sub>H</sub>	ADCD [R/W] 000000XX XXXXXXXX		-	ADBL [R/W] ----- 0	
0000A4 <sub>H</sub>	-	DACR [R/W] ----- 000	DADR0 [R/W] ----- XX XXXXXXXX		DAC
0000A8 <sub>H</sub>	DADR1 [R/W] ----- XX XXXXXXXX		-	DDBL [R/W] ----- 0	
0000AC <sub>H</sub>	IOTDBL0 [R/W] ----- 000	ICS01 [R/W] 00000000	IOTDBL1 [R/W] ----- 000	ICS23 [R/W] 00000000	Input Capture 0, 1, 2, 3
0000B0 <sub>H</sub>	IPCP0 [R] XXXXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXXXX XXXXXXXX		
0000B4 <sub>H</sub>	IPCP2 [R] XXXXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXXXX XXXXXXXX		
0000B8 <sub>H</sub>	OCS01 [R/W] --- 0 -- 00 0000 -- 00	reserved			Output Compare 0, 1, 2, 3
0000BC <sub>H</sub>	OCCP0 [R/W] XXXXXXXXXX XXXXXXXX	OCCP1 [R/W] XXXXXXXXXX XXXXXXXX			
0000C0 <sub>H</sub>	OCCP2 [R/W] XXXXXXXXXX XXXXXXXX	OCCP3 [R/W] XXXXXXXXXX XXXXXXXX			
0000C4 <sub>H</sub>	-				Reserved
0000C8 <sub>H</sub>	TCDT0 [R/W] XXXXXXXXXX XXXXXXXX		-	TCCS0 [R/W] - 0000000	Free Running Counter 0 for ICU/OCU
0000CC <sub>H</sub>	TCDT1 [R/W] XXXXXXXXXX XXXXXXXX		-	TCCS1 [R/W] - 0000000	Free Running Counter 1 for ICU/OCU
0000D0 <sub>H</sub>	ZPD0 [R/W] 00000010	PWC0 [R/W] -- 000 -- 0	ZPD1 [R/W] 00000010	PWC1 [R/W] 00000 -- 0	SMC 0, 1
0000D4 <sub>H</sub>	ZPD2 [R/W] 00000010	PWC2 [R/W] -- 000 -- 0	ZPD3 [R/W] 00000010	PWC3 [R/W] 00000 -- 0	SMC 2, 3
0000D8 <sub>H</sub>	PWC20 [R/W] XXXXXXXXXX	PWC10 [R/W] XXXXXXXXXX	PWS20 [R/W] - 0000000	PWS10 [R/W] -- 000000	SMC 0
0000DC <sub>H</sub>	PWC21 [R/W] XXXXXXXXXX	PWC11 [R/W] XXXXXXXXXX	PWS21 [R/W] - 0000000	PWS11 [R/W] -- 000000	SMC 1
0000E0 <sub>H</sub>	PWC22 [R/W] XXXXXXXXXX	PWC12 [R/W] XXXXXXXXXX	PWS22 [R/W] - 0000000	PWS12 [R/W] -- 000000	SMC 2
0000E4 <sub>H</sub>	PWC23 [R/W] XXXXXXXXXX	PWC13 [R/W] XXXXXXXXXX	PWS23 [R/W] - 0000000	PWS13 [R/W] -- 000000	SMC 3
0000E8 <sub>H</sub>	SMDBL0 [R/W] ----- 0	SMDBL1 [R/W] ----- 0	SMDBL2 [R/W] ----- 0	SMDBL3 [R/W] ----- 0	SMC 0, 1, 2, 3
0000EC <sub>H</sub>	-	SGDBL [R/W] ----- 0	SGCR [R/W, R] 0----- 00 000 -- 000		Sound generator
0000F0 <sub>H</sub>	SGAR [R/W] 00000000	SGFR [R/W] XXXXXXXXXX	SGTR [R/W] XXXXXXXXXX	SGDR [R/W] XXXXXXXXXX	

**CY91FV360GA/F362GB/F364G**  
**CY91F365GB/366GA/F366GB**  
**CY91F367GB/F368GB/F369GA/F376G**



Address	Register				Block
	+0	+1	+2	+3	
0000F4 <sub>H</sub>	-	WTDBL [R/W] -----0	WTCR [R/W, R] 00000000 000 - 00 - 0		Real Time Clock (WatchTimer)
0000F8 <sub>H</sub>	-	WTBR [R/W] --- XXXXX XXXXXXXX XXXXXXXX			
0000FC <sub>H</sub>	WTHR [R/W] --- 00000	WTMR [R/W] -- 000000	WTSR [R/W] -- 000000	-	
000100 <sub>H</sub>	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3
000104 <sub>H</sub>	-	TMCSR3 [R/W] ---- XX -- --- XXXXX			
000108 <sub>H</sub>	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4
00010C <sub>H</sub>	-	TMCSR4 [R/W] ---- XX -- --- XXXXX			
000110 <sub>H</sub>	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5
000114 <sub>H</sub>	-	TMCSR5 [R/W] ---- XX -- --- XXXXX			
000118 <sub>H</sub>	GCN10 [R/W] 00110010 00010000		PDBL0 [R/W] --- 00000	GCN20 [R/W] ---- 0000	PWM Control 0
00011C <sub>H</sub>	GCN11 [R/W] 00110010 00010000		PDBL1 [R/W] --- 00000	GCN21 [R/W] ---- 0000	PWM Control 1
000120 <sub>H</sub>	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PWM0
000124 <sub>H</sub>	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 0000000 -	PCNL0 [R/W] 000000 - 0	
000128 <sub>H</sub>	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PWM1
00012C <sub>H</sub>	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 0000000 -	PCNL1 [R/W] 000000 - 0	
000130 <sub>H</sub>	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PWM2
000134 <sub>H</sub>	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 0000000 -	PCNL2 [R/W] 000000 - 0	
000138 <sub>H</sub>	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PWM3
00013C <sub>H</sub>	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 0000000 -	PCNL3 [R/W] 000000 - 0	
000140 <sub>H</sub>	PTMR4 [R] 11111111 11111111		PCSR4 [W] XXXXXXXX XXXXXXXX		PWM4
000144 <sub>H</sub>	PDUT4 [W] XXXXXXXX XXXXXXXX		PCNH4 [R/W] 0000000 -	PCNL4 [R/W] 000000 - 0	
000148 <sub>H</sub>	PTMR5 [R] 11111111 11111111		PCSR5 [W] XXXXXXXX XXXXXXXX		PWM5
00014C <sub>H</sub>	PDUT5 [W] XXXXXXXX XXXXXXXX		PCNH5 [R/W] 0000000 -	PCNL5 [R/W] 000000 - 0	

**CY91FV360GA/F362GB/F364G**  
**CY91F365GB/366GA/F366GB**  
**CY91F367GB/F368GB/F369GA/F376G**



Address	Register				Block
	+0	+1	+2	+3	
000150H	PTMR6 [R] 11111111 11111111		PCSR6 [W] XXXXXXXX XXXXXXXX		PWM6
000154H	PDUT 6 [W] XXXXXXXX XXXXXXXX		PCNH6 [R/W] 0000000 -	PCNL6 [R/W] 000000 - 0	
000158H	PTMR7 [R] 11111111 11111111		PCSR7 [W] XXXXXXXX XXXXXXXX		PWM7
00015CH	PDUT7 [W] XXXXXXXX XXXXXXXX		PCNH7 [R/W] 0000000 -	PCNL7 [R/W] 000000 - 0	
000160H	-				Reserved
000164H	CMCR [R/W] 11111111 0000000		CMPR [R/W] ----1001 1 ---0001		Clock Modulation
000168H	CMLS0 [R/W] 01110111 11111111		CMLS1 [R/W] 01110111 11111111		
00016CH	CMLS2 [R/W] 01110111 11111111		CMLS3 [R/W] 01110111 11111111		
000170H	CMLT0 [R/W, R] -----100 00000010		CMLT1 [R/W, R] 11110100 00000010		
000174H	CMLT2 [R/W] -----100 00000010		CMLT3 [R/W, R] -----100 00000010		
000178H	CMAC [R/W] 11111111 11111111		CMTS [R] -000001 01111111		
00017CH	-	PDCRCR [R/W] -----000	-	-	
000180H	ACCCDBL[R/W] -----0	ACSR [R/W, R] -11XXX00	-	-	Alarm comparator
000184H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH [R/W] -----00	ITBAL [R/W] 00000000	I <sup>2</sup> C (new)
000188H	ITMKH [R/W, R] 00 ---- 11	ITMKL [R/W] 11111111	ISMK [R/W] 01111111	ISBA [R/W] - 0000000	
00018CH	IDARH [-] 00000000	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	IDBL2 [R/W] -----0	
000190H	CUCR [R/W, R] -----0 --00		CUTD [R/W] 10000000 00000000		Calibration Unit of 32 kHz oscillator
000194H	CUTR1 [R] ----- 00000000		CUTR2 [R] 00000000 00000000		
000198H to 0001F8H	-				Reserved
0001FC <sub>H</sub>	-	-	F362MD [R/W] 00000000	-	F362GB Mode Register
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				



Address	Register				Block
	+0	+1	+2	+3	
000210 <sub>H</sub>	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214 <sub>H</sub>	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 <sub>H</sub>	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C <sub>H</sub>	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 <sub>H</sub>	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 <sub>H</sub>	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228 <sub>H</sub> to 00023C <sub>H</sub>	-				
000240 <sub>H</sub>	DMACR [R/W] 00 -- 0000 -----				
000244 <sub>H</sub> to 0002FC <sub>H</sub>	-				Reserved
000300 <sub>H</sub>	IRBS [R/W, R] 00000000 00000001 00100000 -----				Instruction Cache
000304 <sub>H</sub>	-		ISIZE [R/W] -----11		
000308 <sub>H</sub> to 0003E0 <sub>H</sub>	-				Reserved
0003E4 <sub>H</sub>	-		ICHCR [R/W] 0-000000		Instruction Cache
0003E8 <sub>H</sub> to 0003EC <sub>H</sub>	-				Reserved
0003F0 <sub>H</sub>	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 <sub>H</sub>	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 <sub>H</sub>	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC <sub>H</sub>	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 <sub>H</sub>	DDRG [R/W] 00000000	DDRH [R/W] 00000000	DDRJ [R/W] ---0---	DDRJ [R/W] 00000000	R-bus Data Direction Register
000404 <sub>H</sub>	DDRK [R/W] 00000000	DDRL [R/W] 00000000	DDRM [R/W] ---0000	DDRN [R/W] --000000	
000408 <sub>H</sub>	DDRO [R/W] 00000000	DDRP [R/W] 00000000	DDRQ [R/W] --000000	DDRR [R/W] 00000000	
00040C <sub>H</sub>	DDRS [R/W] 00000000	-	-	-	



Address	Register				Block
	+0	+1	+2	+3	
000410 <sub>H</sub>	PFRG [R/W] 00000000	PFRH [R/W] 00000000	PFRI [R/W] ---0---	PFRJ [R/W] 00000000	R-bus Port Function Register
000414 <sub>H</sub>	PFRK [R/W] 00000000	PFRL [R/W] 00000000	PFRM [R/W] ---0000	PFRN [R/W] --000000	
000418 <sub>H</sub>	PFRO [R/W] 00000000	PFRP [R/W] 00000000	PFRQ [R/W] --000000	PFRR [R/W] 00000000	
00041C <sub>H</sub>	PFRS [R/W] 00000000	–	–	–	
000420 <sub>H</sub> to 00043C <sub>H</sub>	–				Reserved
000440 <sub>H</sub>	ICR00 [R/W, R] ---11111	ICR01 [R/W, R] ---11111	ICR02 [R/W, R] ---11111	ICR03 [R/W, R] ---11111	Interrupt Control unit
000444 <sub>H</sub>	ICR04 [R/W, R] ---11111	ICR05 [R/W, R] ---11111	ICR06 [R/W, R] ---11111	ICR07 [R/W, R] ---11111	
000448 <sub>H</sub>	ICR08 [R/W, R] ---11111	ICR09 [R/W, R] ---11111	ICR10 [R/W, R] ---11111	ICR11 [R/W, R] ---11111	
00044C <sub>H</sub>	ICR12 [R/W, R] ---11111	ICR13 [R/W, R] ---11111	ICR14 [R/W, R] ---11111	ICR15 [R/W, R] ---11111	
000450 <sub>H</sub>	ICR16 [R/W, R] ---11111	ICR17 [R/W, R] ---11111	ICR18 [R/W, R] ---11111	ICR19 [R/W, R] ---11111	
000454 <sub>H</sub>	ICR20 [R/W, R] ---11111	ICR21 [R/W, R] ---11111	ICR22 [R/W, R] ---11111	ICR23 [R/W, R] ---11111	
000458 <sub>H</sub>	ICR24 [R/W, R] ---11111	ICR25 [R/W, R] ---11111	ICR26 [R/W, R] ---11111	ICR27 [R/W, R] ---11111	
00045C <sub>H</sub>	ICR28 [R/W, R] ---11111	ICR29 [R/W, R] ---11111	ICR30 [R/W, R] ---11111	ICR31 [R/W, R] ---11111	
000460 <sub>H</sub>	ICR32 [R/W, R] ---11111	ICR33 [R/W, R] ---11111	ICR34 [R/W, R] ---11111	ICR35 [R/W, R] ---11111	Interrupt Control unit
000464 <sub>H</sub>	ICR36 [R/W, R] ---11111	ICR37 [R/W, R] ---11111	ICR38 [R/W, R] ---11111	ICR39 [R/W, R] ---11111	
000468 <sub>H</sub>	ICR40 [R/W, R] ---11111	ICR41 [R/W, R] ---11111	ICR42 [R/W, R] ---11111	ICR43 [R/W, R] ---11111	
00046C <sub>H</sub>	ICR44 [R/W, R] ---11111	ICR45 [R/W, R] ---11111	ICR46 [R/W, R] ---11111	ICR47 [R/W, R] ---11111	
000470 <sub>H</sub> to 00047C <sub>H</sub>	–				Reserved
000480 <sub>H</sub>	RSRR [R, R/W] 10000-00	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXXXX	Clock Control unit
000484 <sub>H</sub>	CLKR [R/W] 00000000	WPR [W] XXXXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488 <sub>H</sub> to 0005FC <sub>H</sub>	–				Reserved

**CY91FV360GA/F362GB/F364G**  
**CY91F365GB/366GA/F366GB**  
**CY91F367GB/F368GB/F369GA/F376G**



Address	Register				Block
	+0	+1	+2	+3	
000600 <sub>H</sub>	-	-	-	-	T-unit Port Direction Register
000604 <sub>H</sub>	-	-	-	DDR7 [R/W] 00000000	
000608 <sub>H</sub>	DDR8 [R/W] 00000000	DDR9 [R/W] 00000000	-	DDR8 [R/W] 00000000	
00060C <sub>H</sub>	-				
000610 <sub>H</sub>	-	-	-	-	T-unit Port Function Register
000614 <sub>H</sub>	-	-	-	PFR7 [R/W] 00001111	
000618 <sub>H</sub>	PFR8 [R/W] 111110--	PFR9 [R/W] 11110101	-	PFRB [R/W] 00000000	
00061C <sub>H</sub>	-				
000620 <sub>H</sub>	-				
000624 <sub>H</sub>	-	-	-	PFR27 [R/W] 1111-00-	
000628 <sub>H</sub> to 00063F <sub>H</sub>	-				Reserved
000640 <sub>H</sub>	ASR0 [W] 00000000 00000000		AMR0 [W] 11111000 11111111		T-unit
000644 <sub>H</sub>	ASR1 [W] 00000000 00000000		AMR1 [W] 00000000 00000000		
000648 <sub>H</sub>	ASR2 [W] 00000000 00000000		AMR2 [W] 00000000 00000000		
00064C <sub>H</sub>	ASR3 [W] 00000000 00000000		AMR3 [W] 00000000 00000000		
000650 <sub>H</sub>	ASR4 [W] 00000000 00000000		AMR4 [W] 00000000 00000000		
000654 <sub>H</sub>	ASR5 [W] 00000000 00000000		AMR5 [W] 00000000 00000000		
000658 <sub>H</sub>	ASR6 [W] 00000000 00000000		AMR6 [W] 00000000 00000000		
00065C <sub>H</sub>	ASR7 [W] 00000000 00000000		AMR7 [W] 00000000 00000000		
000660 <sub>H</sub>	AMD0 [R/W] -0000111	AMD1 [R/W] -0000000	AMD2 [R/W] --000000	AMD3 [R/W] --000000	
000664 <sub>H</sub>	AMD4 [R/W] --000000	AMD5 [R/W] --000000	AMD6 [R/W] --000000	AMD7 [R/W] --000000	
000668 <sub>H</sub>	CSE 11000011	-	-	-	
00066C <sub>H</sub>	-				
000670 <sub>H</sub>	CHE 11111111	-	-	-	
000674 <sub>H</sub> to 0007F8 <sub>H</sub>	-				



Address	Register				Block
	+0	+1	+2	+3	
0007FC <sub>H</sub>	–	MODR [W] XXXXXXXX	–	–	Mode Register
000800 <sub>H</sub> to 000AFC <sub>H</sub>	–				Reserved
000B00 <sub>H</sub>	ESTS0 X0000000	ESTS1 XXXXXXXX	ESTS2 XXXXXXXX	–	DSU
000B04 <sub>H</sub>	ECTL0 0X000000	ECTL1 00000000	ECTL2 000X0000	ECTL3 00000X11	
000B08 <sub>H</sub>	ECNT0 XXXXXXXX	ECNT1 XXXXXXXX	EUSA XXX0000X	EDTC 0000XXXX	
000B0C <sub>H</sub>	EWPT XXXXXXXX XXXXXXXX		–		
000B10 <sub>H</sub>	EDTR0 XXXXXXXX XXXXXXXX		EDTR1 XXXXXXXX XXXXXXXX		
000B14 <sub>H</sub> to 000B1C <sub>H</sub>	–				
000B20 <sub>H</sub>	EIA0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24 <sub>H</sub>	EIA1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28 <sub>H</sub>	EIA2 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C <sub>H</sub>	EIA3 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30 <sub>H</sub>	EIA4 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34 <sub>H</sub>	EIA5 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38 <sub>H</sub>	EIA6 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3C <sub>H</sub>	EIA7 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40 <sub>H</sub>	EDTA XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44 <sub>H</sub>	EDTM XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48 <sub>H</sub>	EOA0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4C <sub>H</sub>	EOA1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50 <sub>H</sub>	EPCR XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54 <sub>H</sub>	EPSR XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block	
	+0	+1	+2	+3		
000B58 <sub>H</sub>	EIAM0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU	
000B5C <sub>H</sub>	EIAM1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B60 <sub>H</sub>	EOAM0/EODM0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B64 <sub>H</sub>	EOAM1/EODM1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B68 <sub>H</sub>	EOD0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B6C <sub>H</sub>	EOD1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001000 <sub>H</sub>	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC	
001004 <sub>H</sub>	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001008 <sub>H</sub>	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00100C <sub>H</sub>	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001010 <sub>H</sub>	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001014 <sub>H</sub>	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001018 <sub>H</sub>	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00101C <sub>H</sub>	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001020 <sub>H</sub>	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001024 <sub>H</sub>	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001028 <sub>H</sub> to 003FFC <sub>H</sub>	-					Reserved
004000 <sub>H</sub> to 006FFF <sub>H</sub>	-					Reserved
007000 <sub>H</sub>	FMCS [R, R/W] 1110X000	-	-	-		Flash Memory Control Register
007004 <sub>H</sub>	FMWT [R/W] -0000011	-	-	-		
007008 <sub>H</sub> to 00FFFF <sub>H</sub>	-				Reserved	
010000 <sub>H</sub> to 010FFF <sub>H</sub>	Cache memory is only available on CY91FV360GA.				I-Cache 4 KB	

**CY91FV360GA/F362GB/F364G**  
**CY91F365GB/366GA/F366GB**  
**CY91F367GB/F368GB/F369GA/F376G**



Address	Register				Block
	+0	+1	+2	+3	
011000 <sub>H</sub> to 011FFC <sub>H</sub>	Not available on CY91F364G. On CY91FV360GA, the cache memory can be used in I-RAM mode.				I-RAM 4 4 KB
012000 <sub>H</sub> to 01FFFC <sub>H</sub>	-				Reserved
020000 <sub>H</sub> to 03BFFC <sub>H</sub>	-				Reserved
03C000 <sub>H</sub> to 03FFFC <sub>H</sub>	CY91F362GB, CY91F364G: Only 12 KB (03D000 <sub>H</sub> to 03FFC <sub>H</sub> )				User RAM 16 KB (D-bus)
040000 <sub>H</sub> to 043FFC <sub>H</sub>	CY91F362GB, CY91F364G: Only 4 KB (040000 <sub>H</sub> to 040FFC <sub>H</sub> )				Fast RAM 16 KB (F-bus)
044000 <sub>H</sub> to 0FEFFC <sub>H</sub>	-				Reserved
050000 <sub>H</sub> to 0507FC <sub>H</sub>	-				Boot ROM 2 KB (F-bus)
050800 <sub>H</sub> to 07FFF4 <sub>H</sub>	-				reserved
080000 <sub>H</sub> to 09FFFC <sub>H</sub>	Sector 0 64 KB		Sector 7 64 KB		512 KB Flash on F-bus
0A0000 <sub>H</sub> to 0BFFFC <sub>H</sub>	Sector 1 64 KB		Sector 8 64 KB		
0C0000 <sub>H</sub> to 0DFFFC <sub>H</sub>	Sector 2 64 KB		Sector 9 64 KB		256 KB Flash <sup>a</sup> on F-bus
0E0000 <sub>H</sub> to 0EFFFFC <sub>H</sub>	Sector 3 32 KB		Sector 10 32 KB		
0F0000 <sub>H</sub> to 0F3FFC <sub>H</sub>	Sector 4 8 KB		Sector 11 8 KB		
0F4000 <sub>H</sub> to 0F7FFC <sub>H</sub>	Sector 5 8 KB		Sector 12 8 KB		
0F8000 <sub>H</sub> to 0FFFF4 <sub>H</sub>	Sector 6 16 KB		Sector 13 16 KB		
0FFFF8 <sub>H</sub> <sup>b</sup>	FMV [R] 06 00 00 00 <sub>H</sub>				Mode Vector
0FFFFC <sub>H</sub> <sup>b</sup>	FRV [R] 00 05 00 00 <sub>H</sub> (CY91F376G: 00 04 40 00 <sub>H</sub> )				Fixed Reset Vector

↑  
CY91F376G: Please refer to the CY91F376G Special I/O Map.  
↓



Address	Register				Block
	+0	+1	+2	+3	
10000H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0  Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
10004H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
10008H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
1000CH	ROVR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
10010H	CSR0 [R/W, R] 00000000 00000001		-	LEIR0 [R/W] 000-0000	
10014H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
10018H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
1001CH	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
10020H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10024H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10028H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
1002CH to 10048H	GENERAL PURPOSE RAM [R/W]				
1004CH	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10050H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10054H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10058H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
1005CH	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10060H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10064H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10068H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				

CY91F376G: Please refer to the CY91F376G Special I/O Map.

↑

↓



Address	Register				Block
	+0	+1	+2	+3	
10006C <sub>H</sub>	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				CAN 0
100070 <sub>H</sub>	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100074 <sub>H</sub>	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100078 <sub>H</sub>	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10007C <sub>H</sub>	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100080 <sub>H</sub>	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100084 <sub>H</sub>	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100088 <sub>H</sub>	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10008C <sub>H</sub>	DLCR00 [R/W] -----XXXX		DLCR10 [R/W] -----XXXX		↑
100090 <sub>H</sub>	DLCR20 [R/W] -----XXXX		DLCR30 [R/W] -----XXXX		
100094 <sub>H</sub>	DLCR40 [R/W] -----XXXX		DLCR50 [R/W] -----XXXX		
100098 <sub>H</sub>	DLCR60 [R/W] -----XXXX		DLCR70 [R/W] -----XXXX		
10009C <sub>H</sub>	DLCR80 [R/W] -----XXXX		DLCR90 [R/W] -----XXXX		
1000A0 <sub>H</sub>	DLCR100 [R/W] -----XXXX		DLCR110 [R/W] -----XXXX		
1000A4 <sub>H</sub>	DLCR120 [R/W] -----XXXX		DLCR130 [R/W] -----XXXX		
1000A8 <sub>H</sub>	DLCR140 [R/W] -----XXXX		DLCR150 [R/W] -----XXXX		
1000AC <sub>H</sub>	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000B4 <sub>H</sub>	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000BC <sub>H</sub>	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000C4 <sub>H</sub>	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000CC <sub>H</sub>	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

CY91F376G: Please refer to the CY91F376G Special I/O Map.

↓





Address	Register				Block
	+0	+1	+2	+3	
1000D4 <sub>H</sub>	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
1000DC <sub>H</sub>	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000E4 <sub>H</sub>	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000EC <sub>H</sub>	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000F4 <sub>H</sub>	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000FC <sub>H</sub>	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100104 <sub>H</sub>	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10010C <sub>H</sub>	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100114 <sub>H</sub>	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10011C <sub>H</sub>	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100124 <sub>H</sub>	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10012C <sub>H</sub>	CREG0 [R/W] 00000000 00000110		-		

CY91F376G: Please refer to the CY91F376G Special I/O Map.

Address	Register				Block
	+0	+1	+2	+3	
10020H	BVALR1 [R/W] 00000000 00000000	-	TREQR1 [R/W] 00000000 00000000	-	CAN 1  Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100204H	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
100208H	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
10020CH	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
100210H	CSR1 [R/W, R] 00000000 00000001		-	LEIR1 [R/W] 000-0000	
100214H	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
100218H	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
10021CH	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
100220H	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100224H	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100228H	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10022CH to 100248H	GENERAL PURPOSE RAM [R/W]				
10024CH	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100250H	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100254H	IDR21 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100258H	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10025CH	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100260H	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100264H	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				

CY91F376G: Please refer to the CY91F376G Special I/O Map.



Address	Register				Block
	+0	+1	+2	+3	
100268H	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 1
10026CH	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100270H	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100274H	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100278H	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10027CH	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
100280H	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100284H	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100288H	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10028CH	DLCR01 [R/W] -----XXXX		DLCR11 [R/W] -----XXXX		
100290H	DLCR21 [R/W] -----XXXX		DLCR31 [R/W] -----XXXX		
100294H	DLCR41 [R/W] -----XXXX		DLCR51 [R/W] -----XXXX		
100298H	DLCR61 [R/W] -----XXXX		DLCR71 [R/W] -----XXXX		
10029CH	DLCR81 [R/W] -----XXXX		DLCR91 [R/W] -----XXXX		
1002A0H	DLCR101 [R/W] -----XXXX		DLCR111 [R/W] -----XXXX		
1002A4H	DLCR121 [R/W] -----XXXX		DLCR131 [R/W] -----XXXX		
1002A8H	DLCR141 [R/W] -----XXXX		DLCR151 [R/W] -----XXXX		
1002ACH	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002B4H	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002BCH	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002C4H	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

CY91F376G: Please refer to the CY91F376G Special I/O Map.



Address	Register				Block
	+0	+1	+2	+3	
1002CC <sub>H</sub>	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
1002D4 <sub>H</sub>	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002DC <sub>H</sub>	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002E4 <sub>H</sub>	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002EC <sub>H</sub>	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002F4 <sub>H</sub>	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002FC <sub>H</sub>	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100304 <sub>H</sub>	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10030C <sub>H</sub>	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100314 <sub>H</sub>	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10031C <sub>H</sub>	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100324 <sub>H</sub>	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10032C <sub>H</sub>	CREG1 [R/W] 00000000 00000110		-		

CY91F376G: Please refer to the CY91F376G Special I/O Map.

**CY91FV360GA/F362GB/F364G**  
**CY91F365GB/366GA/F366GB**  
**CY91F367GB/F368GB/F369GA/F376G**



Address	Register				Block
	+0	+1	+2	+3	
10040H	BVALR2 [R/W] 00000000 00000000		TREQR2 [R/W] 00000000 00000000		CAN 2  Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100404H	TCANR2 [W] 00000000 00000000		TCR2 [R/W] 00000000 00000000		
100408H	RCR2 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
10040CH	ROVRR2 [R/W] 00000000 00000000		RIER2 [R/W] 00000000 00000000		
100410H	CSR2 [R/W, R] 00000000 00000001		-	LEIR2 [R/W] 000-0000	
100414H	RTEC2 [R] 00000000 00000000		BTR2 [R/W] -11111111 11111111		
100418H	IDER2 [R/W] XXXXXXXX XXXXXXXX		TRTRR2 [R/W] 00000000 00000000		
10041CH	RFWTR2 [R/W] XXXXXXXX XXXXXXXX		TIER2 [R/W] 00000000 00000000		
100420H	AMSR2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100424H	AMR02 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100428H	AMR12 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10042CH to 100448H	GENERAL PURPOSE RAM [R/W]				
10044CH	IDR02 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100450H	IDR12 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100454H	IDR22[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100458H	IDR32 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10045CH	IDR42 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
100460 <sub>H</sub>	IDR52 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				CAN 2
100464 <sub>H</sub>	IDR62 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100468 <sub>H</sub>	IDR72 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10046C <sub>H</sub>	IDR82 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100470 <sub>H</sub>	IDR92 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100474 <sub>H</sub>	IDR102 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100478 <sub>H</sub>	IDR112 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10047C <sub>H</sub>	IDR122 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX ---				
100480 <sub>H</sub>	IDR132 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100484 <sub>H</sub>	IDR142 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100488 <sub>H</sub>	IDR152 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10048C <sub>H</sub>	DLCR02 [R/W] -----XXXX		DLCR12 [R/W] -----XXXX		
100490 <sub>H</sub>	DLCR22 [R/W] -----XXXX		DLCR32 [R/W] -----XXXX		
100494 <sub>H</sub>	DLCR42 [R/W] -----XXXX		DLCR52 [R/W] -----XXXX		
100498 <sub>H</sub>	DLCR62 [R/W] -----XXXX		DLCR72 [R/W] -----XXXX		
10049C <sub>H</sub>	DLCR82 [R/W] -----XXXX		DLCR92 [R/W] -----XXXX		
1004A0 <sub>H</sub>	DLCR102 [R/W] -----XXXX		DLCR112 [R/W] -----XXXX		
1004A4 <sub>H</sub>	DLCR122 [R/W] -----XXXX		DLCR132 [R/W] -----XXXX		
1004A8 <sub>H</sub>	DLCR142 [R/W] -----XXXX		DLCR152 [R/W] -----XXXX		



Address	Register				Block	
	+0	+1	+2	+3		
1004AC <sub>H</sub>	DTR02 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 2	
1004B4 <sub>H</sub>	DTR12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004BC <sub>H</sub>	DTR22 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004C4 <sub>H</sub>	DTR32 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004CC <sub>H</sub>	DTR42 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004D4 <sub>H</sub>	DTR52 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004DC <sub>H</sub>	DTR62 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004E4 <sub>H</sub>	DTR72 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004EC <sub>H</sub>	DTR82 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004F4 <sub>H</sub>	DTR92 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
1004FC <sub>H</sub>	DTR102 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
100504 <sub>H</sub>	DTR112 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
10050C <sub>H</sub>	DTR122 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
100514 <sub>H</sub>	DTR132 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
10051C <sub>H</sub>	DTR142 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					CAN 2
100524 <sub>H</sub>	DTR152 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
10052C <sub>H</sub>	CREG2 [R/W] 00000000 00000110		-			



Address	Register				Block
	+0	+1	+2	+3	
10060H	BVALR3 [R/W] 00000000 00000000		TREQR3 [R/W] 00000000 00000000		<b>CAN 3</b>  Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100604H	TCANR3 [W] 00000000 00000000		TCR3 [R/W] 00000000 00000000		
100608H	RCR3 [R/W] 00000000 00000000		RRTRR31 [R/W] 00000000 00000000		
10060CH	ROVRR3 [R/W] 00000000 00000000		RIER3 [R/W] 00000000 00000000		
100610H	CSR3 [R/W, R] 00000000 00000001		-	LEIR3 [R/W] 000-0000	
100614H	RTEC3 [R] 00000000 00000000		BTR3 [R/W] -1111111 11111111		
100618H	IDER3 [R/W] XXXXXXXX XXXXXXXX		TRTRR3 [R/W] 00000000 00000000		
10061CH	RFWTR3 [R/W] XXXXXXXX XXXXXXXX		TIER3 [R/W] 00000000 00000000		
100620H	AMSR3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100624H	AMR03 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100628H	AMR13 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10062CH to 100648H	GENERAL PURPOSE RAM [R/W]				
10064CH	IDR03 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100650H	IDR13 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100654H	IDR23 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100658H	IDR33 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				





Address	Register				Block
	+0	+1	+2	+3	
10065C <sub>H</sub>	IDR43 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				CAN 3
100660 <sub>H</sub>	IDR53 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100664 <sub>H</sub>	IDR63 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100668 <sub>H</sub>	IDR73 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10066C <sub>H</sub>	IDR83 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100670 <sub>H</sub>	IDR93 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100674 <sub>H</sub>	IDR103 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100678 <sub>H</sub>	IDR113 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10067C <sub>H</sub>	IDR123 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX ---				
100680 <sub>H</sub>	IDR133 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100684 <sub>H</sub>	IDR143 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
100688 <sub>H</sub>	IDR153 [R/W] XXXXXXXX XXXXXXXX XXXXX --- XXXXXXXX				
10068C <sub>H</sub>	DLCR032 [R/W] -----XXXX		DLCR13 [R/W] -----XXXX		
100690 <sub>H</sub>	DLCR232 [R/W] -----XXXX		DLCR33 [R/W] -----XXXX		
100694 <sub>H</sub>	DLCR43 [R/W] -----XXXX		DLCR53 [R/W] -----XXXX		
100698 <sub>H</sub>	DLCR63 [R/W] -----XXXX		DLCR733 [R/W] -----XXXX		
10069C <sub>H</sub>	DLCR83 [R/W] -----XXXX		DLCR93 [R/W] -----XXXX		
1006A0 <sub>H</sub>	DLCR103 [R/W] -----XXXX		DLCR113 [R/W] -----XXXX		
1006A4 <sub>H</sub>	DLCR123 [R/W] -----XXXX		DLCR133 [R/W] -----XXXX		
1006A8 <sub>H</sub>	DLCR143 [R/W] -----XXXX		DLCR153 [R/W] -----XXXX		
1006AC <sub>H</sub>	DTR03 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006B4 <sub>H</sub>	DTR13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				



Address	Register				Block
	+0	+1	+2	+3	
1006BC <sub>H</sub>	DTR23 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 3
1006C4 <sub>H</sub>	DTR33 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006CC <sub>H</sub>	DTR43 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006D4 <sub>H</sub>	DTR53 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006DC <sub>H</sub>	DTR63 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006E4 <sub>H</sub>	DTR73 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006EC <sub>H</sub>	DTR83 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006F4 <sub>H</sub>	DTR93 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006FC <sub>H</sub>	DTR103 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100704 <sub>H</sub>	DTR113 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10070C <sub>H</sub>	DTR123 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100714 <sub>H</sub>	DTR133 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10071C <sub>H</sub>	DTR143 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100724 <sub>H</sub>	DTR153 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10072C <sub>H</sub>	CREG3 [R/W] 00000000 00000110		-		

a. Note: For the 256 KB Flash macro, used only on the CY91F364G.

b. Write operations to address 0FFFF8<sub>H</sub> and 0FFFFC<sub>H</sub> are not possible. When reading these addresses, the values shown above will be read.

**Note:** Data in reserved areas and in the areas marked with “-” is indeterminate. Do not use these areas.

### 10. CY91F376G Special I/O Map

Address	Register				Block
	+0	+1	+2	+3	
044000 <sub>H</sub> to 0447FC <sub>H</sub>	_____				Boot ROM 2 KB (F-bus)
044800 <sub>H</sub> to 05FFFC <sub>H</sub>	Sector 0 (parity) 56 KB		Sector 2 (parity) 56 KB		Flash Memory 768 KB (F-bus)
060000 <sub>H</sub> to 07FFFC <sub>H</sub>	Sector 1 64 KB		Sector 3 64 KB		
080000 <sub>H</sub> to 09FFFC <sub>H</sub>	Sector 4 64 KB		Sector 11 64 KB		
0A0000 <sub>H</sub> to 0BFFFC <sub>H</sub>	Sector 5 64 KB		Sector 12 64 KB		
0C0000 <sub>H</sub> to 0DFFFC <sub>H</sub>	Sector 6 64 KB		Sector 13 64 KB		
0E0000 <sub>H</sub> to 0EFFFF <sub>H</sub>	Sector 7 32 KB		Sector 14 32 KB		
0F0000 <sub>H</sub> to 0F3FFC <sub>H</sub>	Sector 8 8 KB		Sector 15 8 KB		
0F4000 <sub>H</sub> to 0F7FFC <sub>H</sub>	Sector 9 8 KB		Sector 16 8 KB		
0F8000 <sub>H</sub> to 0FFFFC <sub>H</sub>	Sector 10 16 KB		Sector 17 16 KB		
	Fixed Mode and Reset Vector				
100000 <sub>H</sub> to 11FFFC <sub>H</sub>	Sector 0 - mirrored 64 KB		Sector 2 - mirrored 64 KB		
120000 <sub>H</sub> to 13FFFC <sub>H</sub>	Sector 1 - mirrored 64 KB		Sector 3 - mirrored 64 KB		



Address	Register				Block
	+0	+1	+2	+3	
20000H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0  Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
20004H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
20008H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
2000CH	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
20010H	CSR0 [R/W, R] 00000000 00000001		-	LEIR0 [R/W] 000-0000	
20014H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
20018H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
2001CH	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
20020H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20024H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20028H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
2002CH to 20048H	GENERAL PURPOSE RAM [R/W]				
2004CH	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20050H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20054H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20058H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
2005CH	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20060H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20064H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20068H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				



Address	Register				Block
	+0	+1	+2	+3	
20006C <sub>H</sub>	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				CAN 0
200070 <sub>H</sub>	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
200074 <sub>H</sub>	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
200078 <sub>H</sub>	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
20007C <sub>H</sub>	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
200080 <sub>H</sub>	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
200084 <sub>H</sub>	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
200088 <sub>H</sub>	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX				
20008C <sub>H</sub>	DLCR00 [R/W] -----XXX		DLCR10 [R/W] -----XXX		
200090 <sub>H</sub>	DLCR20 [R/W] -----XXX		DLCR30 [R/W] -----XXX		
200094 <sub>H</sub>	DLCR40 [R/W] -----XXX		DLCR50 [R/W] -----XXX		
200098 <sub>H</sub>	DLCR60 [R/W] -----XXX		DLCR70 [R/W] -----XXX		
20009C <sub>H</sub>	DLCR80 [R/W] -----XXX		DLCR90 [R/W] -----XXX		
2000A0 <sub>H</sub>	DLCR100 [R/W] -----XXX		DLCR110 [R/W] -----XXX		
2000A4 <sub>H</sub>	DLCR120 [R/W] -----XXX		DLCR130 [R/W] -----XXX		
2000A8 <sub>H</sub>	DLCR140 [R/W] -----XXX		DLCR150 [R/W] -----XXX		
2000AC <sub>H</sub>	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000B4 <sub>H</sub>	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000BC <sub>H</sub>	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				



Address	Register				Block
	+0	+1	+2	+3	
2000C <sub>H</sub>	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
2000CC <sub>H</sub>	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000D <sub>H</sub>	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000DC <sub>H</sub>	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000E <sub>H</sub>	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000EC <sub>H</sub>	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000F <sub>H</sub>	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000FC <sub>H</sub>	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20010 <sub>H</sub>	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20010C <sub>H</sub>	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20011 <sub>H</sub>	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20011C <sub>H</sub>	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20012 <sub>H</sub>	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20012C <sub>H</sub>	CREG0 [R/W] 00000000 00000110		-		



Address	Register				Block
	+0	+1	+2	+3	
200200 <sub>H</sub>	BVALR1 [R/W] 00000000 00000000		TREQR1 [R/W] 00000000 00000000		CAN 1  Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
200204 <sub>H</sub>	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
200208 <sub>H</sub>	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
20020C <sub>H</sub>	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
200210 <sub>H</sub>	CSR1 [R/W] 00000000 00000001		-	LEIR1 [R/W] 000-0000	
200214 <sub>H</sub>	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
200218 <sub>H</sub>	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
20021C <sub>H</sub>	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
200220 <sub>H</sub>	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200224 <sub>H</sub>	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200228 <sub>H</sub>	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20022C <sub>H</sub> to 200248 <sub>H</sub>	GENERAL PURPOSE RAM [R/W]				
20024C <sub>H</sub>	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200250 <sub>H</sub>	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200254 <sub>H</sub>	IDR21 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200258 <sub>H</sub>	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX-				
20025C <sub>H</sub>	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200260 <sub>H</sub>	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200264 <sub>H</sub>	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200268 <sub>H</sub>	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				



Address	Register				Block
	+0	+1	+2	+3	
20026C <sub>H</sub>	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 1
200270 <sub>H</sub>	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200274 <sub>H</sub>	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200278 <sub>H</sub>	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20027C <sub>H</sub>	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
200280 <sub>H</sub>	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200284 <sub>H</sub>	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200288 <sub>H</sub>	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20028C <sub>H</sub>	DLCR01 [R/W] -----XXX		DLCR11 [R/W] -----XXX		
200290 <sub>H</sub>	DLCR21 [R/W] -----XXX		DLCR31 [R/W] -----XXX		
200294 <sub>H</sub>	DLCR41 [R/W] -----XXX		DLCR51 [R/W] -----XXX		
200298 <sub>H</sub>	DLCR61 [R/W] -----XXX		DLCR71 [R/W] -----XXX		
20029C <sub>H</sub>	DLCR81 [R/W] -----XXX		DLCR91 [R/W] -----XXX		
2002A0 <sub>H</sub>	DLCR101 [R/W] -----XXX		DLCR111 [R/W] -----XXX		
2002A4 <sub>H</sub>	DLCR121 [R/W] -----XXX		DLCR131 [R/W] -----XXX		
2002A8 <sub>H</sub>	DLCR141 [R/W] -----XXX		DLCR151 [R/W] -----XXX		
2002AC <sub>H</sub>	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002B4 <sub>H</sub>	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002BC <sub>H</sub>	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				





Address	Register				Block
	+0	+1	+2	+3	
2002C4 <sub>H</sub>	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
2002CC <sub>H</sub>	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002D4 <sub>H</sub>	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002DC <sub>H</sub>	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002E4 <sub>H</sub>	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002EC <sub>H</sub>	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002F4 <sub>H</sub>	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002FC <sub>H</sub>	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200304 <sub>H</sub>	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20030C <sub>H</sub>	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200314 <sub>H</sub>	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20031C <sub>H</sub>	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200324 <sub>H</sub>	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20032C <sub>H</sub>	CREG1 [R/W] 00000000 00000110				

## 11. Interrupt Causes, Interrupt Vectors, and Interrupt Control Register

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
Reset	0	00	–	–	0x3FC <sub>H</sub>	0x000FFFFC <sub>H</sub>	–
Mode vector	1	01	–	–	0x3F8 <sub>H</sub>	0x000FFF8 <sub>H</sub>	–
System reserved	2	02	–	–	0x3F4 <sub>H</sub>	0x000FFF4 <sub>H</sub>	–
System reserved	3	03	–	–	0x3F0 <sub>H</sub>	0x000FFF0 <sub>H</sub>	–
System reserved	4	04	–	–	0x3EC <sub>H</sub>	0x000FFFE <sub>C</sub>	–
System reserved	5	05	–	–	0x3E8 <sub>H</sub>	0x000FFFE8 <sub>H</sub>	–
System reserved	6	06	–	–	0x3E4 <sub>H</sub>	0x000FFFE4 <sub>H</sub>	–
Co-processor default trap *4	7	07	–	–	0x3E0 <sub>H</sub>	0x000FFFE0 <sub>H</sub>	–
Co-processor error trap *4	8	08	–	–	0x3DC <sub>H</sub>	0x000FFFD <sub>C</sub>	–
INTE instruction *4	9	09	–	–	0x3D8 <sub>H</sub>	0x000FFFD8 <sub>H</sub>	–
Instruction break exception *4	10	0A	–	–	0x3D4 <sub>H</sub>	0x000FFFD4 <sub>H</sub>	–
Operand break trap *4	11	0B	–	–	0x3D0 <sub>H</sub>	0x000FFFD0 <sub>H</sub>	–
Step trace trap *4	12	0C	–	–	0x3CC <sub>H</sub>	0x000FFFC <sub>C</sub>	–
NMI interrupt (tool) *4	13	0D	–	–	0x3C8 <sub>H</sub>	0x000FFFC8 <sub>H</sub>	–
Undefined instruction exception	14	0E	–	–	0x3C4 <sub>H</sub>	0x000FFFC4 <sub>H</sub>	–
NMI request	15	0F	F <sub>H</sub> fixed		0x3C0 <sub>H</sub>	0x000FFFC0 <sub>H</sub>	–
External Interrupt 0	16	10	ICR00	0x440 <sub>H</sub>	0x3BC <sub>H</sub>	0x000FFFB <sub>C</sub>	4
External Interrupt 1	17	11	ICR01	0x441 <sub>H</sub>	0x3B8 <sub>H</sub>	0x000FFFB8 <sub>H</sub>	5
External Interrupt 2	18	12	ICR02	0x442 <sub>H</sub>	0x3B4 <sub>H</sub>	0x000FFFB4 <sub>H</sub>	8
External Interrupt 3	19	13	ICR03	0x443 <sub>H</sub>	0x3B0 <sub>H</sub>	0x000FFFB0 <sub>H</sub>	9
External Interrupt 4	20	14	ICR04	0x444 <sub>H</sub>	0x3AC <sub>H</sub>	0x000FFFA <sub>C</sub>	–
External Interrupt 5	21	15	ICR05	0x445 <sub>H</sub>	0x3A8 <sub>H</sub>	0x000FFFA8 <sub>H</sub>	–
External Interrupt 6	22	16	ICR06	0x446 <sub>H</sub>	0x3A4 <sub>H</sub>	0x000FFFA4 <sub>H</sub>	–
External Interrupt 7	23	17	ICR07	0x447 <sub>H</sub>	0x3A0 <sub>H</sub>	0x000FFFA0 <sub>H</sub>	–
Reload Timer 0	24	18	ICR08	0x448 <sub>H</sub>	0x39C <sub>H</sub>	0x000FFF9 <sub>C</sub>	6
Reload Timer 1	25	19	ICR09	0x449 <sub>H</sub>	0x398 <sub>H</sub>	0x000FFF98 <sub>H</sub>	7
Reload Timer 2	26	1A	ICR10	0x44A <sub>H</sub>	0x394 <sub>H</sub>	0x000FFF94 <sub>H</sub>	–
CAN 0 RX	27	1B	ICR11	0x44B <sub>H</sub>	0x390 <sub>H</sub>	0x000FFF90 <sub>H</sub>	–
CAN 0 TX/NS	28	1C	ICR12	0x44C <sub>H</sub>	0x38C <sub>H</sub>	0x000FFF8 <sub>C</sub>	–
CAN 1 RX	29	1D	ICR13	0x44D <sub>H</sub>	0x388 <sub>H</sub>	0x000FFF88 <sub>H</sub>	–
CAN 1 TX/NS	30	1E	ICR14	0x44E <sub>H</sub>	0x384 <sub>H</sub>	0x000FFF84 <sub>H</sub>	–
CAN 2 RX	31	1F	ICR15	0x44F <sub>H</sub>	0x380 <sub>H</sub>	0x000FFF80 <sub>H</sub>	–
CAN 2 TX/NS	32	20	ICR16	0x450 <sub>H</sub>	0x37C <sub>H</sub>	0x000FFF7 <sub>C</sub>	–
CAN 3 RX *5	33	21	ICR17	0x451 <sub>H</sub>	0x378 <sub>H</sub>	0x000FFF78 <sub>H</sub>	–
CAN 3 TX/NS *5	34	22	ICR18	0x452 <sub>H</sub>	0x374 <sub>H</sub>	0x000FFF74 <sub>H</sub>	–
PPG 0/1	35	23	ICR19	0x453 <sub>H</sub>	0x370 <sub>H</sub>	0x000FFF70 <sub>H</sub>	–



Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
PPG 2/3	36	24	ICR20	0x454 <sub>H</sub>	0x36C <sub>H</sub>	0x000FFF6C <sub>H</sub>	–
PPG 4/5	37	25	ICR21	0x455 <sub>H</sub>	0x368 <sub>H</sub>	0x000FFF68 <sub>H</sub>	–
PPG 6/7	38	26	ICR22	0x456 <sub>H</sub>	0x364 <sub>H</sub>	0x000FFF64 <sub>H</sub>	–
Reload Timer 3	39	27	ICR23	0x457 <sub>H</sub>	0x360 <sub>H</sub>	0x000FFF60 <sub>H</sub>	–
Reload Timer 4	40	28	ICR24	0x458 <sub>H</sub>	0x35C <sub>H</sub>	0x000FFF5C <sub>H</sub>	–
Reload Timer 5	41	29	ICR25	0x459 <sub>H</sub>	0x358 <sub>H</sub>	0x000FFF58 <sub>H</sub>	–
ICU 0/1	42	2A	ICR26	0x45A <sub>H</sub>	0x354 <sub>H</sub>	0x000FFF54 <sub>H</sub>	–
OCU 0/1	43	2B	ICR27	0x45B <sub>H</sub>	0x350 <sub>H</sub>	0x000FFF50 <sub>H</sub>	–
ICU 2/3	44	2C	ICR28	0x45C <sub>H</sub>	0x34C <sub>H</sub>	0x000FFF4C <sub>H</sub>	–
OCU 2/3	45	2D	ICR29	0x45D <sub>H</sub>	0x348 <sub>H</sub>	0x000FFF48 <sub>H</sub>	–
ADC	46	2E	ICR30	0x45E <sub>H</sub>	0x344 <sub>H</sub>	0x000FFF44 <sub>H</sub>	14
Timebase Overflow	47	2F	ICR31	0x45F <sub>H</sub>	0x340 <sub>H</sub>	0x000FFF40 <sub>H</sub>	–
Free Running Counter 0	48	30	ICR32	0x460 <sub>H</sub>	0x33C <sub>H</sub>	0x000FFF3C <sub>H</sub>	–
Free Running Counter 1	49	31	ICR33	0x461 <sub>H</sub>	0x338 <sub>H</sub>	0x000FFF38 <sub>H</sub>	–
SIO 0 *6	50	32	ICR34	0x462 <sub>H</sub>	0x334 <sub>H</sub>	0x000FFF34 <sub>H</sub>	12
SIO 1 *6	51	33	ICR35	0x463 <sub>H</sub>	0x330 <sub>H</sub>	0x000FFF30 <sub>H</sub>	15
Sound Generator	52	34	ICR36	0x464 <sub>H</sub>	0x32C <sub>H</sub>	0x000FFF2C <sub>H</sub>	–
UART 0 RX	53	35	ICR37	0x465 <sub>H</sub>	0x328 <sub>H</sub>	0x000FFF28 <sub>H</sub>	0
UART 0 TX	54	36	ICR38	0x466 <sub>H</sub>	0x324 <sub>H</sub>	0x000FFF24 <sub>H</sub>	1
UART 1 RX	55	37	ICR39	0x467 <sub>H</sub>	0x320 <sub>H</sub>	0x000FFF20 <sub>H</sub>	2
UART 1 TX	56	38	ICR40	0x468 <sub>H</sub>	0x31C <sub>H</sub>	0x000FFF1C <sub>H</sub>	3
UART 2 RX	57	39	ICR41	0x469 <sub>H</sub>	0x318 <sub>H</sub>	0x000FFF18 <sub>H</sub>	10
UART 2 TX	58	3A	ICR42	0x46A <sub>H</sub>	0x314 <sub>H</sub>	0x000FFF14 <sub>H</sub>	11
I <sup>2</sup> C *7	59	3B	ICR43	0x46B <sub>H</sub>	0x310 <sub>H</sub>	0x000FFF10 <sub>H</sub>	13
Alarm Comparator	60	3C	ICR44	0x46C <sub>H</sub>	0x30C <sub>H</sub>	0x000FFF0C <sub>H</sub>	–
RTC (Watchtimer) / Calibration Unit	61	3D	ICR45	0x46D <sub>H</sub>	0x308 <sub>H</sub>	0x000FFF08 <sub>H</sub>	–
DMA	62	3E	ICR46	0x46E <sub>H</sub>	0x304 <sub>H</sub>	0x000FFF04 <sub>H</sub>	–
Delayed interrupt activation bit	63	3F	ICR47	0x46F <sub>H</sub>	0x300 <sub>H</sub>	0x000FFF00 <sub>H</sub>	–
System reserved *3	64	40	–	–	0x2FC <sub>H</sub>	0x000FFEFC <sub>H</sub>	–
System reserved *3	65	41	–	–	0x2F8 <sub>H</sub>	0x000FFE8 <sub>H</sub>	–
Security vector	66	42	–	–	0x2F4 <sub>H</sub>	0x000FEF4 <sub>H</sub>	–
System reserved	67	43	(ICR51)	0x473 <sub>H</sub>	0x2F0 <sub>H</sub>	0x000FEF0 <sub>H</sub>	–
System reserved	68	44	(ICR52)	0x474 <sub>H</sub>	0x2EC <sub>H</sub>	0x000FEEC <sub>H</sub>	–
System reserved	69	45	(ICR53)	0x475 <sub>H</sub>	0x2E8 <sub>H</sub>	0x000FEE8 <sub>H</sub>	–
System reserved	70	46	(ICR54)	0x476 <sub>H</sub>	0x2E4 <sub>H</sub>	0x000FEE4 <sub>H</sub>	–
System reserved	71	47	(ICR55)	0x477 <sub>H</sub>	0x2E0 <sub>H</sub>	0x000FEE0 <sub>H</sub>	–
System reserved	72	48	(ICR56)	0x478 <sub>H</sub>	0x2DC <sub>H</sub>	0x000FEDC <sub>H</sub>	–



Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
System reserved	73	49	(ICR57)	0x479H	0x2D8H	0x000FFED8H	–
System reserved	74	4A	(ICR58)	0x47AH	0x2D4H	0x000FFED4H	–
System reserved	75	4B	(ICR59)	0x47BH	0x2D0H	0x000FFED0H	–
System reserved	76	4C	(ICR60)	0x47CH	0x2CCH	0x000FFECCH	–
System reserved	77	4D	(ICR61)	0x47DH	0x2C8H	0x000FFEC8H	–
System reserved	78	4E	(ICR62)	0x47EH	0x2C4H	0x000FFEC4H	–
System reserved	79	4F	(ICR63)	0x47FH	0x2C0H	0x000FFEC0H	–
Used by the INT instruction.	80 to 255	50 to FF	–	–	0x2BC <sub>H</sub> to 0x000 <sub>H</sub>	0x000FFEC <sub>H</sub> to 0x000FFC0 <sub>H</sub>	–
							–
							–

\*1: The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

\*2: The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00<sub>H</sub>). The TBR is initialized to this value by a reset. After execution of the internal boot ROM TBR is set to 0x00FFC00<sub>H</sub>.

\*3: ..... Used by REALOS

\*4: ..... System reserved

\*5: ..... Only available on CY91FV360GA

\*6: USART5/6 in CY91F364G, UART1/2 in all other devices.

\*7: DMA to/from the USARTs in CY91F364G is not implemented.

#### Remarks:

The 1-Kbyte area from the address specified in TBR is the EIT vector area.

Each vector consists of four bytes. The following formula shows the relationship between the vector number and vector address.

$$\begin{aligned} \text{vctadr} &= \text{TBR} + \text{vctofs} \\ &= \text{TBR} + (3\text{FCH} - 4 \times \text{vct}) \end{aligned}$$

vctadr: Vector address, vctofs: Vector offset, vct: Vector number

## 12. Peripheral Resources

### 12.1 Instruction Cache

This section describes the instruction cache memory included in FR50 Family members and its operation. This only applies to CY91FV360GA.

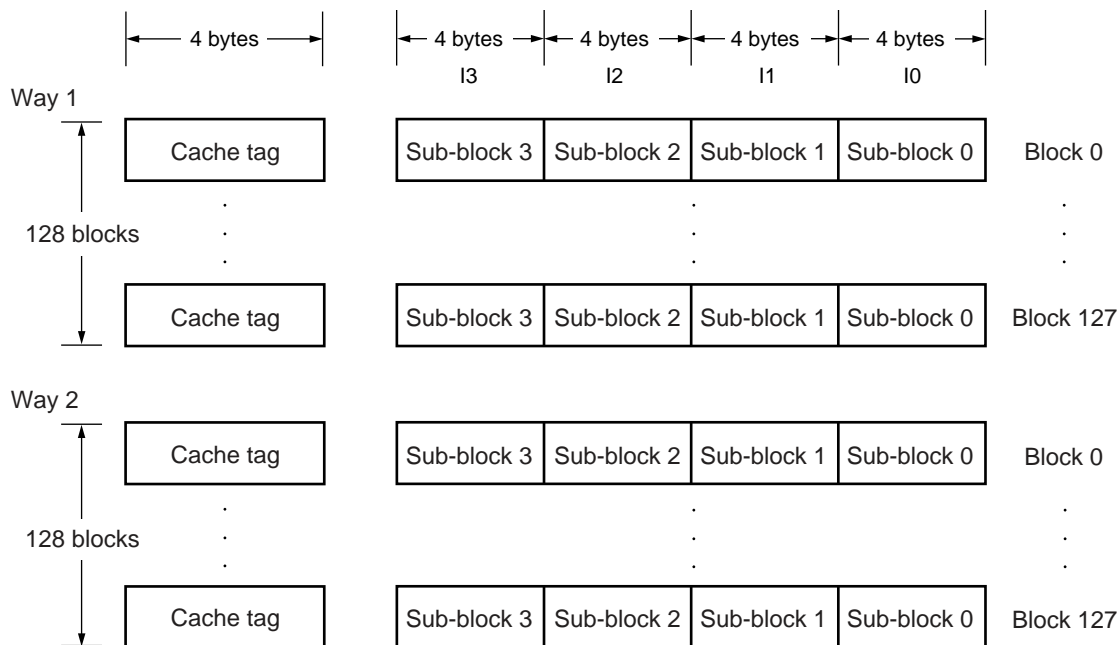
#### 12.1.1 General Description

The instruction cache is temporary memory. When an external low-speed memory accesses an instruction code, the instruction cache stores the single-accessed code to increase the second and subsequent access speeds. Setting this memory to the RAM mode enables software to directly read and write instruction cache data RAM and tag RAM.

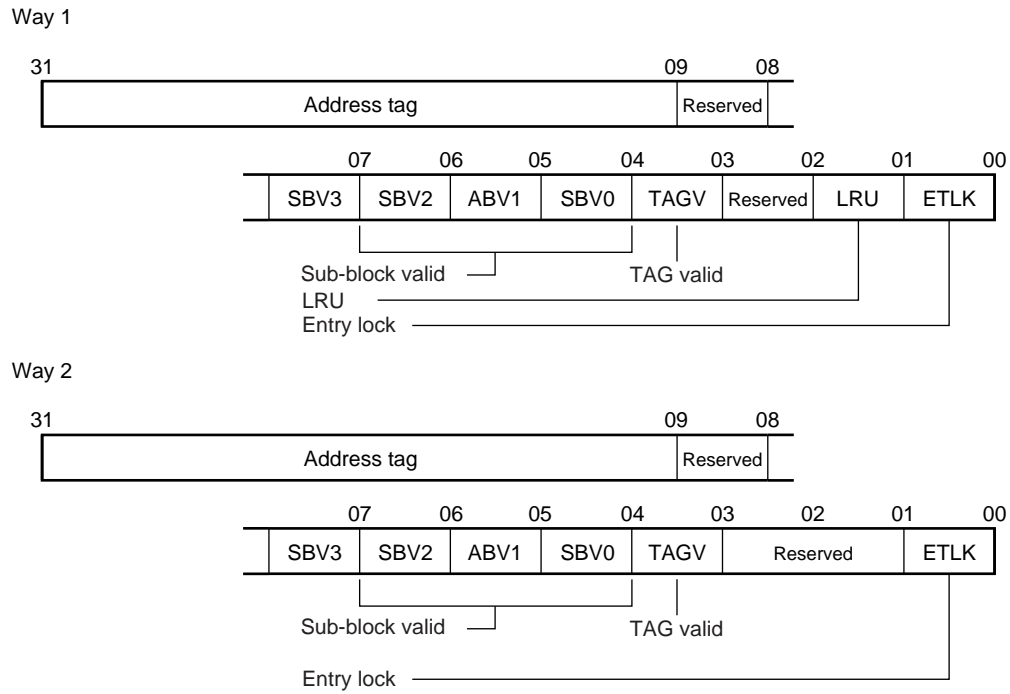
#### 12.1.2 Main Body Structure

- FR basic instruction length: 2 bytes
- Block arrangement system: 2-way set associative system
- Block
  - One way consists of 128 blocks.
  - One block consists of 16 bytes (= 4 sub-blocks).
  - One sub-block consists of 4 bytes (= 1 bus access unit).

**Figure 12-1. Instruction Cache Structure**



**Figure 12-2. Instruction Cache Tag**



12.0.1 Control Register Structure

IRBS (32 bits)	31	30	29	28	27	26	25	24	Initial value
Address: 00000300 <sub>H</sub>	0	0	0	0	0	0	0	0	00000000 <sub>B</sub>
	R	R	R	R	R	R	R	R	

	23	22	21	20	19	18	17	16	Initial value
	0	0	0	0	0	0	0	1	00000001 <sub>B</sub>
	R	R	R	R	R	R	R	R	ICR26

Address: 00000302 <sub>H</sub>	15	14	13	12	11	10	9	8	Initial value
	IRBS	IRBS	IRBS	IRBS	—	—	—	—	0010 ---- <sub>B</sub>
	R/W	R/W	R/W	R/W	—	—	—	—	

	7	6	5	4	3	2	1	0	Initial value
	—	—	—	—	—	—	—	—	----- <sub>B</sub>
	—	—	—	—	—	—	—	—	

IRBS [bits 15 to 12] These bits are used to set the base address of cache RAM at access in the RAM mode. Align cache RAM in units of 4K bytes. These bits are initialized by INIT. The initial value is the 00012000<sub>H</sub> address.

ISIZE (8 bits)	7	6	5	4	3	2	1	0	Initial value
00000307 <sub>H</sub>	—	—	—	—	—	—	SIZE1	SIZE0	----- 11 <sub>B</sub>
	—	—	—	—	—	—	R/W	R/W	

The ICHCR (I-CacHe Control Register) controls the instruction cache operations. Writing to the ICHCR does not affect caching of instructions fetched within three subsequent cycles.

ICHCR (8 bits)	7	6	5	4	3	2	1	0	Initial value
000003E7 <sub>H</sub>	RAM	—	GBLK	ALFL	EOLK	ELKR	FLSH	ENAB	0 - 000000 <sub>B</sub>
	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	

## 12.1 Boot ROM

The Boot ROM is a fixed start-up routine which is located at FF000<sub>H</sub> (Reset entry) and will therefore be executed after every RST or INIT. The purpose of this ROM is to configure the device after a reset and to provide a simple serial bootloader for programming the embedded Flash memories.

The Boot ROM contains three logical parts:

### 12.1.1 Chip Initializations

Immediately after each reset, the following settings will be made:

CS0: 200000<sub>H</sub>...2FFFFFF<sub>H</sub>, 32 Bit Bus, 1 wait-state (default external access)

CS7: 100000<sub>H</sub>...10FFFF<sub>H</sub>, 16 Bit Bus, 1 wait-state (CAN)

In addition, the Table-Base Register will be initialized to 1FFC00<sub>H</sub> (F361GA only) and the synchronous reset (see TBCR) will be enabled.

### 12.1.2 Check for Bootcondition

After the chip initialization, the “Security-Vector” will be checked (Vector #66). The purpose of this feature is to disable the bootst-raploader due to security reasons.

The RSRR (reset cause register) will be read and saved. If no power-on reset (external INITX input, RSRR = 0x80) is indicated, a branch to the user application will be initiated (Branch to 1F4000<sub>H</sub>).

If INITX was detected and the “Security-Vector” check okay, the following conditions must be met in order to start the Bootstrap-loader:

Within a certain time, the start-up character “V” must be received via UART0 (9600, 8N1). The time-out is set to 200 ms.

### 12.1.3 Bootstraploader

If the Bootcondition was met, an acknowledge character “F” will be transmitted via UART0 to indicate that the Bootloader is ready to accept commands. 4 different commands are possible:

- Receive and write to a specified memory block
- Dump the contents of a specified memory block
- Initiate a “CALL” to a certain location
- Re-dump a calculated checksum for verification

### 12.1.4 Configuration Register (F362 mode register F362MD)

This register is used to control which pins of the external bus interface are active, where the pins for the external DMA channel are located and which I<sup>2</sup>C module is used.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
00001FE <sub>H</sub>	ADRSWAP	ASYMCLKT	HIZ_D_A	HIZ_ECLK	HIZ_D_23_16	HIZ_D_15_0	DMASWP	IICSEL
access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

## 12.2 Clock Modulator

An important property of MCUs and other electronic devices is their electromagnetic compatibility - EMC. Besides a low susceptibility against external interferences, a low radiated emission is desired to avoid interference of adjacent devices.

Particularly the system clock and derived signals such as data- and address busses contribute significantly to the radiated emission. The purpose of the clock modulator is to spread the energy of these signals over a wide range of frequencies and thus reducing the amplitudes of the fundamental and harmonic frequencies.

With the use of an advanced frequency modulation algorithm, the Cypress built in clock modulator can achieve an attenuation of up to 20-25 dB compared to non modulated clock operation. Since the modulator is highly configurable, it can be optimally adjusted to the actual application in order to achieve minimal electromagnetic interference.

By default, the modulator is disabled and the MCU is running with unmodulated clock.

If you plan to use this feature, please contact Cypress.



### 12.3 I/O Ports

The I/O port registers consist of the “port data registers (PDR)”, the “data direction registers (DDR)” and the “port function registers (PFR)”.

The bits in PDRs correspond to the bits in DDRs and PFRs. Similarly, the register bits correspond to the port pins.

The port data registers contain the port I/O data and the data direction registers specify whether the corresponding bits (pins) are inputs or outputs. Bits set to “0” are inputs and bits set to “1” are outputs. The port function registers specify whether the port is used as peripheral port or as “I/O” port. Usually bits set to “0” mean I/O port and bits set to “1” mean functional port.

In case of analog peripherals there is additional circuitry to ensure that the digital logic is not disturbed by the analog signals. If the analog input function e.g. ADC is enabled the digital input is fixed to “0”.

- Input mode (DDR = “0”)

- PDR read: Reads the level on the corresponding external pin.

- PDR write: writes the PDR setting value.

- Output mode (DDR = “1”)

- PDR read: Reads the PDR value.

- PDR write: Outputs the PDR value to the corresponding external pins.

12.3.1 Register Configuration

**Port Data Register**

PDR7	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000007 <sub>H</sub>	P77	P76	P75	P74	P73	P72	P71	P70	1111XXXX <sub>B</sub>	R/W
PDR8	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000008 <sub>H</sub>	P87	P86	P85	P84	P83	P82	P81	P80	XXXXXXXX <sub>B</sub>	R/W
PDR9	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000009 <sub>H</sub>	P97	P96	P95	P94	P93	P92	P91	P90	XXXXXXXX1 <sub>B</sub>	R/W
PDRB	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000000B <sub>H</sub>	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	XXXXXXXX <sub>B</sub>	R/W
PDRG	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000010 <sub>H</sub>	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	XXXXXXXX <sub>B</sub>	R/W
PDRH	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000011 <sub>H</sub>	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	XXXXXXXX <sub>B</sub>	R/W
PDRI	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000012 <sub>H</sub>	P17	—	—	—	PI3	—	—	—	X --- X --- <sub>B</sub>	R/W
PDRJ	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000013 <sub>H</sub>	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	XXXXXXXX <sub>B</sub>	R/W
PDRK	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000014 <sub>H</sub>	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	XXXXXXXX <sub>B</sub>	R/W
PDRL	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000015 <sub>H</sub>	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	XXXXXXXX <sub>B</sub>	R/W
PDRM	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000016 <sub>H</sub>	—	—	—	—	PM3	PM2	PM1	PM0	---- XXXX <sub>B</sub>	R/W
PDRN	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000017 <sub>H</sub>	—	—	PN5	PN4	PN3	PN2	PN1	PN0	- - XXXXXX <sub>B</sub>	R/W
PDRO	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000018 <sub>H</sub>	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	XXXXXXXX <sub>B</sub>	R/W

*(Continued)*

(Continued)

PDRP		7	6	5	4	3	2	1	0	Initial value	Access
Address:	00000019 <sub>H</sub>	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	XXXXXXXX <sub>B</sub>	R/W

PDRQ		7	6	5	4	3	2	1	0	Initial value	Access
Address:	0000001A <sub>H</sub>	—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0	--XXXXXX <sub>B</sub>	R/W

PDRR		7	6	5	4	3	2	1	0	Initial value	Access
Address:	0000001B <sub>H</sub>	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	XXXXXXXX <sub>B</sub>	R/W

PDRS		7	6	5	4	3	2	1	0	Initial value	Access
Address:	0000001C <sub>H</sub>	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	XXXXXXXX <sub>B</sub>	R/W

**Data Direction Register (DDR)**

DDR7	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000607 <sub>H</sub>	P77	P76	P75	P74	P73	P72	P71	P70	00000000 <sub>B</sub>	R/W
DDR8	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000608 <sub>H</sub>	P87	P86	P85	P84	P83	P82	P81	P80	00000000 <sub>B</sub>	R/W
DDR9	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000609 <sub>H</sub>	P97	P96	P95	P94	P93	P92	P91	P90	00000000 <sub>B</sub>	R/W
DDRB	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000600B <sub>H</sub>	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000 <sub>B</sub>	R/W
DDRG	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000400 <sub>H</sub>	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	00000000 <sub>B</sub>	R/W
DDRH	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000401 <sub>H</sub>	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000 <sub>B</sub>	R/W
DDRI	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000402 <sub>H</sub>	—	—	—	—	PI3	—	—	—	--- 0 --- <sub>B</sub>	R/W
DDRJ	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000403 <sub>H</sub>	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000 <sub>B</sub>	R/W
DDRK	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000404 <sub>H</sub>	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000 <sub>B</sub>	R/W
DDRL	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000405 <sub>H</sub>	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000 <sub>B</sub>	R/W
DDRM	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000406 <sub>H</sub>	—	—	—	—	PM3	PM2	PM1	PM0	--- 0000 <sub>B</sub>	R/W
DDRN	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000407 <sub>H</sub>	—	—	PN5	PN4	PN3	PN2	PN1	PN0	--000000 <sub>B</sub>	R/W
DDRO	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000408 <sub>H</sub>	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000 <sub>B</sub>	R/W

*(Continued)*

(Continued)

DDRP	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000409 <sub>H</sub>	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	00000000 <sub>B</sub>	R/W
DDRQ	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000040A <sub>H</sub>	—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0	--000000 <sub>B</sub>	R/W
DDRR	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000040B <sub>H</sub>	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	00000000 <sub>B</sub>	R/W
DDRS	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000040C <sub>H</sub>	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	00000000 <sub>B</sub>	R/W

**Port Function Registers (PFR)**

PFR7	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000617 <sub>H</sub>	P77	P76	P75	P74	P73	P72	P71	P70	00001111 <sub>B</sub>	R/W
PFR8	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000618 <sub>H</sub>	P87	P86	P85	P84	P83	P82	—	—	111110 -- <sub>B</sub>	R/W
PFR9	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000619 <sub>H</sub>	P97	P96	P95	P94	P93	P92	P91	P90	11110101 <sub>B</sub>	R/W
PFRB	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000061B <sub>H</sub>	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000 <sub>B</sub>	R/W
PFR27	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000627 <sub>H</sub>	P277	P276	P275	P274	P273	P272	P271	P270	1111 -00 - <sub>B</sub>	R/W
PFRG	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000410 <sub>H</sub>	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	00000000 <sub>B</sub>	R/W
PFRH	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000411 <sub>H</sub>	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000 <sub>B</sub>	R/W
PFR I	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000412 <sub>H</sub>	—	—	—	—	PI3	—	—	—	----0 --- <sub>B</sub>	R/W
PFRJ	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000413 <sub>H</sub>	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000 <sub>B</sub>	R/W
PFRK	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000414 <sub>H</sub>	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000 <sub>B</sub>	R/W
PFR L	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000415 <sub>H</sub>	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000 <sub>B</sub>	R/W
PFRM	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000416 <sub>H</sub>	—	—	—	—	PM3	PM2	PM1	PM0	---- 0000 <sub>B</sub>	R/W
PFRN	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000417 <sub>H</sub>	—	—	PN5	PN4	PN3	PN2	PN1	PN0	-- 000000 <sub>B</sub>	R/W

*(Continued)*

(Continued)

	PFRQ	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000418 <sub>H</sub>		PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000 <sub>B</sub>	R/W

	PFRP	7	6	5	4	3	2	1	0	Initial value	Access
Address: 00000419 <sub>H</sub>		PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	00000000 <sub>B</sub>	R/W

	PFRQ	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000041A <sub>H</sub>		—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0	-- 000000 <sub>B</sub>	R/W

	PFRR	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000041B <sub>H</sub>		PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	00000000 <sub>B</sub>	R/W

	PFRS	7	6	5	4	3	2	1	0	Initial value	Access
Address: 0000041C <sub>H</sub>		PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	00000000 <sub>B</sub>	R/W

## 12.4 DMA Controller (DMAC)

The DMAC module is used to implement direct memory access (DMA) transfer in FR50 family devices.

In a DMA transfer controlled by this module, various types of data can be transferred at high speed without involving the CPU, thus increasing system performance.

### 12.4.1 Hardware Configuration

The following are the main components of the DMAC module:

- Five independent DMA channels
- 5-channel independent access control circuit
- 32-bit address registers (Reload can be specified: Two registers for each channel.)
- 16-bit transfer count registers (Reload can be specified: One register for each channel.)
- 4-bit block count registers (One register for each channel)
- External transfer request input pins DREQ0, DREQ1, and DREQ2 (only ch0, ch1, and ch2)
- External transfer request acceptance output pins DACK0, DACK1, and DACK2 (only ch0, ch1, and ch2)
- DMA termination output pins DEOP0, DEOP1, and DEOP2 (only ch0, ch1, and ch2)
- Two-cycle transfer

### 12.4.2 Main Functions

The following are the main functions of data transfer performed by the module:

- Independent data transfer in multiple channels is enabled (5 channels).
  - a: Priority (ch0 > ch1 > ch2 > ch3 > ch4)
  - b: Priority can be alternated between ch0 and ch1.
  - c: DMAC start cause
    - External-only pin input (edge detection/level detection channels 0 to 2 only)
    - Internal peripheral request (interrupt request is shared, including external interrupts)
    - Software request (register write)
  - d: Transfer mode
    - Demand transfer, burst transfer, step transfer, block transfer
    - Addressing mode 32-bit full address specification (increase, decrease, fixed)  
(An address increment/decrement size of -255 to +255 can be specified.)
    - Data types of byte, halfword, and word lengths
    - Single-shot/reload selectable

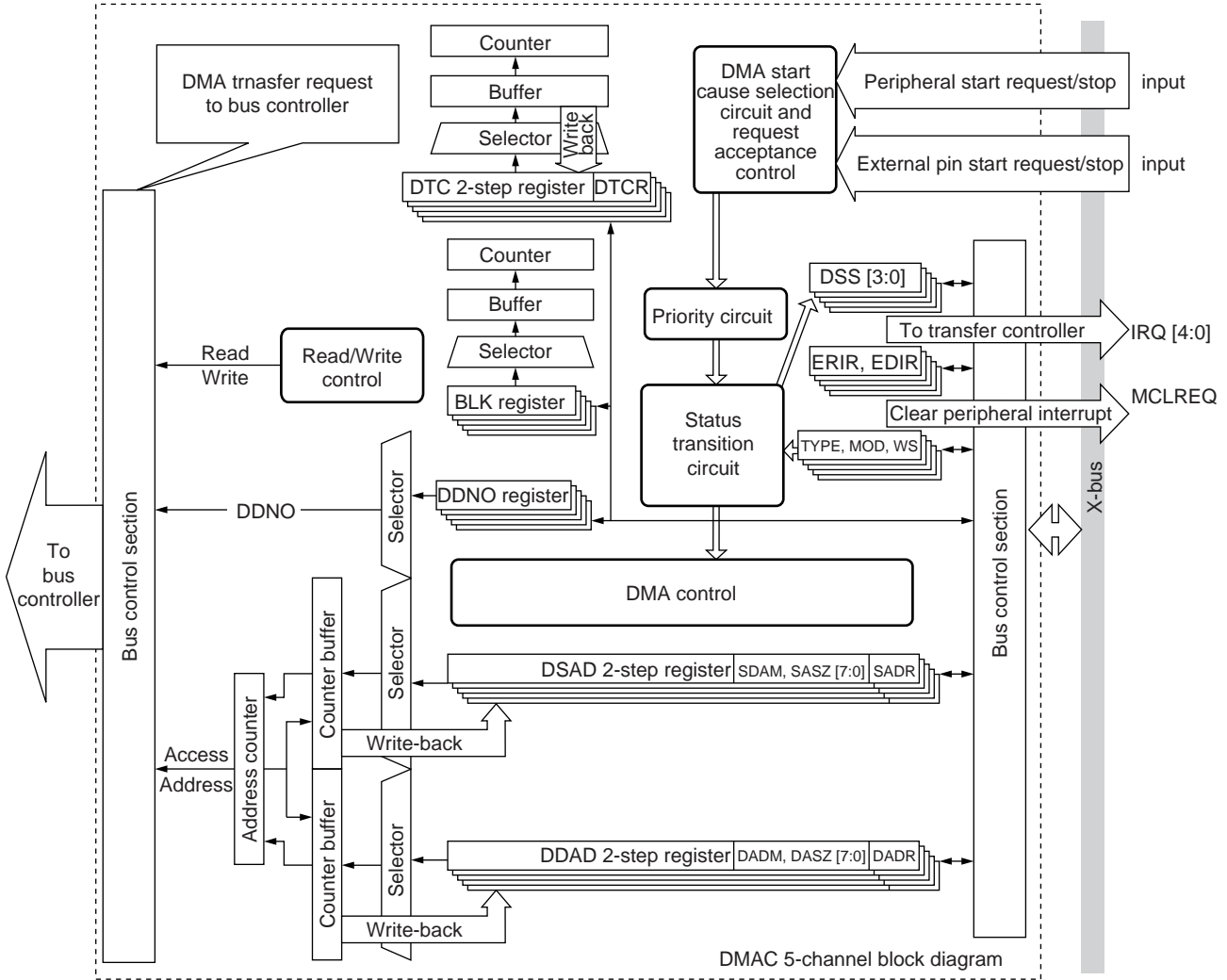


12.4.3 Registers Configuration

Channel 0 control/status register A	DMACA0 0000200H	<input type="text"/>
Channel 0 control/status register B	DMACB0 0000204H	<input type="text"/>
Channel 1 control/status register A	DMACA1 0000208H	<input type="text"/>
Channel 1 control/status register B	DMACB1 000020CH	<input type="text"/>
Channel 2 control/status register A	DMACA2 0000210H	<input type="text"/>
Channel 2 control/status register B	DMACB2 0000214H	<input type="text"/>
Channel 3 control/status register A	DMACA3 0000218H	<input type="text"/>
Channel 3 control/status register B	DMACB3 000021CH	<input type="text"/>
Channel 4 control/status register A	DMACA4 0000220H	<input type="text"/>
Channel 4 control/status register B	DMACB4 0000224H	<input type="text"/>
Overall control register	DMACR 0000240H	<input type="text"/>

Channel 0 transfer source address register	DMASA0 0001000H	<input type="text"/>
Channel 0 transfer destination address register	DMADA0 0001004H	<input type="text"/>
Channel 1 transfer source address register	DMASA1 0001008H	<input type="text"/>
Channel 1 transfer destination address register	DMADA1 000100CH	<input type="text"/>
Channel 2 transfer source address register	DMASA2 0001010H	<input type="text"/>
Channel 2 transfer destination address register	DMADA2 0001014H	<input type="text"/>
Channel 3 transfer source address register	DMASA3 0001018H	<input type="text"/>
Channel 3 transfer destination address register	DMADA3 000101CH	<input type="text"/>
Channel 4 transfer source address register	DMASA4 0001020H	<input type="text"/>
Channel 4 transfer destination address register	DMADA4 0001024H	<input type="text"/>

12.4.4 Block Diagram



## 12.5 UART

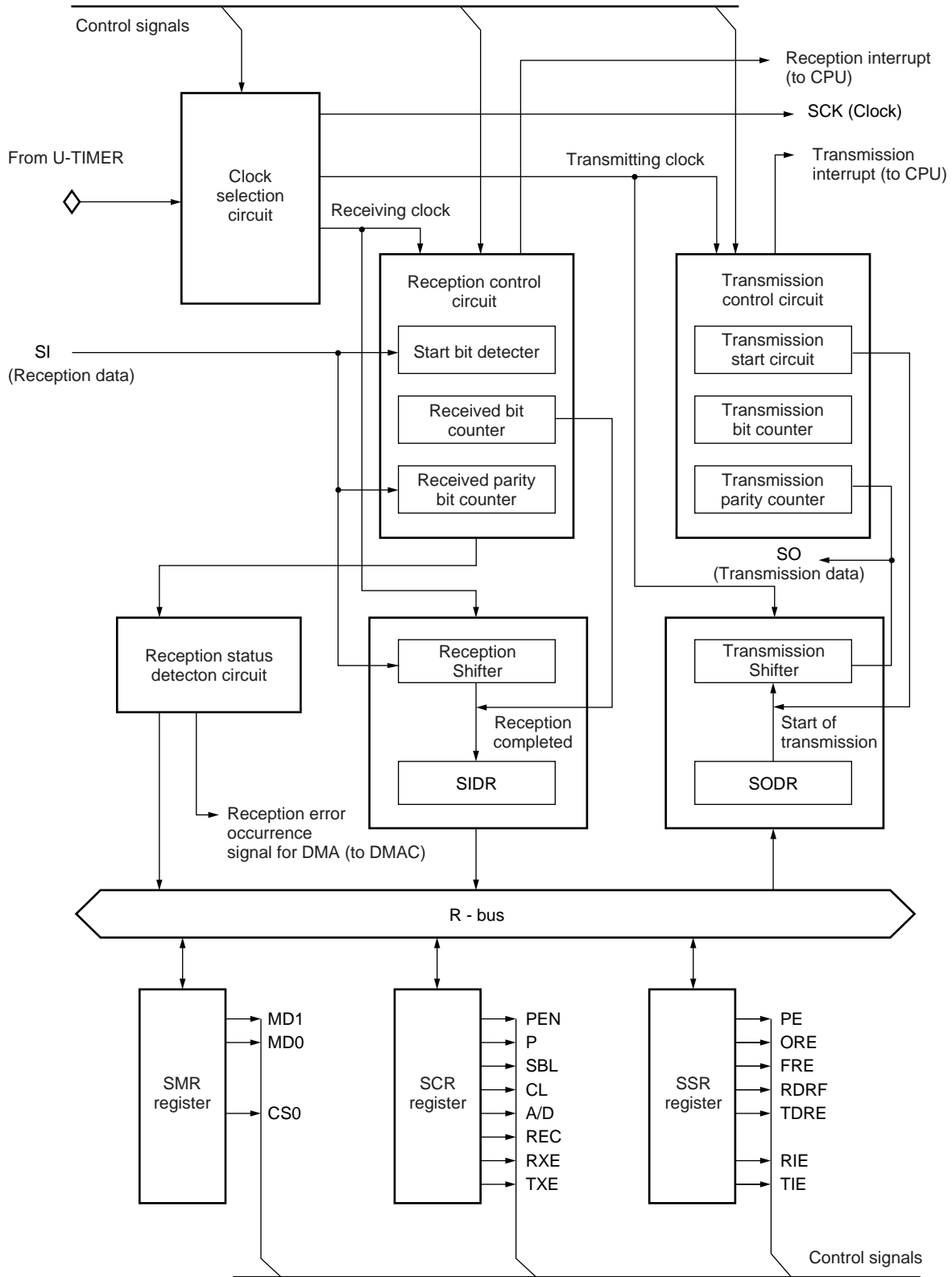
The UART is a serial I/O port for performing asynchronous (stop-start synchronization) communications. The CY91360G series contains three UART channels.

### 12.5.1 Features

- Full-duplex, double buffering
- Supports asynchronous (stop-start synchronization) communications
- Supports multi-processor mode
- Fully programmable baud rate  
The baud rate can be set using an internal timer. (See the U-TIMER section.)
- Supports flexible baud rate setting using an external clock
- Error detection function (parity, framing, overrun)
- Non return to zero (NRZ) transfer signal
- Supports DMA transfer activation using an interrupt



12.5.3 Block Diagram

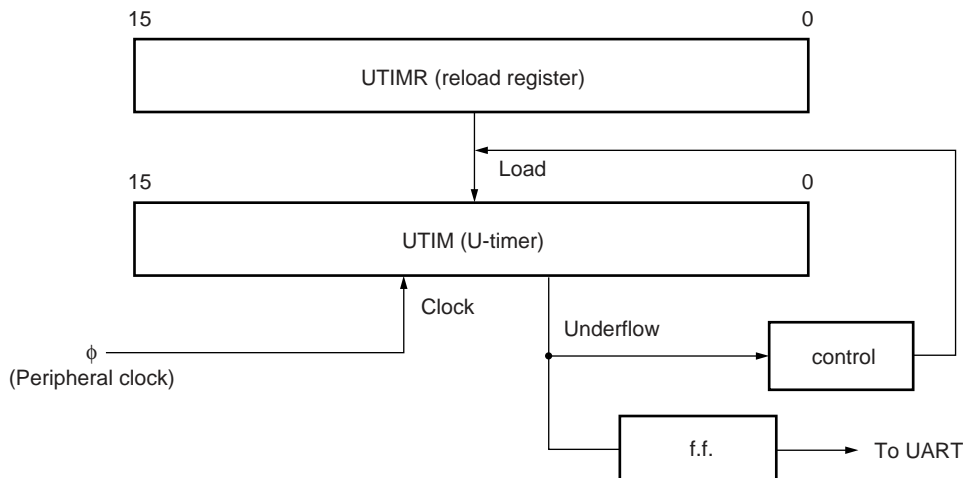


### 12.6 U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-timer (U-TIMER) is a 16-bit timer used to generate the baud rate for the UART. The operating frequency of the chip and the U-TIMER reload value can be combined to set a user-defined baud rate.

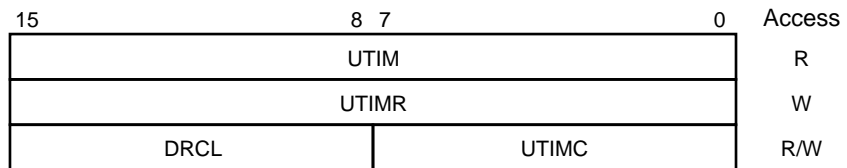
The CY91360G series contains three U-TIMER channels. The intervaltimers can count for a maximum of  $216 \times \phi$ .

#### 12.6.1 Block Diagram



#### 12.6.2 Register Configuration

Register structure



R : Read,  
W : Write

UTIM	Address	Bits	15	14	.....	2	1	0	Initial value	Access
ch0	00000068 <sub>H</sub>		b15	b14		b2	b1	b0	0	R
ch1	00000074 <sub>H</sub>									
ch2	00000080 <sub>H</sub>									

UTIMR Reload Register

UTIMR	Address	Bits	15	14	.....	2	1	0	Initial value	Access
ch0	00000068 <sub>H</sub>		b15	b14		b2	b1	b0	0	W
ch1	00000074 <sub>H</sub>									
ch2	00000080 <sub>H</sub>									

UTIMC U Timer Control Register

UTIMC	Address	7	6	5	4	3	2	1	0	Initial value	Access
ch0	0000006B <sub>H</sub>	UCC1	—	—	—	UNDR	Reserved	UTST	UTCR	0---0001	R/W
ch1	00000077 <sub>H</sub>										
ch2	00000083 <sub>H</sub>										

## 12.7 PWM Timer

The PWM (Pulse Width Modulation) timer can output high-precision pulse waves at an arbitrary cycle and pulse width (duty ratio).

The CY91360G series contains eight PWM timer channels. Each of the channels consists of a 16-bit down-counter, cycle setting register, duty setting register, and pin controller.

The control status register for each channel is used to indicate the operation status of the PWM timer. General control registers 1 and 2 are common registers shared by four channels, serving for input and software triggering.

### 12.7.1 Features

- The count clock for the 16-bit down-counter can be selected from among the following four types:  
Internal clocks:  $\phi$ ,  $\phi/4$ ,  $\phi/16$ ,  $\phi/64$  ( $\phi$ : Machine clock for peripherals)
- The counter can be initialized to “FFFFH” by a reset or underflow.  
The 16-bit down-counter causes an underflow when it changes from “0000H” to “FFFFH”.
- Each channel has PWM outputs.  
Eight channels: Eight output pins
- Registers
  - Cycle setting register: Data reload register with buffer  
Data transfer from the buffer is performed either when an activation trigger is detected or when the down-counter causes an underflow (cycle match). The output is inverted at a cycle match.
  - Duty setting register: Compare register with buffer.  
The value set in this register is compared to the counter value. The output is inverted when the values match (duty match).
- Pin control
  - A duty match causes a reset to “1” (given priority).
  - An underflow causes a reset to “0”.
  - The output value fix mode enables output of all “L” or all “H”.
  - The polarity can also be specified.
- Interrupt requests can be generated by selecting the following interrupt sources:
  - Activation of the PWM timer (software trigger or trigger input)
  - Occurrence of an underflow (cycle match)
  - Occurrence of a duty match
  - Occurrence of an underflow (cycle match) or duty match
- You can set simultaneous activation of two or more channels using software or another interval timer. You can also set restarting the PWM timer during operation.

### 12.7.2 Register Configuration for ch 0 to ch 3

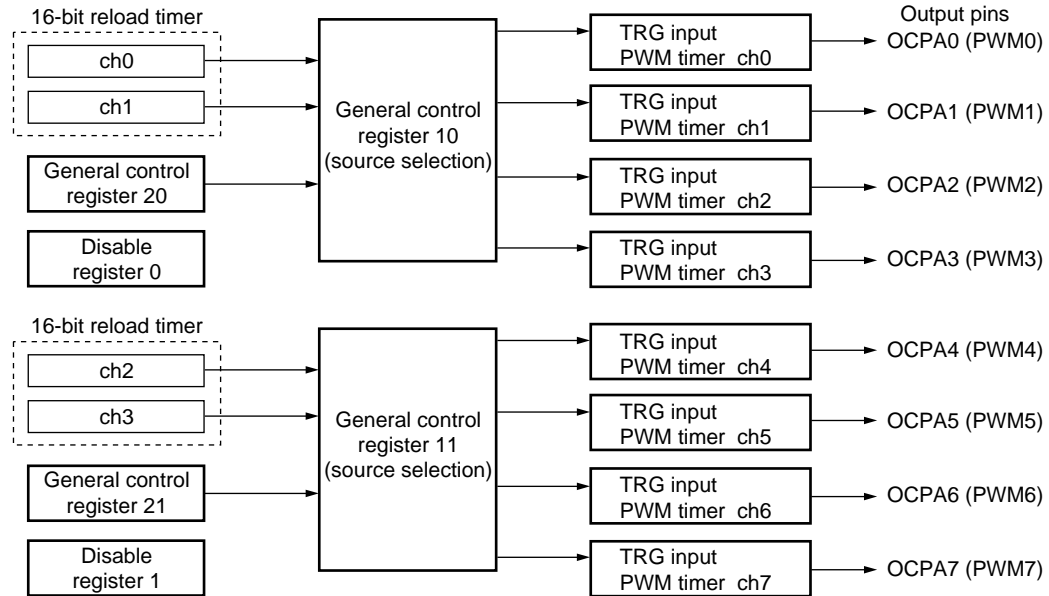
Address	Bits		Access	Register name
	15	8 7 0		
00000118H	GCN10		R/W	General control register 10
0000011AH	PDBL0	GCN20	R/W	Disable/General control register 20
-----				
PWM timer ch 0				
00000120H	PTMR0		R	ch0 timer register
00000122H	PCSR0		W	ch0 cycle setting register
00000124H	PDUT0		W	ch0 duty setting register
00000126H	PCNH0	PCNL0	R/W	ch0 control status registers
-----				
PWM timer ch 1				
00000128H	PTMR1		R	ch1 timer register
0000012AH	PCSR1		W	ch1 cycle setting register
0000012CH	PDUT1		W	ch1 duty setting register
0000012EH	PCNH1	PCNL1	R/W	ch1 control status registers
-----				
PWM timer ch 2				
00000130H	PTMR2		R	ch2 timer register
00000132H	PCSR2		W	ch2 cycle setting register
00000134H	PDUT2		W	ch2 duty setting register
00000136H	PCNH2	PCNL2	R/W	ch2 control status registers
-----				
PWM timer ch 3				
00000138H	PTMR3		R	ch3 timer register
0000013AH	PCSR3		W	ch3 cycle setting register
0000013CH	PDUT3		W	ch3 duty setting register
0000013EH	PCNH3	PCNL3	R/W	ch3 control status registers



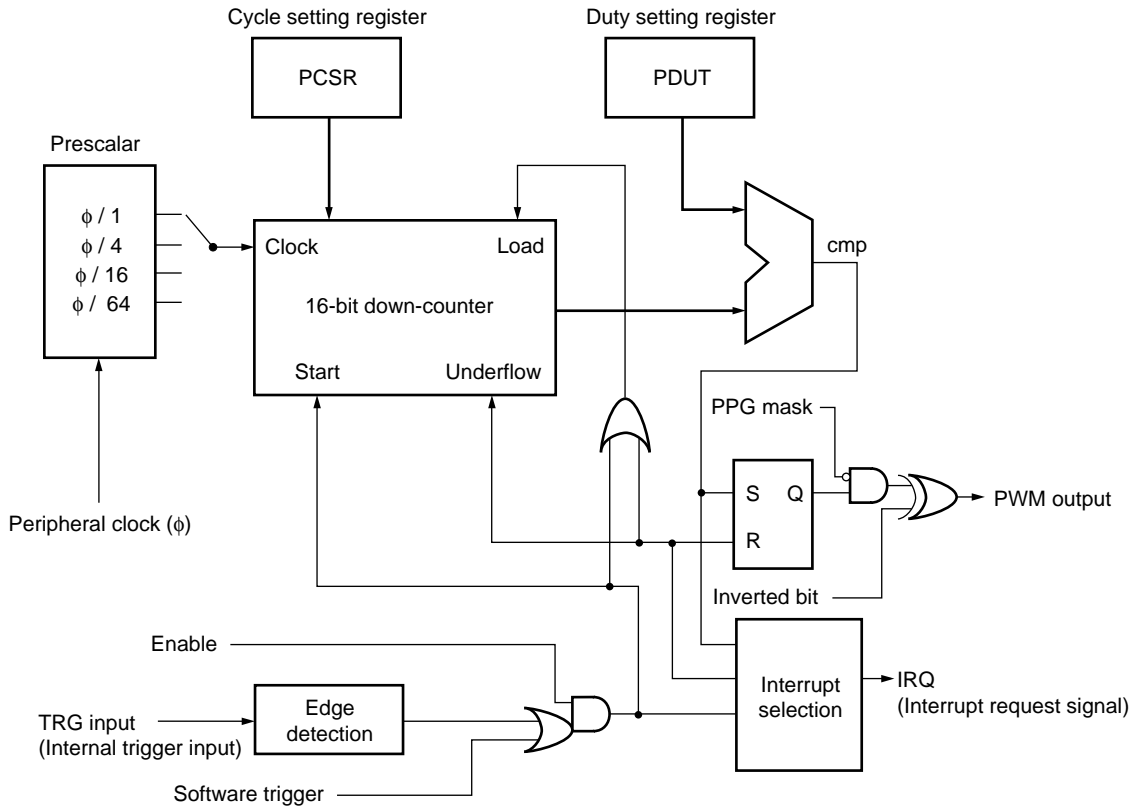
### 12.7.3 PWM Timer Registers for ch 4 to ch 7

Address	Bits		Access	Register name
	15	8 7 0		
0000011CH	GCN11		R/W	General control register 11
0000011EH	PDBL1	GCN21	R/W	Disable/General control register 21
-----				
PWM timer ch 4				
00000140H	PTMR4		R	ch4 timer register
00000142H	PCSR4		W	ch4 cycle setting register
00000144H	PDUT4		W	ch4 duty setting register
00000146H	PCNH4	PCNL4	R/W	ch4 control status registers
-----				
PWM timer ch 5				
00000148H	PTMR5		R	ch5 timer register
0000014AH	PCSR5		W	ch5 cycle setting register
0000014CH	PDUT5		W	ch5 duty setting register
0000014EH	PCNH5	PCNL5	R/W	ch5 control status registers
-----				
PWM timer ch 6				
00000150H	PTMR6		R	ch6 timer register
00000152H	PCSR6		W	ch6 cycle setting register
00000154H	PDUT6		W	ch6 duty setting register
00000156H	PCNH6	PCNL6	R/W	ch6 control status registers
-----				
PWM timer ch 7				
00000158H	PTMR7		R	ch7 timer register
0000015AH	PCSR7		W	ch7 cycle setting register
0000015CH	PDUT7		W	ch7 duty setting register
0000015EH	PCNH7	PCNL7	R/W	ch7 control status registers

12.7.4 Configuration Diagram of the Entire PWM Timer



12.7.5 Configuration Diagram of PWM Timer 1 ch



## 12.8 16-bit Reload Timer

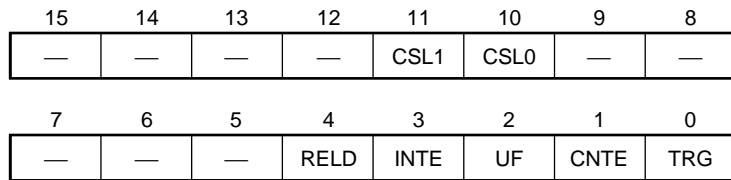
Each 16-bit reload timer consists of a 16-bit down-counter, a 16-bit reload register, a prescaler for generating the internal count clock, and a control register.

The 16-bit reload timer can also activate DMA transfer using interrupts.

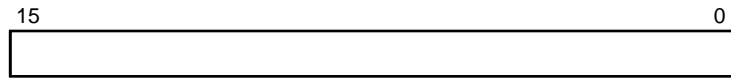
The CY91360G series contains six 16-bit reload timer channels.

### 12.8.1 16-bit Reload Timer Register Configuration

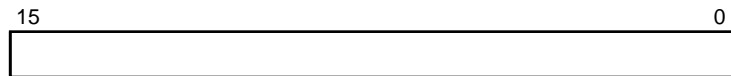
Control status register (TMCSR)



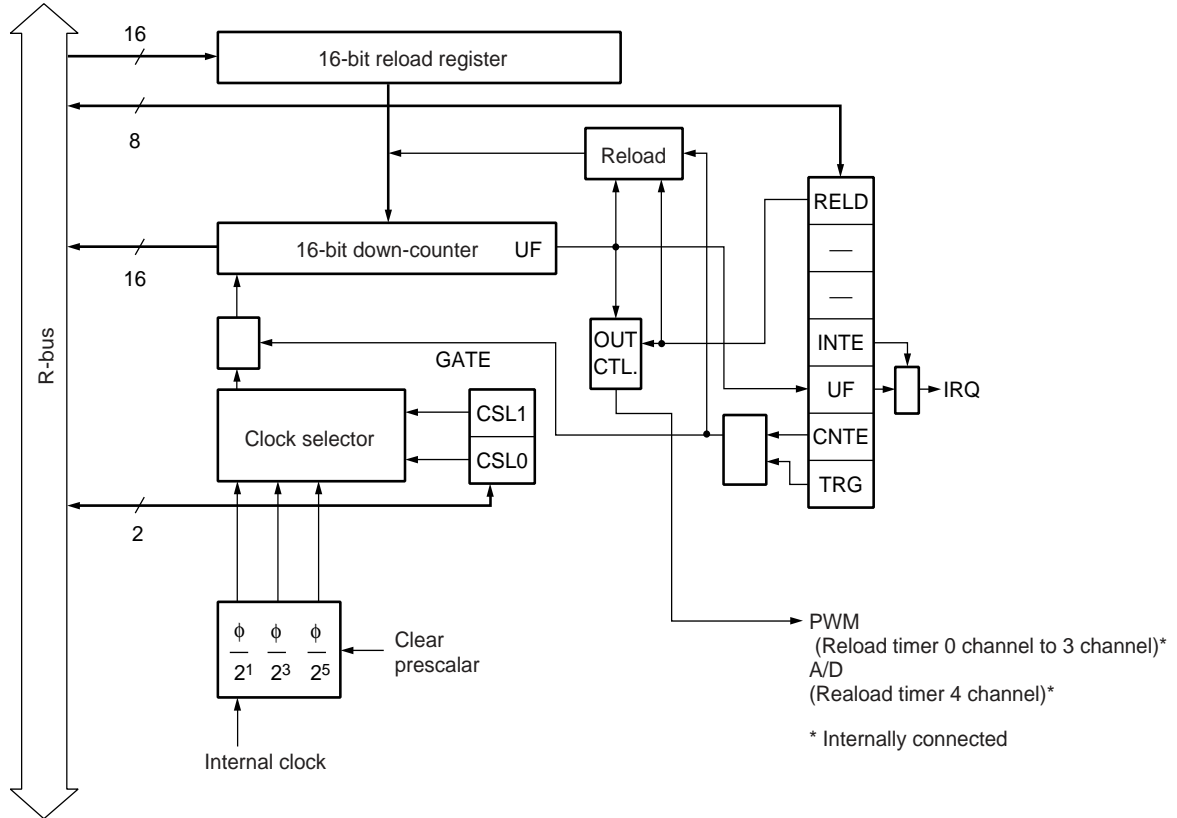
16-bit timer register (TMR)



16-bit reload register (TMRLR)



12.8.2 Block Diagram





## 12.9 Bit Search Module

The bit search module searches for a “0”, “1”, or change-point in the data written to the input register and returns the position of the detected bit.

This section describes the data register for detecting zeros (BSD0), data register for detecting ones (BSD1), data register for detecting change-points (BSDC), and detection result register (BSRR).

### a: Data register for detecting zeros (BSD0)

Address	31	Register structure	0	Initial value	Access
0000 03F0H				Indeterminate	W

### b: Data register for detecting ones (BSD1)

Address	31	Register structure	0	Initial value	Access
0000 03F4H				Indeterminate	R/W

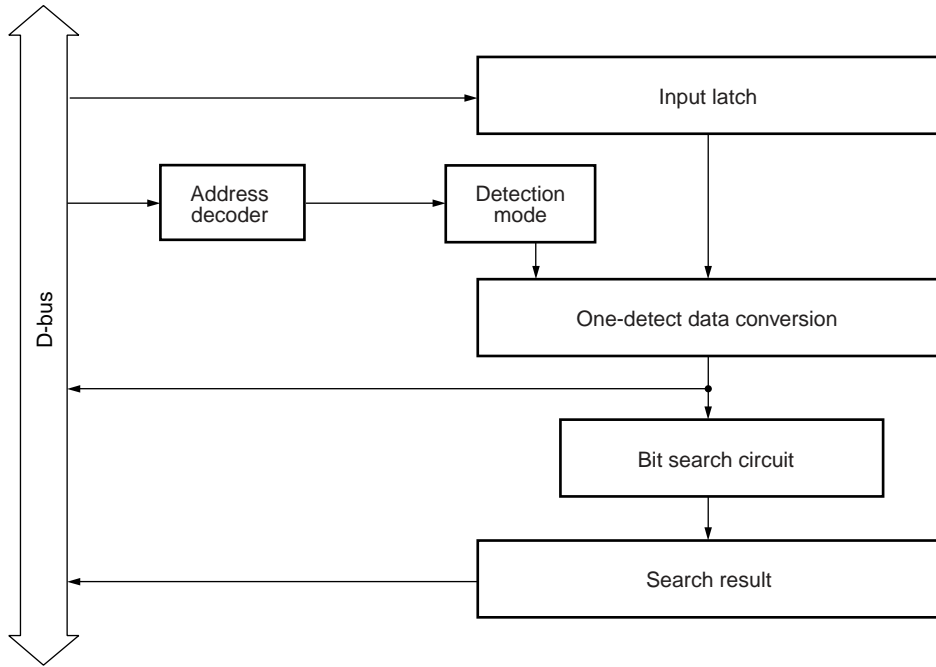
### c: Data register for detecting change points (BSDC)

Address	31	Register structure	0	Initial value	Access
0000 03F8H				Indeterminate	W

### d: Detection Result Register (BSRR)

Address	31	Register structure	0	Initial value	Access
0000 03FCH				Indeterminate	R

12.9.1 Block Diagram of the Bit Search Module



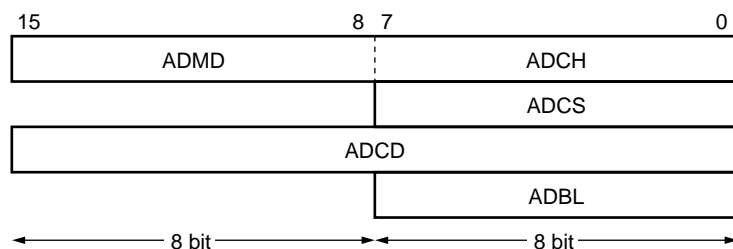
## 12.10 10-bit A/D Converter (Successive Approximation Conversion Type)

This section provides an overview of the A/D converter, describes the register structure and functions, and describes the operation of the A/D converter.

A/D Converter converts analog input voltage into digital values, and provides the following features.

- Conversion time: minimum 178 cycles (32 MHz: 5.6  $\mu$ s, 24 MHz: 7.4  $\mu$ s, 16 MHz: 11.2  $\mu$ s) per channel
- RC type successive approximation conversion with sample & hold circuit
- 10-bit resolution
- Program selection analog input from 16 channels
  - Single conversion mode: conversion of one selected channel
  - Scan conversion mode: continuous conversion of multiple channels, programmable for up to 16 channels
  - Single conversion mode: Convert the specified channel once only.
- Continuous mode: Repeatedly convert the specified channels.
- Stop mode: Convert one channel then temporarily halt until the next activation.  
(Enables synchronization of the conversion start timing.)
- A/D conversion can be followed by an A/D conversion interrupt request to CPU. This interrupt, an option that is ideal for continuous processing can be used to start a DMA transfer of the results of A/D conversion to memory.
- Startup may be by software, external trigger (falling edge) or timer (rising edge)





Channel setting register (ADCH)

bit	7	6	5	4	3	2	1	0
Address: 00009D <sub>H</sub>	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0

Mode register (ADMD)

bit	15	14	13	12	11	10	9	8
Address: 00009C <sub>H</sub>	—	—	—	—	MOD1	MOD0	STS1	STS0

Control status register (ADCS)

bit	7	6	5	4	3	2	1	0
Address: 00009F <sub>H</sub>	BUSY	INT	INTE	PAUS	—	—	STRT	Reserved

Data register (ADCD)

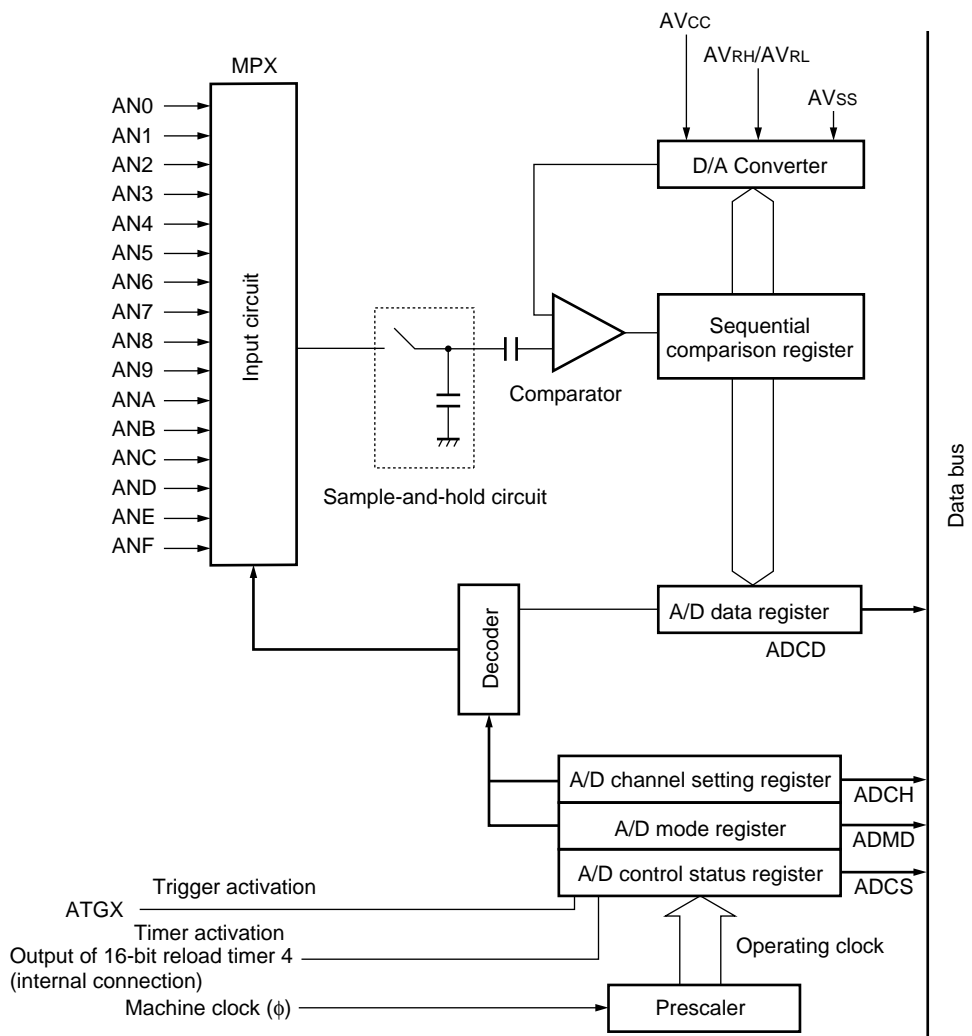
bit	7	6	5	4	3	2	1	0
Address: 0000A1 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0

bit	15	14	13	12	11	10	9	8
Address: 0000A0 <sub>H</sub>	—	—	—	—	—	—	D9	D8

Disable register (ADBL)

bit	15	14	13	12	11	10	9	8
Address: 0000A3 <sub>H</sub>	—	—	—	—	—	—	—	DBL

## 12.10.1 Block Diagram



## 12.11 Interrupt Controller

An interrupt controller controls interrupt acceptance and arbitration processing.

### Hardware Configuration

This module consists of the following:

- ICR register
- Interrupt priority evaluation circuit
- Interrupt level and interrupt number (vector) generator
- Hold request cancel request generator

### Major Functions

This module has the following major functions:

- Detecting an NMI request or interrupt request
- Priority evaluation (using the level or number)
- Transferring the level of the interrupt cause in the evaluation result (to the CPU)
- Transferring the number of the interrupt cause in the evaluation result (to the CPU)
- Instructing recovery from stop mode due to an NMI or interrupt level other than 11111 (to the CPU)
- Generating a hold request cancel request for the bus master

12.11.1 Register Configuration

	bit 7	6	5	4	3	2	1	0	
Address: 00000440H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00
Address: 00000441H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01
Address: 00000442H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02
Address: 00000443H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03
Address: 00000444H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04
Address: 00000445H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05
Address: 00000446H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06
Address: 00000447H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07
Address: 00000448H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08
Address: 00000449H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09
Address: 0000044AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10
Address: 0000044BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11
Address: 0000044CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12
Address: 0000044DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13
Address: 0000044EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14
Address: 0000044FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15
Address: 00000450H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16
Address: 00000451H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17
Address: 00000452H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18
Address: 00000453H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19
Address: 00000454H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20
Address: 00000455H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21
Address: 00000456H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22
Address: 00000457H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23
Address: 00000458H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24
Address: 00000459H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25
Address: 0000045AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26
Address: 0000045BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27
Address: 0000045CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28
Address: 0000045DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29
Address: 0000045EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30
Address: 0000045FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31
				R	R/W	R/W	R/W	R/W	

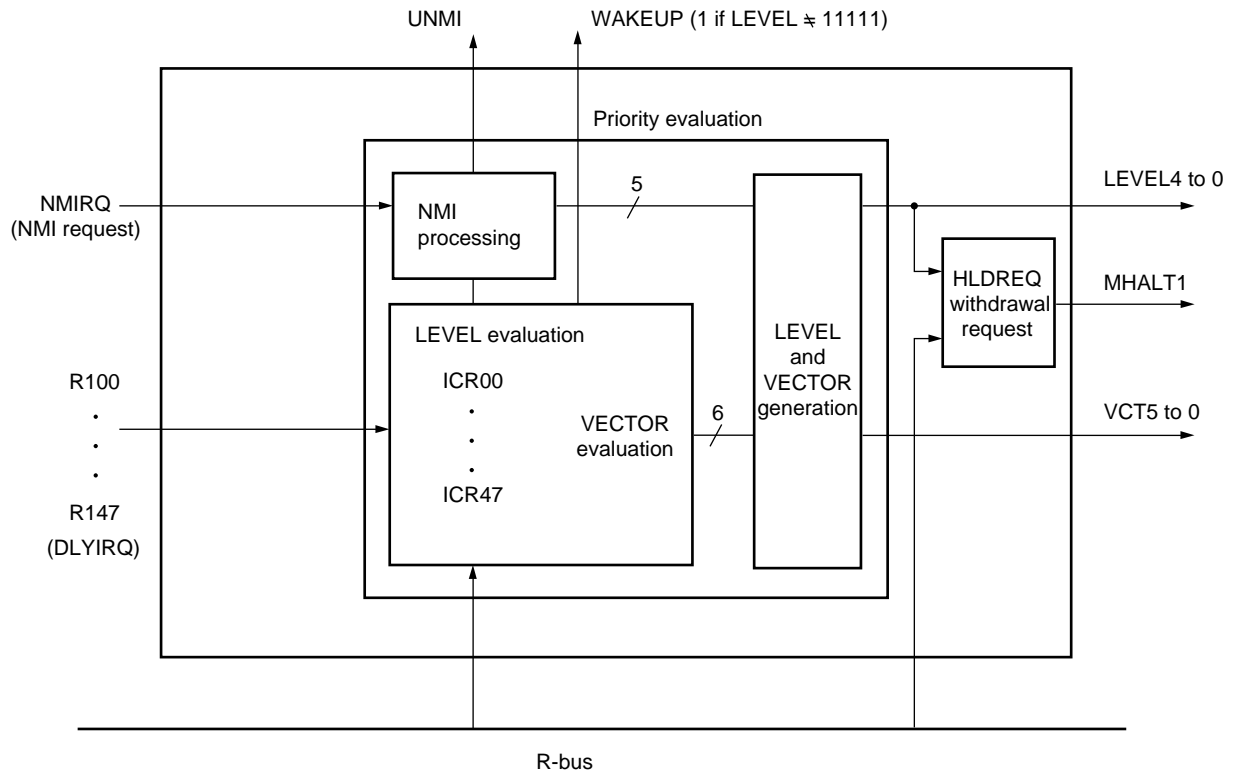
(Continued)

(Continued)

	bit 7	6	5	4	3	2	1	0	
Address: 00000460H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32
Address: 00000461H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33
Address: 00000462H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34
Address: 00000463H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35
Address: 00000464H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36
Address: 00000465H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37
Address: 00000466H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38
Address: 00000467H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39
Address: 00000468H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40
Address: 00000469H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41
Address: 0000046AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42
Address: 0000046BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43
Address: 0000046CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44
Address: 0000046DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45
Address: 0000046EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46
Address: 0000046FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47
				R	R/W	R/W	R/W	R/W	

Address: 00000045H	MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL
	R/W			R	R/W	R/W	R/W	R/W	

12.11.2 Block Diagram



## 12.12 External Interrupt/NMI Control Block

The external interrupt/NMI controller controls external interrupt requests input from the NMIX and INT0 to INT7 pins.

Detection of “H” levels, “L” levels, rising edges, or falling edges can be selected (except for the NMI).

The external interrupt/NMI controller can also be used for DMA requests.

This section lists the registers of the controller and provides its block diagram.

### 12.12.1 Register Configuration of the External Interrupt NMI Controller

External interruption permission register (ENIR)

Bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interruption factors register (EIRR)

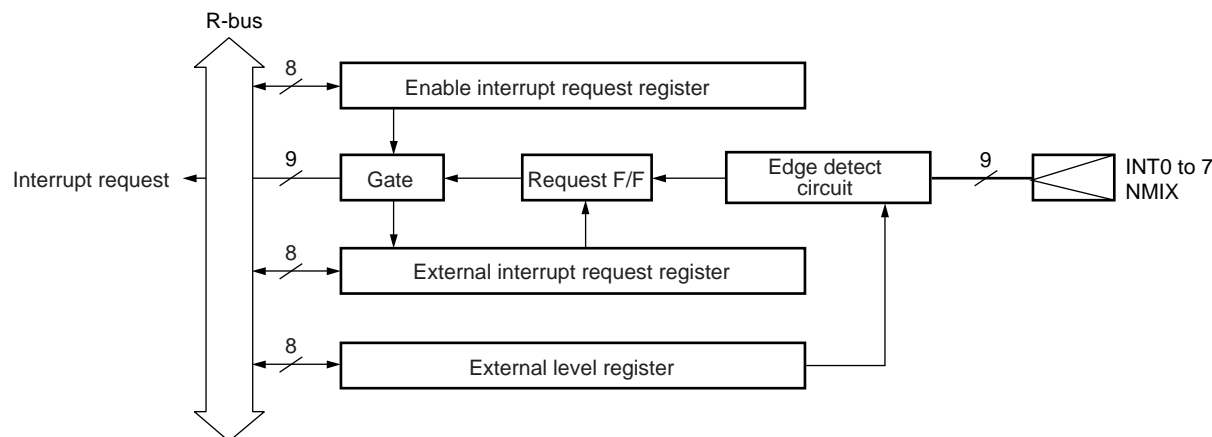
Bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

Request level setting register (ELVR)

Bit	15	14	13	12	11	10	9	8
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

Bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

### 12.12.2 Block Diagram





### 12.13 Delayed Interrupt

#### 12.13.1 Delayed interrupt control register (DICR)

The delayed interrupt control register (DICR) is a delayed interrupt generator register and is used to generate the task switching interrupt.

#### Structure of the DICR

Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000044H		—	—	—	—	—	—	—	DLYI	----- 0
									R/W	← Access

### 12.14 Clock Generation

The CY91360G series generates internal operating clocks as follows:

- Base clock generation: Device scales clock source input by 2 (X clock) or oscillates base clock with PLL to generate basic clock (PLL clock)
- Generation of each internal clock: Device scales base clock to generate clocks supplied to each block

Generation and control of each clock are explained below.

Some devices allow the operation of the RTC module based on a separate 32 kHz subclock. See the section “27. Subclock” for more details.

#### 12.14.1 Register Configuration

#### RSRR: Reset source register, Watchdog timer control register

	bit	15	14	13	12	11	10	9	8
address: 00000480H		INIT	HSTB	WDOG	ERST	SRST	—	WT1	WT0
access		R	R	R	R	R	—	R/W	R/W
Initial Value (INITX)		1	0	0	0	0	—	0	0
Initial Value (INIT)		*	*	*	X	X	—	0	0
Initial Value (RST)		X	X	X	*	*	—	0	0
After Boot ROM **		0	0	0	0	0	0	0	0

\*: varies with reset factor

x: not initialized

\*\*: After execution of the program in the internal boot ROM the reset source is visible

#### STCR: Standby control register

	bit	7	6	5	4	3	2	1	0
address: 00000481H		STOP	SLEEP	HIZ	SRST	OS1	OS0	OSCD2	OSCD1
access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INITX)		0	0	1	1	0	0	1	1
Initial Value (HSTX) *		0	0	1	1	1	1	1	1
Initial Value (INIT)		0	0	1	1	X	X	1	1
Initial Value (RST)		0	0	X	1	X	X	X	X

\*: Valid only when this initialization is performed simultaneously with initialization by INITX: others same as INIT.

(Continued)



**TBCR: Time-based counter control register**

bit	15	14	13	12	11	10	9	8
address: 00000482 <sub>H</sub>	TBIF	TBIE	TBC2	TBC1	TBC0	—	SYNCR	SYNCS
Initial Value (INIT)	0	0	X	X	X	X	0	0
Initial Value (RST)	0	0	X	X	X	X	X	X
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**CTBR: Time-based counter clear register**

bit	7	6	5	4	3	2	1	0
address: 00000483 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value (INIT)	X	X	X	X	X	X	X	X
Initial Value (RST)	X	X	X	X	X	X	X	X
	W	W	W	W	W	W	W	W

**CLKR: Clock source control register**

bit	15	14	13	12	11	10	9	8
address: 00000484 <sub>H</sub>	PLL2S0	PLL1S2	PLL1S1	PLL1S0	PLL2EN	PLL1EN	CLKS1	CLKS0
Initial Value (INIT)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (RST)	0	0	0	0	0	0	0	0
	X	X	X	X	X	X	X	X

**WPR Watchdog reset generation postponement register**

bit	7	6	5	4	3	2	1	0
address: 00000485 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value (INIT)	W	W	W	W	W	W	W	W
Initial Value (RST)	X	X	X	X	X	X	X	X
	X	X	X	X	X	X	X	X

**DIVR0: Base clock division setting register 0**

bit	7	6	5	4	3	2	1	0
address: 00000486 <sub>H</sub>	B3	B2	B1	B0	P3	P2	P1	P0
Initial Value (INIT)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (RST)	0	0	0	0	0	0	1	1
	X	X	X	X	X	X	X	X

**DIVR1: Base clock division setting register 1**

bit	7	6	5	4	3	2	1	0
address: 00000487 <sub>H</sub>	T3	T2	T1	T0	S3	S2	S1	S0
Initial Value (INIT)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (RST)	0	0	0	0	0	0	0	0
	X	X	X	X	X	X	X	X

*(Continued)*

(Continued)

**CMCR: Clock control for CAN modules**

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	initial
0164H	PRE7	PRE6	PRE5	PRE4	PRE3	PRE2	PRE1	PRE0	11111111
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	1	1	1	1	1	1	1	1	

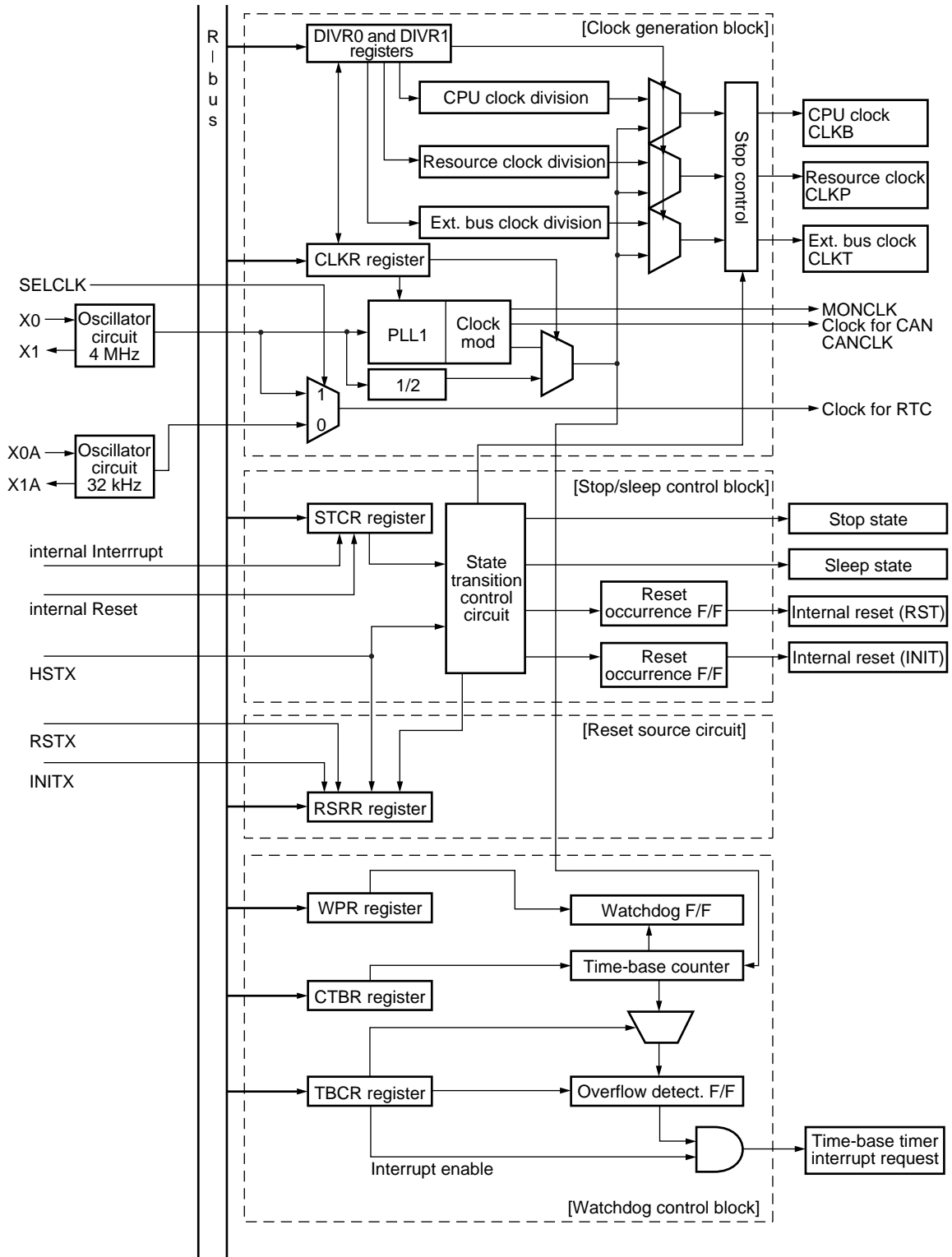
address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	initial
0165H	PRES	CDSELE	IRNG	CAL	MSEL	MTST	SCLK	MSRT	00000000
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

**Subclock RTC32 (CLKR2)**

This register is used to control the RTC32 mode bit for use in subclock system.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
000046H	—	—	—	—	—	—	—	RTC32
access	—	—	—	—	—	R/W	R/W	R/W
initial value	—	—	—	—	—	0	0	0

12.14.2 Block Diagram



### 12.15 Bus Interface

The external bus interface controls the interfaces with the external memory and external I/Os.

- Up to 32-bit (4 GB) address output.
- Up to eight independent banks provided by chip-select function
  - The banks can be set in 64-KB (minimum) at any position in the logic address space.
  - Can be set to no area
- 32/16/8 bit bus width setup can be performed for each chip-select area.
- Programmable automatic memory wait (up to 7 cycles) insertion
- Unused address/data pins can be used as I/O ports. (But see notes below)

Note: Chip Select Area CS7 is used for the internal CAN modules. The necessary register settings are done by an internal boot routine. Take care not to overwrite register bits related to this CS area.  
If the CAN macros which are connected internally to the external bus (also called User Logic Bus) are used, a certain number of data, address and control ports of the external bus interface cannot be configured as general purpose I/O ports.

#### 12.15.1 Register Configuration

##### Area select registers (ASR0 to ASR7)

Register	15	14	13	12	...	2	1	0	Initial value	Access
ASR0 00000640 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST 0000 <sub>H</sub>	W
ASR1 00000644 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W
ASR2 00000648 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W
ASR3 0000064C <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W
ASR4 0000650 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W
ASR5 00000654 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W
ASR6 00000658 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W
ASR7 0000065C <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT 0000 <sub>H</sub> RST XXXX <sub>H</sub>	W

Note: After execution of the code in the initial boot ROM ASR0 is set to "0x20", and ASR7 to "0x10".

*(Continued)*

(Continued)

**Area mask register (AMR0 to AMR7)**

Register	15	14	13	12	...	2	1	0	Initial value	Access
AMR0 00000642 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST FFFF <sub>H</sub> FFFF <sub>H</sub>	W
AMR1 00000646 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W
AMR2 0000064A <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W
AMR3 0000064E <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W
AMR4 00000652 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W
AMR5 00000656 <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W
AMR6 0000065A <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W
AMR7 0000065E <sub>H</sub>	A31	A30	A29	...	...	A18	A17	A16	INIT RST 0000 <sub>H</sub> XXXX <sub>H</sub>	W

**Area mode registers (AMD0 to AMD7)**

00000660 <sub>H</sub>	—	—	RDYE	BW1	BW0	WTC2	WTC1	WTC0	INIT	RST	R/W
00000661 <sub>H</sub>									-000111 <sub>B</sub>	-00XX111 <sub>B</sub>	
00000662 <sub>H</sub>									-000000 <sub>B</sub>	-XXXXXXX <sub>B</sub>	
to									--00000 <sub>B</sub>	--XXXXXX <sub>B</sub>	
00000667 <sub>H</sub>									to	to	

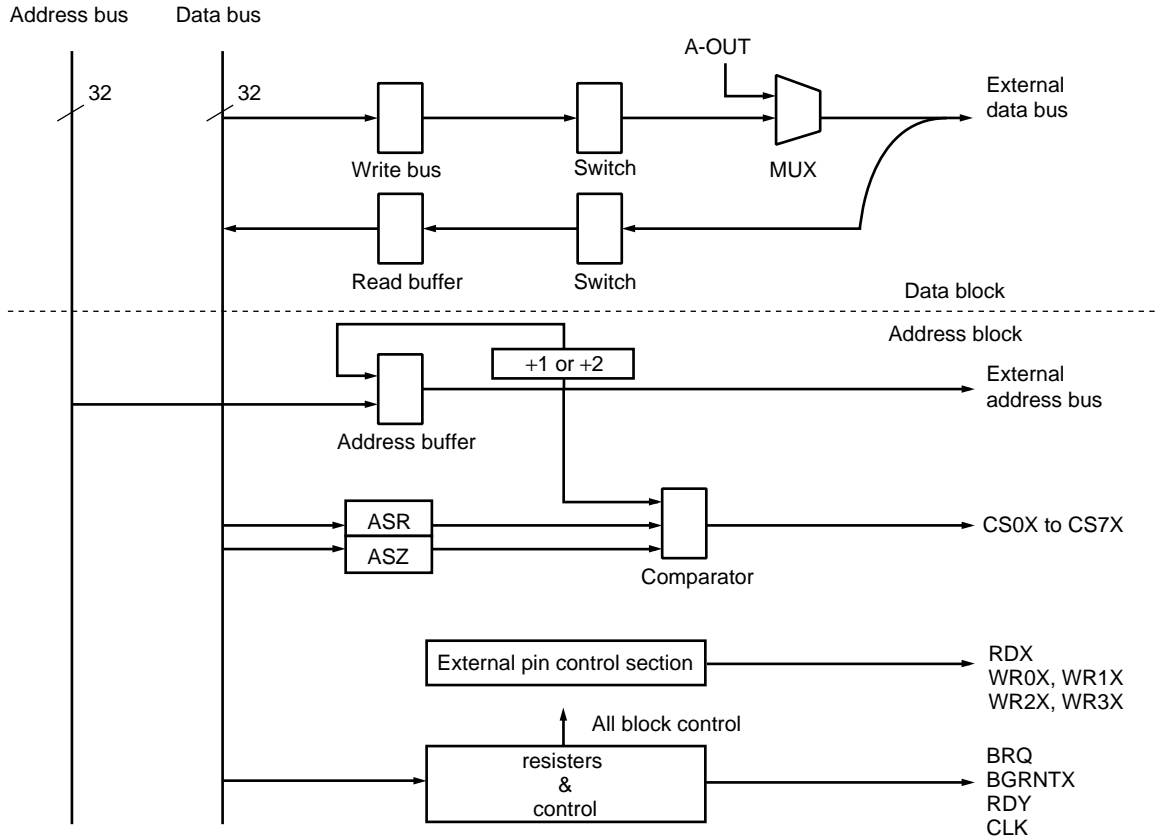
**CHE (CaChE Enable register)**

00000670 <sub>H</sub>	CHE7	CHE6	CHE5	CHE4	CHE3	CHE2	CHE1	CHE0	11111111 <sub>B</sub>	R/W
-----------------------	------	------	------	------	------	------	------	------	-----------------------	-----

**CSE (Chip Select Enable register)**

00000668 <sub>H</sub>	CSE7	CSE6	CSE5	CSE4	CSE3	CSE2	CSE1	CSE0	00000001 <sub>B</sub>	R/W
-----------------------	------	------	------	------	------	------	------	------	-----------------------	-----

12.15.2 Block Diagram



## 12.16 CAN Controller

This section provides an overview of the CAN Interface, describes the register structure and functions, and describes the operation of the CAN Interface.

The CAN controller is a module built into a CY91360G series. The CAN (Controller Area Network) is the standard protocol for serial communication between automobile controllers and is widely used in industrial applications.

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Supports full-bit comparison, full-bit mask and partial bit mask filtering.
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbits/s to 1 Mbits/s (when input clock is at 16 MHz)

The following sections only describe CAN 0. For the addresses of the registers of the other CAN channels see the I/O map. The address shown assume that the CS7 area is defined as described in the chapter about the internal Boot ROM.

### 12.16.1 List of Control Registers

**Table 12-1. List of Control Registers**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN0</b>				
10000H	Message buffer valid register	BVALR0	R/W	00000000 00000000
10001H				
10002H	Transmit request register	TREQR0	R/W	00000000 00000000
10003H				
10004H	Transmit cancel register	TCANR0	W	00000000 00000000
10005H				
10006H	Transmit complete register	TCR0	R/W	00000000 00000000
10007H				
10008H	Receive complete register	RCR0	R/W	00000000 00000000
10009H				
1000AH	Remote request receiving register	RRTRR0	R/W	00000000 00000000
1000BH				
1000CH	Receive overrun register	ROVRR0	R/W	00000000 00000000
1000DH				
1000EH	Receive interrupt enable register	RIER0	R/W	00000000 00000000
1000FH				
10010H	Control status register	CSR0	R/W, R	00 --- 000 0 ---- 0 - 1
10011H				
10012H	Last event indicator register	LEIR0	R/W	----- 000 - 0000
10013H				

**Table 12-1. List of Control Registers (continued)**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN0</b>				
100014 <sub>H</sub>	Receive/transmit error counter	RTEC0	R	00000000 00000000
100015 <sub>H</sub>				
100016 <sub>H</sub>	Bit timing register	BTR0	R/W	-1111111 11111111
100017 <sub>H</sub>				
100018 <sub>H</sub>	IDE register	IDER0	R/W	XXXXXXXX XXXXXXXXXX
100019 <sub>H</sub>				
10001A <sub>H</sub>	Transmit RTR register	TRTRR0	R/W	00000000 00000000
10001B <sub>H</sub>				
10001C <sub>H</sub>	Remote frame receive waiting register	RFWTR0	R/W	XXXXXXXX XXXXXXXXXX
10001D <sub>H</sub>				
10001E <sub>H</sub>	Transmit interrupt enable register	TIER0	R/W	00000000 00000000
10001F <sub>H</sub>				
100020 <sub>H</sub>	Acceptance mask select register	AMSR0	R/W	XXXXXXXX XXXXXXXXXX
100021 <sub>H</sub>				
100022 <sub>H</sub>				
100023 <sub>H</sub>				
100024 <sub>H</sub>	Acceptance mask register 0	AMR00	R/W	XXXXXXXX XXXXXXXXXX
100025 <sub>H</sub>				
100026 <sub>H</sub>				
100027 <sub>H</sub>				
100028 <sub>H</sub>	Acceptance mask register 1	AMR10	R/W	XXXXXXXX XXXXXXXXXX
100029 <sub>H</sub>				
10002A <sub>H</sub>				
10002B <sub>H</sub>				

12.16.2 Message Buffers

**Table 12-2. List of Message Buffers (ID Registers)**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN0</b>				
10002C <sub>H</sub> to 10004B <sub>H</sub>	General-purpose RAM	–	R/W	XXXXXXXX to XXXXXXXX
10004C <sub>H</sub>	ID register 0	IDR00	R/W	XXXXXXXX XXXXXXXXXX
10004D <sub>H</sub>				
10004E <sub>H</sub>				
10004F <sub>H</sub>				



**Table 12-2. List of Message Buffers (ID Registers) (continued)**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN0</b>				
100050 <sub>H</sub>	ID register 1	IDR10	R/W	XXXXXXXX XXXXXXXX
100051 <sub>H</sub>				
100052 <sub>H</sub>				XXXXX --- XXXXXXXX
100053 <sub>H</sub>				
100054 <sub>H</sub>	ID register 2	IDR20	R/W	XXXXXXXX XXXXXXXX
100055 <sub>H</sub>				
100056 <sub>H</sub>				XXXXX --- XXXXXXXX
100057 <sub>H</sub>				
100058 <sub>H</sub>	ID register 3	IDR30	R/W	XXXXXXXX XXXXXXXX
100059 <sub>H</sub>				
10005A <sub>H</sub>				XXXXX --- XXXXXXXX
10005B <sub>H</sub>				
10005C <sub>H</sub>	ID register 4	IDR40	R/W	XXXXXXXX XXXXXXXX
10005D <sub>H</sub>				
10005E <sub>H</sub>				XXXXX --- XXXXXXXX
10005F <sub>H</sub>				
100060 <sub>H</sub>	ID register 5	IDR50	R/W	XXXXXXXX XXXXXXXX
100061 <sub>H</sub>				
100062 <sub>H</sub>				XXXXX --- XXXXXXXX
100063 <sub>H</sub>				
100064 <sub>H</sub>	ID register 6	IDR60	R/W	XXXXXXXX XXXXXXXX
100065 <sub>H</sub>				
100066 <sub>H</sub>				XXXXX --- XXXXXXXX
100067 <sub>H</sub>				
100068 <sub>H</sub>	ID register 7	IDR70	R/W	XXXXXXXX XXXXXXXX
100069 <sub>H</sub>				
10006A <sub>H</sub>				XXXXX --- XXXXXXXX
10006B <sub>H</sub>				
10006C <sub>H</sub>	ID register 8	IDR80	R/W	XXXXXXXX XXXXXXXX
10006D <sub>H</sub>				
10006E <sub>H</sub>				XXXXX --- XXXXXXXX
10006F <sub>H</sub>				
100070 <sub>H</sub>	ID register 9	IDR90	R/W	XXXXXXXX XXXXXXXX
100071 <sub>H</sub>				
100072 <sub>H</sub>				XXXXX --- XXXXXXXX
100073 <sub>H</sub>				

**Table 12-2. List of Message Buffers (ID Registers) (continued)**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN0</b>				
100074 <sub>H</sub>	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX
100075 <sub>H</sub>				
100076 <sub>H</sub>				XXXXX --- XXXXXXXX
100077 <sub>H</sub>				
100078 <sub>H</sub>	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX
100079 <sub>H</sub>				
10007A <sub>H</sub>				XXXXX --- XXXXXXXX
10007B <sub>H</sub>				
10007C <sub>H</sub>	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX
10007D <sub>H</sub>				
10007E <sub>H</sub>				XXXXX --- XXXXXXXX
10007F <sub>H</sub>				
100080 <sub>H</sub>	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX
100081 <sub>H</sub>				
100082 <sub>H</sub>				XXXXX --- XXXXXXXX
100083 <sub>H</sub>				
100084 <sub>H</sub>	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX
100085 <sub>H</sub>				
100086 <sub>H</sub>				XXXXX --- XXXXXXXX
100087 <sub>H</sub>				
100088 <sub>H</sub>	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX
100089 <sub>H</sub>				
10008A <sub>H</sub>				XXXXX --- XXXXXXXX
10008B <sub>H</sub>				

**Table 12-3. List of Message Buffers (DLC Registers and Data Registers)**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN0</b>				
10008C <sub>H</sub>	DLC register 0	DLCR00	R/W	---- XXXX
10008D <sub>H</sub>				
10008E <sub>H</sub>	DLC register 1	DLCR10	R/W	---- XXXX
10008F <sub>H</sub>				
100090 <sub>H</sub>	DLC register 2	DLCR20	R/W	---- XXXX
100091 <sub>H</sub>				
100092 <sub>H</sub>	DLC register 3	DLCR30	R/W	---- XXXX
100093 <sub>H</sub>				
100094 <sub>H</sub>	DLC register 4	DLCR40	R/W	---- XXXX
100095 <sub>H</sub>				

**Table 12-3. List of Message Buffers (DLC Registers and Data Registers) (continued)**

Address	Register	Abbreviation	Access	Initial Value
100096 <sub>H</sub>	DLC register 5	DLCR50	R/W	----XXXX
100097 <sub>H</sub>				
100098 <sub>H</sub>	DLC register 6	DLCR60	R/W	----XXXX
100099 <sub>H</sub>				
10009A <sub>H</sub>	DLC register 7	DLCR70	R/W	----XXXX
10009B <sub>H</sub>				
10009C <sub>H</sub>	DLC register 8	DLCR80	R/W	----XXXX
10009D <sub>H</sub>				
10009E <sub>H</sub>	DLC register 9	DLCR90	R/W	----XXXX
10009F <sub>H</sub>				
1000A0 <sub>H</sub>	DLC register 10	DLCR100	R/W	----XXXX
1000A1 <sub>H</sub>				
1000A2 <sub>H</sub>	DLC register 11	DLCR110	R/W	----XXXX
1000A3 <sub>H</sub>				
1000A4 <sub>H</sub>	DLC register 12	DLCR120	R/W	----XXXX
1000A5 <sub>H</sub>				
1000A6 <sub>H</sub>	DLC register 13	DLCR130	R/W	----XXXX
1000A7 <sub>H</sub>				
1000A8 <sub>H</sub>	DLC register 14	DLCR140	R/W	----XXXX
1000A9 <sub>H</sub>				
1000AA <sub>H</sub>	DLC register 15	DLCR150	R/W	----XXXX
1000AB <sub>H</sub>				
1000AC <sub>H</sub> to 1000B3 <sub>H</sub>	Data register 0 (8 bytes)	DTR00	R/W	XXXXXXXX to XXXXXXXX
1000B4 <sub>H</sub> to 1000BB <sub>H</sub>	Data register 1 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
1000BC <sub>H</sub> to 1000C3 <sub>H</sub>	Data register 2 (8 bytes)	DTR20	R/W	XXXXXXXX to XXXXXXXX
1000C4 <sub>H</sub> to 1000CB <sub>H</sub>	Data register 3 (8 bytes)	DTR30	R/W	XXXXXXXX to XXXXXXXX
1000CC <sub>H</sub> to 1000D3 <sub>H</sub>	Data register 4 (8 bytes)	DTR40	R/W	XXXXXXXX to XXXXXXXX
1000D4 <sub>H</sub> to 1000DB <sub>H</sub>	Data register 5 (8 bytes)	DTR50	R/W	XXXXXXXX to XXXXXXXX
1000DC <sub>H</sub> to 1000E3 <sub>H</sub>	Data register 6 (8 bytes)	DTR60	R/W	XXXXXXXX to XXXXXXXX

**Table 12-3. List of Message Buffers (DLC Registers and Data Registers) (continued)**

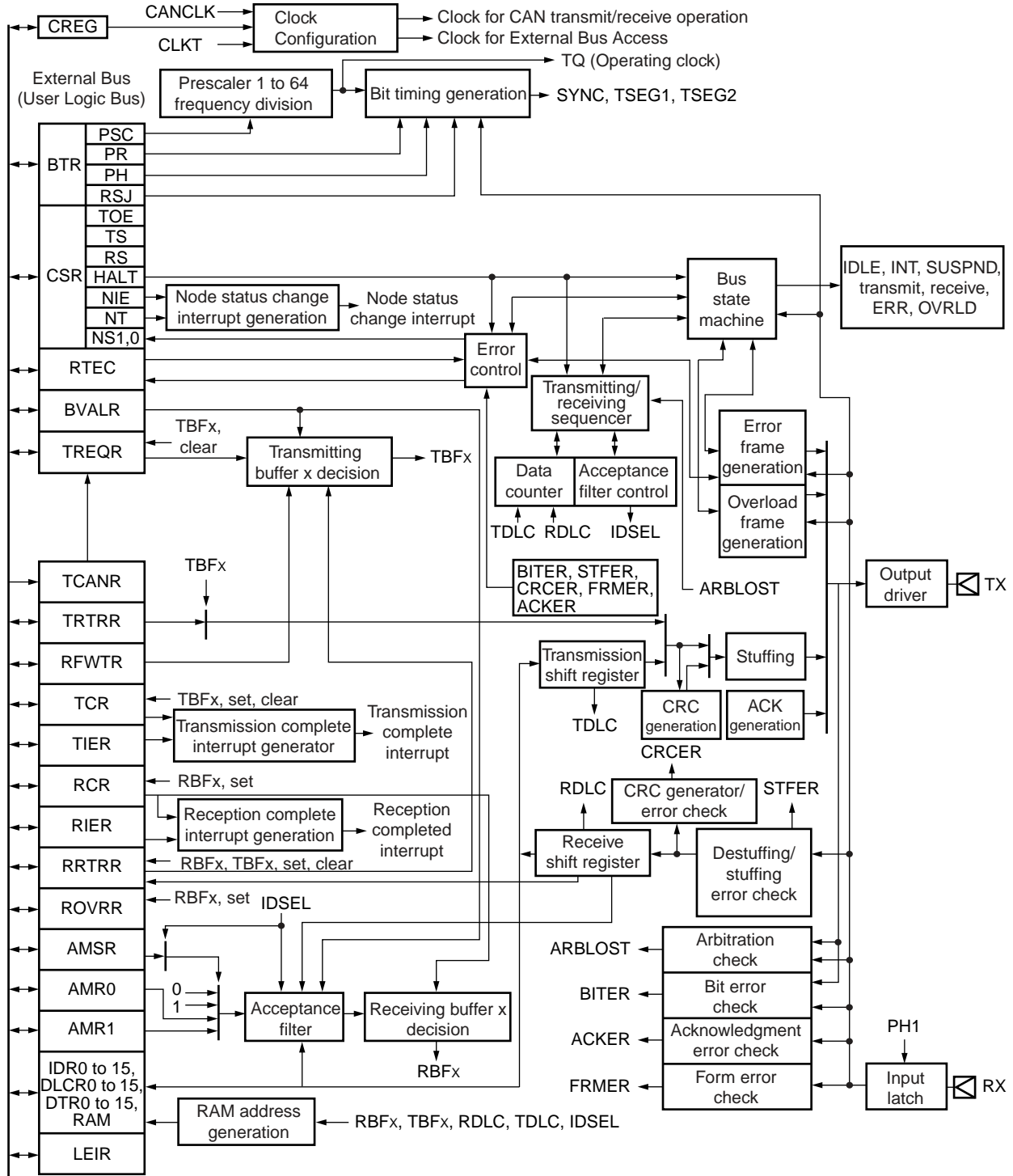
Address	Register	Abbreviation	Access	Initial Value
CAN0				
1000E4 <sub>H</sub> to 1000EB <sub>H</sub>	Data register 7 (8 bytes)	DTR70	R/W	XXXXXXXX to XXXXXXXX
1000EC <sub>H</sub> to 1000F3 <sub>H</sub>	Data register 8 (8 bytes)	DTR80	R/W	XXXXXXXX to XXXXXXXX
1000F4 <sub>H</sub> to 1000FB <sub>H</sub>	Data register 9 (8 bytes)	DTR90	R/W	XXXXXXXX to XXXXXXXX
1000FC <sub>H</sub> to 100103 <sub>H</sub>	Data register 10 (8 bytes)	DTR100	R/W	XXXXXXXX to XXXXXXXX
100104 <sub>H</sub> to 10010B <sub>H</sub>	Data register 11 (8 bytes)	DTR110	R/W	XXXXXXXX to XXXXXXXX
10010C <sub>H</sub> to 100113 <sub>H</sub>	Data register 12 (8 bytes)	DTR120	R/W	XXXXXXXX to XXXXXXXX
100114 <sub>H</sub> to 10011B <sub>H</sub>	Data register 13 (8 bytes)	DTR130	R/W	XXXXXXXX to XXXXXXXX
10011C <sub>H</sub> to 100123 <sub>H</sub>	Data register 14 (8 bytes)	DTR140	R/W	XXXXXXXX to XXXXXXXX
100124 <sub>H</sub> to 10012B <sub>H</sub>	Data register 15 (8 bytes)	DTR150	R/W	XXXXXXXX to XXXXXXXX

**Table 12-4. Configuration Register (CREG)**

Address	Register	Abbreviation	Access	Initial Value
CAN0				
10012C <sub>H</sub> 10012D <sub>H</sub>	Configuration register	CREG0	R/W	00000000 00000110



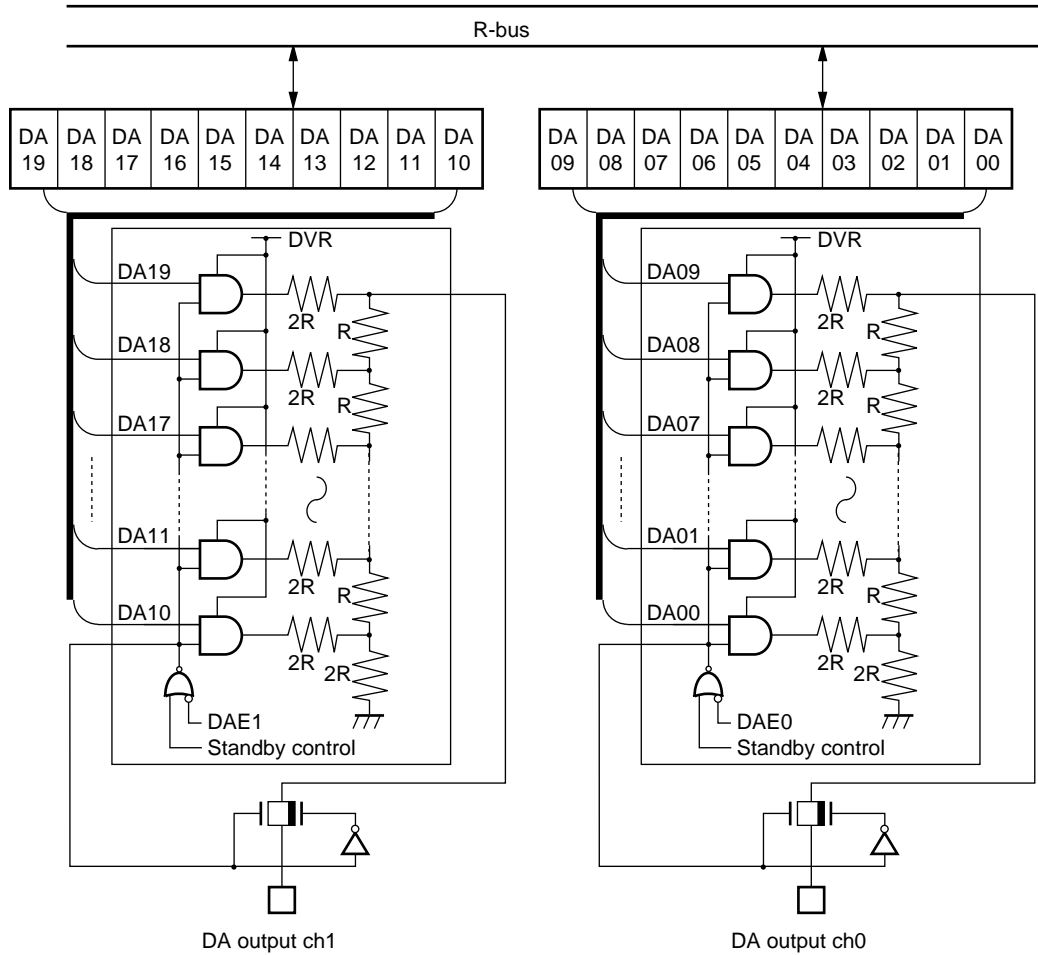
12.16.3 Block Diagram



### 12.17 D/A Converter

This section provides an overview of the D/A converter, describes the register structure and functions, and describes the operation of D/A converter. This block is an R-2R format D/A converter, having ten-bit resolution. The D/A converter has two channels. Output control can be performed independently for the two channels using the D/A control register.

#### 12.17.1 Block Diagram



12.17.2 Registers

D/A control register (DACR)

bit	7	6	5	4	3	2	1	0
Address: 0000A5H	—	—	—	—	—	MODE	DAE1	DAE0

D/A converter data register (ch 0) (DADR0)

bit	15	14	13	12	11	10	9	8
Address: 0000A6H	—	—	—	—	—	—	DA09	DA08

bit	7	6	5	4	3	2	1	0
Address: 0000A7H	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00

D/A converter data register (ch 1) (DADR1)

bit	15	14	13	12	11	10	9	8
Address: 0000A8H	—	—	—	—	—	—	DA19	DA18

bit	7	6	5	4	3	2	1	0
Address: 0000A9H	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10

D/A clock control (DDBL)

bit	7	6	5	4	3	2	1	0
Address: 0000ABH	—	—	—	—	—	—	—	DBL

## 12.18 400 kHz I<sup>2</sup>C Interface

This section describes the functions and operation of the fast I<sup>2</sup>C interface.

The I<sup>2</sup>C interface is a serial I/O port supporting the Inter IC bus, operating as a master/slave device on the I<sup>2</sup>C bus.

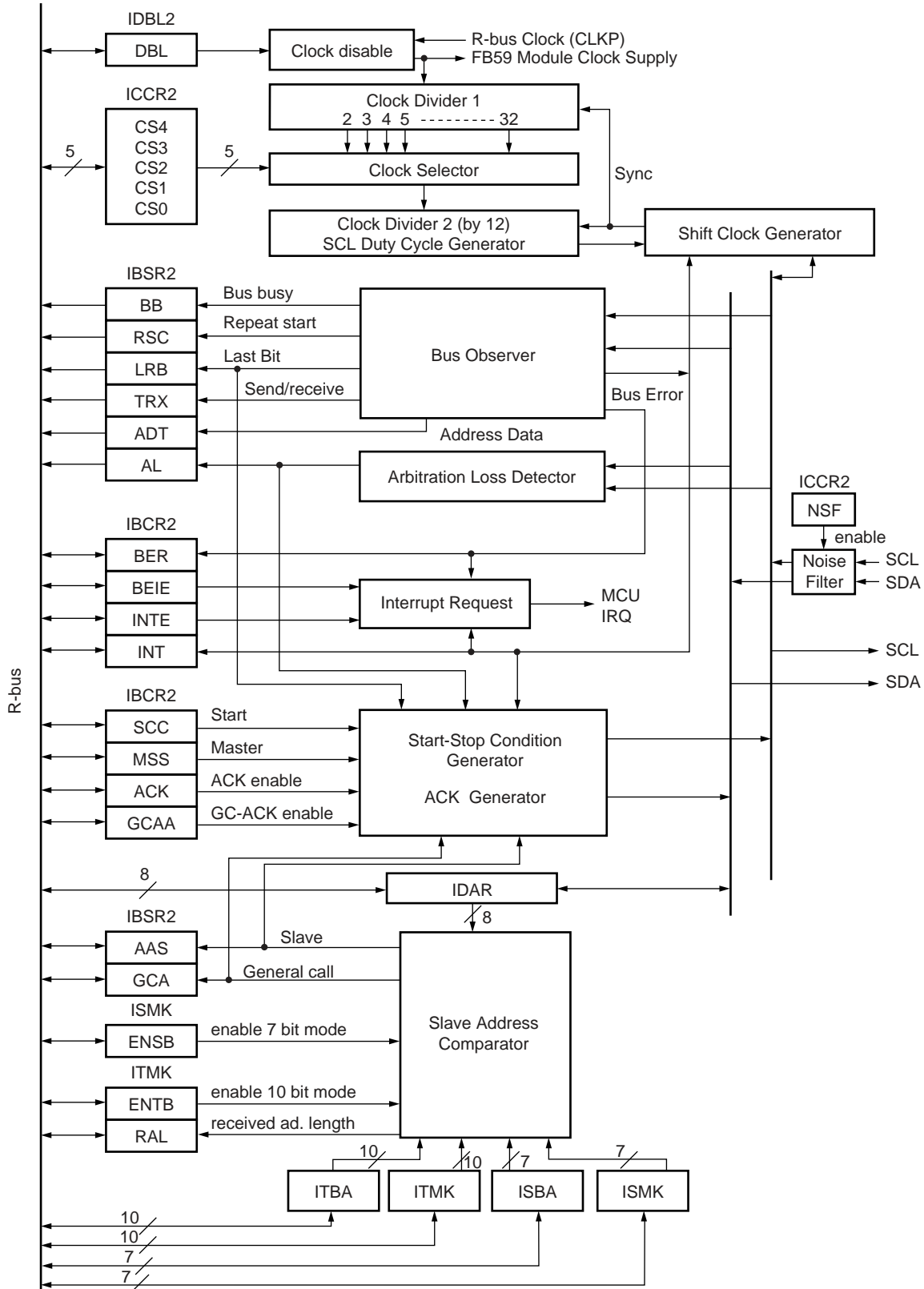
### 12.18.1 Features

- Master/slave transmitting and receiving functions
- Arbitration function
- Clock synchronization function
- General call addressing support
- Transfer direction detection function
- Repeated start condition generation and detection function
- Bus error detection function
- 7 bit addressing as master and slave
- 10 bit addressing as master and slave
- Possibility to give the interface a seven and a ten bit slave address
- Acknowledging upon slave address reception can be disabled (Master-only operation)
- Address masking to give interface several slave addresses (in 7 and 10 bit mode)
- Up to 400 KBit transfer rate
- Possibility to use built-in noise filters for SDA and SCL
- Can receive data at 400 KBit if R-bus-Clock is higher than 6 MHz regardless of prescaler setting
- Can generate MCU interrupts on transmission and bus error events
- Supports being slowed down by a slave on bit and byte level

The I<sup>2</sup>C interface does not support SCL clock stretching on bit level since it can receive the full 400 KBit data rate if the R-bus-Clock (CLKP) is higher than 6 MHz regardless of the prescaler setting. However, clock stretching on byte level is performed since SCL is pulled low during an interrupt (INT = "1" in IBCR register).



12.18.2 Block Diagram



12.18.3 I<sup>2</sup>C Interface Registers

**a: Bus control register (IBCR2)**

	bit 15	14	13	12	11	10	9	8	...
Address: 000184 <sub>H</sub>	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	
Read/write ⇒	(R/W)	(R/W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

**b: Bus status register (IBSR2)**

	bit 7	6	5	4	3	2	1	0
Address: 000185 <sub>H</sub>	BB	RSC	AL	LRB	TRX	AAS	GCA	ADT
Read/write ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**c: Ten bit slave address register (ITBAH, ITBAL)**

Ten Bit Address high byte

	bit 15	14	13	12	11	10	9	8	...
Address: 000186 <sub>H</sub>	—	—	—	—	—	—	TA9	TA8	
Read/write ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Ten Bit Address low byte

	bit 7	6	5	4	3	2	1	0
Address: 000187 <sub>H</sub>	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**d: Ten bit slave address mask register (ITMKH, ITMKL)**

Ten Bit Address Mask high byte

	bit 15	14	13	12	11	10	9	8	...
Address: 000188 <sub>H</sub>	ENTB	RAL	—	—	—	—	TM9	TM8	
Read/write ⇒	(R/W)	(R)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	
Default value ⇒	(0)	(0)	(1)	(1)	(1)	(1)	(1)	(1)	

Ten Bit Address Mask low byte

	bit 7	6	5	4	3	2	1	0
Address: 000189 <sub>H</sub>	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

**e: Seven bit slave address register (ISBA)**

	bit 7	6	5	4	3	2	1	0
Address: 00018B <sub>H</sub>	—	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Read/write ⇒	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

*(Continued)*

(Continued)

**f: Seven bit slave address mask register (ISMK)**

	bit 15	14	13	12	11	10	9	8	...
Address: 00018A <sub>H</sub>	ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0	
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇒	(0)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	

**g: Data register (IDARH, IDAR2)**

Data register high byte

	bit 15	14	13	12	11	10	9	8	...
Address: 00018C <sub>H</sub>	—	—	—	—	—	—	—	—	
Read/write ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(—)	
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Data register

	bit 7	6	5	4	3	2	1	0
Address: 00018D <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**h: Clock control register (ICCR2)**

	bit 15	14	13	12	11	10	9	8	...
Address: 00018E <sub>H</sub>	—	NSF	EN	CS4	CS3	CS2	CS1	CS0	
Read/write ⇒	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇒	(0)	(0)	(0)	(1)	(1)	(1)	(1)	(1)	

**i: Clock disable register (IDBL2)**

	bit 7	6	5	4	3	2	1	0
Address: 00018F <sub>H</sub>	—	—	—	—	—	—	—	DBL
Read/write ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**12.19 16-bit I/O Timer**

The CY91360G Series contains two 16-bit free-running timer modules, two output compare modules, and two input capture modules and supports four input channels and four output channels. The following sections only describes the 16-bit free-running timer, Output Compare 0/1 and Input Capture 0/1.

The remaining modules have the identical functions and the register addresses should be found in the I/O map.

*12.19.1 Function overview*

**a: 16-bit Free-running Timer**

The 16-bit free-run timer consists of a 16-bit up counter, control register, and prescaler. The values output from this timer counter are used as the base timer for input capture and output compare.

- Four counter clocks are available.  
Internal clock:  $\phi/4$ ,  $\phi/16$ ,  $\phi/32$ ,  $\phi/64$
- An interrupt can be generated upon a counter overflow or a match with compare register 0.
- The counter value can be initialized to “0000H” upon a reset, software clear, or match with compare register 0.

**b: Output Compare (2 channels per one module)**

The output compare module consists of two 16-bit compare registers, compare output latch, and control register.

When the 16-bit free-running timer value matches the compare register value, the output level is reversed and an interrupt is issued.

- The two compare registers can be used independently.
  - Output pins and interrupt flags corresponding to compare registers
- Output pins can be controlled based on pairs of the two compare registers.
  - Output pins can be reversed by using the two compare registers.
- Initial values for output pins can be set.
- Interrupts can be generated upon a compare match.

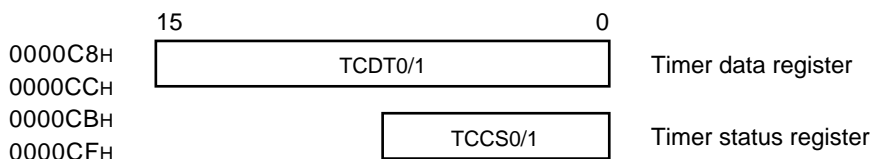
**c: Input Capture (2 channels per one module)**

The input capture module consists of two 16-bit capture registers and control registers corresponding to two independent external input pins. The 16-bit free-running timer value can be stored in the capture register and an interrupt is issued simultaneously upon detection of an edge of a signal input from an external input pin.

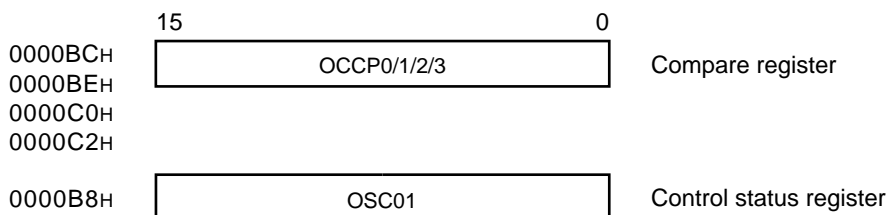
- The detection edge of an external input signal can be specified.
  - Rising, falling, or both edges
- Two input channels can operate independently.
- An interrupt can be issued upon a valid edge of an external input signal.

12.19.2 Registers

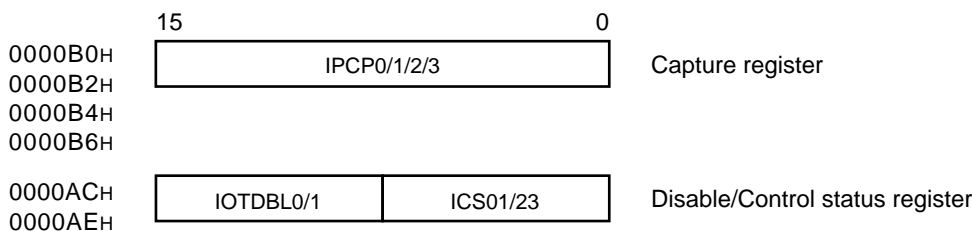
**a: 16-bit free-running timer**



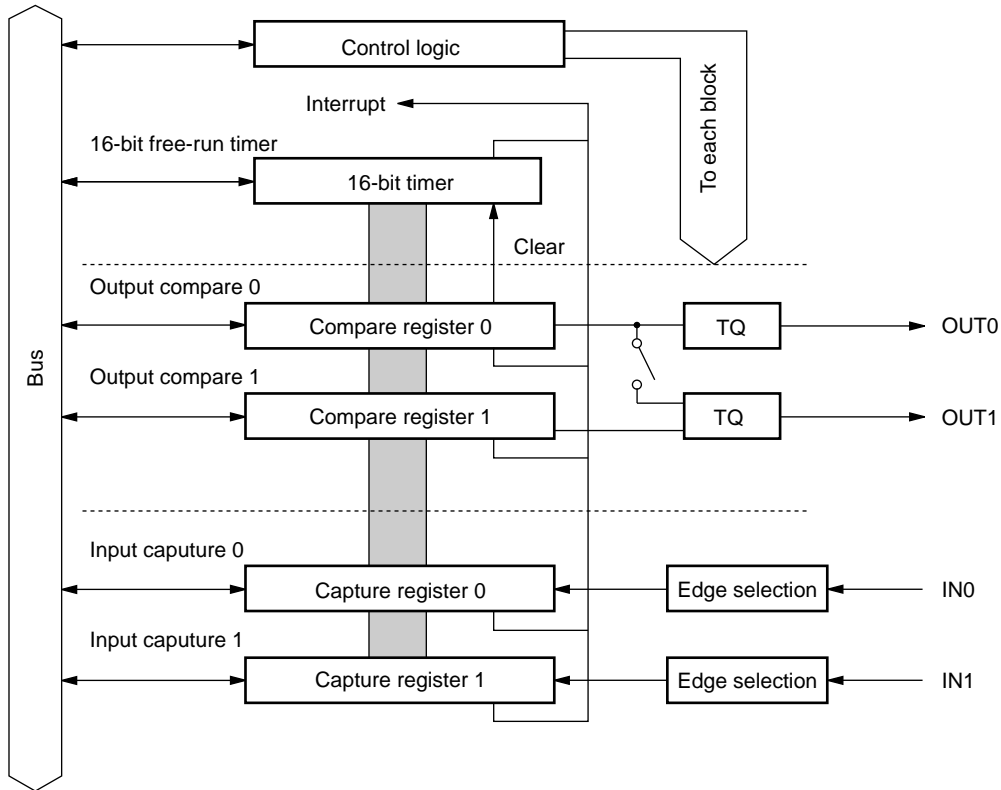
**b: 16-bit output compare**



**c: 16-bit input capture**



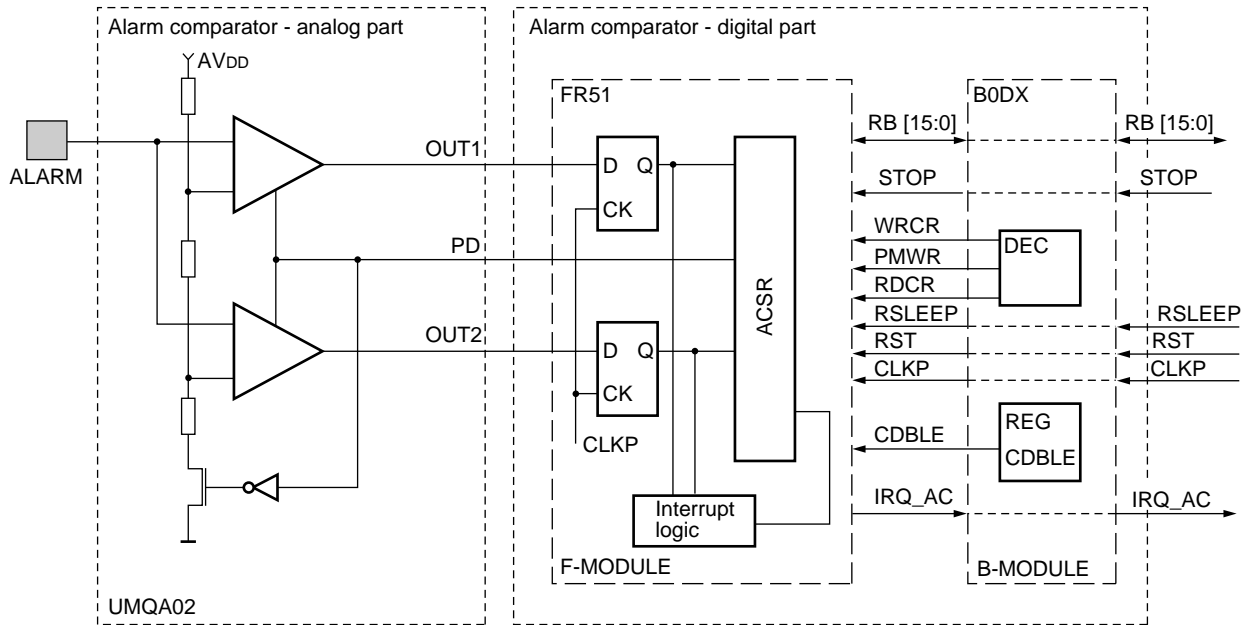
12.19.3 Block Diagram



## 12.20 Alarm Comparator

This section provides an overview of the Alarm Comparator (Also called Under/Overvoltage Detection), describes the register structure and functions, and describes the operation of the Alarm Comparator.

### 12.20.1 Block Diagram



### 12.20.2 Registers

#### Alarm comparator clock disable register (ACCDBL)

Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000180H		—	—	—	—	—	—	—	CDBLE	-----0 <sub>B</sub>
									R/W	← Access

#### Alarm comparator status disable register (ACSR)

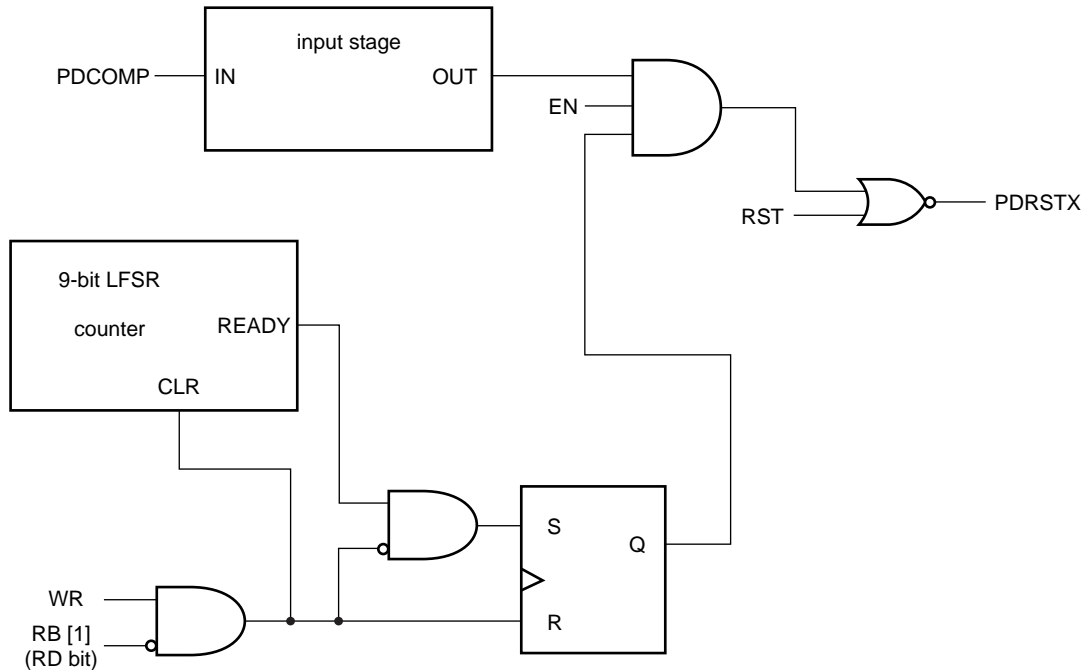
Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000181H		—	OV_EN	UV-EN	OUT2	OUT1	IRQ	IEN	PD	-11xx00 <sub>B</sub>
			R/W	R/W	R	R	R/W	R/W	R/W	← Access

### 12.21 Power Down Reset

This section provides an overview of the Power Down Reset, and describes the register structure.

The power down reset module performs a system reset when  $V_{CC}$  goes below a threshold voltage. The reset signal is disabled and enabled by setting the power down reset control register (PDRCR). For low power applications the digital and the analog part of the power down reset control circuit can be disabled.

#### 12.21.1 Block Diagram



#### 12.21.2 Register

		7	6	5	4	3	2	1	0
PDRCR	00017D <sub>H</sub>	—	—	—	—	—	CDSBLE	PD	EN
access		—	—	—	—	—	R/W	R/W	R/W
initial value (INIT)		—	—	—	—	—	0	0	0
initial value (RST)		X	X	X	X	X	X	X	X

## 12.22 Serial I/O Interface (SIO)

This section provides an overview of the Serial I/O Interface (SIO), and describes the register structure.

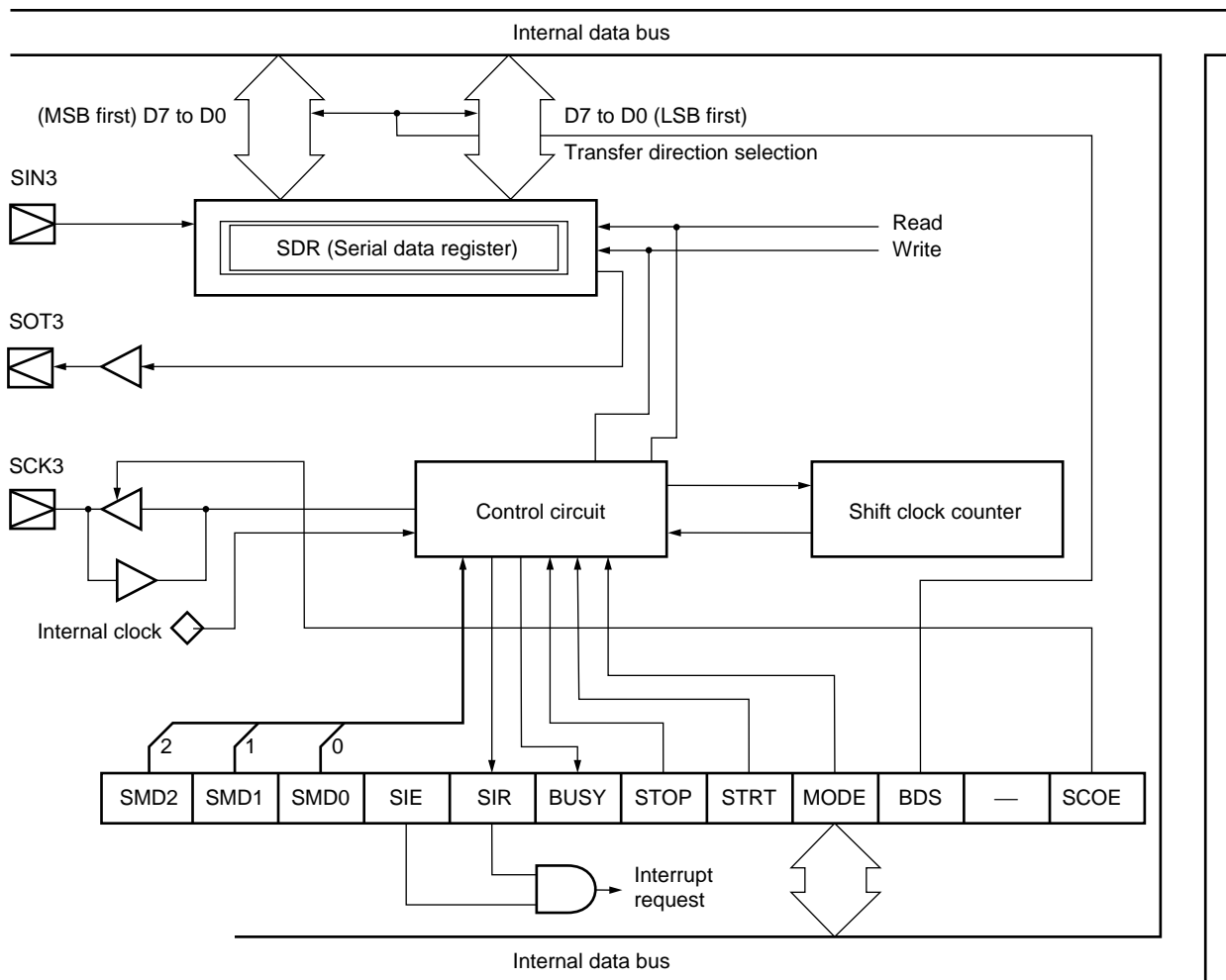
### 12.22.1 Block Diagram

This block is a serial I/O interface that allows data transfer using clock synchronization. The interface consists of a single eight-bit channel. Data can be transferred from the LSB or MSB.

CY91360G series contains two Serial I/O units SIO0 and SIO1. This section only describes SIO0. Please see the I/O map for the register addresses of SIO1.

The serial I/O interface operates in two modes:

- Internal shift clock mode: Data is transferred in synchronization with the internal clock.
- External shift clock mode: Data is transferred in synchronization with the clock supplied via the external pin (SCK). By manipulating the general-purpose port sharing the external pin (SCK), data can also be transferred by a CPU instruction in this mode.





### 12.22.2 Registers

Serial mode control status register (SMCS)

	15	14	13	12	11	10	9	8
Address: 000084 <sub>H</sub>	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT

	7	6	5	4	3	2	1	0
Address: 000085 <sub>H</sub>	—	—	—	—	MODE	BDS	—	SCOE

SIO edge selection/clock disable register (SES)

	15	14	13	12	11	10	9	8
Address: 000086 <sub>H</sub>	—	—	—	—	—	—	DBL	NEG

Serial data register (SDR)

	7	6	5	4	3	2	1	0
Address: 000087 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0

### 12.23 Sound Generator

This section provides an overview of the Sound Generator, and describes the register structure.

The Sound Generator consists of the Sound Control register, Frequency Data register, Amplitude Data register, Decrement Grade register, Tone Count register, Sound Disable register, PWM pulse generator, Frequency counter, Decrement counter and Tone Pulse counter.

### 12.23.1 Registers

#### Sound control register (SGCR)

bit	7	6	5	4	3	2	1	0
Address: 0000EF <sub>H</sub>	S1	S0	TONE	—	—	INTE	INT	ST
Read/write ⇒	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(—)	(—)	(0)	(0)	(0)

bit	15	14	13	12	11	10	9	8
Address: 0000EE <sub>H</sub>	TST	—	—	—	—	—	BUSY	DEC
Read/write ⇒	(R/W)	(—)	(—)	(—)	(—)	(—)	(R)	(R/W)
Default value ⇒	(0)	(—)	(—)	(—)	(—)	(—)	(0)	(0)

#### Frequency data register (SGFR)

bit	7	6	5	4	3	2	1	0
Address: 0000F1 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

#### Amplitude data register (SGAR)

bit	15	14	13	12	11	10	9	8
Address: 0000F0 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

#### Decrement grade register (SGDR)

bit	7	6	5	4	3	2	1	0
Address: 0000F3 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

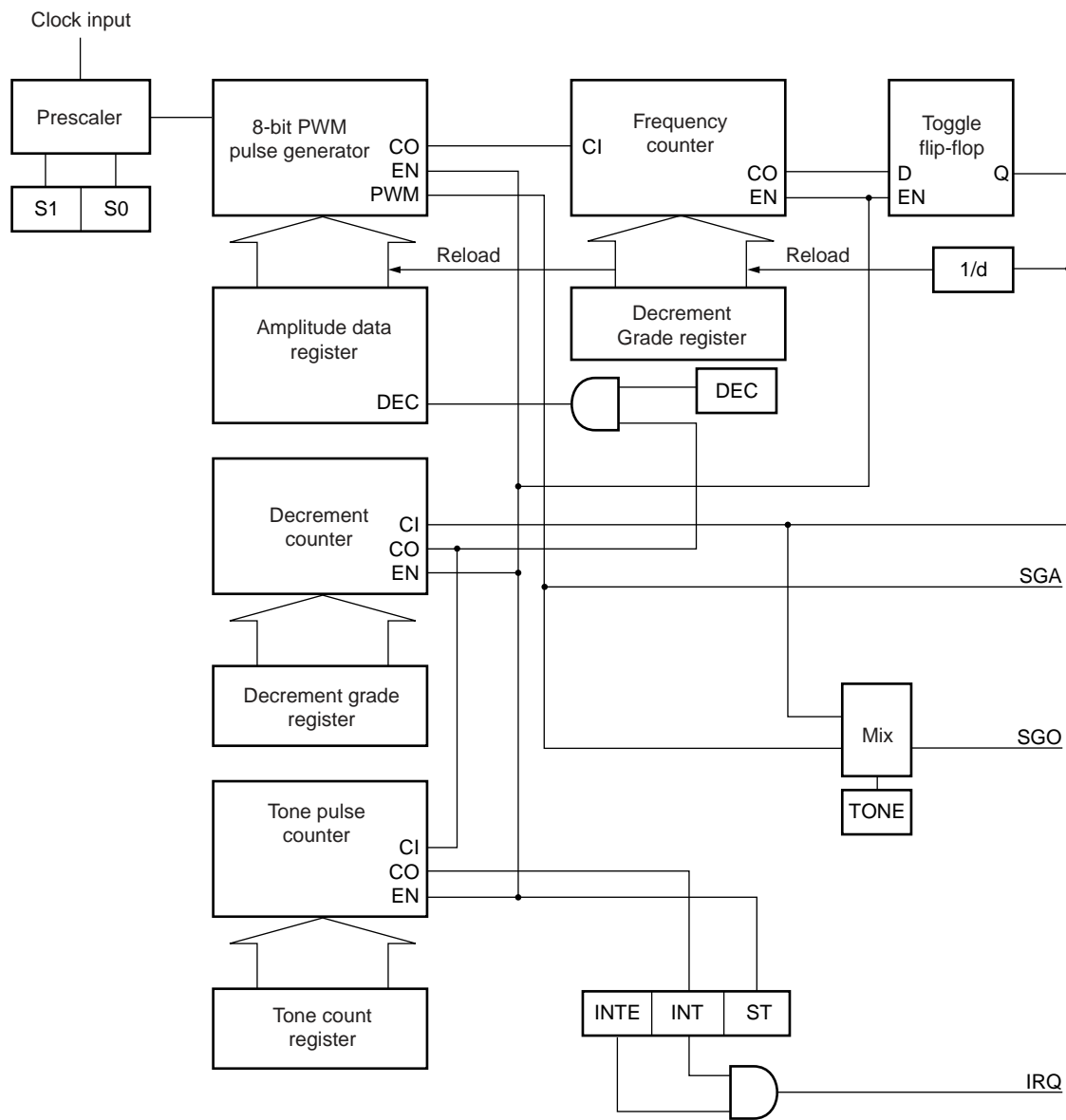
#### Tone count register (SGTR)

bit	15	14	13	12	11	10	9	8
Address: 0000F2 <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

#### Sound disable register (SGDBL)

bit	7	6	5	4	3	2	1	0
Address: 0000ED <sub>H</sub>	—	—	—	—	—	—	—	DBL
Read/write ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

12.23.2 Block Diagram



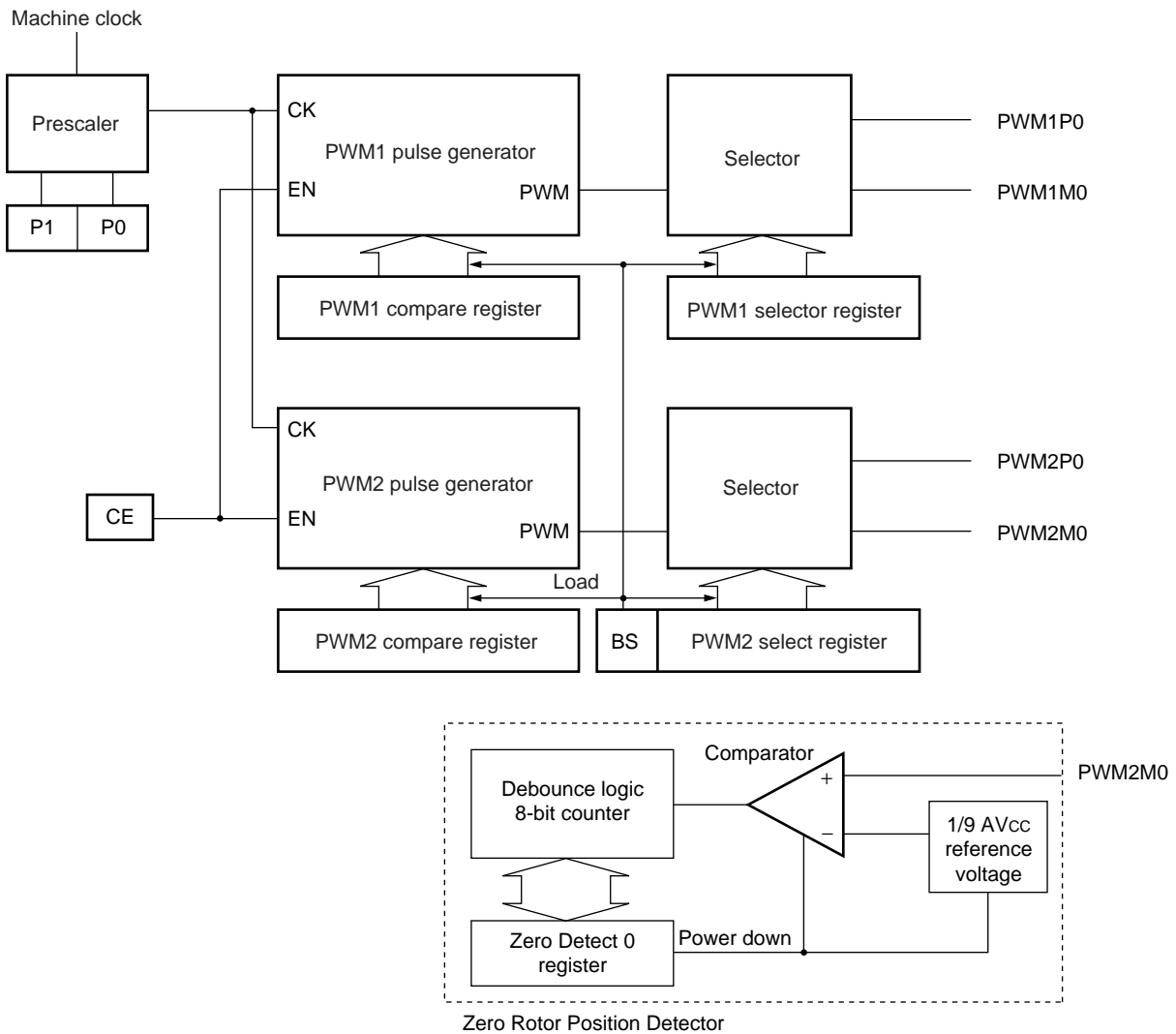
## 12.24 Stepper Motor Controller

This section provides an overview of the Stepper Motor Control Module, and describe the register structure.

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers, Selector Logic and the Zero Rotor Position Detector. The four motor drivers have high output drive capabilities and they can be directly connected to the four ends of two motor coils. The combination of the PWM Pulse Generators and Selector Logic is designed to control the rotation of the motor. A Synchronization mechanism assures the synchronous operations of the two PWMs. The Zero Rotor Position Detector helps CPU obtain feed back information of the rotor movements. The following sections describe the Stepping Motor Controller 0 only. The other controllers have the same functions. The register addresses are found in the I/O map.

Note: The Rotor Zero Position Detection capability is protected by a patent from siemens VDO automatic AG and may only be used with VDO's prior approval.

### 12.24.1 Block Diagram



## 12.24.2 Registers

## PWM control 0 register (PWC0)

bit	7	6	5	4	3	2	1	0
Address: 0000D1H	—	—	P1	P0	CE	—	—	TST
Read/write ⇒	(—)	(—)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)
Default value ⇒	(—)	(—)	(0)	(0)	(0)	(—)	(—)	(0)

## Zero detect 0 register (ZPD0)

bit	15	14	13	12	11	10	9	8
Address: 0000D0H	S1	S0	TS	T2	T1	T0	PD	RS
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)

## PWM1 compare 0 register (PWC10)

bit	7	6	5	4	3	2	1	0
Address: 0000D9H	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

## PWM2 compare 0 register (PWC20)

bit	15	14	13	12	11	10	9	8
Address: 0000D8H	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

## PWM1 select register (PWS10)

bit	7	6	5	4	3	2	1	0
Address: 0000DBH	—	—	P2	P1	P0	M2	M1	M0
Read/write ⇒	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(—)	(—)	(0)	(0)	(0)	(0)	(0)	(0)

## PWM2 select register (PWS20)

bit	15	14	13	12	11	10	9	8
Address: 0000DAH	—	BS	P2	P1	P0	M2	M1	M0
Read/write ⇒	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(—)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

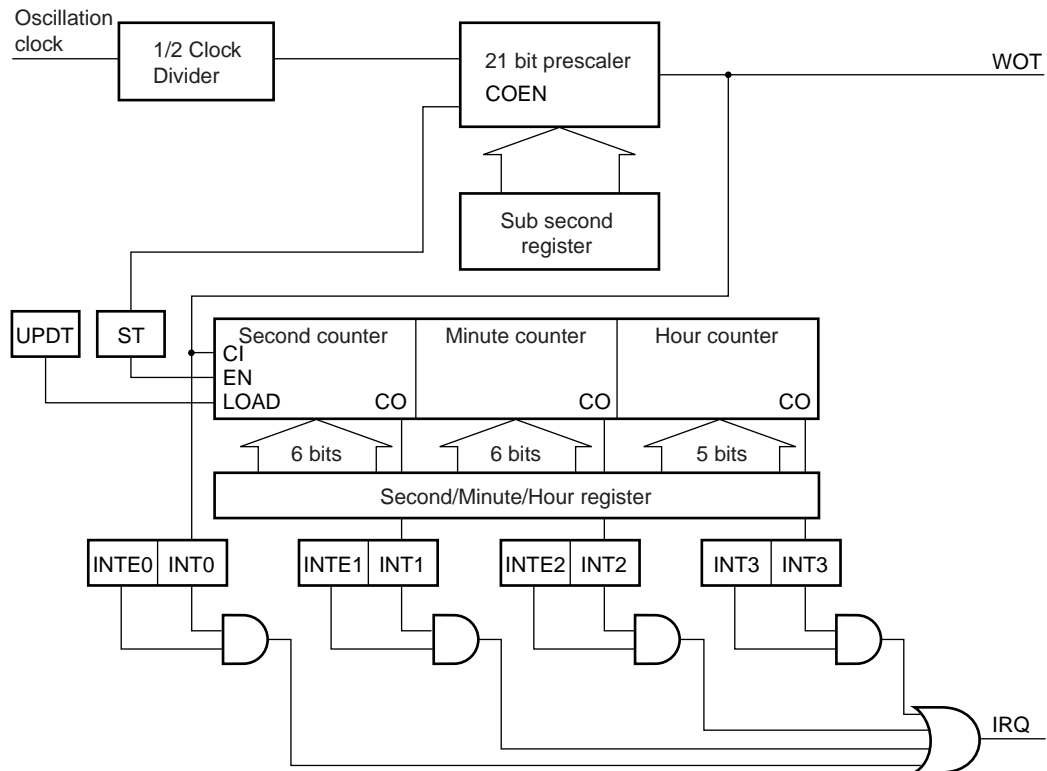
## PWM clock disable register (SMDBL0)

bit	7	6	5	4	3	2	1	0
Address: 0000E8H	—	—	—	—	—	—	—	DBL
Read/write ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

## 12.25 Real Time Clock

This section provides an overview of the Real Time Clock (also called WatchTimer), describes the register structure and functions. The Real Time Clock (Watch Timer) consists of the Timer Control register, Sub-second register, Second/Minute/Hour registers, 1/2 clock divider, 21bit prescaler and Second/Minute/Hour counters. The Real Time Clock operates as the real-world timer and provides the real-world time information.

### 12.25.1 Block Diagram



12.25.2 Registers

Timer disable register (WTDBL)

bit	7	6	5	4	3	2	1	0
Address: 0000F5 <sub>H</sub>	—	—	—	—	—	—	—	DBL
Read/write ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇒	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

Timer control register (WTCR)

bit	7	6	5	4	3	2	1	0
Address: 0000F7 <sub>H</sub>	TST2	TST1	TST0	—	RUN	UPDT	—	ST
Read/write ⇒	(R/W)	(R/W)	(R/W)	(—)	(R)	(R/W)	(—)	(R/W)
Default value ⇒	(0)	(0)	(0)	(—)	(0)	(0)	(—)	(0)

bit	15	14	13	12	11	10	9	8
Address: 0000F6 <sub>H</sub>	INTE3	INT3	INTE2	INT2	INTE1	INT1	INTE0	INT0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Sub-second register (WTBR)

bit	7	6	5	4	3	2	1	0
Address: 0000FB <sub>H</sub>	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

bit	15	14	13	12	11	10	9	8
Address: 0000FA <sub>H</sub>	D15	D14	D13	D12	D11	D10	D9	D8
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

bit	7	6	5	4	3	2	1	0
Address: 0000F9 <sub>H</sub>	—	—	—	D20	D19	D18	D17	D16
Read/write ⇒	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(X)

Second register (WTSR)

bit	15	14	13	12	11	10	9	8
Address: 0000FE <sub>H</sub>	—	—	S5	S4	S3	S2	S1	S0
Read/write ⇒	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)

*(Continued)*

(Continued)

Minute register (WTMR)

bit	7	6	5	4	3	2	1	0
Address: 0000FD <sub>H</sub>	—	—	M5	M4	M3	M2	M1	M0
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)

Hour register (WTHR)

bit	15	14	13	12	11	10	9	8
Address: 0000FC <sub>H</sub>	—	—	—	H4	H3	H2	H1	H0
Read/write ⇨	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(X)



## 12.26 Subclock

The Subclock System provides various power saving modes. The key of the concept is to supply the 32 kHz clock signal only to the Real Time Clock (RTC) Module, while the rest of the MCU is provided with 4 MHz clock signal in order to achieve lower power supply current in the RTC32K mode.

This behavior can be altered by the configuration input, SELCLK pin to switch the RTC module to operate with the 4 MHz clock. The following sections describe the operation with SELCLK connected to “0” and SELCLK connected to “1” respectively.

Note: On CY91F362GB SELCLK should always be connected to “1”, subclock operation is not implemented on those devices.

### 12.26.1 Operation of Subclock (SELCLK = 0)

The next table summarizes the operation states of the components related to the Subclock System. To simplify this table SLEEP modes are not listed but the operation is the same as for RUN modes except that the CPU is stopped.

Mode	Power Dissipation	Operation of Components				
		4 M Osc.	32 K Osc.	RTC	CPU & Peripheral	PLL
RUN	High	Run	Run	Run	Run	Stop/Run
RTC4M32K	Medium Low	Run	Run	Run	Stop	Stop
RTC32K	Low	Stop	Run	Run	Stop	Stop
STOP	Lowest	Stop	Stop	Stop	Stop	Stop

The following table summarizes those operation modes and necessary software settings.

Mode	Software Setting					
	STOP	PLL1EN	PLL2EN	OSCD1	OSCD2	RTC32
RUN	0	0 or 1	1	Don't Care	Don't Care	Don't Care
RTC4M32K	1	Don't Care	1	0	0	Don't Care
RTC32K	1	Don't Care	1	1	0	1
STOP	1	Don't Care	Don't Care	1	1	Don't Care

It is recommended that PLL2EN is set to “1” after the initialization to start the 32 kHz oscillation and this bit should be kept at “1” during the operation. Otherwise the 32 kHz oscillator does not start. Also bits 9 and 10 of the CLKR register (address 0046H) should always be set to “0” during operation.

### 12.26.2 4 MHz Real Time Clock Configuration (SELCLK = 1)

When the SELCLK pad is connected logic level 1, the 32 kHz oscillation is disabled regardless of the software setting. In this configuration, the Real Time Clock Module is supplied with the 4 MHz oscillation clock signal.

The following table summaries the modes available in this configuration.

Mode	Power Dissipation	Operation of Components				
		4 M Osc.	32 K Osc.	RTC	CPU & Peripheral	PLL
RUN	High	Run	Stop	Run	Run	Stop/Run
RTC4M	Medium Low	Run	Stop	Run	Stop	Stop
STOP	Lowest	Stop	Stop	Stop	Stop	Stop

Mode	Software Setting					
	STOP	PLL1EN	PLL2EN	OSCD1	OSCD2	RTC32
RUN	0	0 or 1	Don't Care	Don't Care	Don't Care	Don't Care
RTC4M	1	Don't Care	Don't Care	0	Don't Care	Don't Care
STOP	1	Don't Care	Don't Care	1	Don't Care	Don't Care

### 12.26.3 Use of Real Time Clock Module

There is some additional consideration needed to operate the RTC module to achieve the desired functionality.

Because the RTC module is directly connected to the 32 kHz oscillation clock, the oscillation stabilization time has to be taken care of by the software. This can be achieved by using another timer (e.g the Time Base Timer) to trigger the software to start the RTC module (Setting of ST bit to "1").

It is also important to stop the RTC module before entering the STOP mode. Otherwise, the reactivation from STOP mode results in unpredictable operation of the RTC module.

After the reactivation, the oscillation stabilization time has to be measured again by the software, then the RTC module can be restarted.

## 12.27 32 kHz Clock Calibration Unit

The 32 kHz Clock Calibration Module provides possibilities to calibrate the 32 kHz oscillation clock with respect to the 4 MHz oscillation clock.

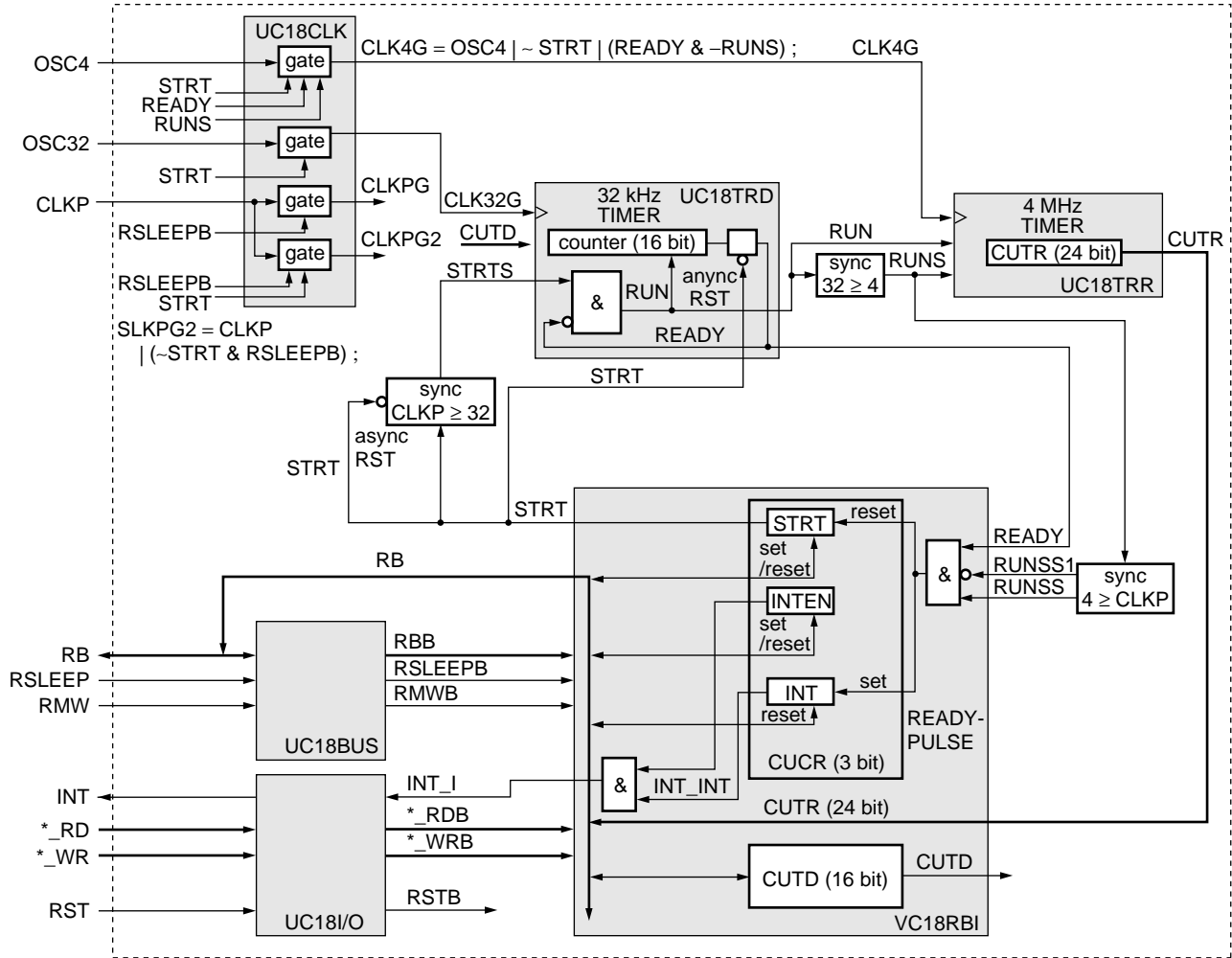
### 12.27.1 Description

This hardware allows the software to measure time generated by the 32 kHz clock with the 4 MHz clock.

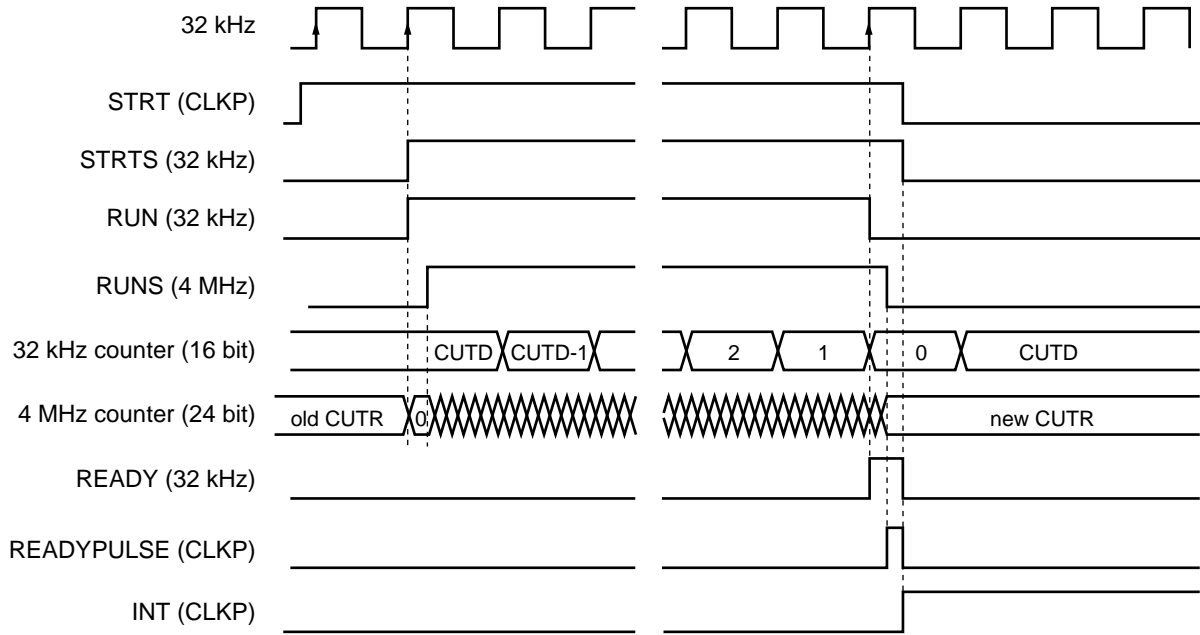
By utilizing this hardware in conjunction with software processing, the accuracy of the 32 kHz clock can come closer to that of the 4 MHz clock. The measurement result from the 32 kHz Clock Calibration Module can be processed by the software and the setting required for the Real Time Clock Module can be obtained.

This module consists of two timers, one operating with the 32 kHz clock and the other operating with the 4 MHz clock. The 32 kHz timer triggers the 4 MHz timer and resulting 4 MHz timer value is stored in a register. The value stored in this register can be used for the subsequent software processing to calculate the desired Real Time Clock module's setting.

12.27.2 Block Diagram



12.27.3 Timing



### 12.27.4 Clocks

The module operates with 3 different clocks: The 4 MHz clock OSC4, the 32 kHz clock OSC32 and the R-bus clock CLKP. Synchronization circuits adapt the different domains.

All 3 clocks are gated. The 32 kHz and the 4 MHz clock are switched off if STRT is 0. CLKPG is gated by RSLEEP and CLKPG2 by RSLEEP and STRT for the 2 bits, which are set/reset by hardware.

The clock frequencies have to fulfill the following requirements:

1.) Clock ratio

$$T_{OSC32} > 2 \times T_{OSC4} + 3 \times T_{CLKP}$$

$$T_{OSC4} < 1 / 2 \times T_{OSC32} - 3 / 2 \times T_{CLKP}$$

$$T_{CLKP} < 1 / 3 \times T_{OSC32} - 2 / 3 \times T_{OSC4}$$

2.) The input frequencies must not exceed the values given in next table.

**Table 12-5. Maximum Operation Frequencies**

	CLKP		OSC32		OSC4	
	Maximum	32 MHz	31.25 ns	4 MHz	250 ns	13 MHz

**Table 12-6. Examples of Valid Clock Ratios which Fulfill Requirements 1 and 2**

	OSC32		OSC4		CLKP		
	Maximum operation speed	4 MHz	250 ns	13 MHz	76.9 ns	32 MHz	31.25 ns
Standard TDIR mode	500 kHz	2000 ns	4 MHz	250 ns	4 MHz	250 ns	
Normal operation	32 kHz	31.25 us	4 MHz	250 ns	> 2 MHz	500 ns	

12.27.5 Register Description

**a: Calibration unit control register (CUCR)**

Control register low byte (CUCRL)

bit	7	6	5	4	3	2	1	0
Address: 000191 <sub>H</sub>	—	—	—	STRT	—	—	INT	INTEN
Read/write ⇒	(R)	(R)	(R)	(R/W)	(R)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**b: 32 kHz timer data register (CUTD)**

32 kHz timer data register high byte (CUTDH)

bit	15	14	13	12	11	10	9	8
Address: 000192 <sub>H</sub>	TDD15	TDD14	TDD13	TDD12	TDD11	TDD10	TDD9	TDD8
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

32 kHz timer data register low byte (CUTDL)

bit	7	6	5	4	3	2	1	0
Address: 000193 <sub>H</sub>	TDD7	TDD6	TDD5	TDD4	TDD3	TDD2	TDD1	TDD0
Read/write ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**c: 4 MHz timer data register (CUTR)**

4 MHz timer data register1 high byte (CUTR1H)

bit	15	14	13	12	11	10	9	8
Address: 000194 <sub>H</sub>	—	—	—	—	—	—	—	—
Read/write ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

4 MHz timer data register1 low byte (CUTR1L)

bit	7	6	5	4	3	2	1	0
Address: 000195 <sub>H</sub>	TDR23	TDR22	TDR21	TDR20	TDR19	TDR18	TDR17	TDR16
Read/write ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

4 MHz timer data register2 high byte (CUTR2H)

bit	15	14	13	12	11	10	9	8
Address: 000196 <sub>H</sub>	TDR15	TDR14	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8
Read/write ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

4 MHz timer data register2 low byte (CUTR2L)

bit	7	6	5	4	3	2	1	0
Address: 000197 <sub>H</sub>	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
Read/write ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇒	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

## 12.28 Flash Memory

CY91360G series devices feature 512 Kbyte of embedded flash memory unit derived from the MB29LV400C and the FLASH Memory interface circuit.

### 12.28.1 Out Line of Flash Memory

The Flash Memory consists of a flash memory unit derived from the MBM29LV400C and a flash memory interface circuit.

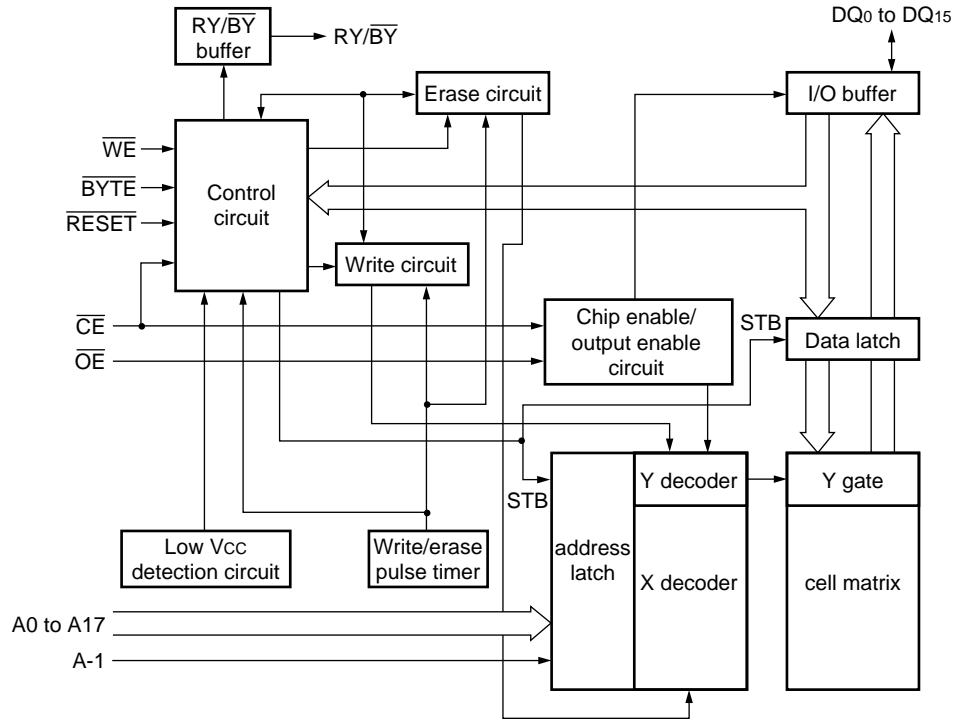
- 512 Kword × 8 bit/256 Kword × 16 bit/128 Kword × 32 bit  
(64 Kbyte × 3 + 32 Kbyte + 8 Kbyte × 2 + 16 Kbyte) sectors
- Uses automatic program algorithm (Embedded Algorithm™\*)
- Erase pause/restart function
- Detects completion of writing/erasing using data polling or toggle bit functions
- Detects completion of writing/erasing by RY/BY pin
- Compatible with JEDEC standard commands
- Performs minimum of 10,000 write/erase operations
- Sector erase function (any combination of sectors)
- Sector protect function
- Temporary sector protect cancellation function
- Allows flash memory interface circuit to write to/erase flash memory both under control of external pin by writer and under control of internal bus by CPU.

\*: Embedded Algorithm™ is a registered trademark of Advanced Micro Devices, Inc.

12.28.2 Block Diagrams of Flash Memory

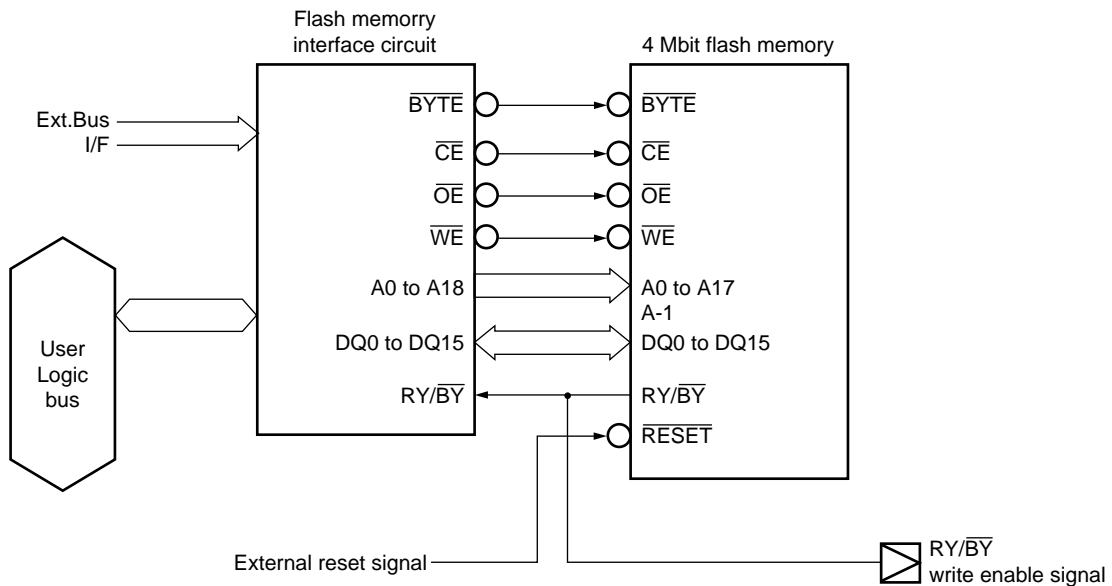
**a: Block Diagram of Flash Memory**

Figure shows the block diagram of the flash memory unit, which has almost the same configuration as the MBM29LV400C.



**b: Entire Block Diagram of Flash Memory**

Figure shows the entire block diagram of the flash memory with the flash memory interface circuit.





**c: Sector Configuration**
**Table 12-7. Write, Byte Read, Half Word Read**

		Flash Memory Mode	Other Modes
8 bit × 2		7FFFF <sub>H</sub>	FFFF <sub>H</sub>
Sector 13	16 KB	7C000 <sub>H</sub>	FC000 <sub>H</sub>
Sector 12	8 KB	7A000 <sub>H</sub>	FA000 <sub>H</sub>
Sector 11	8 KB	78000 <sub>H</sub>	F8000 <sub>H</sub>
Sector 10	32 KB	70000 <sub>H</sub>	F0000 <sub>H</sub>
Sector 9	64 KB	60000 <sub>H</sub>	E0000 <sub>H</sub>
Sector 8	64 KB	50000 <sub>H</sub>	D0000 <sub>H</sub>
Sector 7	64 KB	40000 <sub>H</sub>	C0000 <sub>H</sub>
Sector 6	16 KB	3C000 <sub>H</sub>	BC000 <sub>H</sub>
Sector 5	8 KB	3A000 <sub>H</sub>	BA000 <sub>H</sub>
Sector 4	8 KB	38000 <sub>H</sub>	B8000 <sub>H</sub>
Sector 3	32 KB	30000 <sub>H</sub>	B0000 <sub>H</sub>
Sector 2	64 KB	20000 <sub>H</sub>	A0000 <sub>H</sub>
Sector 1	64 KB	10000 <sub>H</sub>	90000 <sub>H</sub>
Sector 0	64 KB	00000 <sub>H</sub>	80000 <sub>H</sub>

**Table 12-8. Long Word Read**

MSB		LSB		Flash Memory Mode	Other Modes
8 bit × 2		8 bit × 2		7FFFF <sub>H</sub>	FFFF <sub>H</sub>
Sector 13	16 KB	Sector 6	16 KB	78000 <sub>H</sub>	F8000 <sub>H</sub>
Sector 12	8 KB	Sector 5	8 KB	74000 <sub>H</sub>	F4000 <sub>H</sub>
Sector 11	8 KB	Sector 4	8 KB	70000 <sub>H</sub>	F0000 <sub>H</sub>
Sector 10	32 KB	Sector 3	32 KB	60000 <sub>H</sub>	E0000 <sub>H</sub>
Sector 9	64 KB	Sector 2	64 KB	40000 <sub>H</sub>	C0000 <sub>H</sub>
Sector 8	64 KB	Sector 1	64 KB	20000 <sub>H</sub>	A0000 <sub>H</sub>
Sector 7	64 KB	Sector 0	64 KB	00000 <sub>H</sub>	80000 <sub>H</sub>



### 12.28.5 Read/Write Access

In the flash memory mode, read/write access to the flash memory must be under control of the external pins. However, with the CPU access, there are no special timing constraints on read/write access because the flash memory is controlled by the flash memory interface circuit.

In this section, “write access” does not directly mean “program flash memory”. It implies “activation of the flash commands”.

#### a: Read/Write Access in Flash Memory Mode

Next table gives the setting of pins for read/write access in the Flash Memory mode. There is no special problem with control of these pins if connected to a flash memory writer. However, in other cases, timing specifications must be met.

**Table 12-9. Setting Conditions of Pins for Read/Write Access in Flash Memory Mode**

Operations	BGRNTX ( $\overline{\text{CE}}$ )	RDY ( $\overline{\text{OE}}$ )	CS4X ( $\overline{\text{WE}}$ )	A0 to A18	D16 to D31	INIT
Read	L	L	H	Read address	D <sub>OUT</sub>	H
Write	L	H	L	Write address	D <sub>IN</sub>	H
Output disable	L	H	H	x	High-Z	H
Standby	H	x	x	x	High-Z	H
Hardware reset	x	x	x	x	High-Z	L

Note: This table uses pin names from F362GB. Check corresponding pin names of other devices.

#### b: Read Access with CPU

##### Flash Wait Control Register (FMWT)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00007004 <sub>H</sub>	—	—	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0
Access	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	—	0	0	0	0	0	1	1
value after Boot ROM Normal Flash Macro	—	0	0	0	0	0	1	1
value after Boot ROM Fast Flash Macro	—	0	0	1	0	0	1	1

**Normal Flash Macro: Recommended Settings**

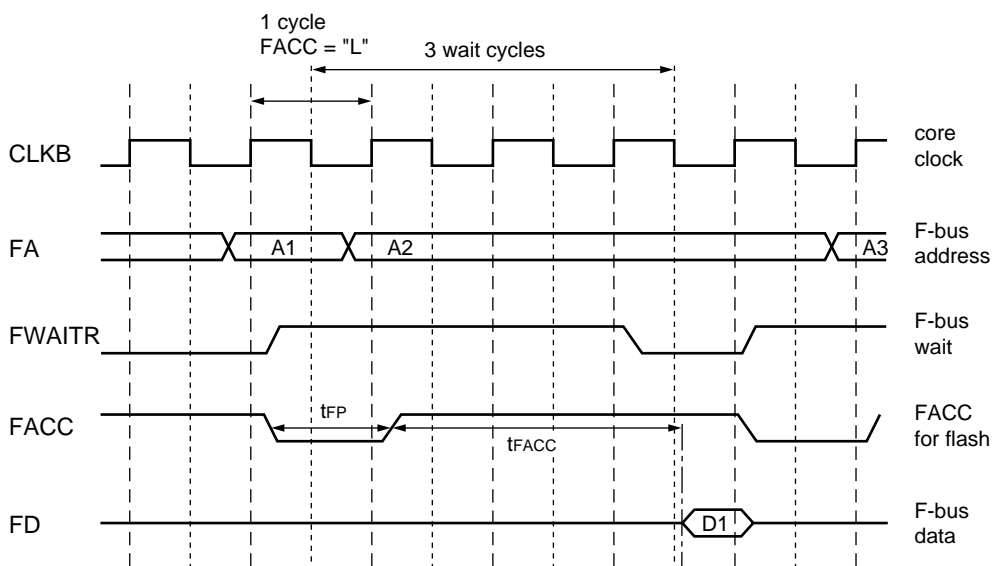
**Table 12-10. Without Applying Clock Modulation**

CLKB Unmodulated Core Clock Frequency [MHz]	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	FACC Low Cycles/Wait Cycles	FMWT
64	0	1	0	0	1	1	1 / 3	13 <sub>H</sub>
48	0	1	0	0	1	1	1 / 3	13 <sub>H</sub>
40	0	1	0	0	1	0	1 / 2	12 <sub>H</sub>
32	0	0	0	0	1	0	0.5 / 2	02 <sub>H</sub>
24	0	0	0	0	0	1	0.5 / 1	01 <sub>H</sub>
16	0	0	0	0	0	1	0.5 / 1	01 <sub>H</sub>

**Table 12-11. When Applying Clock Modulation**

CLKB Core Clock Frequency [MHz]	Peak Max Frequency	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	FACC Low Cycles/Wait Cycles	FMWT
48	64	0	1	0	0	1	1	1 / 3	13 <sub>H</sub>
32	48	0	1	0	0	1	1	1 / 3	13 <sub>H</sub>
24	40	0	1	0	0	1	0	1 / 2	12 <sub>H</sub>
24	32	0	0	0	0	1	0	0.5 / 2	02 <sub>H</sub>
16	24	0	0	0	0	0	1	0.5 / 1	01 <sub>H</sub>

Example for flash memory read access with 1 cycle for the low time of FACC and 3 wait cycles



The minimum value for t<sub>FP</sub> is 15 ns, for t<sub>FACC</sub> it is 40 ns.

**Fast Flash Macro: Recommended Settings**

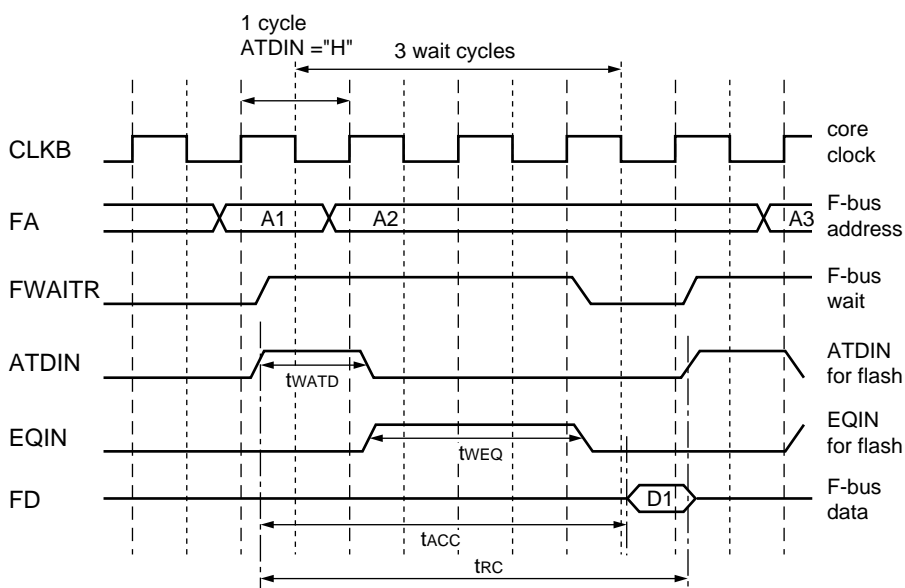
**Table 12-12. Without Applying Clock Modulation**

CLKB Unmodulated Core Clock Frequency [MHz]	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	ATDIN High Cycles/Wait Cycles	FMWT
64	0	1	0	0	1	1	1 / 3	13 <sub>H</sub>
48	0	0	0	0	1	0	0.5 / 2	02 <sub>H</sub>
40	0	0	0	0	1	0	0.5 / 2	02 <sub>H</sub>
32	0	0	1	0	0	1	0.5 / 1	09 <sub>H</sub>
24	0	0	0	0	0	1	0.5 / 1	01 <sub>H</sub>
16	0	0	0	0	0	1	0.5 / 1	01 <sub>H</sub>

**Table 12-13. When Applying Clock Modulation**

CLKB Core Clock Frequency [MHz]	Peak Max Frequency	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	ATDIN High Cycles/Wait Cycles	FMWT
48	64	0	1	0	0	1	1	1 / 3	13 <sub>H</sub>
32	48	0	0	0	0	1	0	0.5 / 2	02 <sub>H</sub>
24	40	0	0	0	0	1	0	0.5 / 2	12 <sub>H</sub>
24	32	0	0	1	0	0	1	0.5 / 1	09 <sub>H</sub>
16	24	0	0	0	0	0	1	0.5 / 1	01 <sub>H</sub>

Example for flash memory read access with 1 cycle for the high time of ATDIN and 3 wait cycles



The minimum value for  $t_{WATD}$  is 10 ns, the minimum value for  $t_{WEQ}$  is 20 ns.

The minimum value for  $t_{RC}$  is 40 ns.

The maximum value for  $t_{ACC}$  is  $t_{WATD} + t_{WEQ} + 5$  ns.

**c: Write Access with CPU**

Recommended settings for WTC2 to WTC0 for write access to the flash memory, FACCEN of FMCS should be set to 1 for writing, so FAC1, FAC0, EQINH bit settings then have no meaning for the write operation

**Table 12-14. Without Applying Clock Modulation**

CLKB Unmodulated Core Clock Frequency [MHz]	WTC2	WTC1	WTC0	Wait Cycles	FMWT
64	setting not allowed for writing				
48	1	0	0	4	X4 <sub>H</sub>
40	1	0	0	4	X4 <sub>H</sub>
32	0	1	0	2	X2 <sub>H</sub>
24	0	1	0	2	X2 <sub>H</sub>
16	0	0	1	1	X1 <sub>H</sub>

**Table 12-15. When Applying Clock Modulation**

CLKB Core Clock Frequency [MHz]	Peak Max Frequency	WTC2	WTC1	WTC0	Wait Cycles	FMWT
48	64	setting not allowed for writing				
32	48	1	0	0	4	X4 <sub>H</sub>
24	40	1	0	0	4	X4 <sub>H</sub>
24	32	0	1	0	2	X2 <sub>H</sub>
16	24	0	1	0	2	X2 <sub>H</sub>

**12.28.6 Automatic Write/Erase**

Irrespective of the Flash Memory mode or other modes, writing to/erasing the flash memory unit is performed by starting the flash memory automatic algorithm.

To start the automatic algorithm, various sequences of write accesses are executed in 1 to 6 cycles. They are called Flash commands.

**a: Flash Commands**

There are four commands for starting the automatic algorithm of the Flash Memory unit; Read/Reset, Write, Chip Erase, and Sector Erase. There are also Erase Suspend and Erase Resume commands for the sector erase operation.

Next tables give the command sequence lists in the flash memory and other modes.

**b: Command Sequence**

**Table 12-16. Command Sequence List (CPU access)**

Command Sequence	Write Cycle of Bus	Write Cycle of First Bus		Write Cycle of Second Bus		Write Cycle of Third Bus		Read/ Write Cycle of Fourth Bus		Write Cycle of Fifth Bus		Write Cycle of Sixth Bus	
		Ad- dress	Data	Ad- dress	Data	Ad- dress	Data	Ad- dress	Data	Ad- dress	Data	Ad- dress	Data
Read/ Reset <sup>a</sup>	1	**xxxx	xxF0	–	–	–	–	–	–	–	–	–	–
Read/ Reset <sup>a</sup>	4	**5554	xxAA	**aaa8	xx55	**5554	xxF0	RA	RD	–	–	–	–
Write	4	**5554	xxAA	**aaa8	xx55	**5554	xxA0	PA (even)	PD (half word)	–	–	–	–
Chip Erase	6	**5554	xxAA	**aaa8	xx55	**5554	xx80	**5554	xxAA	**aaa8	xx55	**5554	xx10
Sector Erase	6	**5554	xxAA	**aaa8	xx55	**5554	xx80	**5554	xxAA	**aaa8	xx55	SA (even)	xx30
Sector Erase Suspend	Input of address **xxxx or data (xxB0 <sub>H</sub> ) suspends sector erasing.												
Sector Erase Resume	Input of address **xxxx or data (xx30 <sub>H</sub> ) suspends and resumes sector erasing.												

a. Two Read/Reset commands reset Flash memory to the read mode.

Addresses in the table are the values in the CPU memory space. All addresses and data are hexadecimal values, where x is any value and \*\* may be 08 to 0F.

**Table 12-17. Command Sequence List (Flash Memory Mode)**

Command Sequence	Write Cycle of Bus	Write Cycle of First Bus		Write Cycle of Second Bus		Write Cycle of Third Bus		Read/ Write Cycle of Fourth Bus		Write Cycle of Fifth Bus		Write Cycle of Sixth Bus	
		Ad- dress	Data	Ad- dress	Data	Ad- dress	Data	Ad- dress	Data	Ad- dress	Data	Ad- dress	Data
Read/ Reset <sup>a</sup>	1	nxxxx	F0	–	–	–	–	–	–	–	–	–	–
Read/ Reset <sup>a</sup>	4	naaaa	AA	n5554	55	naaaa	F0	RA	RD	–	–	–	–
Write	4	naaaa	AA	n5554	55	naaaa	A0	PA (even)	PD (word)	–	–	–	–
Chip Erase	6	naaaa	AA	n5554	55	naaaa	80	naaaa	AA	n5554	55	naaaa	10
Sector Erase	6	naaaa	AA	n5554	55	naaaa	80	naaaa	AA	n5554	55	SA (even)	30
Sector Erase Suspend	Input of address nxxxx or data (B0 <sub>H</sub> ) suspends sector erasing.												
Sector Erase Resume	Input of address nxxxx or data (30 <sub>H</sub> ) suspends and resumes sector erasing.												

a. Two Read/Reset commands reset Flash memory to the read mode.

Addresses in the table are values for writer addresses. All addresses and data are hexadecimal values, where x is any value and n may be 0 to 7.

RA: Read address

PA: Write address. Only even addresses can be specified.

SA: Sector address (See next table). Only even addresses can be specified.

RD: Read data

PD: Write data. Only word data can be specified.

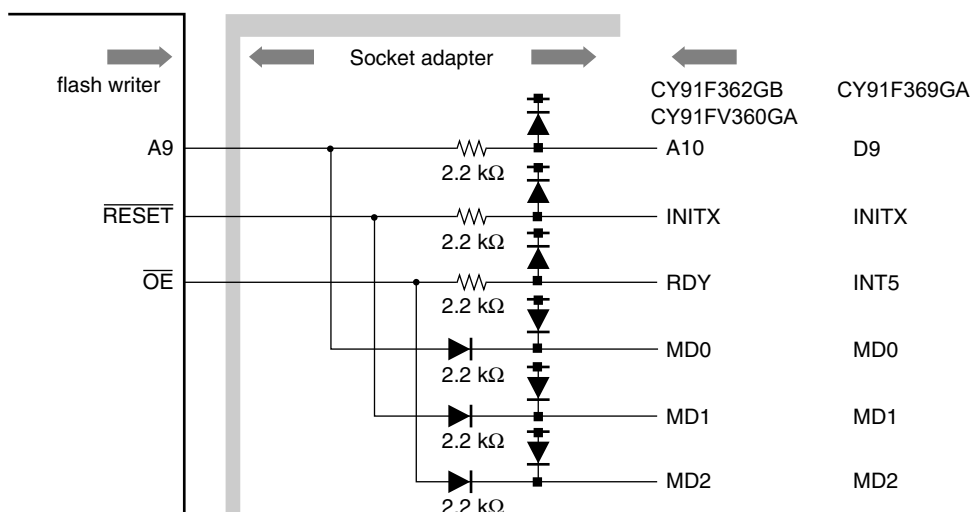
**Table 12-18. Sector Address for Half Word Mode**

Sector	A18	A17	A16	A15	A14	A13	Address Range
SA13	1	1	1	1	1	–	7C000 <sub>H</sub> to 7FFFF <sub>H</sub>
SA12	1	1	1	1	0	1	7A000 <sub>H</sub> to 7BFFF <sub>H</sub>
SA11	1	1	1	1	0	0	78000 <sub>H</sub> to 79FFF <sub>H</sub>
SA10	1	1	1	0	–	–	70000 <sub>H</sub> to 77FFF <sub>H</sub>
SA9	1	1	0	–	–	–	60000 <sub>H</sub> to 6FFFF <sub>H</sub>
SA8	1	0	1	–	–	–	50000 <sub>H</sub> to 5FFFF <sub>H</sub>
SA7	1	0	0	–	–	–	40000 <sub>H</sub> to 4FFFF <sub>H</sub>
SA6	0	1	1	1	1	–	3C000 <sub>H</sub> to 3FFFF <sub>H</sub>
SA5	0	1	1	1	0	1	3A000 <sub>H</sub> to 3BFFF <sub>H</sub>
SA4	0	1	1	1	0	0	38000 <sub>H</sub> to 39FFF <sub>H</sub>
SA3	0	1	1	0	–	–	30000 <sub>H</sub> to 37FFF <sub>H</sub>
SA2	0	1	0	–	–	–	20000 <sub>H</sub> to 2FFFF <sub>H</sub>
SA1	0	0	1	–	–	–	10000 <sub>H</sub> to 1FFFF <sub>H</sub>
SA0	0	0	0	–	–	–	00000 <sub>H</sub> to 0FFFF <sub>H</sub>



### 12.28.7 Connection to Flash Memory

The Flash Memory mode of the CY91360G series devices is intended mainly for external connection to a flash memory writer. As indicated in Table Flash Control Signals, there is a slight difference between the external pins of the CY91360G series devices and the MBM29LV400C (4 Mbit flash memory). Connection to an MBM29LV400C writer requires the socket adapter.



### 12.28.8 Notes to Use of Flash Memory

Notes on the flash memory in CY91360G series devices are given below.

#### a: Input of Hardware Reset (INITX)

To input a hardware reset when the automatic algorithm is not started, where reading is in progress, a minimum of 500 ns should be taken at a low-level width. In this case, a maximum of 500 ns is required until data can be read from the flash memory after a hardware reset has been activated.

Similarly, to input a hardware reset when the automatic algorithm is activated, where writing/erasing is in progress, a minimum of 50 ns should be taken in a low-level width. In this case, 20 μs are required until data can be read after the executing operation has been terminated to initialize the flash memory.

A hardware reset during writing undefined data being written. A hardware reset during erasing may make the sector being erased unusable.

#### b: Canceling Software Reset, Watchdog Timer Reset, and Hardware Standby

When writing/erasing the flash memory with the CPU access and if reset conditions occur while the automatic algorithm is active, the CPU may run away. This occurs because these reset conditions cause the automatic algorithm to continue without initializing the flash memory unit, possibly preventing the flash memory unit from entering the read state when the CPU starts the sequence after the reset has been deasserted. These reset conditions should be inhibited during writing/erasing the Flash Memory.

#### c: Program Access to Flash Memory

When the automatic algorithm is operating, read access to the flash memory is disabled. With the memory access mode of the CPU set to the internal ROM mode, writing/erasing should be started after switching the program area to another area such as RAM.

In this case, when sectors containing interrupt vectors are erased, interrupt processing cannot be executed.

For the same reason, all interrupt sources should be disabled while the automatic algorithm is operating.

**d: Hold Function**

When the CPU accepts a hold request, the Write signal  $\overline{WE}$  of the flash memory unit may be skewed and many cause erroneous writing/erasing. When the acceptance of a hold request is enabled, ensure that the WE bit of the FLASH control status register (FMCS) is 0.

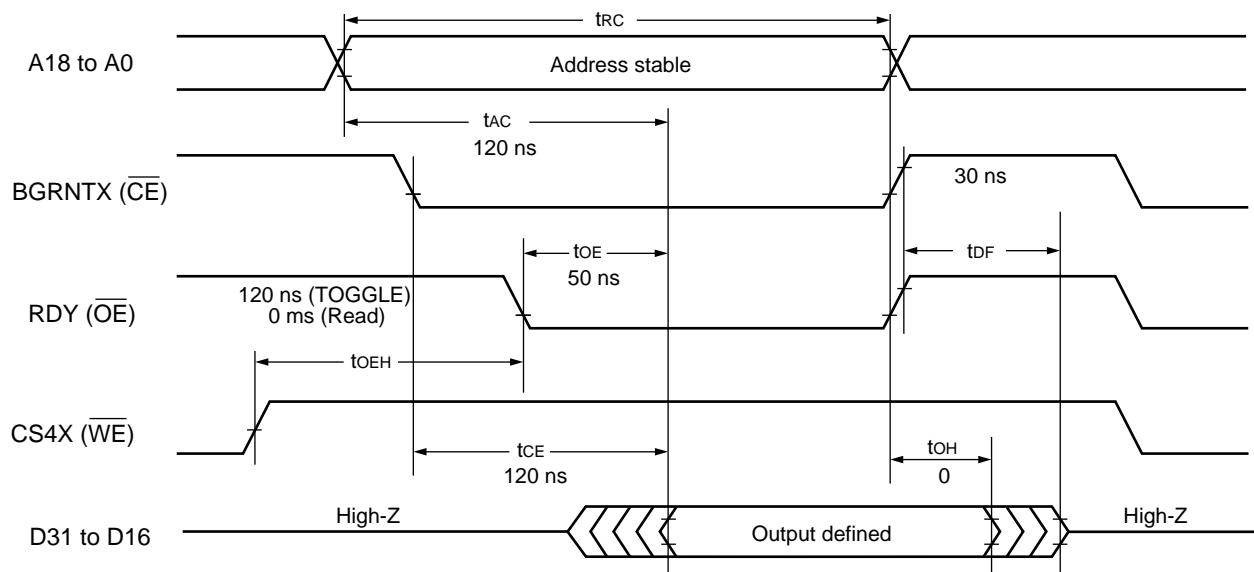
**e: Applying  $V_{ID}$**

Applying  $V_{ID}$  required for the sector protect operation should always be started and terminated when the supply voltage is on.

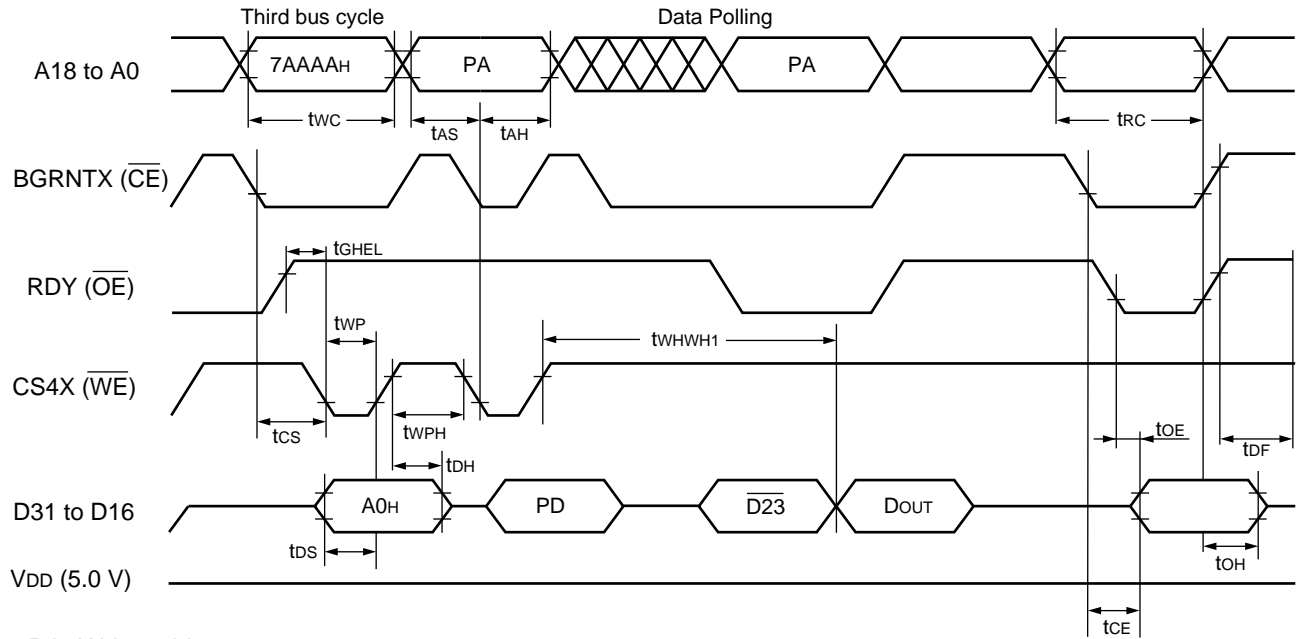
**12.28.9 Timing Diagrams in Flash Mode**

Each timing diagram for the external pins of the CY91360G series in the Flash Memory mode is shown below.

**a: Data read by Read Access**



**b: Write Data Polling Read ( $\overline{WE}$  control)**



PA: Write address

PD: Write data

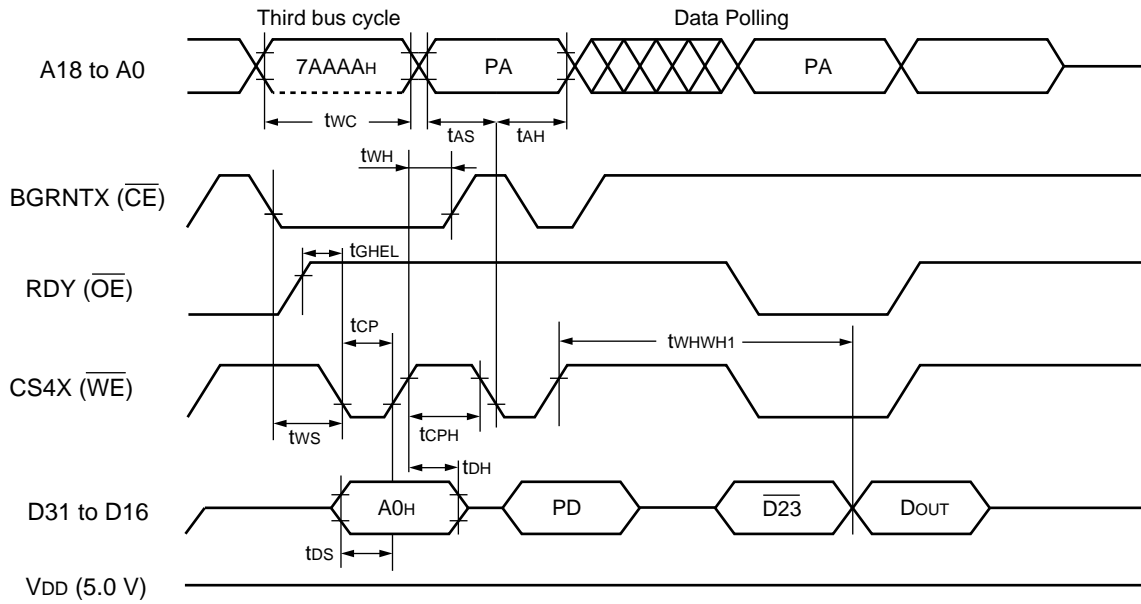
D23: Reverse output of write data

D<sub>OUT</sub>: Output of write data

Note: The last two bus cycle sequences out of the four are described.



c: Write Data Polling Read ( $\overline{CE}$  control)



PA: Write address

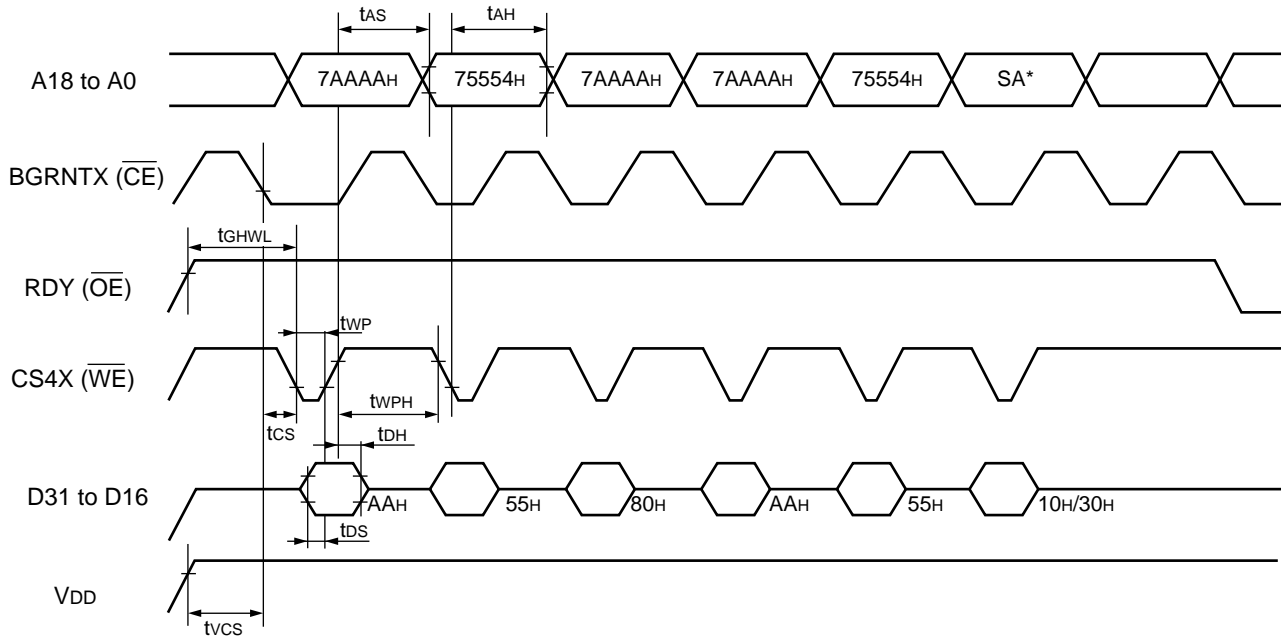
PD: Write data

$\overline{D23}$ : Reverse output of write data

DOUT: Output of write data

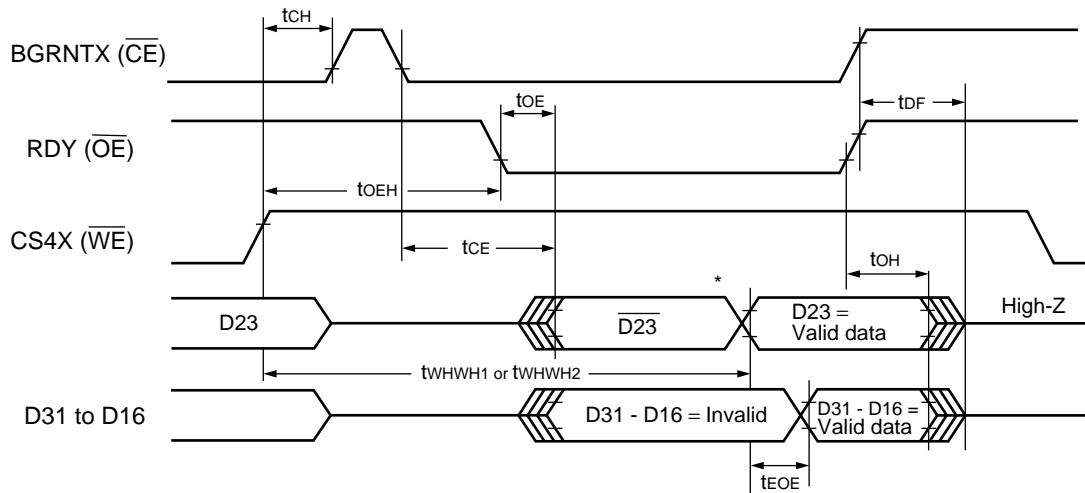
Note: The last two bus cycle sequences out of the four are described.

**d: Chip Erase/Sector Erase Command Sequence**



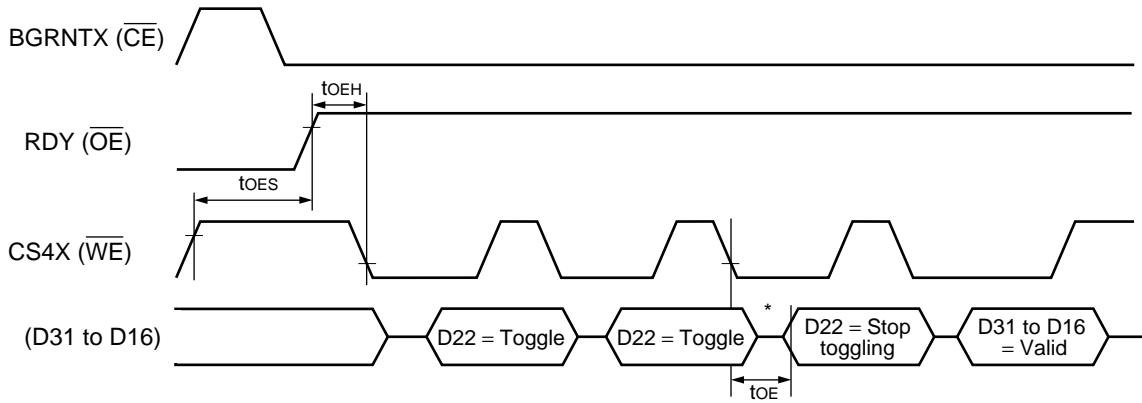
Note: SA is the sector address at sector erasing. 7AAAA<sub>H</sub> (or 6AAAA<sub>H</sub>) is the address at chip erasing.

**e: Data Polling**



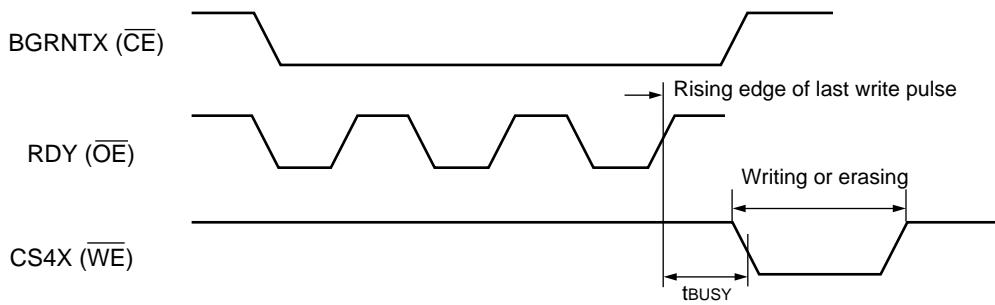
\*: DQ7 is valid data (The device terminates automatic operation).

**f: Toggle Bit**

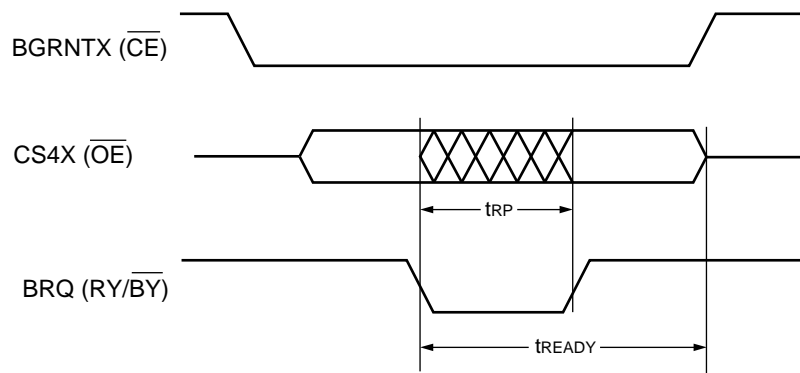


\*: DQ6 stops toggling (The device terminates automatic operation).

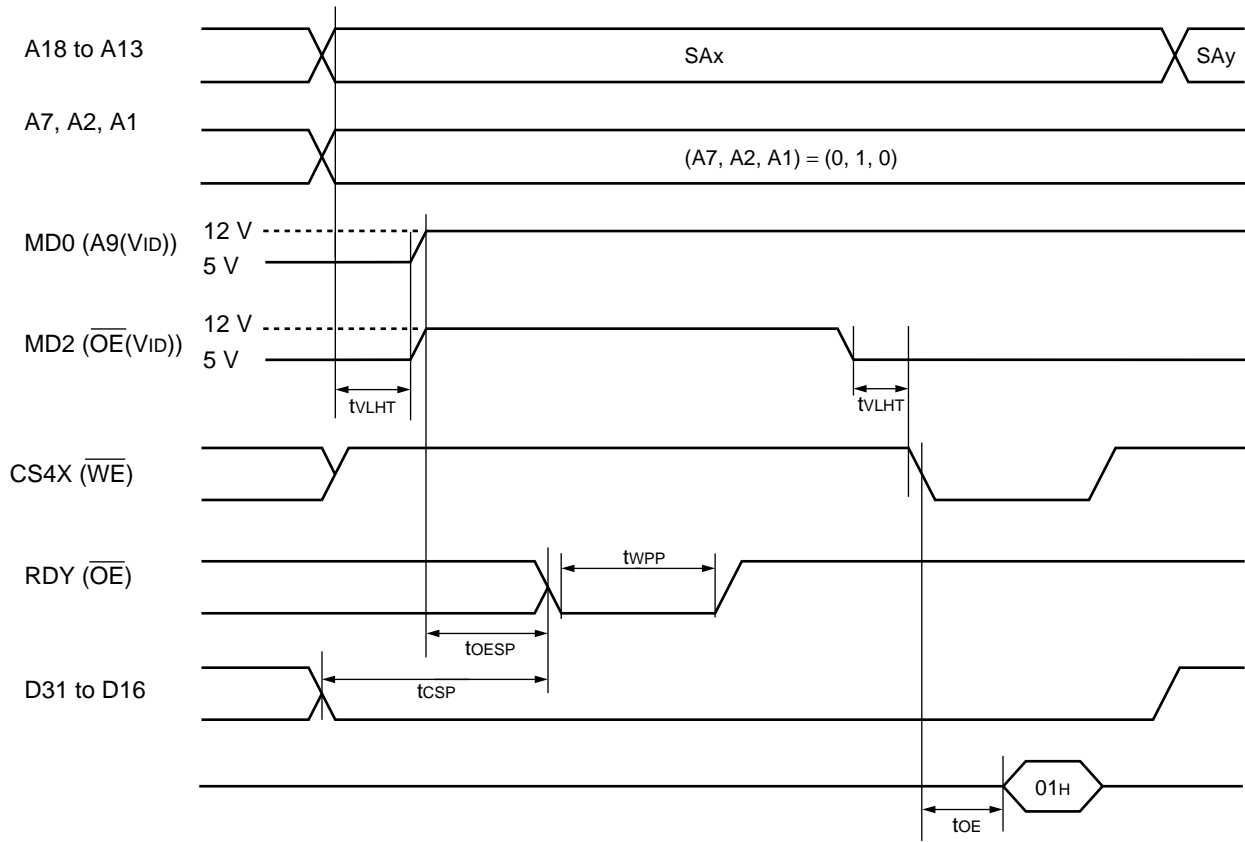
**g: RY/BY Timing during Writing/Erasing**



**h: INITX and RY/BY Timing**

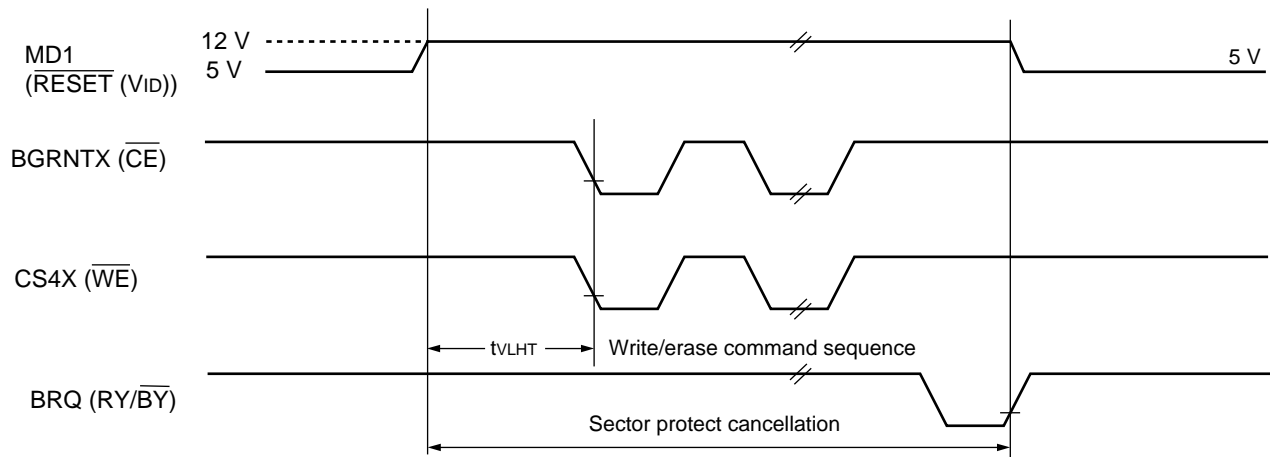


**i: Enable Sector Protect/Verify Sector Protect**



SA<sub>x</sub>: First sector address  
 SA<sub>y</sub>: Next sector address

**j: Temporary Sector Protect Cancellation**





12.28.10 AC Characteristics in Flash Memory Mode

The AC specifications for the external pins of the CY91360G series in the Flash Memory mode are shown below. They apply to the case where the user performs read/write access in the Flash Memory mode. They are not needed for access in the normal mode and for use of a flash memory writer.

The values are subject to change without prior notice.

**a: Read Access**

**Table 12-19. AC Characteristics for Read Access**

(Under recommended conditions)

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Read cycle time	$t_{RC}$	–	120	–	–	ns
Address access time	$t_{ACC}$	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	–	–	120	ns
$\overline{CE}$ to data output	$t_{CE}$	$\overline{OE} = V_{IL}$	–	–	120	ns
$\overline{OE}$ to data output	$t_{OE}$	–	–	–	50	ns
$\overline{CE}$ to output floating	$t_{DF}$	–	–	–	30	ns
$\overline{OE}$ to output floating	$t_{DF}$	–	–	–	30	ns
Previous cycle data output hold time	$t_{OH}$	–	0	–	–	ns
INITX pin to return to read mode	$t_{Ready}$	–	–	–	20	$\mu$ s

**b: Write [write/erase command] access ( $\overline{WE}$  control)**

**Table 12-20. AC Characteristics for Write Access ( $\overline{WE}$  Control)**

(Under recommended conditions)

Parameter	Symbol	Value			Unit	
		Min	Typ	Max		
Write cycle time	$t_{WC}$	120	–	–	ns	
Address setup time	$t_{AS}$	0	–	–	ns	
Address hold time	$t_{AH}$	50	–	–	ns	
Data setup time	$t_{DS}$	50	–	–	ns	
Data hold time	$t_{DH}$	0	–	–	ns	
Output enable setup time	$t_{OES}$	0	–	–	ns	
Output enable hold time	Read	$t_{OEH}$	0	–	–	ns
	Toggle and data polling		10	–	–	ns
Read recovery time before write	$t_{GHWL}$	0	–	–	ns	
$\overline{CE}$ setup time	$t_{CS}$	0	–	–	ns	
$\overline{CE}$ hold time	$t_{CH}$	0	–	–	ns	
Write pulse width	$t_{WP}$	50	–	–	ns	
Write pulse width High level	$t_{WPH}$	20	–	–	ns	
Write continuation time	$t_{WHWH1}$	–	8	–	$\mu$ s	
Sector erase continuation time*1	$t_{WHWH2}$	–	1	15	s	
$V_{CC}$ setup time	$t_{VCS}$	50	–	–	$\mu$ s	

**Table 12-20. AC Characteristics for Write Access ( $\overline{WE}$  Control)**

(Under recommended conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Voltage transition time*2	$t_{VLHL}$	4	–	–	$\mu\text{s}$
Write pulse width*2	$t_{WPP}$	100	–	–	$\mu\text{s}$
OE setup time for validating $\overline{WE}$ *2	$t_{OESP}$	4	–	–	$\mu\text{s}$
CE setup time for validating $\overline{WE}$ *2	$t_{CSP}$	4	–	–	$\mu\text{s}$
$\overline{INIT}$ pulse width	$t_{RP}$	500	–	–	ns
$\overline{RY}/\overline{BY}$ delay until write/erase is enabled	$t_{BUSY}$	50	–	–	ns

\*1: The internal preprogramming time before erasing is not included.

\*2: Applies only to sector protection

**c: Write [write/erase command] access ( $\overline{CE}$  control)**

**Table 12-21. AC Characteristics for Write Access ( $\overline{CE}$  Control)**

(Under recommended conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Write cycle time	$t_{WC}$	120	–	–	ns
Address setup time	$t_{AS}$	0	–	–	ns
Address hold time	$t_{AH}$	50	–	–	ns
Data setup time	$t_{DS}$	50	–	–	ns
Data hold time	$t_{DH}$	0	–	–	ns
Output enable setup time	$t_{OES}$	0	–	–	ns
Output enable hold time	Read	$t_{OEH}$	0	–	ns
		Toggle and data polling	10	–	ns
Read recovery time before write	$t_{GHWL}$	0	–	–	ns
$\overline{WE}$ setup time	$t_{WS}$	0	–	–	ns
$\overline{WE}$ hold time	$t_{WH}$	0	–	–	ns
$\overline{CE}$ pulse width	$t_{CP}$	50	–	–	ns
$\overline{CE}$ pulse width High level	$t_{CPH}$	20	–	–	ns
Write continuation time	$t_{WHWH1}$	–	16	–	$\mu\text{s}$
Sector erase continuation time*	$t_{WHWH2}$	–	1.5	30	s
$V_{CC}$ setup time	$t_{VCS}$	50	–	–	$\mu\text{s}$
$\overline{INIT}$ pulse width	$t_{RP}$	500	–	–	ns
$\overline{RY}/\overline{BY}$ delay until write/erase is enabled	$t_{BUSY}$	50	–	–	ns

\*: The internal preprogramming time before erasing is not included.

### 13. Flash Memory Mode Signal Assignment

#### CY91FV360GA/F362GB/F364G/F369GA

Table 13-1. Pins Used in Flash Memory Mode

MBM29LV 400C	CY91FV360GA		CY91F362GB		CY91F364G		CY91F369GA		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
A-1	202	A0	9	A0	92	PR0	157	A0	Address A(0)
A0	310	A1	10	A1	93	PR1	158	A1	Address A(1)
A1	201	A2	11	A2	94	PR2	159	A2	Address A(2)
A2	357	A3	12	A3	95	PR3	160	A3	Address A(3)
A3	257	A4	13	A4	96	PR4	136	D15	Address A(4)
A4	144	A5	14	A5	97	PR5	135	D14	Address A(5)
A5	309	A6	15	A6	98	PR6	134	D13	Address A(6)
A6	256	A7	16	A7	99	PR7	133	D12	Address A(7)
A7	200	A8	17	A8	102	LED0	132	D11	Address A(8)
A8	356	A9	18	A9	103	LED1	131	D10	Address A(9)
A9	308	A10	19	A10	104	LED2	130	D9	Address A(10)
A10	92	A11	20	A11	105	LED3	129	D8	Address A(11)
A11	44	A12	21	A12	107	LED4	128	D7	Address A(12)
A12	255	A13	22	A13	108	LED5	127	D6	Address A(13)
A13	143	A14	23	A14	109	LED6	126	D5	Address A(14)
A14	199	A15	24	A15	110	LED7	125	D4	Address A(15)
A15	307	A16	27	A16	113	PO4	124	D3	Address A(16)
A16	91	A17	28	A17	114	PO5	123	D2	Address A(17)
A17	142	A18	29	A18	115	PO6	122	D1	Address A(18)
A18	–	–	–	–	–	–	121	D0	See notes
[A20]	–	–	–	–	117	DA0	–	–	See notes
WE	140	CS4X	32	CS4X	116	PO7	72	INT4	Write enabled
BYTE	196	CS5X	33	CS5X	2	AN1	71	INT3	Byte access
OE	305	RDY	35	RDY	54	TESTX	73	INT5	Output enabled
CE	139	BGRNTX	36	BGRNTX	55	CPUTESTX	69	INT1	Chip enabled
RY/BY	88	BRQ	37	BRQ	56	ATGX	68	INT0	Ready/Busy (open drain)
A9 (V <sub>ID</sub> )	293	MD0	111	MD0	57	MD0	58	MD0	VDA9 High voltage
RESET (V <sub>ID</sub> )	31	MD1	112	MD1	58	MD1	59	MD1	VDRS High voltage
OE (V <sub>ID</sub> )	239	MD2	113	MD2	59	MD2	60	MD2	VDOE High voltage
RESET	30	INITX	115	INITX	60	INITX	62	INITX	Reset
DQ0	46	D16	201	D16	44	IN0	139	D16	Data I/O
DQ1	95	D17	202	D17	45	IN1	140	D17	Data I/O

**Table 13-1. Pins Used in Flash Memory Mode (continued)**

MBM29LV 400C	CY91FV360GA		CY91F362GB		CY91F364G		CY91F369GA		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
DQ2	1	D18	203	D18	46	IN2	141	D18	Data I/O
DQ3	148	D19	204	D19	47	IN3	142	D19	Data I/O
DQ4	205	D20	205	D20	48	OUT0	143	D20	Data I/O
DQ5	45	D21	206	D21	49	OUT1	144	D21	Data I/O
DQ6	94	D22	207	D22	50	OUT2	145	D22	Data I/O
DQ7	260	D23	208	D23	51	OUT3	146	D23	Data I/O
DQ8	312	D24	1	D24	34	INT0	147	D24	Data I/O
DQ9	204	D25	2	D25	35	INT1	148	D25	Data I/O
DQ10	147	D26	3	D26	36	INT2	149	D26	Data I/O
DQ11	93	D27	4	D27	37	INT3	150	D27	Data I/O
DQ12	259	D28	5	D28	38	INT4	151	D28	Data I/O
DQ13	203	D29	6	D29	39	INT5	152	D29	Data I/O
DQ14	146	D30	7	D30	40	INT6	153	D30	Data I/O
DQ15	258	D31	8	D31	41	INT7	154	D31	Data I/O
[TMODX]	89	CS6X	34	CS6X	118	DA1	70	INT2	Test mode Pull-up
[ATDIN]	253	DREQ2	–	–	1	AN0	74	INT6	ATD test Pull-down
[EQIN]	42	A26	–	–	90	LTESTX	75	INT7	EQ test Pull-down

**Notes:**
**■ CY91F362GB:**

A19 (pin 30) and A20 (pin 32) must be pulled “L” level in Flash Memory Mode.  
 At reading from Flash memory, D0 to D15 (p183 to pin 197, pin 200) are switched to the output mode.  
 See “Pins not used in flash memory mode (CY91F362GB)”.

**■ CY91F364G:**

DA0 (pin 117) must be pulled “H” level in Flash Memory Mode.

**■ CY91F369GA:** Pin 70 must be pulled “H” level in Flash Memory Mode. Also, pin 74 and pin 75 must be pulled “L” level in Flash Memory Mode.

ALARM (pin 54) must be pulled “L” level.  
 The other pins should be set to open at Flash Memory Mode.

**Table 13-2. Pins Not Used in Flash Memory Mode (CY91F362GB)**

CY91F362GB			Remarks
Pin No.	Normal Function	Flash Memory Mode	
75, 76	DA0, DA1	Output	Open
77	ALARM	Input	Pull-down
81 to 83	TESTX, CPUTESTX, LTESTX	Input	Pull-up or open (Initial pull-up)
114	HSTX	Input	Pull-up or open (Initial pull-up)
116	MONCLK	Output	Open
117	SELCLK	Input	Pull-up
119, 121	X0, X0A	Input	Pull-down
120, 122	X1, X1A	Output	Open
124	CPO	Output	Open
125	VCI	Input	Pull-down
Other signal		Input	Pull-up

**CY91F365GB/F366GB/F367GB/F368GB/F376G**
**Table 13-3. Pins Used in Flash Memory Mode**

MBM29LV 400C	CY91F365GB/ CY91F366GB		CY91F367GB/ CY91F368GB		CY91F376G		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
A-1	96	PWM1P0	96	PR0	96	PWM1P0	Address A(0)
A0	97	PWM1M0	97	PR1	97	PWM1M0	Address A(1)
A1	98	PWM2P0	98	PR2	98	PWM2P0	Address A(2)
A2	99	PWM2M0	99	PR3	99	PWM2M0	Address A(3)
A3	101	PWM1P1	101	PR4	101	PWM1P1	Address A(4)
A4	102	PWM1M1	102	PR5	102	PWM1M1	Address A(5)
A5	103	PWM2P1	103	PR6	103	PWM2P1	Address A(6)
A6	104	PWM2M1	104	PR7	104	PWM2M1	Address A(7)
A7	106	PWM1P2	106	PS0	106	PWM1P2	Address A(8)
A8	107	PWM1M2	107	PS1	107	PWM1M2	Address A(9)
A9	108	PWM2P2	108	PS2	108	PWM2P2	Address A(10)
A10	109	PWM2M2	109	PS3	109	PWM2M2	Address A(11)
A11	111	PWM1P3	111	PS4	111	PWM1P3	Address A(12)
A12	112	PWM1M3	112	PS5	112	PWM1M3	Address A(13)
A13	113	PWM2P3	113	PS6	113	PWM2P3	Address A(14)
A14	114	PWM2M3	114	PS7	114	PWM2M3	Address A(15)
A15	91	PG3	91	PG3	91	PG3	Address A(16)
A16	92	PG4	92	PG4	92	PG4	Address A(17)
A17	93	PG5	93	PG5	93	PG5	Address A(18)
A18	–	–	–	–	89	PG1	Address A(19)
[A20]	–	–	–	–	88	PG0	Pull-up See note
WE	31	BOOT	31	BOOT	31	BOOT	Write enabled
BYTE	32	TESTX	32	TESTX	32	TESTX	Byte access
OE	51	IN1	51	IN1	51	IN1	Output enabled
CE	50	IN0	50	IN0	50	IN0	Chip enabled
RY/ $\overline{\text{BY}}$	38	MONCLK	38	MONCLK	38	MONCLK	Ready/ $\overline{\text{Busy}}$ (open drain)
A9 ( $V_{\text{ID}}$ )	57	MD0	57	MD0	57	MD0	VDA9 High voltage
$\overline{\text{RESET}}$ ( $V_{\text{ID}}$ )	58	MD1	58	MD1	58	MD1	VDRS High voltage
$\overline{\text{OE}}$ ( $V_{\text{ID}}$ )	59	MD2	59	MD2	59	MD2	VDOE High voltage
RESET	60	INITX	60	INITX	60	INITX	Reset
DQ0	117	PJ0	117	PJ0	117	PJ0	Data I/O
DQ1	118	PJ1	118	PJ1	118	PJ1	Data I/O
DQ2	119	PJ2	119	PJ2	119	PJ2	Data I/O
DQ3	120	PJ3	120	PJ3	120	PJ3	Data I/O

**Table 13-3. Pins Used in Flash Memory Mode**

MBM29LV 400C	CY91F365GB/ CY91F366GB		CY91F367GB/ CY91F368GB		CY91F376G		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
DQ4	52	IN2	52	IN2	52	IN2	Data I/O
DQ5	53	IN3	53	IN3	53	IN3	Data I/O
DQ6	54	OUT0	54	OUT0	54	OUT0	Data I/O
DQ7	55	OUT1	55	OUT1	55	OUT1	Data I/O
DQ8	39	INT0	39	INT0	39	INT0	Data I/O
DQ9	40	INT1	40	INT1	40	INT1	Data I/O
DQ10	41	INT2	41	INT2	41	INT2	Data I/O
DQ11	42	INT3	42	INT3	42	INT3	Data I/O
DQ12	43	INT4	43	INT4	43	INT4	Data I/O
DQ13	44	INT5	44	INT5	44	INT5	Data I/O
DQ14	45	INT6	45	INT6	45	INT6	Data I/O
DQ15	46	INT7	46	INT7	46	INT7	Data I/O
[TMODX]	33	CPUTESTX	33	CPUTESTX	33	CPUTESTX	Test mode Pull-up
[ATDIN]	63	SOT4	63	SOT4	63	SOT4	ATD test Pull-down
[EQIN]	90	PG2	90	PG2	90	PG2	EQ test Pull-down

Note: CY91F376G: At using for 768KB Flash macro, A18 is used as the append input pin of Flash macro. Line (A20) which is connected to pin 88 (PG0) should be set to “H” level.

**Table 13-4. Pins Not Used in Flash Memory Mode (CY91F365GB/F366GB/F367GB/F368GB/F376G)**

CY91F365GB/F366GB/F367GB/F368GB/F376G			Remarks
Pin No.	Normal Function	Pin State	
35	X0	Input	Pull-up
36	X1	Output	Open
66	SIN3	Output	Open
67	SOT3	Output	Open
68	SCK3	Output	Open
27	DA0/X0A	Output/Input	Open/Pull-up
28	DA1/X1A	Output	Open
29	ALARM	Input	Pull-up
Other signal		Input	Pull-up

## 14. Electrical Characteristics

### 14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Condition
		Min	Max		
Digital supply voltage	$V_{DD}-V_{SS}$	-0.3	+6.0	V	
External interface supply	$V_{DD35}-V_{SS}$	-0.3	+6.0	V	*4
Stepper motor control supply voltage	$HV_{DD}-HV_{SS}$	-0.3	+6.5	V	
Storage temperature	Tstg	-55	+125	°C	
Power consumption	$P_{TOT}$	-	*3	W	$T_A = +25^{\circ}\text{C}$
Digital input voltage	$V_{DIG}$	-0.3*1	+5.8	V	$V_{SS} = 0\text{ V}, V_{DD} = 5\text{ V}$
Analog input voltage	$V_{IA}$	-0.3	+5.8	V	$AV_{SS} = 0\text{ V}, AV_{CC} = 5\text{ V}$
Analog supply voltage	$AV_{CC}-AV_{SS}$	-0.3	+5.8	V	$AV_{SS} = 0\text{ V}$
Analog reference voltage	$V_{REFH/L}-V_{SSA}$	-0.3	+5.8	V	$AV_{SS} = 0\text{ V}$
Static DC current into digital I/O	$I_{/ODC}$	-2.0	+2.0	mA	$\sum I_{/ODC} < I_{SRUN}, *2$
Static total DC current into digital I/O	$\sum  I_{/ODC} $	-	20	mA	*2

\*1: Making full use of the allowed static DC current into digital I/O will lead to lower values for  $V_{DIG}$  Min.

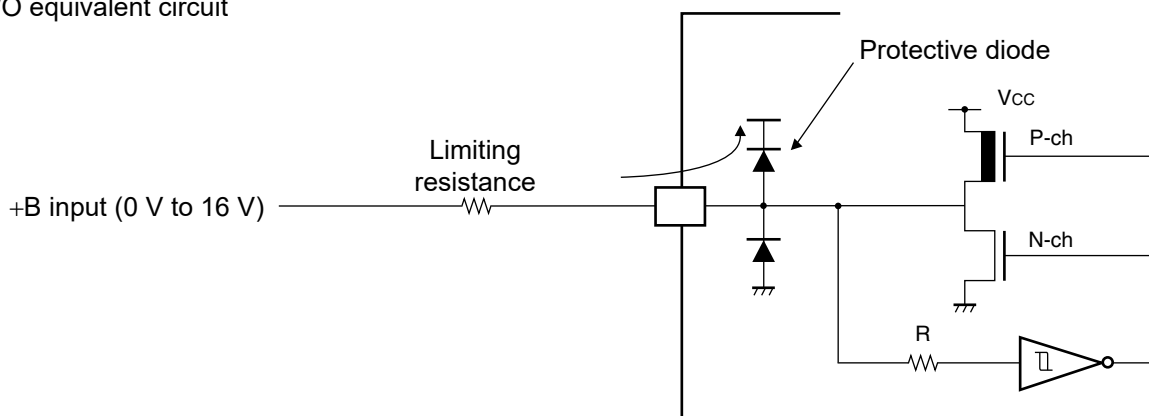
\*2:

- Applicable to pins: D0 to D31, A0 to A20, CS0X to CS6X, RDY, BGRNTX, BRQ, RDX, WR0X to WR3X, AS, ALE, CLK, DREQ0, DACK0, DEOP0, INT0 to INT7, SGO, SGA, SDA, SCL, SOT0, SIN0, SCK0, OCPA0 to OCPA3, TX0, TX1, RX0, RX1, SOT3, SOT4, SIN3, SIN4, SCK3, SCK4, LED0 to LED7 (CY91F362GB only), IN0 to IN3 (CY91F362GB only), OUT0 to OUT3 (CY91F362GB only), OCPA4 to OCPA7 (CY91F362GB only), SOT1, SOT2 (CY91F362GB only), SIH1, SIH2 (CY91F362GB only), SCK1, SCK2 (CY91F362GB only), PWM1P0 to PWM1P3 (CY91F362GB only), PWM1M0 to PWM1M3 (CY91F362GB only), PWM2P0 to PWM2P3 (CY91F362GB only), PWM2M0 to PWM2M3 (CY91F362GB only)
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.



■ Sample recommended circuits

- I/O equivalent circuit



\*3: Dependent on each product (see Maximum power consumption)

\*4: The external interface on CY91F362GB and CY91F369GA can be operated with low voltage (typical 3.3 V) at the V<sub>DD35</sub> pins.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**Table 14-1. Maximum Power Consumption**

Device	Maximum Power Consumption
CY91FV360GA	2.5 W
CY91F362GB	2.5 W
CY91F364G	1.2 W
CY91F376G	1.2 W
CY91F369GA	2.5 W

Device	Maximum Power Consumption
CY91F365GB	1.3 W
CY91F366GB	1.3 W
CY91F367GB	1.3 W
CY91F368GB	1.3 W
CY91366GA	1.3 W

**Table 14-2. Absolute Maximum I/O Output Current**

Parameter	Symbol	Rating		Unit	I/O Circuit Type/ Remark
		Min	Max		
“L” level maximum output current *1	IOL1	–	15	mA	*3
	IOL2	–	35	mA	J (LED)
	IOL3	–	40	mA	K, M (SMC)
	IOL4	–	10	mA	Y, TA (I <sup>2</sup> C)
	IOL5	–	20	mA	Q1 (MONCLK)
“L” level average output current *2	IOLAV1	–	4	mA	*3
	IOLAV2	–	24	mA	J (LED)
	IOLAV3	–	30	mA	K, M (SMC)
	IOLAV4	–	3	mA	Y, TA (I <sup>2</sup> C)
	IOLAV5	–	8	mA	Q1 (MONCLK)

**Table 14-2. Absolute Maximum I/O Output Current (continued)**

Parameter	Symbol	Rating		Unit	I/O Circuit Type/ Remark
		Min	Max		
“L” level total output current	$\Sigma$ IOL1	–	100	mA	*3
	$\Sigma$ IOL2	–	100	mA	J (LED)
	$\Sigma$ IOL3	–	240	mA	K, M (SMC)
	$\Sigma$ IOL4	–	–	mA	Y, TA (I <sup>2</sup> C) *4
	$\Sigma$ IOL5	–	–	mA	Q1 (MONCLK) *4
“L” level total average output current *2	$\Sigma$ IOLAV1	–	50	mA	*3
	$\Sigma$ IOLAV2	–	50	mA	J (LED)
	$\Sigma$ IOLAV3	–	155	mA	K, M (SMC)
	$\Sigma$ IOLAV4	–	–	mA	Y, TA (I <sup>2</sup> C) *4
	$\Sigma$ IOLAV5	–	–	mA	Q1 (MONCLK) *4
“H” level maximum output current *1	IOH1	–	–15	mA	*3
	IOH2	–	–25	mA	J (LED)
	IOH3	–	–40	mA	K, M (SMC)
	IOH4	–	–10	mA	Y, TA (I <sup>2</sup> C) *4
	IOH5	–	–20	mA	Q1 (MONCLK) *4
“H” level average output current *2	IOHAV1	–	–4	mA	*3
	IOHAV2	–	–14	mA	J (LED)
	IOHAV3	–	–30	mA	K, M (SMC)
	IOHAV4	–	–3	mA	Y, TA (I <sup>2</sup> C)
	IOHAV5	–	–8	mA	Q1 (MONCLK)
“H” level total output current	$\Sigma$ IOH1	–	–100	mA	*3
	$\Sigma$ IOH2	–	–50	mA	J (LED)
	$\Sigma$ IOH3	–	–240	mA	K, M (SMC)
	$\Sigma$ IOH4	–	–	mA	Y, TA (I <sup>2</sup> C) *4
	$\Sigma$ IOH5	–	–	mA	Q1 (MONCLK) *4
“H” level total average output current *2	$\Sigma$ IOHAV1	–	–50	mA	*3
	$\Sigma$ IOHAV2	–	–25	mA	J (LED)
	$\Sigma$ IOHAV3	–	–155	mA	K, M (SMC)
	$\Sigma$ IOHAV4	–	–	mA	Y, TA (I <sup>2</sup> C) *4
	$\Sigma$ IOHAV5	–	–	mA	Q1 (MONCLK) *4

\*1: Maximum output current means peak current.

\*2: Average output current = operating current x operating efficiency

\*3: All I/O circuit types not specially mentioned.

\*4: No total current values because there are only 2 pins for I<sup>2</sup>C and one for MONCLK.  
 For an overview of the I/O circuit types, see [I/O Circuit Type](#).

## 14.2 Recommended Operating Conditions

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Operating temperature		$T_A$	-40	-	+85	°C	Other than CY91F364G
			-40	-	+105		CY91F364G, *2
Supply voltage (Internal voltage regulator)	Digital supply	$V_{DD} - V_{SS}$	4.25*1	5	5.25	V	$V_{DDCORE} = 3.3\text{ V}$
	Stepper motor control supply	$HV_{DD} - HV_{SS}$	4.75	5	5.25	V	$HV_{SS} = 0\text{ V}$
	Analog supply	$V_{DDA} - V_{SSA}$	4.9	5	5.1	V	$V_{SSA} = 0\text{ V}$
	External interface supply	$V_{DD35} - V_{SS}$	3.0	3.5	3.6	V	*3
4.25			5	5.25			
RAM data retention voltage		$V_{DD} - V_{SS}$	3.0	-	-	V	

\*1: This is only valid if the integrated power-down reset circuit is switched-off, else a reset can be triggered at voltages less or equal than 4.5 V.

The minimum voltage is 4.75 V during operation at 64 MHz.

\*2: The external interface on CY91F362GB and CY91F369GA can be operated with low voltage (typical 3.3 V) at the  $V_{DD35}$  pins.

\*3: CY91F364G can be used at  $T_A = +85\text{ °C}$  to  $+105\text{ °C}$  under the following conditions.

- The maximum frequency of core clock ( $f_{CLKS}$ ) must not exceed 48 MHz.
- The total current consumption inclusive pads must not exceed 125 mA  
(The core current needs approx. 90 mA at 48 MHz).

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

### 14.3 DC Characteristics

Parameter		Symbol	Value			Unit	Condition	
			Min	Typ	Max			
Current consumption	Run mode	$I_{srun}$	–	–	*1	mA	$T_A = +25\text{ }^\circ\text{C}$	
	Sleep mode	CY91F364G	$I_{ssleep}$	–	50 40	80 60	mA mA	64 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *4 48 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *5
		CY91F376G	$I_{ssleep}$	–	60 50	120 *6 100 *6	mA mA	64 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *4 48 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *5
		CY91FV360GA	$I_{ssleep}$	–	200 165	250 200	mA mA	64 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *4 48 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *5
		all other devices	$I_{ssleep}$	–	145 110	170 140	mA mA	64 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *4 48 MHz, $T_A = +25\text{ }^\circ\text{C}$ , *5
	RTC mode	$I_{sRTC}$	–	0.5 –	1.25 500	mA $\mu\text{A}$	Main clock frequency = 4 MHz $T_A = +25\text{ }^\circ\text{C}$ Subclock frequency = 32 kHz $T_A = +25\text{ }^\circ\text{C}$	
Stop mode	$I_{sstop}$	–	10	200	$\mu\text{A}$	Oscillation stop $T_A = +25\text{ }^\circ\text{C}$ At Software Standby		
Stepper motor control	H-port output voltage	$V_{OHH}$	$HV_{DD} - 500$	–	$HV_{DD} - 125$	mV	$I_{ol} = \pm 30\text{ mA}$ , $T_c = +25\text{ }^\circ\text{C}$	
		$V_{OHL}$	$HV_{SS} + 125$	–	$HV_{SS} + 500$	mV	$I_{ol} = \pm 30\text{ mA}$ , $T_c = +25\text{ }^\circ\text{C}$	
		$V_{OHH}$	$HV_{DD} - 500$	–	$HV_{DD} - 125$	mV	$I_{ol} = \pm 27\text{ mA}$ , $T_c = +85\text{ }^\circ\text{C}$	
		$V_{OHL}$	$HV_{SS} + 125$	–	$HV_{SS} + 500$	mV	$I_{ol} = \pm 27\text{ mA}$ , $T_c = +85\text{ }^\circ\text{C}$	
		$V_{OHH}$	$HV_{DD} - 500$	–	$HV_{DD} - 125$	mV	$I_{ol} = \pm 30\text{ mA}$ , $T_c = -40\text{ }^\circ\text{C}$	
		$V_{OHL}$	$HV_{SS} + 125$	–	$HV_{SS} + 500$	mV	$I_{ol} = \pm 30\text{ mA}$ , $T_c = -40\text{ }^\circ\text{C}$	
	SMC comparator threshold voltage	$V_{THcomp}$	$HV_{DD} / 9 - 70$	$HV_{DD} / 9$	$HV_{DD} / 9 + 70$	mV		
	Slew rate	–	–	40	–	ns	Load = 0 pF	
Alarm comparator	Threshold voltage	Over-voltage	$V_{TAH}$	$^{4/5} V_{DDA} - 5\%$	$^{4/5} V_{DDA}$	$^{4/5} V_{DDA} + 5\%$	V	(external 4 : 1 divider)
		Under-voltage	$V_{TAL}$	$^{2/5} V_{DDA} - 5\%$	$^{2/5} V_{DDA}$	$^{2/5} V_{DDA} + 5\%$	V	
	Switching hysteresis	$V_{TAHYS}$	12.5	25	50	mV		
	Alarm sense time	$t_{AS}$	–	–	10	$\mu\text{s}$		
	Input resistance	$R_{in}$	5	–	–	M $\Omega$	at $V_{TAH}$ , $V_{TAL}$	
Power down Reset	Threshold voltage	$V_{TPOR}$	3.5	4.0	4.5	V		
	Switching hysteresis	$V_{TPORHYS}$	20	50	80	mV		
	Reset sense time	$t_{RS}$	–	–	10	$\mu\text{s}$		
Digital outputs	Output "H" voltage	$V_{OH}$	$V_{DD} - 0.5$	–	$V_{DD}$	V	$I_{load} = -4\text{ mA}$	
		$V_{OH35}$	$V_{DD35} - 0.8$	–	$V_{DD35}$	V	$I_{load} = -4\text{ mA}$ , *3	
			$V_{DD35} - 0.5$	–	$V_{DD35}$	V	$I_{load} = -2.5\text{ mA}$	
	Output "L" voltage	$V_{OL}$	$V_{SS}$	–	$V_{SS} + 0.4$	V	$I_{load} = 4\text{ mA}$	
		$V_{OL35}$	$V_{SS}$	–	$V_{SS} + 0.7$ $V_{SS} + 0.4$	V	$I_{load} = 4\text{ mA}$ , *3 $I_{load} = 2.5\text{ mA}$	

Parameter			Symbol	Value			Unit	Condition
				Min	Typ	Max		
Digital Inputs*2	CMOS (Type: Q, S, Y, T)	High voltage range	$V_{IH}$	$0.65 \times V_{DD}$	–	$V_{DD}$	V	
			$V_{IH35}$	$0.65 \times V_{DD35}$	–	$V_{DD35}$	V	$V_{DD35} < 4.25 \text{ V}, *3$
		Low voltage range	$V_{IL}$	$V_{SS}$	–	$0.25 \times V_{DD}$	V	
			$V_{IL35}$	$V_{SS}$	–	$0.25 \times V_{DD35}$	V	$V_{DD35} < 4.25 \text{ V}, *3$
	CMOS Schmitt-Trigger (Types: E, F, U)	High voltage range	$V_{IH}$	$0.8 \times V_{DD}$	–	$V_{DD}$	V	
		Low voltage range	$V_{IL}$	$V_{SS}$	–	$0.2 \times V_{DD}$	V	
	CMOS Automotive level Schmitt-Trigger (Types: A, B, K1, M1, J)	High voltage range	$V_{IH}$	$0.8 \times V_{DD}$	–	$V_{DD}$	V	
			$V_{IH35}$	$0.8 \times V_{DD35}$	–	$V_{DD35}$	V	$V_{DD35} < 4.25 \text{ V}, *3$
		Low voltage range	$V_{IL}$	$V_{SS}$	–	$0.5 \times V_{DD}$	V	$V_{DDmin} = 4.25 \text{ V}$
			$V_{IL35}$	$V_{SS}$	–	$0.4 \times V_{DD35}$	V	$V_{DD35} < 4.25 \text{ V}, *3$
	hysteresis voltage	–	–	0.5	–	V		
	CMOS 3/5 V (Type: L, N, O)	High voltage range	$V_{IH}$	$0.65 \times V_{DD}$	–	$V_{DD}$	V	
		Low voltage range	$V_{IL}$	$V_{SS}$	–	$0.25 \times V_{DD}$	V	
	CMOS 3 V (Type: P, W)	High voltage range	$V_{IH}$	$0.65 \times V_{DD}$	–	$V_{DD}$	V	
		Low voltage range	$V_{IL}$	$V_{SS}$	–	$0.25 \times V_{DD}$	V	
Input capacitance		$C_{IN}$	–	–	16	pF		
Input leakage current		$I_{IL}$	–1	–	+1	$\mu\text{A}$	$T_A = +25 \text{ }^\circ\text{C}$	
Pull up resistor		$R_{up1}$ $R_{up2}$	–	50 10	–	k $\Omega$ k $\Omega$	Types: E, U Type: S	
ADC inputs	Reference voltage input	$V_{REFH}$ $V_{REFL}$	$V_{REFL} + 3$ $V_{SSA}$	–	$V_{DDA}$ $V_{REFH} - 3$	V V		
	Input voltage range	$V_{imax}$ $V_{imin}$	$V_{REFL}$ –	–	$V_{REFH}$ –	V V		
	Input resistance	$R_i$	–	–	3.6	k $\Omega$		
	Input capacitance	$C_i$	–	–	30	pF		
	Input leakage current	$I_{IL}$	–1	–	+1	$\mu\text{A}$		
	Impedance of external output driving the ADC input	–	–	–	4.0	k $\Omega$	at sampling time of 1.6 $\mu\text{s}$	

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
DAC analog outputs	Output voltage	$V_{out}$	$V_{SSA}$	–	$V_{DDA}$	V	
	Output impedance	$R_{out}$	2.0	2.9	4.0	k $\Omega$	external voltage follower required
	Output capacitance	$C_{out}$	–	–	20	pF	
Sound generator	Output voltage	$V_{outHIGH}$ $V_{outLOW}$	$V_{DD} - 0.5$ $V_{SS}$	–	$V_{DD}$ $V_{SS} + 0.4$	V V	
	Output current	$I_{out}$	4	–	–	mA	
PPG	Output voltage	$V_{outHIGH}$ $V_{outLOW}$	$V_{DD} - 0.5$ $V_{SS}$	–	$V_{DD}$ $V_{SS} + 0.4$	V V	
	Output current	$I_{out}$	4	–	–	mA	
LED	Output voltage	$V_{outHIGH}$	$V_{DD} - 0.8$	–	–	V	$I_{outHIGH} = 12\text{ mA}$ $I_{outLOW} = 24\text{ mA}$
		$V_{outLOW}$	–	–	$V_{SS} + 0.8$	V	
I <sup>2</sup> C Bus Interface (Open Drain Output)	Output voltage	$V_{outHIGH}$ $V_{outLOW}$	– $V_{SS}$	–	$V_{DD}$ $V_{SS} + 0.4$	V V	$I_{outLOW} = 3\text{ mA}$
	Output current	$I_{out}$	3	–	–	mA	$I_{outLOW} = 3\text{ mA}$
Lock-up time PLL1 (4 MHz → 16 MHz to 64 MHz)		–	–	0.1	1	ms	
ESD Protection (Human body model AEC-Q100 compliant)		$V_{surge}$	1	–	–	kV	$R_{discharge} = 1.5\text{ k}\Omega$ $C_{discharge} = 100\text{ pF}$

\*1: See “4. Run Mode Current/Power Consumption”.

\*2: ..... Valid for bidirectional tristate I/O PAD cell.

\*3: The external interface on CY91F362GB and CY91F369GA can be operated with low voltage (typical 3.3 V) at the V<sub>DD35</sub> pins. The parameters are tested at V<sub>DD35</sub> = (4.25 V to 5.5 V). The parameters at lower voltage are guaranteed by design.

\*4: Sleep mode current consumption given for CLKB : CLKP : CLKT = 64 : 32 : 4 MHz, V<sub>DD</sub> = 5.25 V.

\*5: Sleep mode current consumption given for CLKB : CLKP : CLKT = 48 : 24 : 4 MHz, V<sub>DD</sub> = 5.25 V.

\*6: The current consumption values of CY91F376G are currently under evaluation.

#### 14.4 Run Mode Current/Power Consumption

The power dissipation during normal operation is determined by the total power dissipation of the internal logic  $P_C$ , the dissipation from analog modules  $P_A$  and the power dissipation  $P_{IO}$  of the I/O buffers. Among the I/O buffers the dissipation caused by the stepper motor drivers  $P_{SMC}$  should be taken into special consideration.

So the overall power consumption  $P_D$  will be calculated as a sum of  $P_C + P_A + P_{SMC} + P_{IO}$ .

##### 14.4.1 Logic Power Consumption

The following formula can be used to calculate the maximum core current consumption when the PLL is used depending on the frequency settings for the internal clocks:

$$I_{CC} = B \times CLKB \text{ [MHz]} + P \times CLKP \text{ [MHz]} + T \times CLKT \text{ [MHz]} + 35.5 \text{ [mA]}$$

The factors B, P, and T depend of the device, see table “Current consumption factors”.

If clock modulation is used the following value must be added to this result:  $0.24 \text{ [mA/MHz]} \times CLKB \text{ [MHz]}$ .

This results in the following values (higher clock settings are not allowed):

**Table 14-3. Current Consumption Factors**

Product	B [mA/MHz]	T [mA/MHz]	P [mA/MHz]	Remarks
CY91FV360GA CY91F362GB	3.45	2.52	0.72	
CY91F364G	1.25	1.70	0.40	
CY91F365GB CY91F366GB CY91F367GB CY91F368GB	2.30	2.70	0.50	
CY91366GA	2.30	2.70	0.50	
CY91F376G	1.25	1.70	0.40	
CY91F369GA	2.30	2.70	0.50	

Clock Frequencies [MHz]			Logic Current Consumption at 5.25 V [mA]	Logic Power Consumption PC at 5.25 V [W]	Remarks
CLKB	CLKP	CLKT			
64	16	16	308	1.62	no clock modulation possible
48	24	24	290	1.52	
48	16	16	264	1.39	
32	32	32	257	1.35	
32	16	16	205	1.08	
24	24	24	202	1.06	
24	12	12	163	0.86	
16	16	16	146	0.77	
2	2	2	40	0.21	no PLL, no clock modulation
0.125	0.125	0.125	30	0.16	no PLL, no clock modulation

In addition to this power consumption of the MCU core logic the following contributions to the overall power consumption have to be considered:

- Analog power consumption
- I/O and SMC power consumption

See the following sections.

#### 14.4.2 Analog Power Consumption

Module	Typical Current Consumption	Maximum Current Consumption	Remarks
DAC		1 mA / channel	current at AV <sub>CC</sub>
ADC	3 mA	7 mA	current at AV <sub>CC</sub>
	1.6 mA	2.6 mA	current at AVR <sub>H</sub>
Power down reset	0.26 mA	0.5 mA	current at V <sub>DD</sub>
Alarm Comparator	0.31 mA	0.5 mA	current at AV <sub>CC</sub>
Zero point detection	0.13 mA	0.25 mA	current at AV <sub>CC</sub>

To calculate the analog power consumption P<sub>A</sub>, the current contributions of the active modules have to be multiplied by the maximum analog supply voltage of 5.1 V-or by the maximum digital supply voltage as in case of the Power down reset.

#### 14.4.3 I/O and SMC Power Consumption

##### SMC Drivers:

The average current consumption per SMC channel is 38.2 mA, for four channels this results in 152.8 mA. At 2 × 0.5 V this results in 153 mW power consumption P<sub>SMC</sub> for four channels of stepper motor drivers.

##### Other I/O Buffers:

The power dissipation (P<sub>IO</sub>) (at 5.25 V) of the I/O buffers is represented as the sum of the dynamic power dissipation (P<sub>AC5V</sub>, P<sub>AC3V</sub>) and the static power consumption (P<sub>DC</sub>).

$$P_{IO} = P_{AC5V} \times 1.1 + P_{AC3V} \times 1.2 + P_{DC}$$

The following table lists values for P<sub>AC5V</sub> and P<sub>AC3V</sub>:

Buffer Type	Dynamic Power Dissipation P <sub>AC5V</sub> P <sub>IB</sub> /P <sub>OB</sub> at 5V	Dynamic Power Dissipation P <sub>AC3V</sub> P <sub>IB</sub> /P <sub>OB</sub> at 3.3V	Unit
Normal Input	12.4	12.4	μW/MHz (pF in C <sub>L</sub> )
Bidirectional Input			
4 mA Bidirectional Output	194 + 25 C <sub>L</sub>	85.5 + 11 C <sub>L</sub>	
4 mA Output			
8 mA Bidirectional Output	353 + 25 C <sub>L</sub>	154 + 11 C <sub>L</sub>	
8 mA Output			

$$P_{AC} = P_{IB} \times I_n \times f \times \text{operating rate} + P_{OB} \times O_n \times f \times \text{operating rate}$$

- P<sub>IB</sub>: Power Consumption of Input Buffers and Bidirectional Inputs
- P<sub>OB</sub>: Power Consumption of Output Buffers and Bidirectional Outputs
- I<sub>n</sub>: Total number of input buffers and bidirectional buffer inputs
- O<sub>n</sub>: Total number of output buffers and bidirectional buffer outputs
- f: System frequency
- Operating rate: 1.0 if all buffers are switched simultaneously at system frequency

P<sub>DC</sub> is the caused by off chip loads which are drawing static currents.

$$P_{DC} = V_O \times I_O \times DC_N$$

- V<sub>O</sub>: Output voltage drop - usually 0.4 V
- I<sub>O</sub>: Output current - usually 4 mA
- DC<sub>N</sub>: Number of output buffers and bidirectional buffers driving off chip loads causing static currents.



## 14.5 Clock Settings

Clock Domain	Clock Name	Max Frequency Setting	Remark
Core	CLKB	64 MHz	under normal operating conditions
		32 MHz	
Resource bus	CLKP	32 MHz	
Ext. Bus	CLKT	32 MHz	
Clock for CAN	CANCLK	32 MHz	

## 14.6 Converter Characteristics

### 14.6.1 A/D Converter

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Resolution	–	–	–	10	Bit	
Total error	–	–	–	±5.0	LSB	overall error
Non-linearity error	–	–	–	±2.5	LSB	
Differential Non-linearity error	–	–	–	±1.9	LSB	
Zero Reading voltage	V <sub>0T</sub>	AVRL – 3.5	AVRL + 0.5	AVRL + 4.5	LSB	
Full scale reading voltage	V <sub>FST</sub>	AVRH – 5.5	AVRH – 1.5	AVRH + 2.5	LSB	
Input current	I <sub>A</sub>	–	3.0	7.0	mA	
Reference voltage current	I <sub>R</sub>	–	1.6	2.6	mA	
Conversion time	–	178 cycles CLKP	–	1 ms		
Ripple of supply voltage	–	–	–	±5.0	mV	

### 14.6.2 D/A Converter

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Resolution	–	–	–	10	Bit	
Differential linearity error	–	–0.9	–	+0.9	LSB	
Conversion time	–	–	3	–	μs	100pF external load

## 14.7 A/D Converter Glossary

### ■ Resolution

The smallest change in analog voltage detected by A/D converter.

### ■ Linearity Error

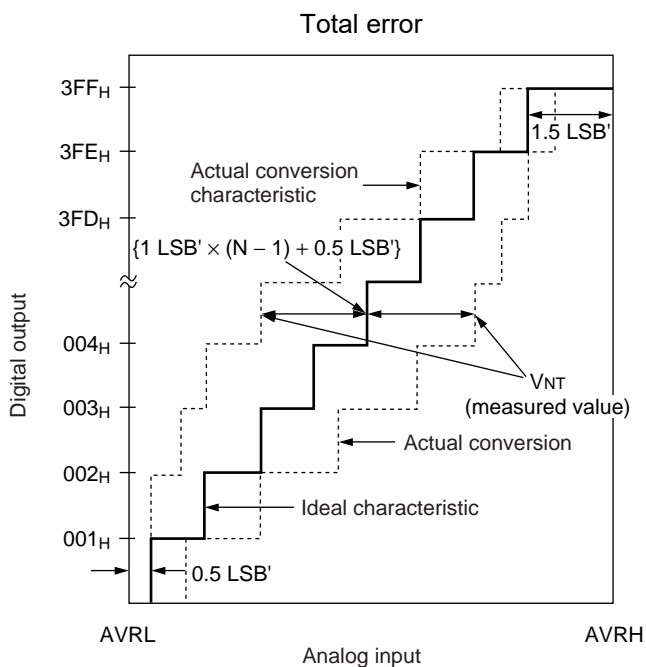
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”).

### ■ Differential Linearity Error

A deviation of a step voltage for changing the LSB of output code from ideal input voltage.

### ■ Total Error

A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'} \text{ [LSB]}$$

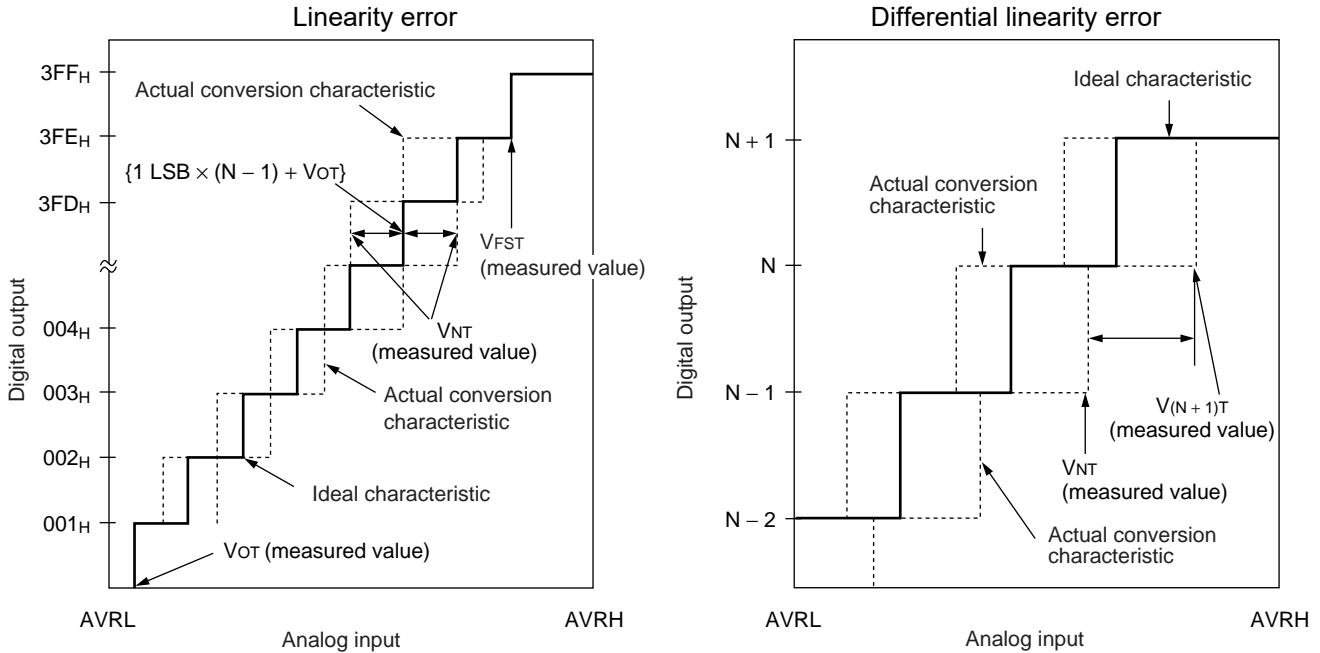
$$V_{OT}' \text{ (Ideal value)} = AVRL + 0.5 \text{ LSB}' \text{ [V]}$$

$$V_{FST}' \text{ (Ideal value)} = AVRH - 1.5 \text{ LSB}' \text{ [V]}$$

$V_{NT}$ : A voltage for causing transition of digital output from  $(N - 1)$  to  $N$

(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}'} - 1 \text{ [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

$$1 \text{ LSB}' (\text{ideal value}) = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$V_{OT}$ : A voltage for causing transition of digital output from (000)<sub>H</sub> to (001)<sub>H</sub>

$V_{FST}$ : A voltage for causing transition of digital output from (3FE)<sub>H</sub> to (3FF)<sub>H</sub>

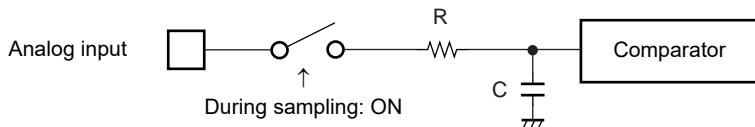
$V_{NT}$ : A voltage for causing transition of digital output from (N - 1)<sub>H</sub> to N<sub>H</sub>

## 14.8 Notes on Using A/D Converter

### 14.8.1 About the External Impedance of Analog Input and its Sampling Time

■ A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



	<b>R</b>	<b>C</b>
Mask products*1	3.6 kΩ (Max)	30.0 pF (Max)
Flash products*2	3.6 kΩ (Max)	24.0 pF (Max)

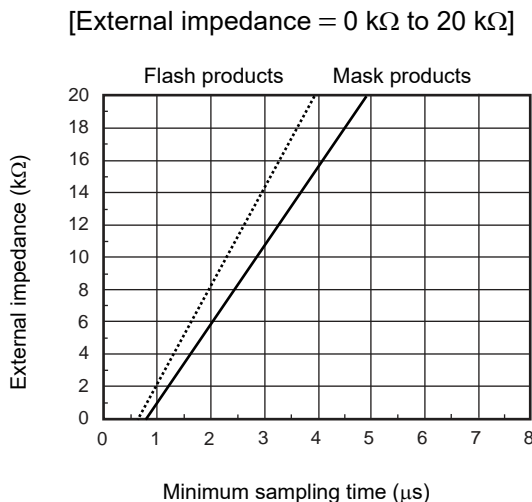
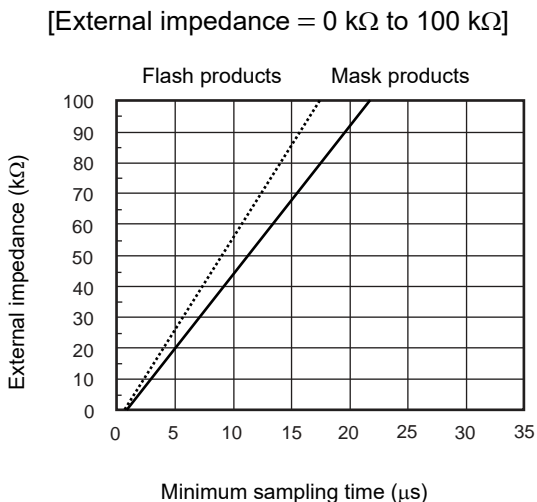
\*1: CY91366GA

\*2: CY91FV360GA/F362GB/F364G/F369GA/F365GB/F366GB/F367GB/F368GB/F376G

Note: The values are reference values.

■ To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time



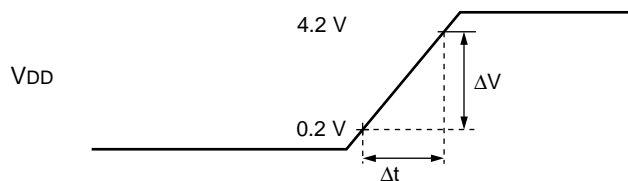
■ If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

### 14.8.2 About Errors

As  $|AVRH - AV_{SS}|$  becomes smaller, values of relative errors grow larger.

### 14.9 Time for Power Supply

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply raising slope	$\Delta V/\Delta t$	–	–	0.05	V/ $\mu$ s
Power supply raising slope	$t_r$	80	–	–	$\mu$ s



### 14.10 Flash Memory

**Table 14-4. Erase and Programming Performance**

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$ , $V_{DD} = 5.0\text{ V}$	–	1	15*	s	Excludes 00H programming prior erasure
Chip erase time		–	14	–	s	Excludes 00H programming prior erasure
Half word (16-bit) programming time		–	16	3,600*	$\mu$ s	Excludes system-level overhead
Erase/Program cycle	–	10,000	–	–	cycle	
Data retention time	–	100,000	–	–	h	

\*:  $T_A = +85\text{ }^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V}$

### 14.11 AC Characteristics

#### 14.11.1 Measurement Conditions

Parameter	Symbol	Value	Unit	Conditions
"H" level input voltage	$V_{IH}$	according to I/O spec	V	$V_{DD} = 4.25\text{ to }5.25\text{ V}$ , $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$
"L" level input voltage	$V_{IL}$		V	
"H" level output voltage	$V_{OH}$	$0.5 \times V_{DD}$	V	
"L" level output voltage	$V_{OL}$	$0.5 \times V_{DD}$	V	
"H" level input voltage	$V_{IH}$	3.0	V	$V_{DD} = 3.0\text{ to }3.6\text{ V}$ , $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$
"L" level input voltage	$V_{IL}$	0	V	
"H" level output voltage	$V_{OH}$	$0.5 \times V_{DD}$	V	
"L" level output voltage	$V_{OL}$	$0.5 \times V_{DD}$	V	

Load conditions

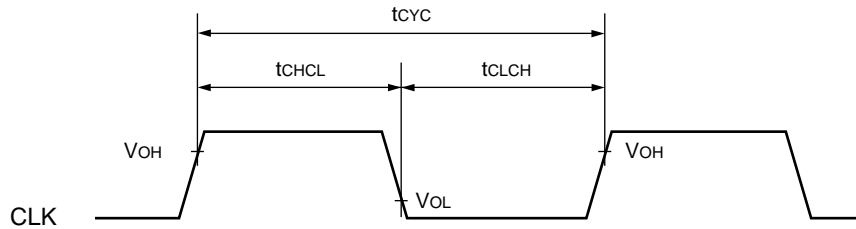


14.11.2 External Bus Clock

(V<sub>DD</sub> = 4.25 V to 5.25 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
CLK cycle	t <sub>CYC</sub>	CLK	t <sub>CPT</sub>	–	ns
CLK rise → CLK fall	t <sub>CHCL</sub>	CLK	t <sub>CYC</sub> / 2 – 10	t <sub>CYC</sub> / 2 + 10	ns
CLK fall → CLK rise	t <sub>CLCH</sub>	CLK	t <sub>CYC</sub> / 2 – 10	t <sub>CYC</sub> / 2 + 10	ns

Note: This is only valid for operation without clock modulator

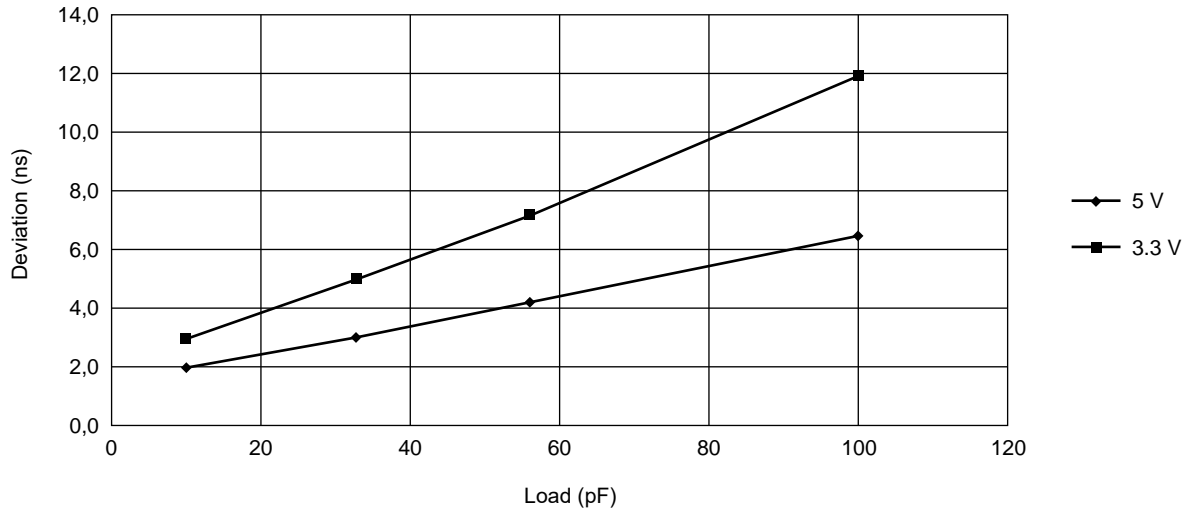


The values for t<sub>CHCL</sub> and t<sub>CLCH</sub> are heavily dependent on the load connected to the CLK pin. The following diagrams show this dependency for the worst case situation. The first diagram shows the situation for even division ratios between CLK<sub>B</sub> and CLK<sub>T</sub>, the second diagram shows this for odd division ratios between CLK<sub>B</sub> and CLK<sub>T</sub> (ASYMCLKT bit is not set).

It has to note that when the combination of CLK frequency and load at CLK pin is such that rise or fall times are longer than t<sub>CYC</sub> / 2 the duty ratio can get worse.

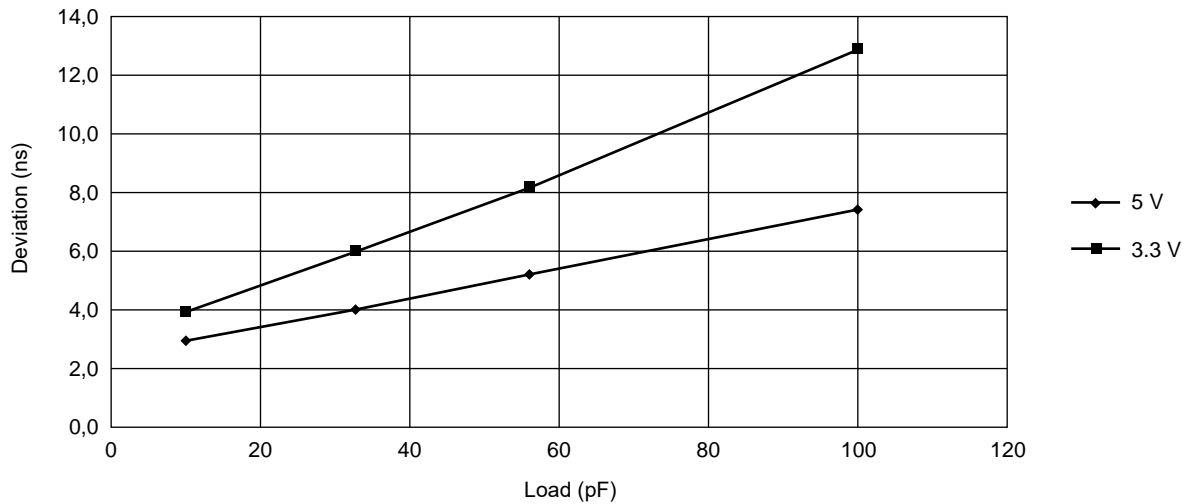
**Deviation of  $t_{CHCL}$  from  $t_{CYC} / 2$  versus Load (Even CLKB/CLKT division ratios):**

deviation of  $t_{CHCL}$  from  $t_{CYC} / 2$  versus load



**Deviation of  $t_{CHCL}$  from  $t_{CYC} / 2$  versus Load (Odd CLKB/CLKT division ratios):**

deviation of  $t_{CHCL}$  from  $t_{CYC} / 2$  versus load



## 14.11.3 External Bus Interface

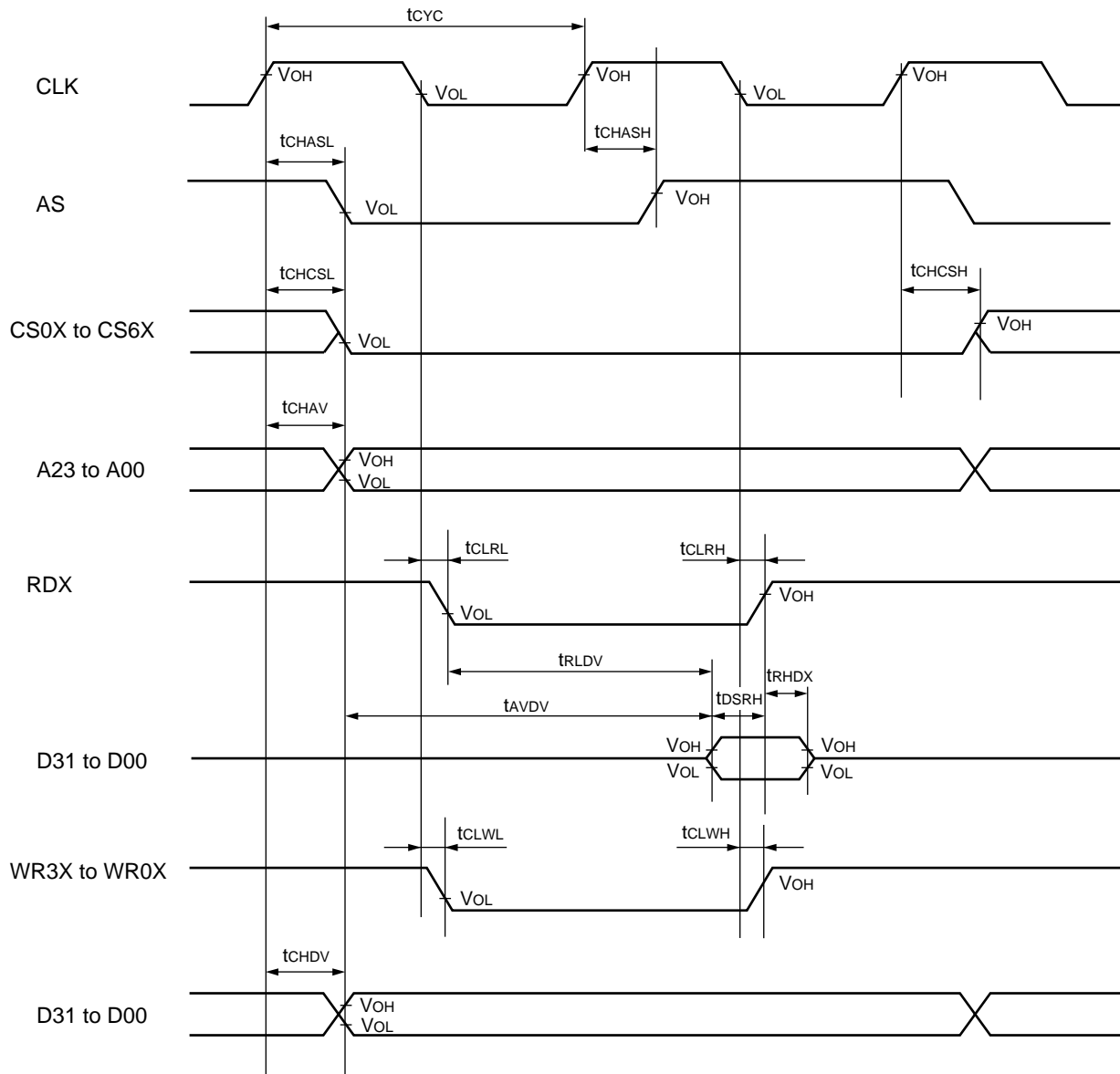
 (V<sub>DD</sub> = 4.25 V to 5.25 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
CS6X to CS0X delay time	t <sub>CHCSL</sub>	CLK, CS6X to CS0X	–	15	ns
CS6X to CS0X delay time	t <sub>CHCSH</sub>		–	15	ns
Address delay time	t <sub>CHAV</sub>	CLK, A20 to A0	–	20	ns
Data delay time	t <sub>CHDV</sub>	CLK, D31 to D0	–	16	ns
RDX delay time	t <sub>CLRL</sub>	CLK, RDX	–	15	ns
RDX delay time	t <sub>CLRH</sub>		–	15	ns
WR3X to WR0X delay time	t <sub>CLWL</sub>	CLK, WR3X to WR0X	–	15	ns
WR3X to WR0X delay time	t <sub>CLWH</sub>		–	15	ns
Effective address → Effect data input time	t <sub>AVDV</sub>	A20 to A0, D31 to D0	–	3 / 2 × t <sub>cyc</sub> – 30	ns
RDX (↓) → Effect data input time	t <sub>RLDV</sub>	RDX, D31 to D0	–	t <sub>cyc</sub> – 20 <sup>*1</sup> t <sub>cyc</sub> – 25 <sup>*2</sup>	ns
Data set up → RDX (↑) time	t <sub>DSRH</sub>		25 <sup>*1</sup> 30 <sup>*2</sup>	–	ns
RDX (↑) → Data hold time	t <sub>RHDX</sub>		0	–	ns
AS delay time	t <sub>CHASL</sub>	CLK → AS	–	15	ns
AS delay time	t <sub>CHASH</sub>	CLK → AS	–	15	ns

 \*1: Values valid for 4.25 V ≤ V<sub>DD</sub> ≤ 5.25 V

 \*2: Values valid for 3.00 V ≤ V<sub>DD</sub> ≤ 4.25 V





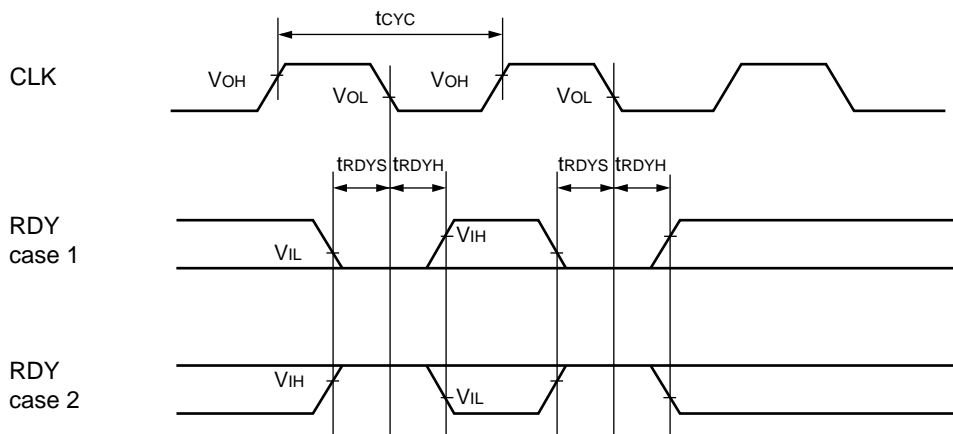
14.11.4 RDY

(V<sub>DD</sub> = 4.25 V to 5.25 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
RDY setup	t <sub>RDYS</sub>	CLK, RDY	16 *1 25 *2	–	ns
RDY hold	t <sub>RDYH</sub>	CLK, RDY	0	–	ns

\*1: Values valid for 4.25 V ≤ V<sub>DD</sub> ≤ 5.25 V

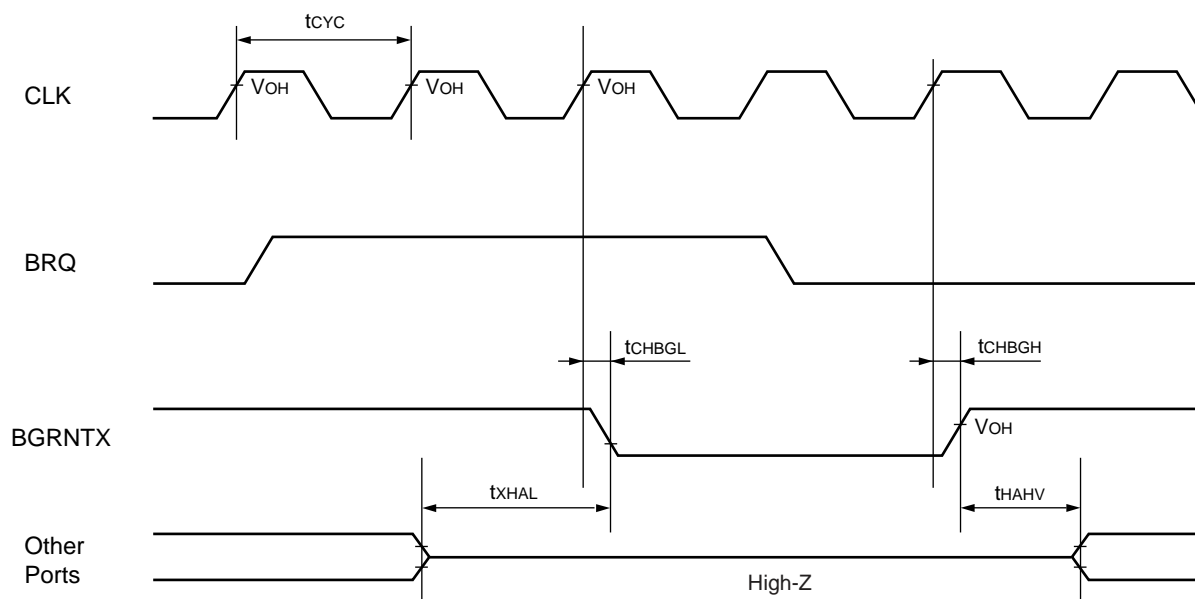
\*2: Values valid for 3.00 V ≤ V<sub>DD</sub> ≤ 4.25 V



## 14.11.5 BGRNTX

 (V<sub>DD</sub> = 4.25 V to 5.25 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
BGRNTX	t <sub>CHBGL</sub>	CLK, BGRNTX	-	10	ns
BGRNTX	t <sub>CHBGH</sub>		-	10	ns
Bus access enabled BGRNTX falling	t <sub>XHAL</sub>	BGRNTX	t <sub>cyc</sub> - 15	t <sub>cyc</sub> + 15	ns
Bus access disabled BGRNTX rising	t <sub>HAHV</sub>		t <sub>cyc</sub> - 15	t <sub>cyc</sub> + 15	ns

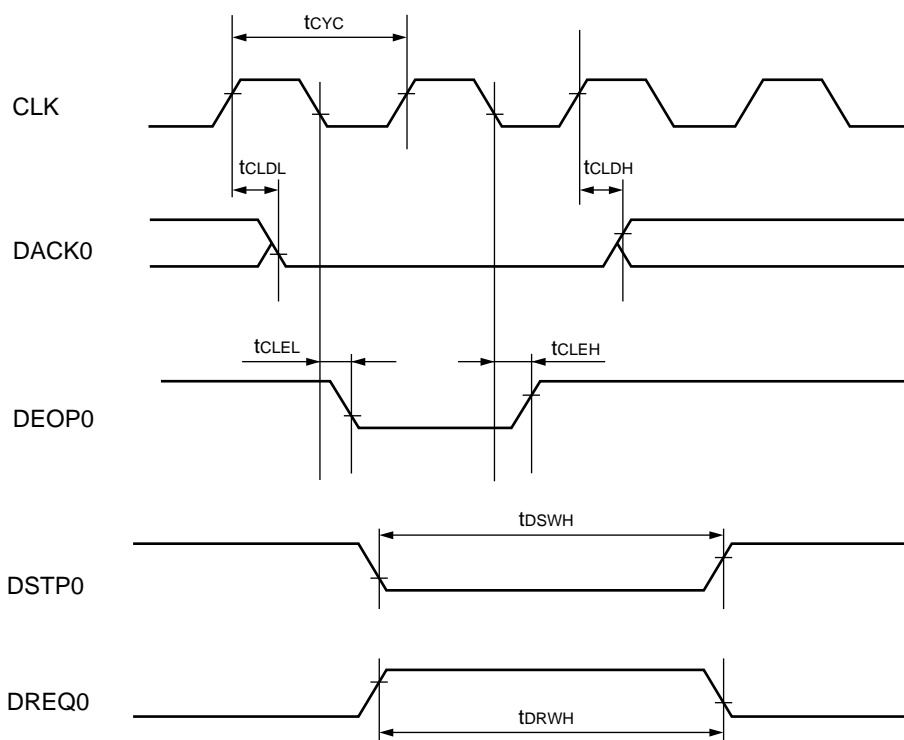


14.11.6 DMA

(V<sub>DD</sub> = 4.25 V to 5.25 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
DREQ	t <sub>DRWH</sub>	DREQ0	5t <sub>cyC</sub>	–	ns
DSTP	t <sub>DSWH</sub>	DSTP0*	5t <sub>cyC</sub>	–	ns
DACK	t <sub>CLDL</sub>	CLK, DACK0	–	20	ns
	t <sub>CLDH</sub>		–	20	
DEOP	t <sub>CLEL</sub>	CLK, DEOP0	–	20	ns
	t <sub>CLEH</sub>		–	20	

\*: DSTP and DEOP share a pin. The pin is possible to change DSTP and DEOP functions using a port function register.



## 15. Package Thermal Resistance and Max Allowed Power Consumption

Package	Thermal Resistance [ °C/W]				Maximum Allowed Power Consumption [W] *
	$\theta_{ja}$ (junction to ambient)			$\theta_{jc}$ (junction to case)	
	0 m/s	1 m/s	3 m/s		
LQM120	30	27	25	5	1.33
HQA160	16	13	11	2.5	2.5
HQB208	16	13	11	2.5	2.5

\*: The maximum allowed ambient temperature is +85 °C, the maximum allowed junction temperature is +125 °C. Under these conditions, the maximum allowed power consumption will be

$$P_{MAX} = (125\text{ °C} - 85\text{ °C}) / \theta_{ja} \text{ (K/W)}$$

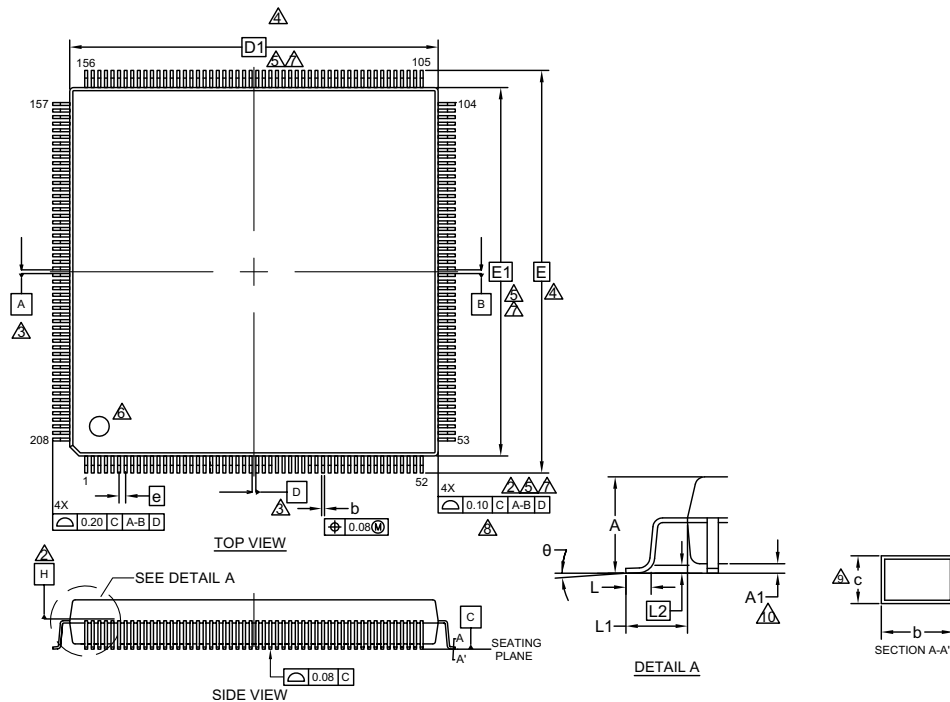
$\theta_{ja}$  is the thermal resistance of this package at 0 m/s when used on a multi-layer board with separate power and ground planes.

## 16. Ordering Information

Part Number	Package	Remarks
CY91F362GBPVS-R-G-UJE2	208-pin plastic QFP (HQB208)	
CY91F376GSPMC3-GS-UJE2	120-pin plastic LQFP (LQM120)	

## 17. Package Dimensions

Package Type	Package Code
208-pin Plastic QFP	HQB208



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.95
A1	0.25	—	0.50
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.60 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.60 BSC		
E1	28.00 BSC		
theta	0°	—	8°
L	0.45	0.60	0.75
L1	1.30 REF		
L2	0.25 BSC		

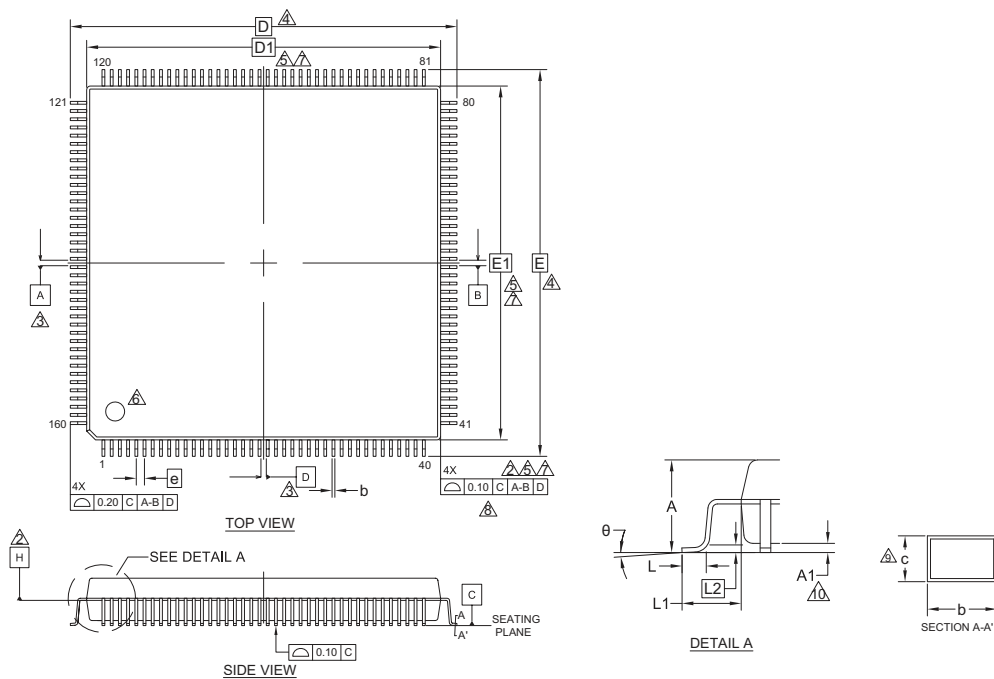
### NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-18454 \*\*

PACKAGE OUTLINE, 208 LEAD QFP  
 28.00X28.00X3.95 MM HQB208 REV.\*\*

Package Type	Package Code
160-pin Plastic QFP	HQA160



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	4.10
A1	0.25	—	0.50
b	0.25	0.32	0.40
c	0.14	—	0.22
D	31.20 BSC		
D1	28.00 BSC		
e	0.65 BSC		
E	31.20 BSC		
E1	28.00 BSC		
$\theta$	0°	—	8°
L	0.73	0.88	1.03
L1	1.60 REF		
L2	0.25 BSC		

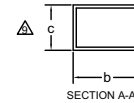
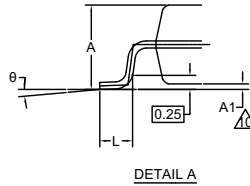
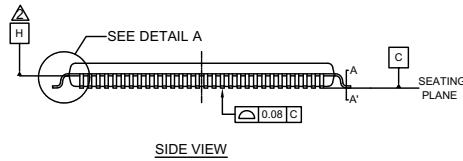
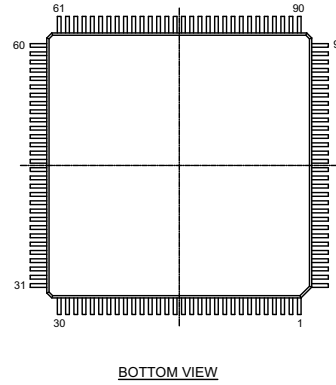
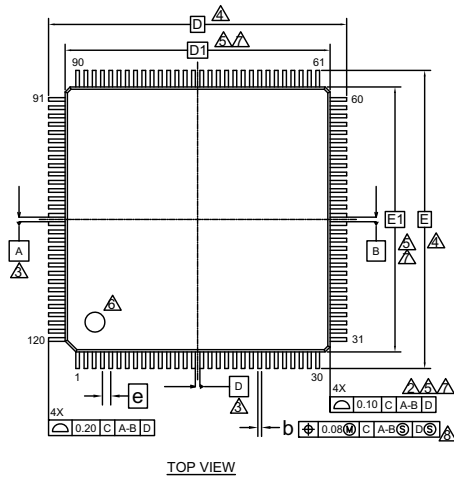
**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-19674 \*\*

PACKAGE OUTLINE, 160 LEAD QFP  
28.00X28.00X4.10 MM HQA160

Package Type	Package Code
120-pin plastic LQFP	LQM120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- JEDEC SPECIFICATION NO. REF: N/A.

002-16172 \*\*

PACKAGE OUTLINE, 120 LEAD LQFP  
18.0X18.0X1.7 MM LQM120 REV\*\*



## 18. Major Changes

Spansion Publication Number: DS07-16401-4Ea

Page	Section	Change Results
Rev. *B		
213	16. Ordering Information	Revised Marketing Part Numbers as follows:  Before) - MB91F362GBPFVS - MB91F376GPMT  After) - CY91F362GBPVS-R-G-UJE2 - CY91F376GSPMC3-GS-UJE2  Removed Marketing Part Numbers as follows:  Before) - MB91F369GAPQS1 - MB91F365GBPMT - MB91F366GBPMT - MB91F367GBPMT - MB91F368GBPMT - MB91366GAPMT - MB91F364GPMT
217	Major Changes	Added section "18. Major Changes".
218	Document History	Added Document History
Rev. *C		
197	DC Characteristics	Revised the shading parts as below:  14.3 DC Characteristics  Parameter:  Before) ESD Protection (Human body model MIL883-B compliant)  After) ESD Protection (Human body model AEC-Q100 compliant)  Value: Min:  Before) 2 kV  After) 1 kV

## 19. Document History Page

<b>Document Title: CY91FV360GA/F362GB/F364G/CY91F365GB/366GA/F366GB/CY91F367GB/F368GB/F369GA/F376G,                      32-bit Microcontroller FR50 CY91360G Series</b> <b>Document Number: 002-08044</b>			
Revision	ECN	Submission Date	Description of Change
**	–	06/17/2005	Migrated to Cypress and assigned document number 002-08044. No change to document contents or format.
*A	6059170	02/05/2018	Deleted MB91FV360GACR and PGA-401C-A02 package. Changed following packages; FPT-208P-M04 --> HQB208 FPT-160P-M15 --> HQA160 FPT-120P-M21 --> LQM120 Updated to Cypress template.
*B	6952285	08/20/2020	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 16. Ordering Information 18. Major Changes For details, please see Major Changes section.
*C	7167796	06/23/2021	Revised the following items: 14.3 DC Characteristics For details, please see Major Changes section.  Updated to new template.



## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

#### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

#### Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2005–2021. This document is the property of Cypress Semiconductor Corporation, an Infineon Technologies company, and its affiliates ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, including its affiliates, and its directors, officers, employees, agents, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, Traveo, WICED, and ModusToolbox are trademarks or registered trademarks of Cypress or a subsidiary of Cypress in the United States or in other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.