STK14C88-3

256 Kbit (32K x 8) AutoStore nvSRAM

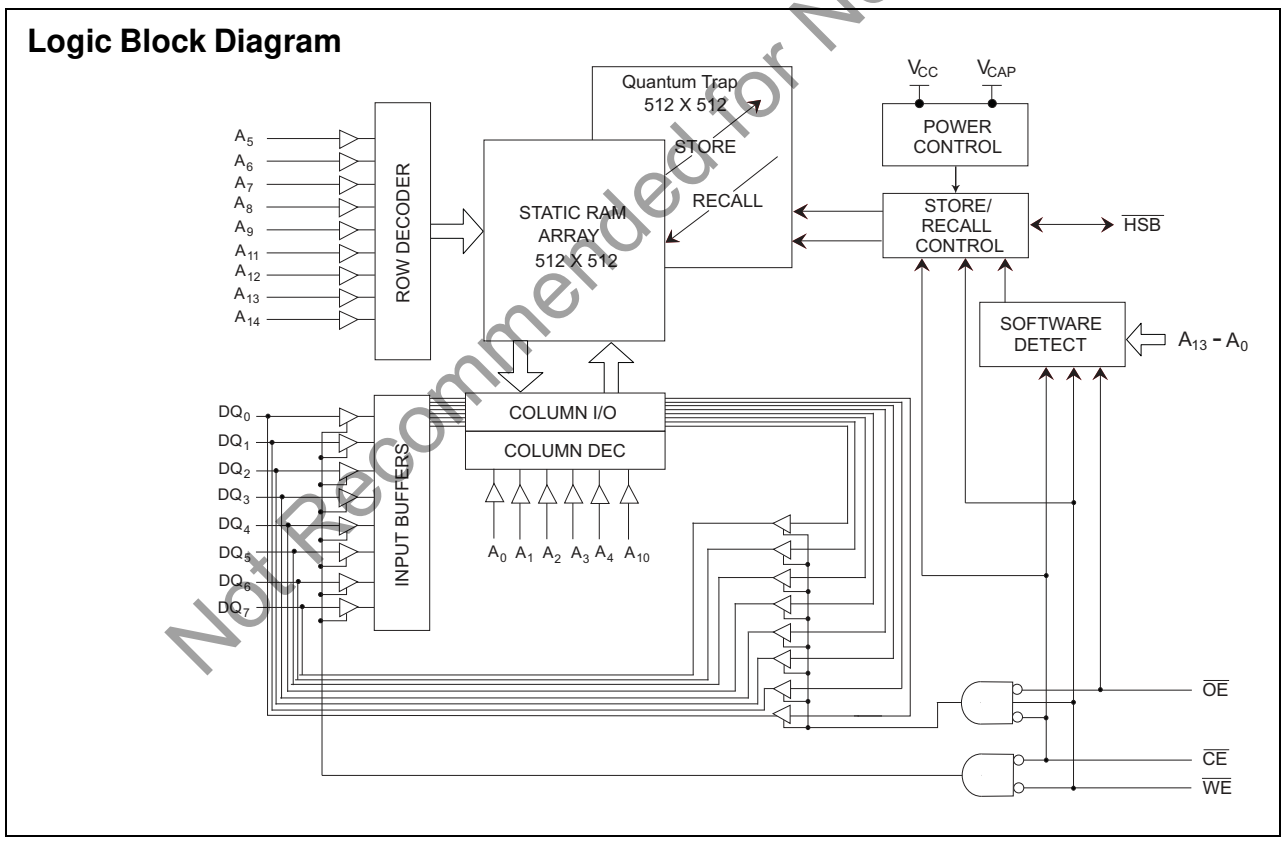
Features

- 35 ns and 45 ns Access Times
- Automatic Nonvolatile STORE on power loss
- Nonvolatile STORE under Hardware or Software control
- Automatic RECALL to SRAM on power up
- Unlimited Read/Write endurance
- Unlimited RECALL Cycles
- 1,000,000 STORE Cycles
- 100 year Data Retention
- Single 3.3V±0.3V Power Supply
- Commercial and Industrial Temperatures
- 32-pin (300mil) SOIC and 32-pin (600 mil) PDIP packages
- RoHS compliance

Functional Description

The Cypress STK14C88-3 is a 256 Kb fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

Logic Block Diagram



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Pin Configurations

Figure 1. Pin Diagram - 32-Pin SOIC/32-Pin PDIP

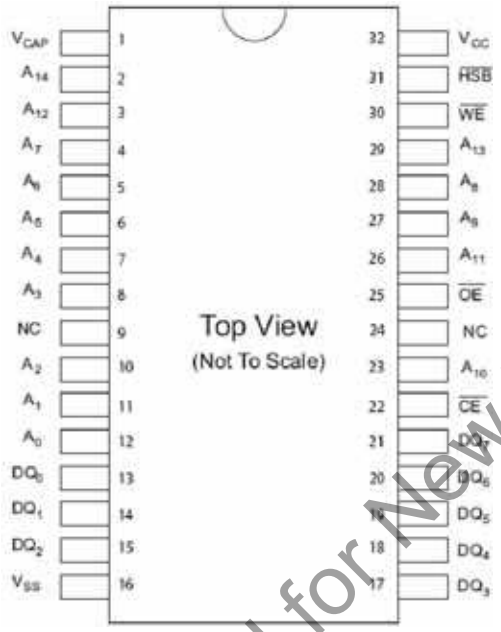


Table 1. Pin Definitions - 32-Pin SOIC/32-Pin PDIP

Pin Name	Alt	I/O Type	Description
A_0–A_{14}		Input	**Address Inputs**. Used to select one of the 32,768 bytes of the nvSRAM.
DQ_0-DQ_7		Input or Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	**Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
V_{SS}		Ground	**Ground for the Device**. The device is connected to ground of the system.
V_{CC}		Power Supply	**Power Supply Inputs to the Device**.
$\overline{HSB}$		Input or Output	**Hardware Store Busy (HSB)**. When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V_{CAP}		Power Supply	**AutoStore Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The STK14C88-3 nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The STK14C88-3 supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

SRAM Read

The STK14C88-3 performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-14} determines the 32,768 data bytes accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-7} are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. Keep $\overline{OE}$ HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

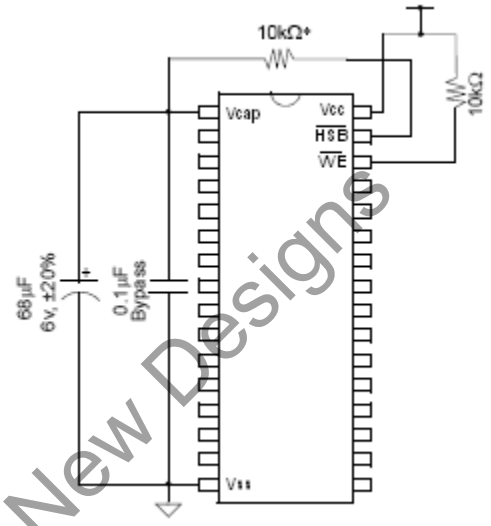
AutoStore Operation

The STK14C88-3 can be powered in one of three storage operations:

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. A charge storage capacitor having a capacity of between 68 uF and 220 uF (±20%) rated at 4.7V should be provided.

Figure 2. AutoStore Mode



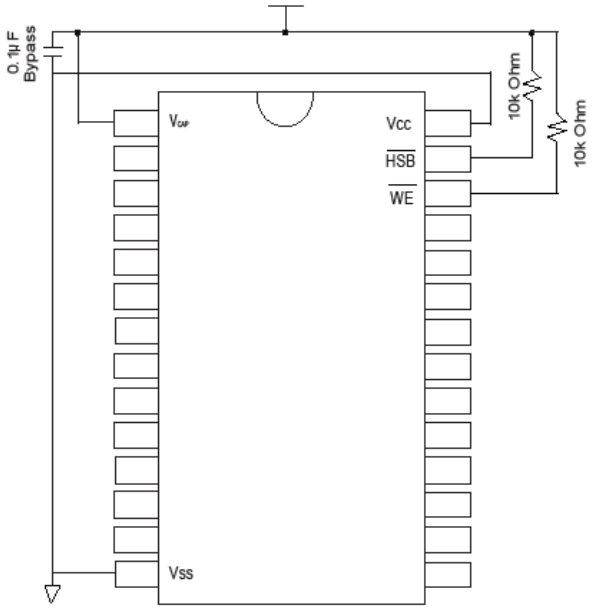
To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored, unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to $\overline{HSB}$. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

If the power supply drops faster than 20 us/volt before Vcc reaches V_{SWITCH}, then a 1 ohm resistor should be connected between V_{CC} and the system supply to avoid momentary excess of current between V_{CC} and V_{CAP}.

AutoStore Inhibit Mode

If an automatic STORE on power loss is not required, then V_{CC} is tied to ground and +3.3V is applied to V_{CAP} (Figure 3 on page 5). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the STK14C88-3 is operated in this configuration, references to V_{CC} are changed to V_{CAP} throughout this data sheet. In this mode, STORE operations are triggered through software control. It is not permissible to change between these options “On the fly”.

Figure 3. AutoStore Inhibit Mode



Hardware STORE ($\overline{HSB}$) Operation

The STK14C88-3 provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the STK14C88-3 conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to V_{CAP} if $\overline{HSB}$ is used as a driver.

SRAM READ and WRITE operations, that are in progress when $\overline{HSB}$ is driven LOW by any means, are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes LOW, the STK14C88-3 continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations take place. If a WRITE is in progress when $\overline{HSB}$ is pulled LOW, it allows a time, t_{DELAY} to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH.

The $\overline{HSB}$ pin is used to synchronize multiple STK14C88-3 while using a single larger capacitor. To operate in this mode, the $\overline{HSB}$ pin is connected together to the $\overline{HSB}$ pins from the other STK14C88-3. An external pull up resistor to V_{CAP} is required, since $\overline{HSB}$ acts as an open drain pull down. The V_{CAP} pins from the other STK14C88-3 parts are tied together and share a single capacitor. The capacitor size is scaled by the number of devices connected to it. When any one of the STK14C88-3 detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin causes all parts to request a STORE cycle. (A STORE takes place in those STK14C88-3 that are written since the last nonvolatile cycle.)

During any STORE operation, regardless of how it is initiated, the STK14C88-3 continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the STK14C88-3 remains disabled until the $\overline{HSB}$ pin returns HIGH.

If $\overline{HSB}$ is not used, it is left unconnected.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC} < V_{RESET}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the STK14C88-3 is in a WRITE state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between $\overline{WE}$ and system V_{CC} or between $\overline{CE}$ and system V_{CC}.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK14C88-3 software STORE cycle is initiated by executing sequential $\overline{CE}$ controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence is clocked with $\overline{CE}$ controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that $\overline{OE}$ is LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled READ operations is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

Preventing STORE

The STORE function can be disabled on the fly by holding $\overline{HSB}$ high with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2V, because it has to overpower the internal pull down device. This device drives $\overline{HSB}$ LOW for 20 µs at the onset of a STORE. When the STK14C88-3 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK14C88-3 attempts to pull $\overline{HSB}$ LOW. If $\overline{HSB}$ does not actually get below V_{IL}, the part stops trying to pull $\overline{HSB}$ LOW and aborts the STORE attempt.

Hardware Protect

The STK14C88-3 offers hardware protection against inadvertent STORE operation and SRAM WRITEs during low voltage conditions. When $V_{CAP}<V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs are inhibited.

Noise Considerations

The STK14C88-3 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Low Average Active Power

CMOS technology provides the STK14C88-3 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 and Figure 5 show the relationship between I_{CC} and READ or WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 3.6V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14C88-3 depends on the following items:

1. The duty cycle of chip enable
2. The overall cycle rate for accesses
3. The ratio of READs to WRITEs
4. CMOS versus TTL input levels
5. The operating temperature
6. The V_{CC} level
7. I/O loading

Figure 4. Current Versus Cycle Time (READ)

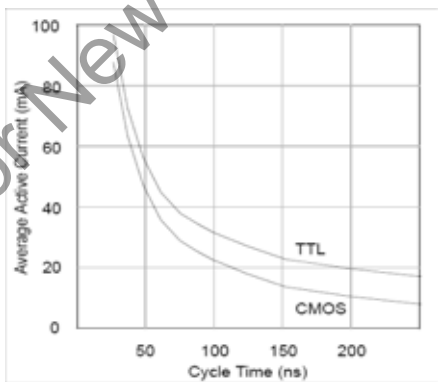
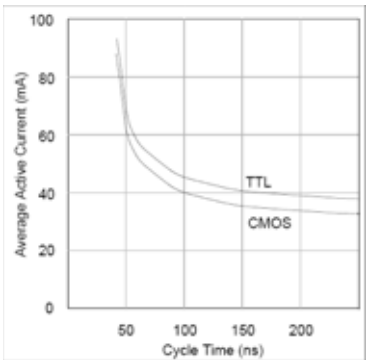


Figure 5. Current Versus Cycle Time (WRITE)



Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites, sometimes, reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration and cold or warm boot status, should always program a unique NV pattern (for example, a complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently. Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs or incoming inspection routines).
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{CAP} value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger V_{CAP} value to ensure there is extra store charge should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Table 2. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{HSB}$	$A_{13} - A_0$	Mode	I/O	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active[1]
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile Store	Output High Z	I_{CC2}[2]
L	H	H	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 3, 4, 5]
L	H	H	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 3, 4, 5]

Notes
1. I/O state assumes $\overline{OE} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{OE}$.
2. HSB STORE operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the STORE (if any) completes, the part will go into standby mode, inhibiting all operations until HSB rises.
3. $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH for output behavior.
4. The six consecutive addresses must be in the order listed. $\overline{WE}$ must be high during all six consecutive $\overline{CE}$ controlled cycles to enable a nonvolatile cycle.
5. While there are 15 addresses on the STK14C88-3, only the lower 14 are used to control software modes.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Temperature under bias..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 7.0V

Voltage on Input Relative to Vss..... –0.6V to V_{CC} + 0.5V

Voltage on DQ_{0-7} or $\overline{HSB}$ .....–0.5V to Vcc + 0.5V

Power Dissipation 1.0W

DC output Current (1 output at a time, 1s duration) .... 15 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.0V to 3.6V
Industrial	-40°C to +85°C	3.0V to 3.6V

DC Electrical Characteristics

Over the operating range (V_{CC} = 3.0V to 3.6V) [6]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		50 42	mA mA
			Industrial		52 44	mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{RC}= 200 ns, 5V, 25°C Typical	$\overline{WE} \geq (V_{CC} - 0.2V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			9	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			2	mA
I_{SB1} [7]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)	t_{RC}=35ns, $\overline{CE} \geq V_{IH}$ t_{RC}=45ns, $\overline{CE} \geq V_{IH}$	Commercial		18 16	mA
			Industrial		19 17	mA
I_{SB2} [7]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)	$\overline{CE} \geq (V_{CC} - 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$.			1	mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		-1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		-1	+1	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –4 mA except $\overline{HSB}$		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 8 mA except $\overline{HSB}$			0.4	V
V_{BL}	Logic ‘0’ Voltage on $\overline{HSB}$ output	I_{OUT} = 3 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and Vss, 68 to 220uF ±20%, 4.7V rated.		54	264	uF

Notes

6. V_{CC} reference levels throughout this data sheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if V_{CC} is connected to ground.
7. $\overline{CE} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	100	Years
NV_C	Nonvolatile STORE Operations	1,000	K

Capacitance

In the following table, the capacitance parameters are listed.[8]

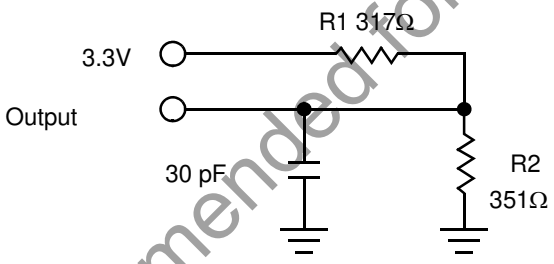
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0 V	5	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[8]

Parameter	Description	Test Conditions	32-SOIC	32-PDIP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Figure 6. AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels ..... 1.5 V

Note
8. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
t_{ACE}	t_{ELQV}	Chip Enable Access Time		35		45	ns
t_{RC} [9]	t_{AVAV}, t_{ELEH}	Read Cycle Time	35		45		ns
t_{AA} [10]	t_{AVQV}	Address Access Time		35		45	ns
t_{DOE}	t_{GLQV}	Output Enable to Data Valid		15		20	ns
t_{OHA} [10]	t_{AXQX}	Output Hold After Address Change	5		5		ns
t_{LZCE} [11]	t_{ELQX}	Chip Enable to Output Active	5		5		ns
t_{HZCE} [11]	t_{EHQZ}	Chip Disable to Output Inactive		13		15	ns
t_{LZOE} [11]	t_{GLQX}	Output Enable to Output Active	0		0		ns
t_{HZOE} [11]	t_{GHQZ}	Output Disable to Output Inactive		13		15	ns
t_{PU} [8]	t_{ELICCH}	Chip Enable to Power Active	0		0		ns
t_{PD} [8]	t_{EHICCL}	Chip Disable to Power Standby		35		45	ns

Switching Waveforms

Figure 7. SRAM Read Cycle 1: Address Controlled [9, 10]

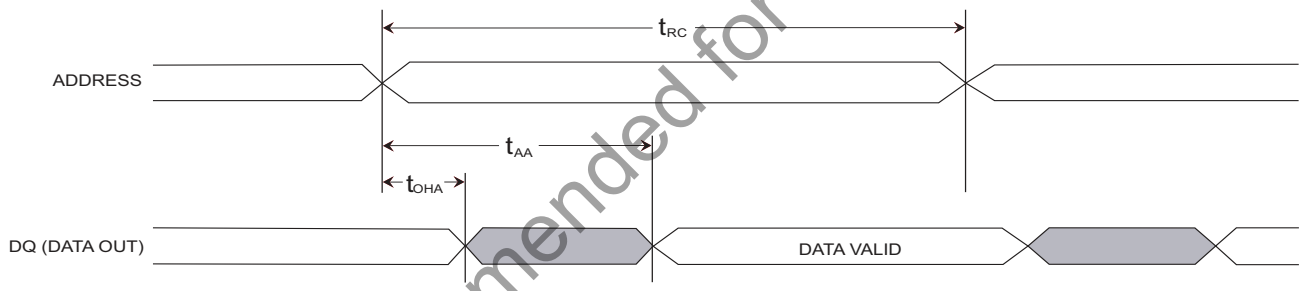
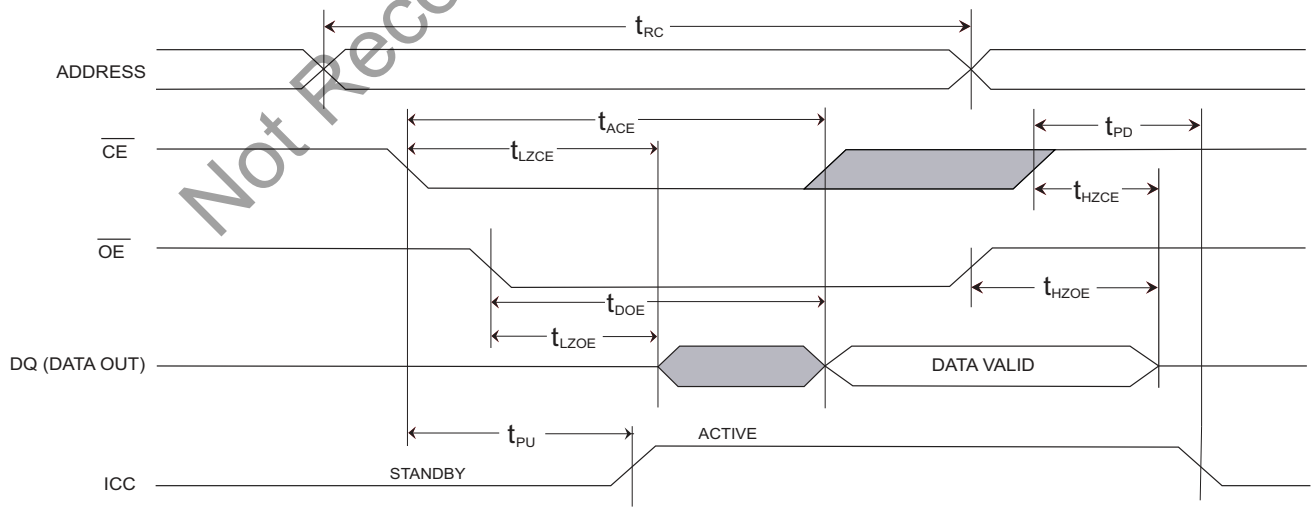


Figure 8. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [9]



Notes
9. $\overline{WE}$ and $\overline{HSB}$ must be HIGH during SRAM Read Cycles.
10. I/O state assumes $\overline{CE}$ and $\overline{OE} \leq V_{IL}$ and $\overline{WE} \geq V_{IH}$; device is continuously selected.
11. Measured ±200 mV from steady state output voltage.

Table 3. SRAM Write Cycle

Parameter		Description	35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write Cycle Time	35		45		ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write Pulse Width	25		30		ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip Enable To End of Write	25		30		ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data Setup to End of Write	12		15		ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data Hold After End of Write	0		0		ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address Setup to End of Write	25		30		ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address Setup to Start of Write	0		0		ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address Hold After End of Write	0		0		ns
t_{HZWE} [11,12]	t_{WLQZ}	Write Enable to Output Disable		13		15	ns
t_{LZWE} [11]	t_{WHQX}	Output Active After End of Write	5		5		ns

Switching Waveforms

Figure 9. SRAM Write Cycle 1: $\overline{WE}$ Controlled [13, 14]

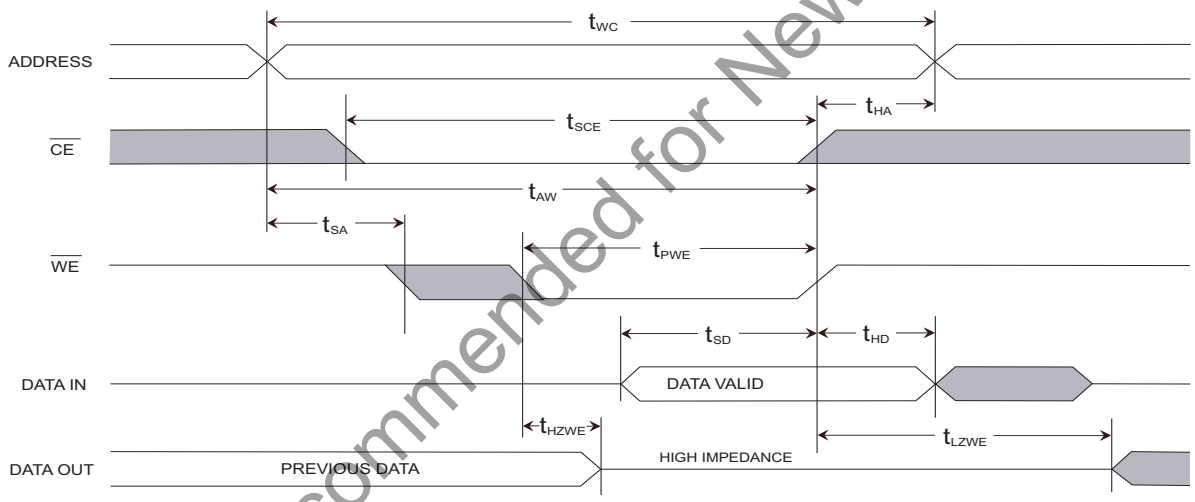
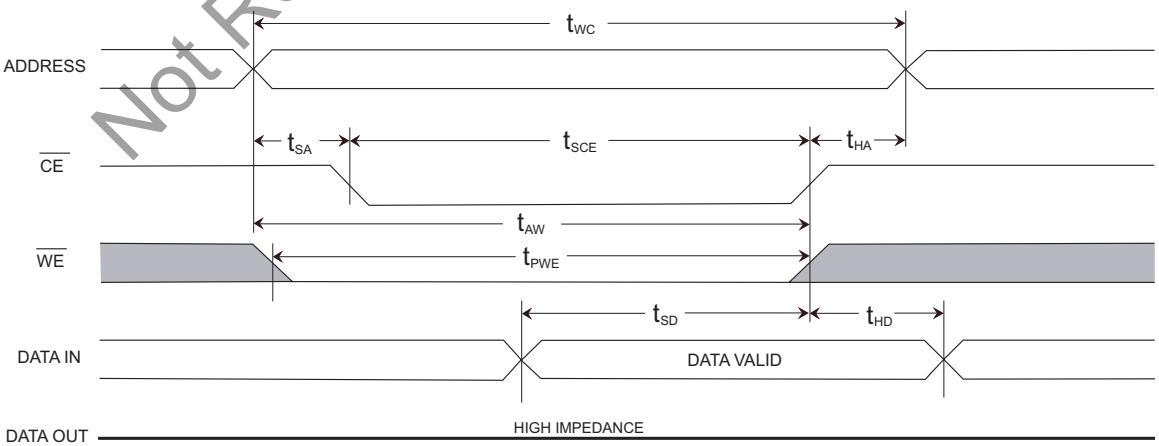


Figure 10. SRAM Write Cycle 2: $\overline{CE}$ Controlled [13, 14]



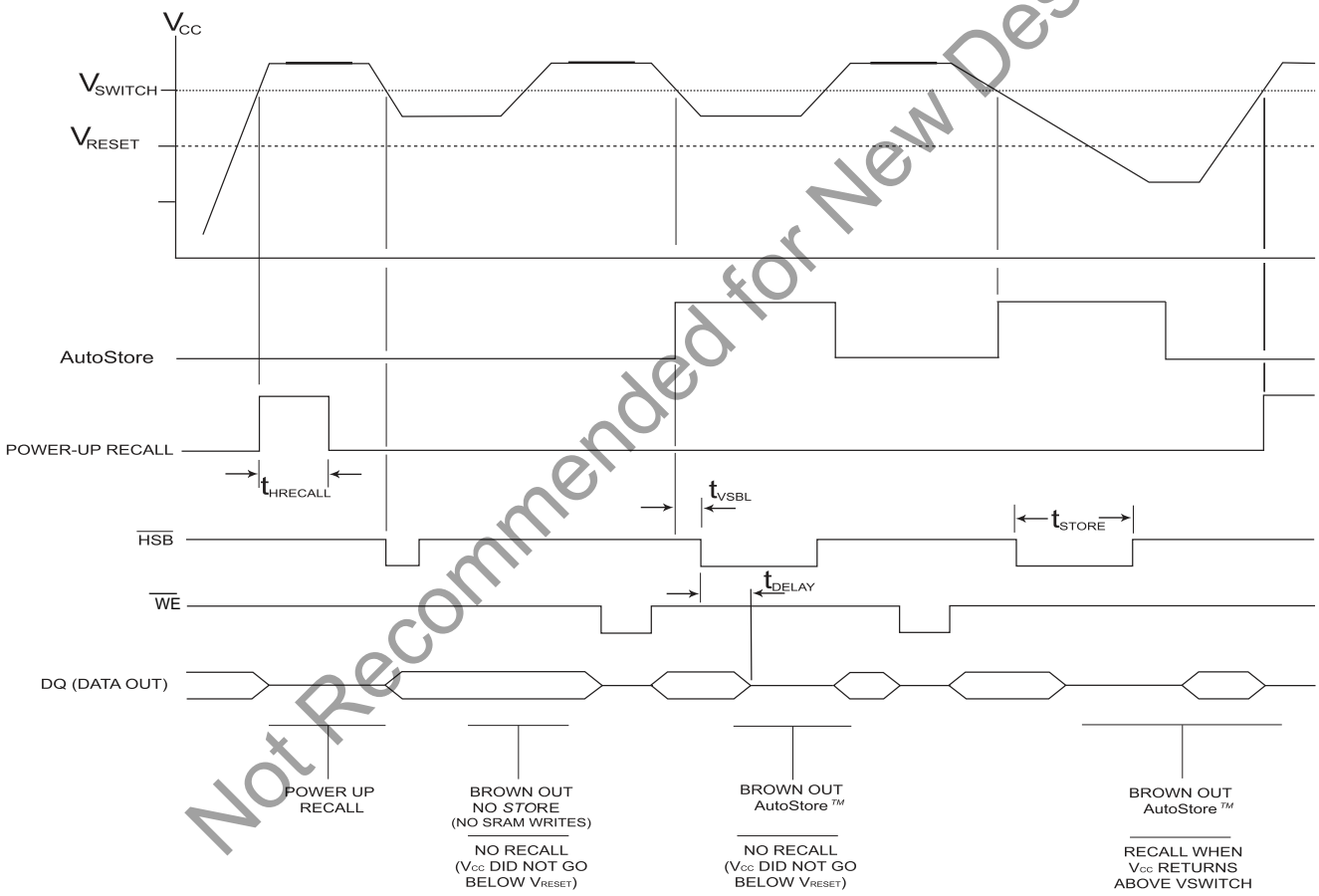
Notes
12. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
13. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.
14. HSB must be HIGH during SRAM WRITE cycles.

AutoStore or Power Up RECALL

Parameter	Alt	Description	STK14C88-3		Unit
			Min	Max	
$t_{HRECALL}$ [15]	$t_{RESTORE}$	Power up RECALL Duration		550	µs
t_{STORE} [16, 17]	t_{HLHZ}	STORE Cycle Duration		10	ms
t_{VSBL} [16]		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ low		300	ns
V_{RESET}		Low Voltage Reset Level		2.4	V
V_{SWITCH}		Low Voltage Trigger Level	2.7	2.95	V
t_{DELAY} [16]	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs

Switching Waveforms

Figure 11. AutoStore/Power Up RECALL



Notes

15. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
16. $\overline{CE}$ and $\overline{OE}$ low and $\overline{WE}$ high for output behavior.
17. $\overline{HSB}$ is asserted low for 1us when V_{CAP} drops through V_{SWITCH}. If an SRAM WRITE has not taken place since the last nonvolatile cycle, $\overline{HSB}$ will be released and no store will take place.

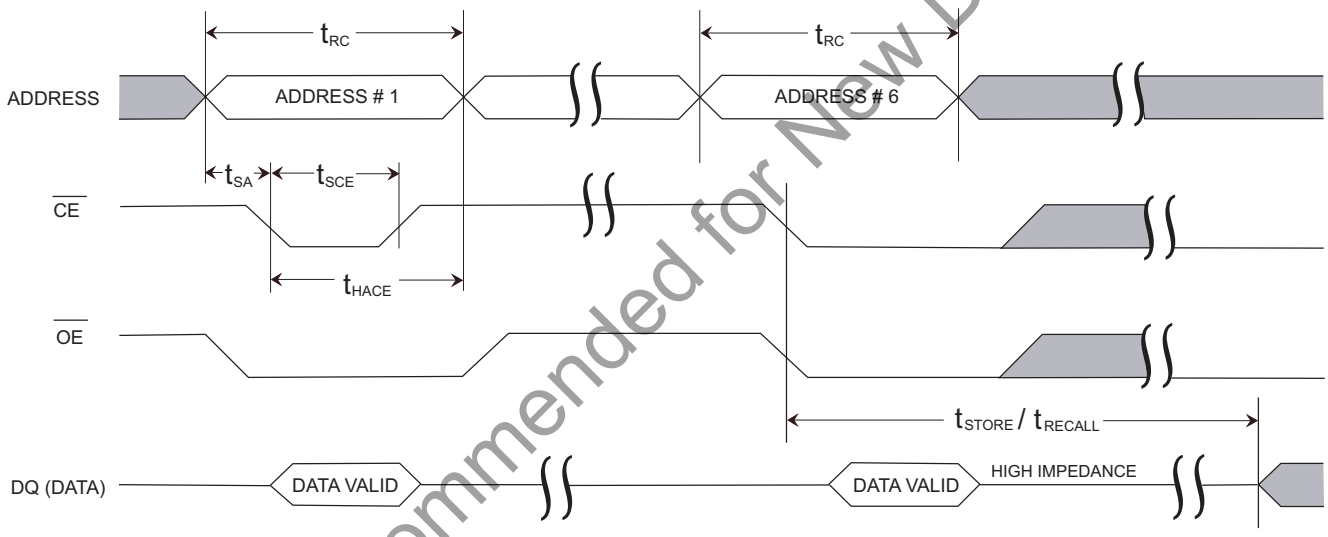
Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [18, 19]

Parameter	Alt	Description	35 ns		45 ns		Unit
			Min	Max	Min	Max	
t_{RC}[16]	t_{AVAV}	STORE/RECALL Initiation Cycle Time	35		45		ns
t_{SA}[18, 19]	t_{AVEL}	Address Setup Time	0		0		ns
t_{CW}[18, 19]	t_{ELEH}	Clock Pulse Width	25		30		ns
t_{HACE}[18, 19]	t_{ELAX}	Address Hold Time	20		20		ns
t_{RECALL}		RECALL Duration		20		20	µs

Switching Waveforms

Figure 12. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [19]



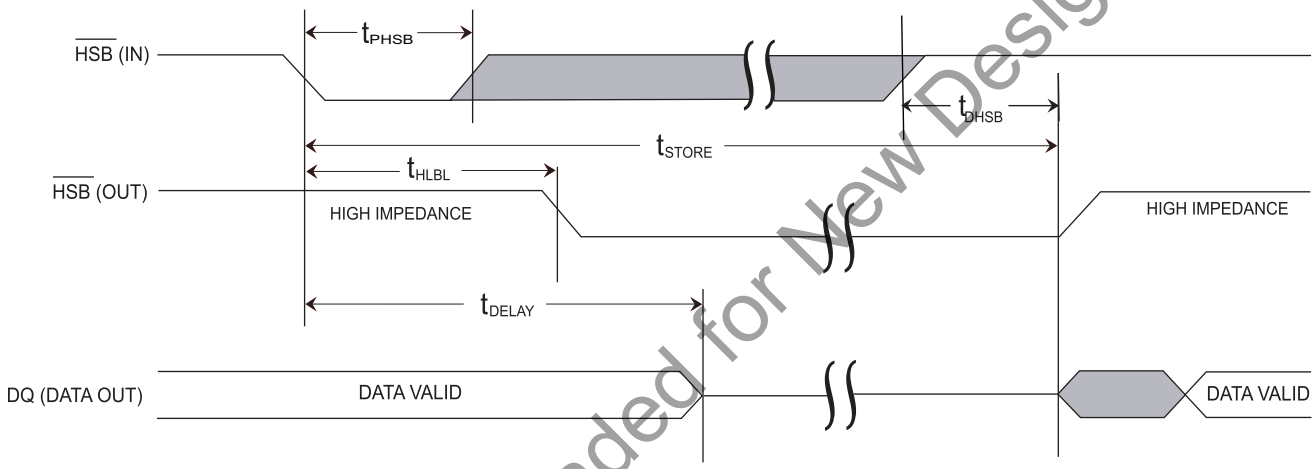
Notes
18. The software sequence is clocked on the falling edge of $\overline{CE}$ without involving $\overline{OE}$ (double clocking will abort the sequence).
19. The six consecutive addresses must be read in the order listed in the Mode Selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.

Hardware STORE Cycle

Parameter	Alt	Description	STK14C88-3		Unit
			Min	Max	
t_{PHSB}	t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{DHSB} [16, 20]	$t_{RECOVER}$, t_{HHQX}	Hardware STORE High to Inhibit Off		700	ns
t_{HLBL}		Hardware STORE Low to STORE Busy		300	ns

Switching Waveforms

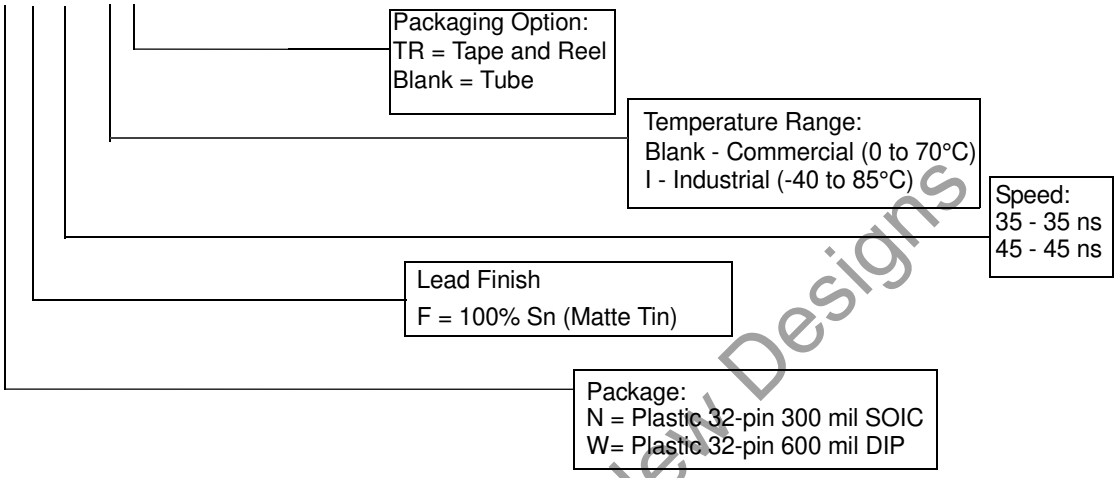
Figure 13. Hardware STORE Cycle



Note
20. t_{DHSB} is only applicable after t_{STORE} is complete.

Part Numbering Nomenclature

STK14C88- 3N F 45 I TR



Ordering Information

These parts are not recommended for new designs.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
35	STK14C88-3NF35TR	51-85127	32-pin SOIC	Commercial
	STK14C88-3NF35	51-85127	32-pin SOIC	
	STK14C88-3WF35	51-85018	32-pin PDIP	
	STK14C88-3NF35ITR	51-85127	32-pin SOIC	Industrial
	STK14C88-3NF35I	51-85127	32-pin SOIC	
	STK14C88-3WF35I	51-85018	32-pin PDIP	
45	STK14C88-3NF45TR	51-85127	32-pin SOIC	Commercial
	STK14C88-3NF45	51-85127	32-pin SOIC	
	STK14C88-3WF45	51-85018	32-pin PDIP	
	STK14C88-3NF45ITR	51-85127	32-pin SOIC	Industrial
	STK14C88-3NF45I	51-85127	32-pin SOIC	
	STK14C88-3WF45I	51-85018	32-pin PDIP	

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 14. 32-Pin (300 Mil) SOIC (51-85127)

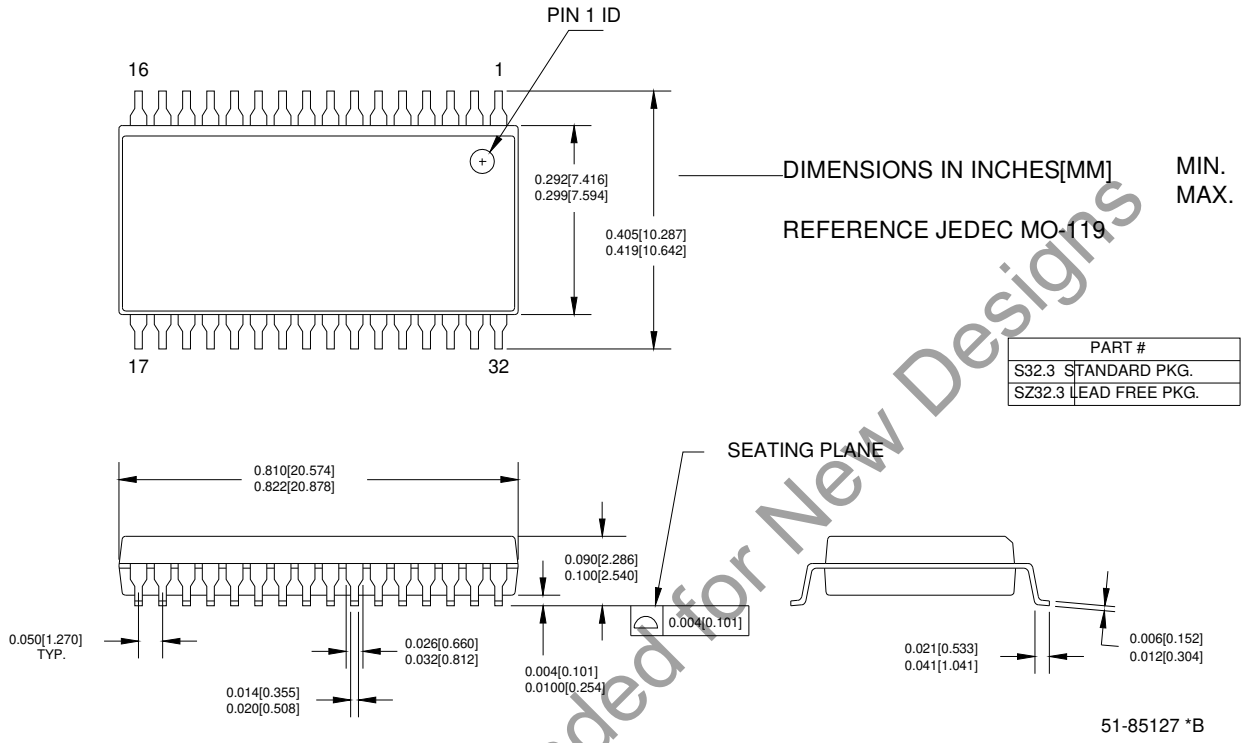
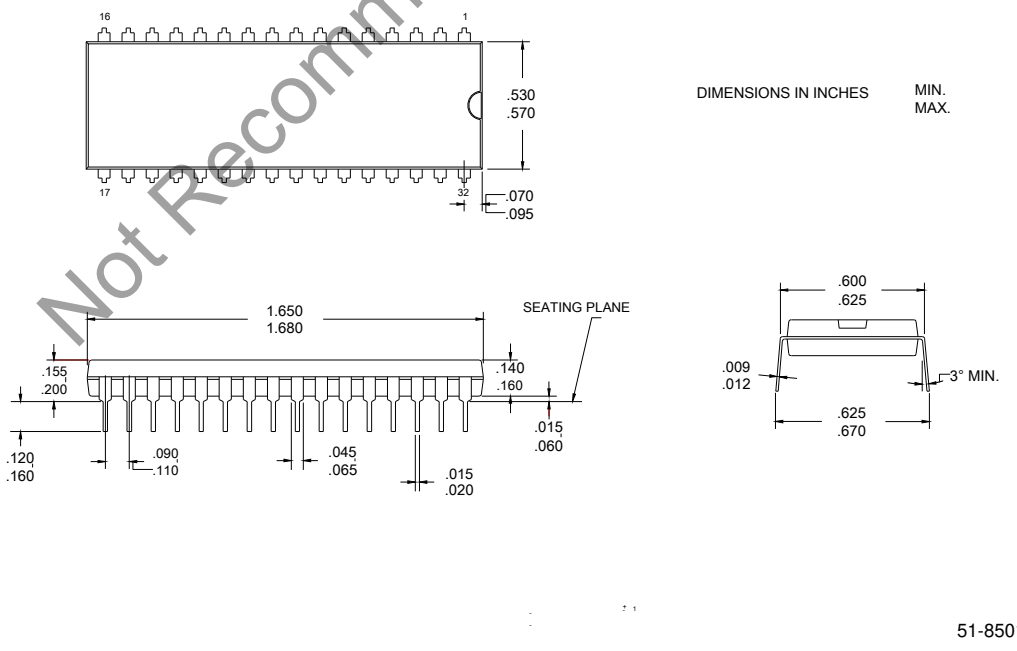


Figure 15. 32-Pin (600 Mil) PDIP (51-85018)



Document History Page

Document Title: STK14C88-3 256 Kbit (32K x 8) AutoStore nvSRAM Document Number: 001-50592				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2625096	GVCH/PYRS	12/19/08	New data sheet
*A	2821358	GVCH	12/04/2009	Added a note in Ordering information mentioning that these parts are not recommended for new designs. Added “Not Recommended for New Designs” watermark in the PDF. Added Contents on page 2..

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