






SPECIFICATIONS

CUSTOMER : _____
MODEL NO. : **GFG128128DA-GPFE**
VERSION : **B**
DATE : **2022.11.02**
CERTIFICATION : **ROHS**

Customer Sign	Approved By	Prepared By	Prepared By
			

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1. SCOPE

This specification covers the engineering requirements for the GFG128128DA-GPFE liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 128 × 128 dot matrix LCD
- STN(Gray) , Positive mode LCD panel
- Transflective , wide temperature type
- Viewing Direction: 6 o'clock
- Multiplexing driving : 1/128duty, 1/12bias
- LCD driver IC : ST7571

2.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	128 × 128
Dot dimensions(mm)	0.292 × 0.324 mm
Dot spacing (mm)	0.312 × 0.344 mm
Module dimensions (Horizontal × Vertical × Thickness, mm)	51 × 61.5 × 2.9 mm
Viewing area (Horizontal × Vertical, mm)	46 × 50 mm
Active area (Horizontal × Vertical, mm)	39.916 × 44.012 mm

2.3 Absolute Maximum Ratings (Without LED back-light)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	V _{DD}	V	-0.3 to +7.0
Input Voltage	V _{IN}	V	-0.3 to V _{DD} +0.3

Note 1: Referenced to V_{SS}=0V



2.4 Electrical Characteristics (Without LED back-light)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Logic Supply Voltage	$V_{DD} - V_{SS}$	-	2.7	3.0	3.3	V	
LCD Drive Voltage (Recommended Voltage)	$V_{OP}=V_0-V_{SS}$	VDD=3.0V, Ta=25°C	12.2	12.5	12.8	V	
Input Voltage	"H" Level	V_{IH}	-	0.8V _{DD}	-	V _{DD}	V
	"L" Level	V_{IL}		V _{SS}	-	0.2V _{DD}	V
Output Voltage	"H" Level	V_{oH}	-	0.8V _{DD}	-	V _{DD}	V
	"L" Level	V_{oL}		V _{SS}	-	0.2V _{DD}	V
Current Consumption	I_{DD}	VDD=3.0V	-	-	3.0	mA	

NOTE: 1) Duty Ratio=1/128, Bias Ratio=1/12

2) Measuring in Dots ON-state

2.5 Optical Characteristics Absolute maximum ratings

Item	Symbol	Rating	Unit
Operating temperature range	Top	-20 ~ +70	°C
Storage temperature range	Tst	-30 ~ +80	°C

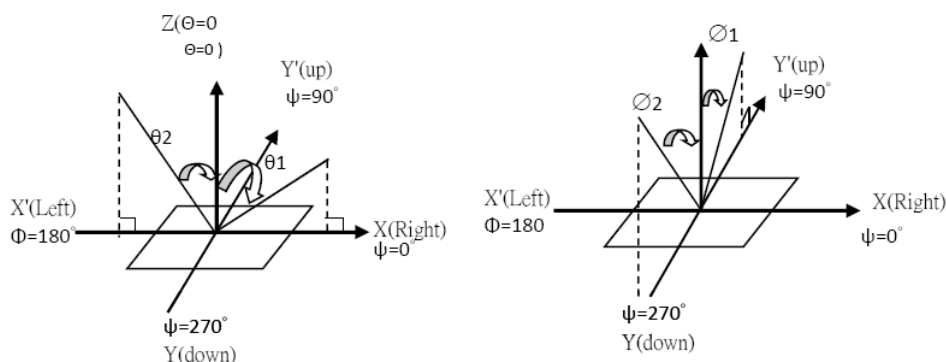


2.6. Optical Characteristics

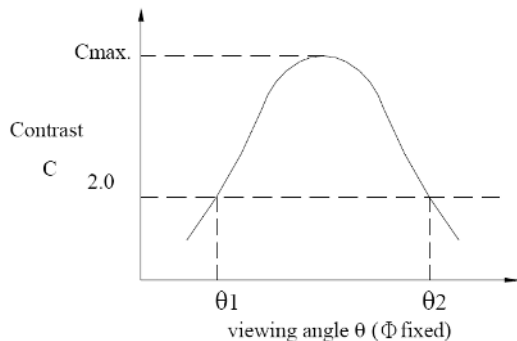
1/128 duty, 1/12 bias, $V_{op}=12.5\text{ V}$, $T_a=25^\circ\text{C}$

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	V_{op}		12.2	12.5	12.8	
Viewing angle	θ_1 、 θ_2	$C \geq 2.0, \varnothing = 0^\circ\text{C}$	30°	-	-	Notes 1 & 2
Contrast	C	$\theta = 5^\circ, \varnothing = 0^\circ$	2.0	-	-	Note 3
Response time(rise)	t_{on}	$\theta = 5^\circ, \varnothing = 0^\circ$	-	-	350ms	Note 4
Response time(fall)	t_{off}	$\theta = 5^\circ, \varnothing = 0^\circ$	-	-	450ms	Note 4

Note 1: Definition of angles θ and \varnothing

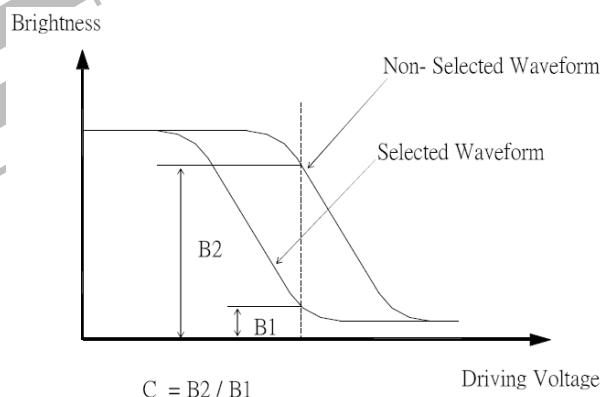


Note 2: Definition of viewing angles θ_1 and θ_2

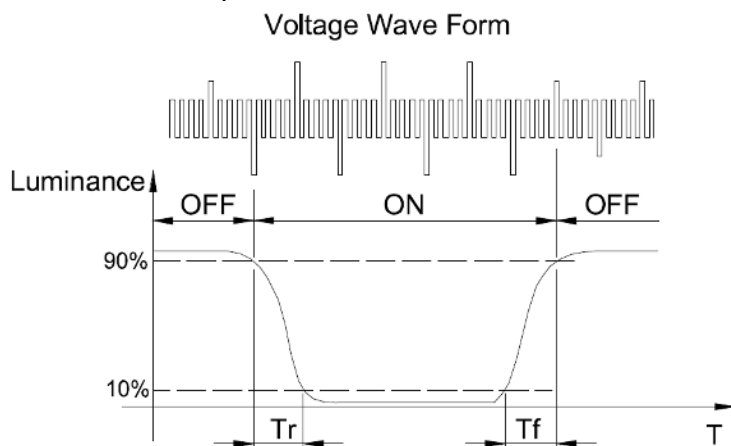


Note : Optimum viewing angle with the naked eye and viewing angle θ at C_{max} . Above are not always the same

Note 3: Definition of contrast C



Note 4: Definition of response time





2.7 LED Back-light Characteristics

2.7.1 Electrical / optical specifications

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V _f	I _f =60mA, WHITE	2.9	3.2	3.5	V
LED *Luminous Intensity	I _v	I _f =60mA, WHITE	1000	1500	--	cd/m ²
Chromaticity Coordinate	x	I _f =60mA, WHITE	0.26	-	0.30	
	y		0.265	-	0.305	
Luminous Uniformity	ΔL _v	I _f =60mA, WHITE	70			%

Note: * Measured at the bare LED back-light unit.

2.7.2 LED Maximum Operating Range

Item	Symbol	WHITE	Unit
Power Dissipation	P _{AD}	204	mW
Forward Current	I _F	105	mA
Reverse Voltage	V _R	5	V



3. RELIABILITY

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	80°C	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-30°C	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40°C 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	70°C	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	-20°C	120 hrs	Appearance Without defect	
6	Thermal Shock	-20°C, 30min. → 70°C, 30min. ↑ (1cycle)		Appearance Without defect	10 cycles

** Dissipation current, contrast and display functions

** Polarizing filter deterioration, other appearance defects

** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.



4. OPERATING INSTRUCTIONS

4.1 Interface description

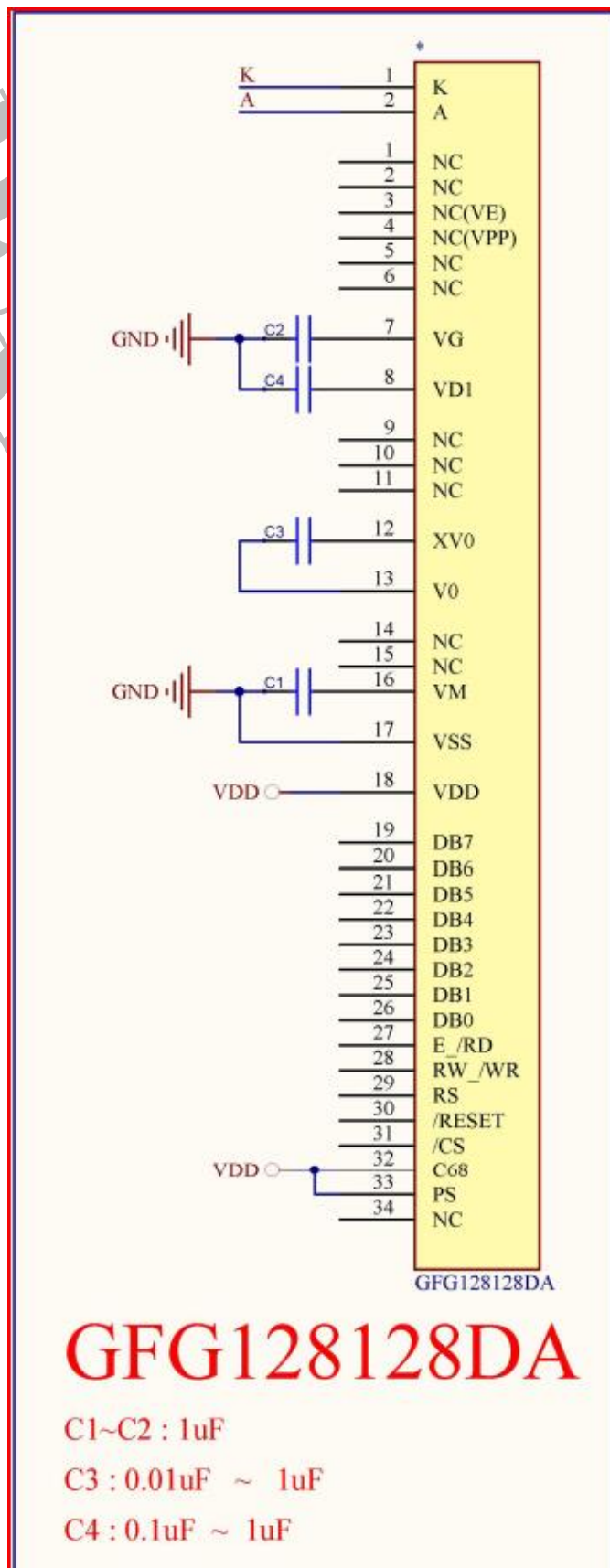
NO.	Symbol	Function															
1	NC	No connection.															
2	NC	No connection.															
3	NC(VE)	No connection (When writing EEPROM, VE should be pull-high externally.)															
4	NC(VPP)	No connection (When writing EEPROM, it needs external power supply voltage.)															
5	NC	No connection.															
6	NC	No connection.															
7	VG	LCD driving voltage ($1.8V \leq VG < VDD-0.4V$)															
8	VD1	power supply pin of the internal digital power regulator.															
9	NC	No connection.															
10	NC	No connection.															
11	NC	No connection.															
12	XV0	LCD driving voltage.															
13	V0	LCD driving voltage ($V0 \geq VG > VM > VSS \geq XV0$)															
14	NC	No connection.															
15	NC	No connection.															
16	VM	LCD driving voltage. ($0.7V < VM < VG$).															
17	VSS	Ground															
18	VDD	power supply input															
19~26	DB7 DB0	8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS="L"); DB0 to DB5: high impedance DB6: serial input clock (SCLK) DB7: serial input data (SID) When chip select is not active, DB0 to DB7 may be high impedance.															
27	E_/RD	Read / Write execution control pin. <table border="1"> <thead> <tr> <th>C68</th> <th>PS0</th> <th>MPU Type</th> <th>RWR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>6800-series</td> <td>E</td> <td>The data on D[7:0] are latched at the falling edge of the E signal.</td> </tr> <tr> <td>L</td> <td>H</td> <td>8080-series</td> <td>/RD</td> <td>Keep this pin at "H" level.</td> </tr> </tbody> </table> ERD is not used in serial interface, it is recommend to fix ERD at "H" by VDD1	C68	PS0	MPU Type	RWR	Description	H	H	6800-series	E	The data on D[7:0] are latched at the falling edge of the E signal.	L	H	8080-series	/RD	Keep this pin at "H" level.
C68	PS0	MPU Type	RWR	Description													
H	H	6800-series	E	The data on D[7:0] are latched at the falling edge of the E signal.													
L	H	8080-series	/RD	Keep this pin at "H" level.													
28	RW_/WR	Write execution control pin.															



		C68	PS0	MPU Type	RWR	Description																					
		H	H	6800-series	R/W	Write control input pin. Keep this pin at "L" level.																					
		L	H	8080-series	/WR	The data on D[7:0] are latched at the rising edge of the /WR signal.																					
		RWR is not used in serial interface, it is recommend to fix RWR at "H" by VDD1																									
29	RS	Register select input pins RS="H": DB0 to DB7 are display data RS="L": DB0 to DB7 are control data.																									
30	/RESET	Reset input pin. When RST is "L", initialization is executed.																									
31	/CS	Chip Select input pins Data/Instruction I/O is enabled only when CSB is "L". When chip select s non-active, DB[7: 0] are high impedance.																									
32	C68	Microprocessor interface select input pin																									
		<table border="1"> <thead> <tr> <th>Interface Select</th> <th>6800 series</th> <th>8080 series</th> <th>4 pin SPI</th> <th>3 pin SPI</th> </tr> </thead> <tbody> <tr> <td>PS</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>C86</td> <td>H</td> <td>L</td> <td>H</td> <td>L</td> </tr> </tbody> </table>					Interface Select	6800 series	8080 series	4 pin SPI	3 pin SPI	PS	H	H	L	L	C86	H	L	H	L						
Interface Select	6800 series	8080 series	4 pin SPI	3 pin SPI																							
PS	H	H	L	L																							
C86	H	L	H	L																							
33	PS	Parallel / Serial data select input.																									
		<table border="1"> <thead> <tr> <th>PS</th> <th>Interface Mode</th> <th>Chip Select</th> <th>Data / Instruction</th> <th>Data</th> <th>Read / Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Parallel</td> <td>CSB</td> <td>RS</td> <td>DB7 to DB0</td> <td>E_RD, RW_WR</td> <td>—</td> </tr> <tr> <td>L</td> <td>Serial</td> <td>CSB</td> <td>RS</td> <td>DB7(SID)</td> <td>Write Only</td> <td>DB6 (SCLK)</td> </tr> </tbody> </table>					PS	Interface Mode	Chip Select	Data / Instruction	Data	Read / Write	Serial Clock	H	Parallel	CSB	RS	DB7 to DB0	E_RD, RW_WR	—	L	Serial	CSB	RS	DB7(SID)	Write Only	DB6 (SCLK)
PS	Interface Mode	Chip Select	Data / Instruction	Data	Read / Write	Serial Clock																					
H	Parallel	CSB	RS	DB7 to DB0	E_RD, RW_WR	—																					
L	Serial	CSB	RS	DB7(SID)	Write Only	DB6 (SCLK)																					
		Note : In serial mode, it cannot read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L".																									
34	NC	No connection.																									



4.2 Application circuit and external components





4.3 Timing Diagram

8080 Series MPU

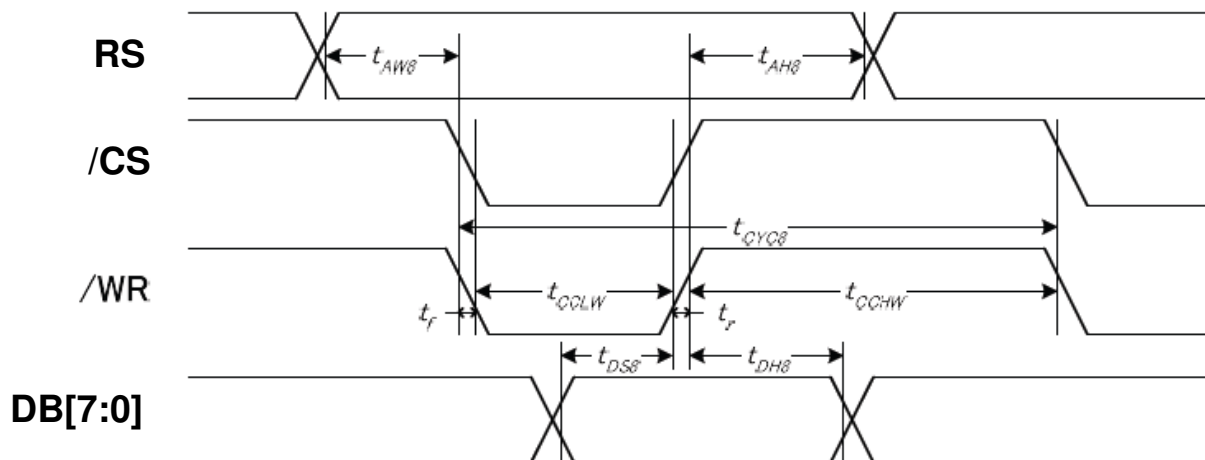


Fig. 32

(VDD1 = 1.8V~3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	RS	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time	/WR	tCYC8		500	—	
Write L pulse width		tCCLW		250	—	
Write H pulse width		tCCHW		250	—	
WRITE Data setup time	DB[7:0]	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	

- The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ is specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- tCCLW is specified as the overlap between /CS being "L" and /WR being at the "L" level.



6800 Series MPU

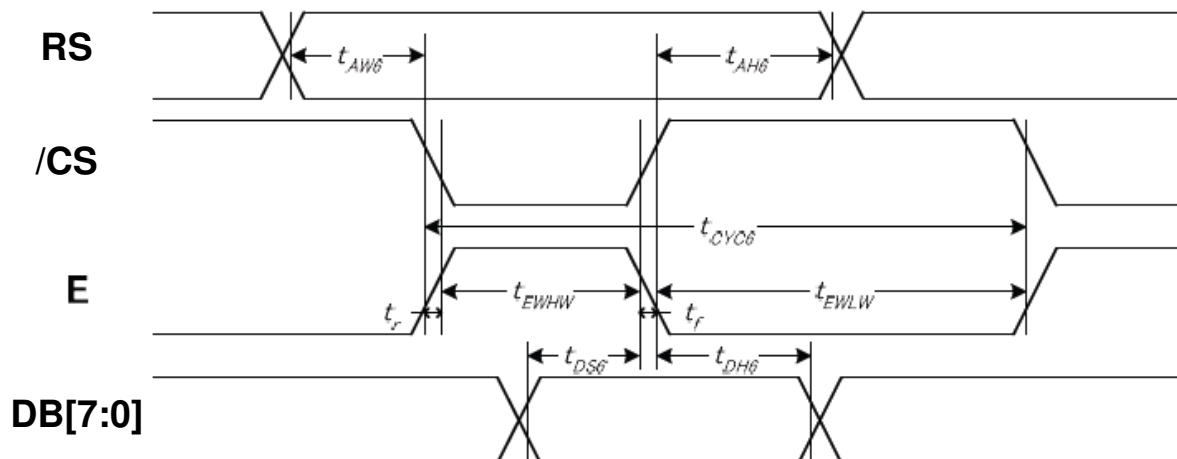


Fig. 33

(VDD1 = 1.8V~3.3V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	RS	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time	E	tCYC6		500	—	
Enable L pulse width (Write)		tEHLW		250	—	
Enable H pulse width (Write)		tEHHW		250	—	
WRITE Data setup time	DB[7:0]	tDSL6		80	—	
WRITE Data hold time		tDHL6		30	—	

- The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC6} - t_{EHLW} - t_{EHHW})$ is specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- tEHLW is specified as the overlap between /CS being "H" and E being "L".
- R/W signal is always "L".



Serial 4-Line Interface

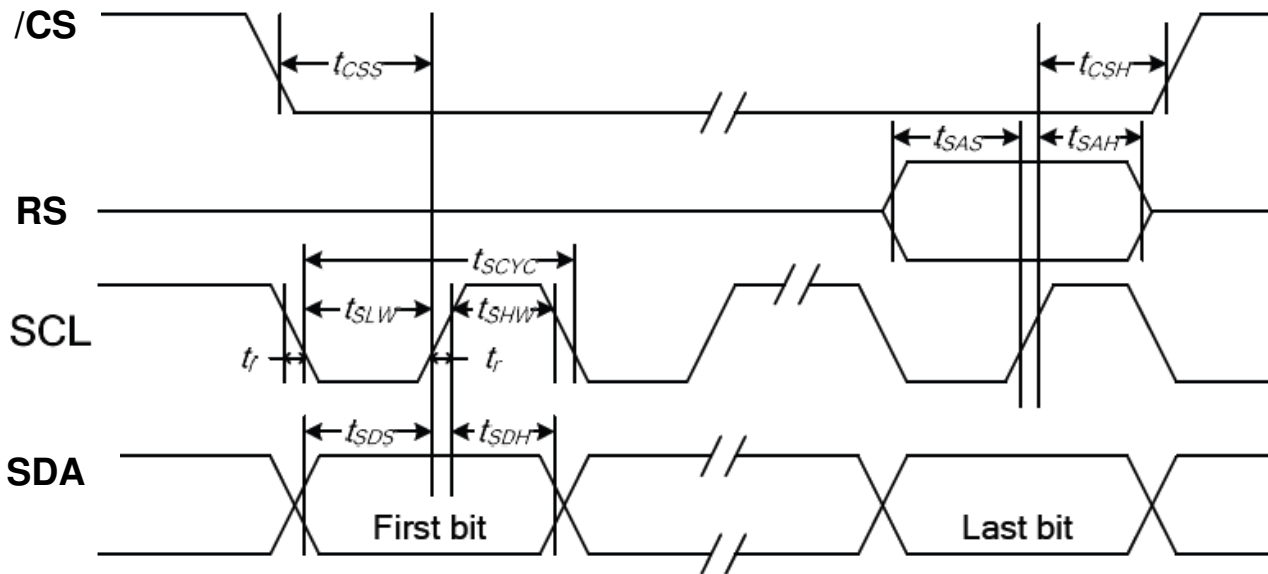


Fig. 34

(VDD1 = 1.8V~3.3V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	RS	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		40	—	
CS-SCL time		tCSH		100	—	

- The input signal rise and fall time (t_r , t_f) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDD1 as the standard.



Serial 3-Line Interface

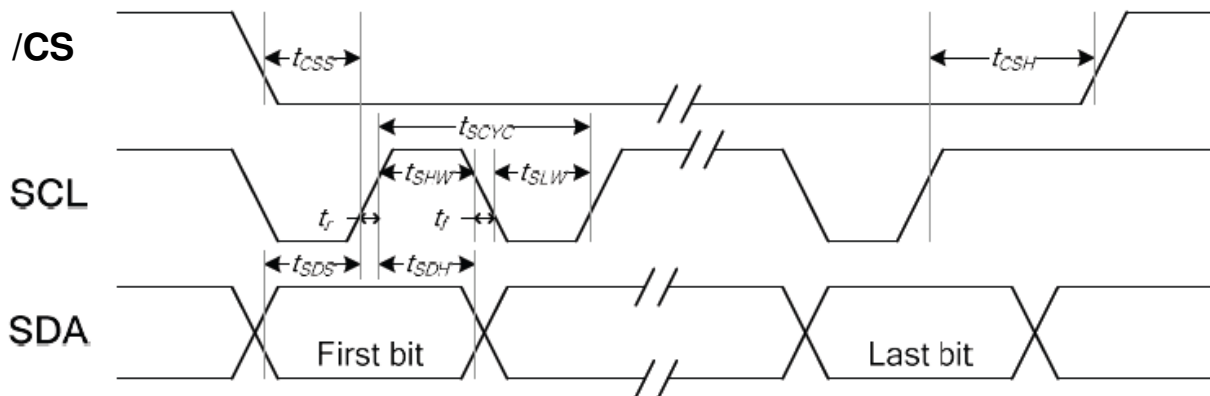


Fig. 35

(VDD1 = 1.8V~3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		40	—	
CS-SCL time		tCSH		100	—	

- The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDD1 as the standard.



5. Instruction Description

Instruction	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
Set Mode	0	0	0	0	1	1	1	0	0	0	2-byte instruction
	0	0	FR3	FR2	FR1	FR0	BE1	BE0	--	0	FR[3:0]: Set frame frequency BE[1:0]: Set booster efficiency
Write Display Data	1	0	Write data							Write data into DDRAM	
Set ICON	0	0	1	0	1	0	0	0	1	ION	ION=0: Disable icon function ION=1: Enable icon function and set Page Address = 16
Set Page Address	0	0	1	0	1	1	P3	P2	P1	P0	Set Page Address
Set Column Address (MSB)	0	0	0	0	0	1	0	X7	X6	X5	Set MSB of Column Address
Set Column Address (LSB)	0	0	0	0	0	0	X4	X3	X2	X1	Set LSB of Column Address
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON
Set Display Start Line	0	0	0	1	0	0	0	0	--	--	2-byte instruction. Specify Line Address for the 1 st display line of DDRAM (vertical scrolling).
	0	0	--	S6	S5	S4	S3	S2	S1	S0	
Set COM0	0	0	0	1	0	0	0	1	--	--	2-byte instruction. Specify a COM pin to be COM0 (moving partial display window).
	0	0	--	C6	C5	C4	C3	C2	C1	C0	
Set Display Duty	0	0	0	1	0	0	1	0	--	--	2-byte instruction. Set display duty
	0	0	L7	L6	L5	L4	L3	L2	L1	L0	
Set N-line Inversion	0	0	0	1	0	0	1	1	--	--	2-byte instruction. Set N-line inversion counter
	0	0	--	--	--	N4	N3	N2	N1	N0	
Release N-line Inversion	0	0	1	1	1	0	0	1	0	0	Exit N-line inversion mode
Reverse Display	0	0	1	0	1	0	0	1	1	REV	REV=0: Normal display REV=1: Reverse display
Entire Display ON	0	0	1	0	1	0	0	1	0	EON	EON=0: Normal display EON=1: Entire display ON



Instruction	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
Power Control	0	0	0	0	1	0	1	VC	VR	VF	Set internal power ON/OFF
Select Regulator Register	0	0	0	0	1	0	0	R2	R1	R0	Select internal Regulator resistor
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Select EV for internal Regulator's reference
	0	0	--	--	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Set COM Scan Direction	0	0	1	1	0	0	MY	--	--	--	Set COM scan direction: MY=0: Normal direction MY=1: Reverse direction
Set SEG Scan Direction	0	0	1	0	1	0	0	0	0	MX	Set SEG scan direction: MX=0: Normal direction MX=1: Reverse direction
Oscillator ON	0	0	1	0	1	0	1	0	1	1	Turn ON internal Oscillator
Set Power-Save Mode	0	0	1	0	1	0	1	0	0	P	P=0: Normal mode P=1: Enable Power-Save mode
Release Power-Save Mode	0	0	1	1	1	0	0	0	0	1	Exit Power-Save mode
RESET	0	0	1	1	1	0	0	0	1	0	Software reset
Set Display Data Length	--	--	1	1	1	0	1	0	0	0	2-byte instruction. Set the data counter in 3-Line SPI only
	--	--	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Reserved	0	0	1	1	1	0	0	0	0	0	Do NOT use
Reserved	0	0	1	1	1	0	1	1	1	0	Do NOT use
Reserved	0	0	1	1	1	1	--	--	--	--	Reserved for testing
Extension Command Set1	0	0	1	1	1	1	1	1	0	TE1	TE1=1: Enter extension Mode1
Extension Command Set2	0	0	1	1	0	1	0	0	0	TE2	TE2=1: Enter extension Mode2
Extension Command Set3	0	0	0	1	1	1	1	0	1	TE3	TE3=1: Enter extension Mode3

100%



Instruction	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
EXTENSION COMMAND SET 1											
Set dark gray scale	0	0	0	0	0	1	GDA3	GDA2	GDA1	GDA0	Select gray level for dark
Set light gray scale	0	0	0	0	1	0	GLA3	GLA2	GLA1	GLA0	Select gray level for light
Increase Vop offset	0	0	0	1	0	1	0	0	0	1	Increase vop offset by 1step
Decrease Vop offset	0	0	0	1	0	1	0	0	1	0	Decrease vop offset by 1 step
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
EXTENSION COMMAND SET 2											
Disable autoread	0	0	1	0	1	0	1	0	1	0	Disable autoread
Enter EEPROM mode	0	0	0	0	0	1	0	0	1	1	Enter EEPROM mode
Enable read mode	0	0	0	0	1	0	0	0	0	0	Enable read mode
Set read pulse	0	0	0	1	1	1	0	0	0	1	Set read pulse width
Exit EEPROM mode	0	0	1	0	0	0	0	0	1	1	Exit EEPROM mode
Enable erase mode	0	0	0	1	0	0	1	0	1	0	Enable erase mode
Set erase pulse	0	0	0	1	0	1	0	1	0	1	Set erase pulse width
Enable write mode	0	0	0	0	1	1	0	1	0	1	Enable write mode
Set write pulse	0	0	0	1	1	0	1	0	1	0	Set write pulse width
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
EXTENSION COMMAND SET 3											
Set Color Mode	0	0	0	0	0	1	0	0	0	B/G	Select Black/White or Gray mode B/G=1: Black/White mode; B/G=0: Gray mode (default)
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode

Note: Do NOT use non-specified instructions in any extension command mode.



6. NOTES

▪ Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is $25\text{ }^{\circ}\text{C}\pm 10\text{ }^{\circ}\text{C}$ and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

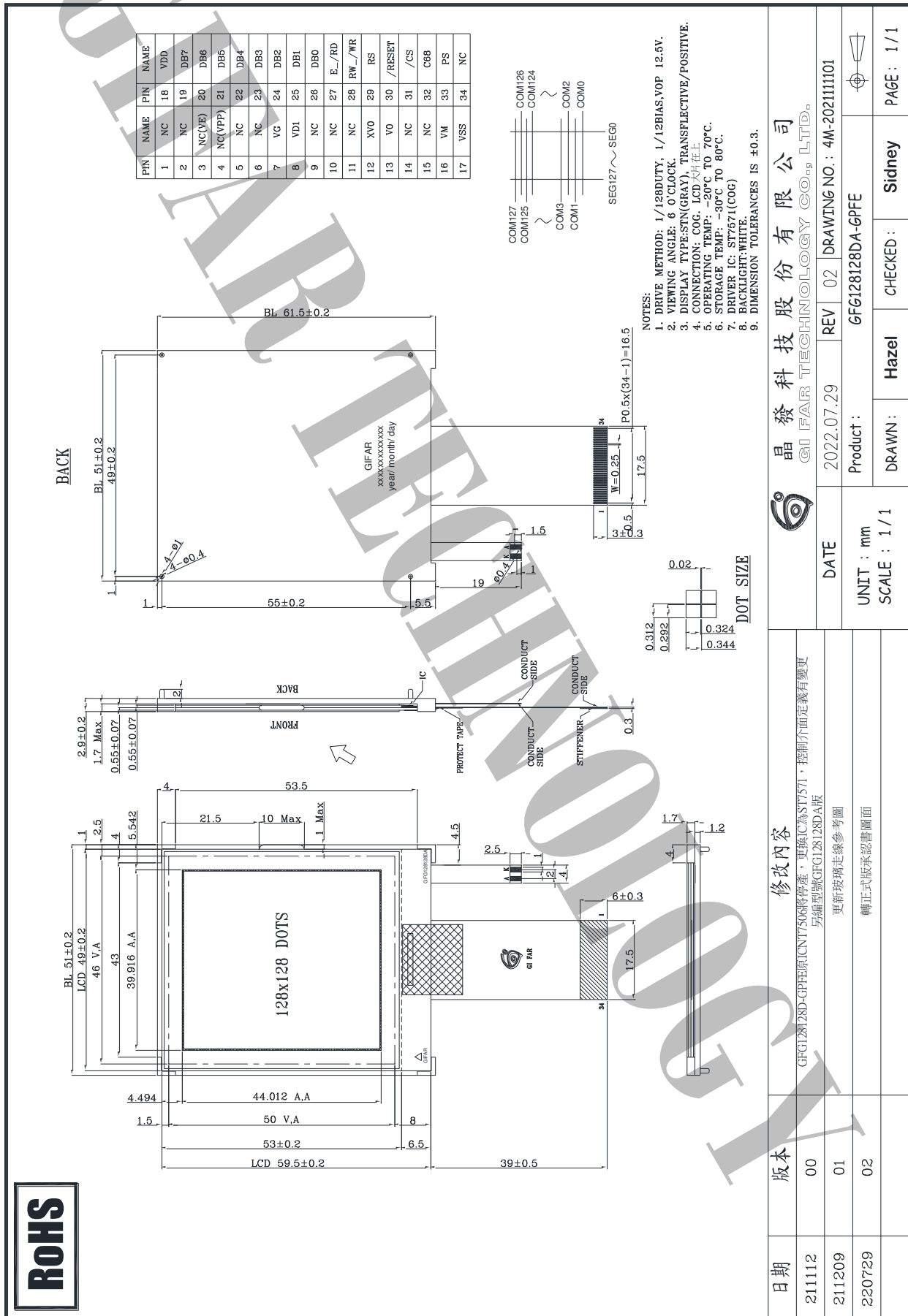
7. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

Quality warranty period: Within one year after shipment date (excluding abnormal usage way and abnormal environments.)



8. LCM Dimension



日期	版本	修改內容	DATE	REV	Product	DRAWN	CHECKED	PAGE
211112	00	GHG128128D-GPFE原(CNT1750)將標產・車標(C為ST7571・控制介面定義有變更 另編型號GHG128128DA版	2022.07.29	02	GF6128128DA-GPFE	Hazel	Sidney	1 / 1
211209	01	更新玻璃走線參考圖						
220729	02	轉正式版承認書圖面						

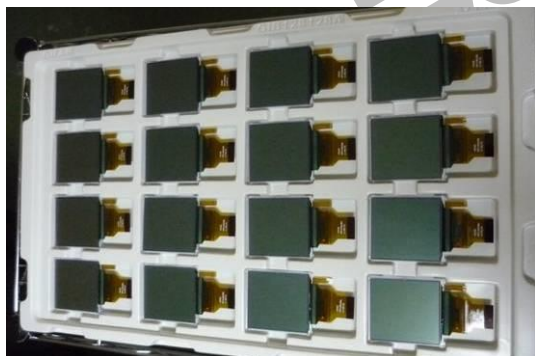


9. PACKAGE INFORMATION

1	1 Tray	:	16 pcs (modules)
2	1 stack	:	10 tray +1 Cover tray
3	1 Carton	:	(1 Cover tray + 10 tray)x 3 stack
4	Total pcs	:	1 Carton (16pcs*10tray *3stack) = 480 pcs
5	Carton size = NO. 17	:	495*315*435mm
7	Net weight	:	(6.3) KG
8	Gross weight	:	(11.6) KG

** 包裝示意圖片 **

- 一個 tray 盤 可放 16PCS 模組



- 10 盤+1 空盤=1 疊，TRAY 盤上、下兩層需交叉堆疊放置



- 使用 17 號箱，可放入 3 疊，並使用防震材將旁邊空隙填滿



出貨檢驗標準書
Shipping inspection standard

核准 Approved by	審核 Checked by	作成 Made by
ANDY	JACKY	RUBY

1.目的 Purpose :

規範出貨產品之檢驗項目及判斷標準，確保產品出貨能滿足客戶要求。

Standardize the inspection items and judgment standards to ensure the products that shipped out can meet customer's requirements.

2.範圍 Area :

適用於出廠之所有產品。

Applicable to all products shipped from the factory.

3.名詞解釋 Explanation of terms :

3-1 主要缺陷：亦會造成功能缺失或嚴重外觀缺陷。

Major Defects: It also causes loss of function or serious appearance defects.

3-2 次要缺陷：稍有缺陷但不影響客戶使用。

Minor defect: Slightly defective but does not affect customer use.

4.檢驗體制 Inspection system :

4-1 抽樣計劃：依 ANSI/ASQ Z1.4 一般檢驗水準 II 之 正常檢驗一次抽驗方案。

Sampling plan: According to ANSI/ASQ Z1.4 general inspection level II the normal inspection one-time sampling plan.

4-2 允收水準 Acceptable Level : (AQL)

主要缺陷 Major defect : 0.4 %

次要缺陷 Minor defect : 0.65 %

5.檢驗條件 Inspection conditions :

5-1 使用相關之檢測儀器及測試、量測工具。

Use relevant testing instrument, testing and measuring tools .

5-2 環境要求：其條件需控制在常溫下 $23^{\circ}\text{C}\pm 3^{\circ}\text{C}$ 及溼度 70%RH 以下。

Environmental requirements: The conditions should be controlled at room temperature $23^{\circ}\text{C}\pm 3^{\circ}\text{C}$ and humidity below 70%RH.

5-3 外觀檢驗：須在 $380\pm 20\%$ LUX 的白色日光燈下，其目視距離需於產品離 30 ± 5 cm 檢驗。

Appearance inspection: Under the white fluorescent lamp of $380\pm 20\%$ LUX , the visual distance shall be checked above the product 30 ± 5 cm.

5-4 電性測試 Electrical Testing :

5-4-1 有背光之產品需關燈並在 $5\sim 300\text{Lux}\pm 3\%$ 下檢驗。

The products with backlight should be tested at $5\sim 300\pm 3\%$ Lux.

5-4-2 無背光之產品需開燈並在 $60\sim 300\text{Lux}\pm 3\%$ 白色日光燈下檢驗。

Products without backlight need to be turned on and tested under $60\sim 300 \pm 3\%$ LUX white fluorescent lamps .

5-5 檢查視角依產品視角方向。

Check the viewing angle according to the product viewing angle.

5-6 其不良現象檢視區域 Bad phenomenon View area

5-6-1 適用種類 Applicable category : COB、TFT



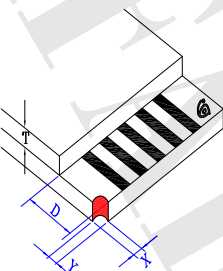
5-6-2 適用種類 Applicable category : COG、TAB、TN



種類 Category		COG																			
編號 No.	檢驗項目 Item	檢驗內容及判定標準 Inspection Content & Standard			區域 Zone	類別 Category	缺陷等級 Level														
1	點類(一) Dot(1)	黑點、刺傷...等圓狀 Black dot、Stab...and other round shape $\phi = \frac{(X + Y)}{2}$ 	兩點距離須超過 5 mm Two points have to be ≥ 5 mm		A B	外觀 Appearance	次要 Minor AQL0.65%														
		ϕ (mm)	允收數 Acceptance Qty																		
		$\phi \leq 0.1$	無視 Ignore																		
		$0.1 < \phi \leq 0.25$	3																		
		$0.25 < \phi \leq 0.3$	1																		
		$\phi > 0.3$	0																		
2	點類(二) Dot(2)	氣泡、凹凸點 Bubble、Uneven dots $\phi = \frac{(X + Y)}{2}$ 	兩點距離須超過 5 mm Two points have to be ≥ 5 mm		A B	外觀 Appearance	次要 Minor AQL0.65%														
		ϕ (mm)	允收數 Acceptance Qty																		
		$\phi \leq 0.2$	無視 Ignore																		
		$0.2 < \phi \leq 0.5$	2																		
		$\phi > 0.5$	0																		
3	線類 Line	刮傷、毛屑...等線狀 Scratch、Fiber.. and other linear shape. 	<table border="1"> <thead> <tr> <th>L (mm)</th> <th>W (mm)</th> <th>允收數 Acceptance Qty</th> </tr> </thead> <tbody> <tr> <td>--</td> <td>$W \leq 0.02$</td> <td>無視 Ignore</td> </tr> <tr> <td>$L \leq 5$</td> <td>$W \leq 0.03$</td> <td>3</td> </tr> <tr> <td>$L \leq 3$</td> <td>$W \leq 0.05$</td> <td>2</td> </tr> <tr> <td>$L > 5$</td> <td>$W > 0.05$</td> <td>0</td> </tr> </tbody> </table>	L (mm)	W (mm)	允收數 Acceptance Qty	--	$W \leq 0.02$	無視 Ignore	$L \leq 5$	$W \leq 0.03$	3	$L \leq 3$	$W \leq 0.05$	2	$L > 5$	$W > 0.05$	0	A B	外觀 Appearance	次要 Minor AQL0.65%
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$L \leq 3$	$W \leq 0.05$	2																			
$L > 5$	$W > 0.05$	0																			
4	底色 Background color	同批供貨不能有明顯色差 No obvious color difference allowed in same shipment. (必要時與客端制定限度樣) (According to the gold samples if necessary)			B	外觀 Appearance	次要 Minor AQL0.65%														
5	FPC 外觀 FPC Appearance	※ FPC 上刺傷導致線路無法導通 拒收 Stabbing on the FPC causes the line to fail to conduct Reject ※ FPC 上髒污或是殘留異物以致線路無法導通 拒收 Dirty or residual foreign matter on the FPC makes the circuit unable to conduct Reject ※ FPC 直角折痕、斷裂 拒收 FPC right-angle crease and fracture Reject			C	外觀 Appearance	主要 Major AQL 0.4%														

6	點、線類 (三) Dot、Line (3)	※ 於全黑、白畫面下看見之區塊狀或線狀不良 拒收 There is a block or linear in the view area under the screen is whole black or white. Reject ※ 但依 2% ND Filter 遮蓋無視 允收 But after inspecting by 2% ND Filter without seeing block or linear, it is confirmed Acceptance	A	電訊 Electronics	次要 Minor AQL0.65%
7	點、線類 (四) Dot、Line (4)	畫面中顯示出現黑、白、亮、異色點或線狀 There is a black, white, bright or other dot or lines showing in the view area. ※ 依編號 1、3 之判定標準 According to the inspection standard: No. 1 and 3.	A	電訊 Electronics	次要 Minor AQL0.65%
8	缺字 Lack of characters	顯示時畫面缺少部份字元 拒收 Lacking part of characters in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
9	無動作 No reaction	顯示畫面一直處於起始畫面而無法進行切換 拒收 The display (view area) always show in the initial screen and can't be switched to others. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
10	無畫面 No display	通電後，完全無任何畫面顯示 拒收 After connecting to the power, there is no image. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
11	斷線 Broken line	顯示畫面中少直、橫線 拒收 There is a lack of vertical or horizontal lines in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
12	CROSS TALK	顯示畫面時有局部之條紋或拖影 There are some stripes or shadow/smear showing in the view area. 拒收或與客端簽訂限度樣 Reject or inspect according to the golden sample	A	電訊 Electronics	次要 Minor AQL0.65%
13	I CON	顯示畫面缺少部份顯示圖案 拒收 Lack of partial ICON in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%

14	深淺不一 Color difference	顯示畫面的對比，比其他顯示深或淺並依電氣規格(VOP)值判定 The color contrast of display is obviously lighter or darker than others and according to the VOP value in the electronics specification. 拒收或與客端簽訂限度樣 Reject or inspect according to the golden sample	A	電訊 Electronics	次要 Minor AQL0.65%												
15	畫面異常 Abnormal screen	通電後畫面出現未定義之電訊不良現象 拒收 After connecting to the power, there is an undefined electronics appearance showing in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%												
16	背光色不均 Uneven color of backlight	※ 點亮後 LED 有明暗不均現象依其均勻度判定 拒收 After lighting LEDs have brightness and darkness uneven the determined according to its uniformity. Reject ※ 點亮後 LED 色澤不一致 拒收 LED color is inconsistent after lighting. Reject	A	電訊 Electronics	次要 Minor AQL0.65%												
17	亮度不足 Lack of brightness	波長、色座標、輝度與圖面標示定義不符 拒收 Wave length, chromatic coordinates, brightness don't correspond to the definition of the drawing. Reject	A	電訊 Electronics	主要 Major AQL 0.4%												
18	背光腳柱 Backlit foot post	斷裂、長度不一 拒收 Fracture, different length Reject	--	外觀 Appearance	次要 Minor AQL0.65%												
19	破損 Damaged	<p>Y：破損寬 X：破損長 Y: Damaged width X: Damaged length</p>  <table border="1"> <thead> <tr> <th>Y</th> <th>X</th> <th>判定 Determination</th> </tr> </thead> <tbody> <tr> <td>Y ≤ 1.0</td> <td>-- --</td> <td>允收 Acceptance</td> </tr> <tr> <td>未進入可視區 Did not enter the viewing area</td> <td>≤ 1/8 玻璃該邊長 ≤ 1/8 The side length of the glass</td> <td>允收 Acceptance</td> </tr> <tr> <td>進入可視區 Enter the viewing area</td> <td>-- --</td> <td>拒收 Reject</td> </tr> </tbody> </table>	Y	X	判定 Determination	Y ≤ 1.0	-- --	允收 Acceptance	未進入可視區 Did not enter the viewing area	≤ 1/8 玻璃該邊長 ≤ 1/8 The side length of the glass	允收 Acceptance	進入可視區 Enter the viewing area	-- --	拒收 Reject	B	外觀 Appearance	次要 Minor AQL0.65%
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20	角崩 Corner collapse		Y：破損寬 X：破損長 Y: Damaged width X: Damaged length <table border="1" data-bbox="566 537 1109 846"> <thead> <tr> <th>Y</th> <th>X</th> <th>判定 Determination</th> </tr> </thead> <tbody> <tr> <td>$\leq 1/3D$</td> <td>-- --</td> <td>允收 Acceptance</td> </tr> <tr> <td>$1/3D < Y \leq D$</td> <td>$\leq 1/8$ 玻璃邊長 $\leq 1/8$ The side length of the glass</td> <td>允收 Acceptance</td> </tr> <tr> <td>$> D$</td> <td>-- --</td> <td>拒收 Reject</td> </tr> </tbody> </table>	Y	X	判定 Determination	$\leq 1/3D$	-- --	允收 Acceptance	$1/3D < Y \leq D$	$\leq 1/8$ 玻璃邊長 $\leq 1/8$ The side length of the glass	允收 Acceptance	$> D$	-- --	拒收 Reject	C	外觀 Appearance	次要 Minor AQL0.65%
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21	尺寸量測 Size Measurement	未依圖面上標示 拒收 No correspond to the indication on the drawing. Reject		ALL	外觀 Appearance	主要 Major AQL 0.4%												
22	其他 Other	如發現有上述未定義之不良則與客端簽訂限度樣 If there is another undefined defective situation. It will be listed as others. The inspection standard is according to the golden sample.		ALL	電訊 Electronics 外觀 Appearance	次要 Minor AQL0.65%												