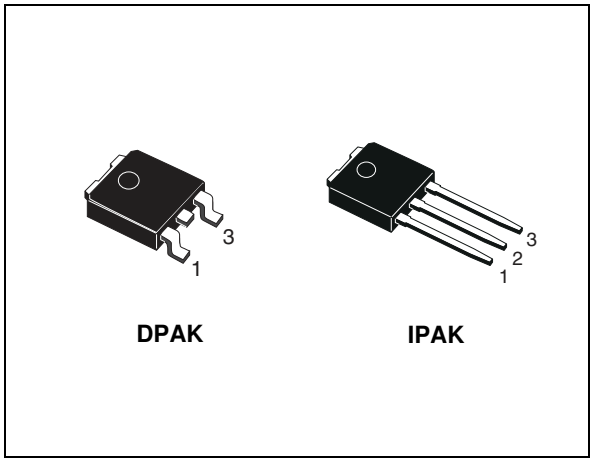
STD65N3LLH5
STU65N3LLH5

N-channel 30 V, 0.0061 Ω, 65 A, DPAK, IPAK STripFET™ V Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STD65N3LLH5	30 V	0.0069 Ω	65 A
STU65N3LLH5	30 V	0.0073 Ω	65 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



Application

Switching applications

Description

This STripFET™V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit.

Figure 1. Internal schematic diagram

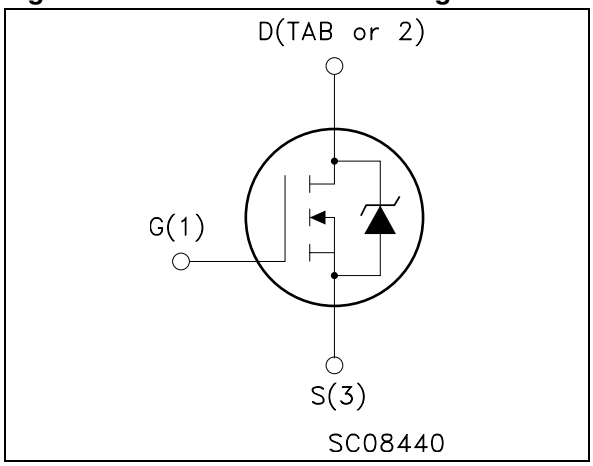


Table 1. Device summary

Order code	Marking	Package	Packaging
STD65N3LLH5	65N3LLH5	DPAK	Tape and reel
STU65N3LLH5	65N3LLH5	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	30	V
V_{GS}	Gate-source voltage	± 22	V
I_D	Drain current (continuous) at T_C = 25 °C	65	A
I_D	Drain current (continuous) at T_C = 100 °C	46	A
I_{DM} (1)	Drain current (pulsed)	260	A
P_{TOT}	Total dissipation at T_C = 25 °C	50	W
	Derating factor	0.3	W/°C
E_{AS} (2)	Single pulse avalanche energy	TBD	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area.
2. Starting Tj = 25 °C, Id = 32.5 A, Vdd = 12 V.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	3	°C/W
Rthj-amb	Thermal resistance junction-case max	100	°C/W
T_j	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 30 V V_{DS} = 30 V,Tc = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	1.8	3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 32.5 A SMD version		0.0061	0.0069	Ω
		V_{GS}= 10 V, I_D= 32.5 A		0.0065	0.0073	Ω
		V_{GS}= 4.5 V, I_D= 32.5 A SMD version		0.0084	0.0093	Ω
		V_{GS}= 4.5 V, I_D= 32.5 A		0.0088	0.0097	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	1290 240 32	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 65 A V_{GS} =4.5 V *(Figure 14)*	-	8 3.6 3.4	-	nC nC nC
R_g	Intrinsic gate resistance	f=1 MHz Gate DC Bias=0 test signal level = 20 mV open drain		1.7		Ω

Table 6. Switching on/off (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=10 V, I_D= 65 A, R_G=4.7 Ω, V_{GS}= 10 V *(Figure 13 and Figure 18)*	-	8.6 11.2	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=10 V, I_D= 25 A, R_G=4.7 Ω, V_{GS}= 10 V *(Figure 13 and Figure 18)*	-	32.4 6	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)(1)		-		65 260	A A
V_{SD}	Forward on voltage	I_{SD}=32.5 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=32.5 A, di/dt =100 A/µs, V_{DD}=20 V, *(Figure 15)*	-	22 15 1.4		ns nC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

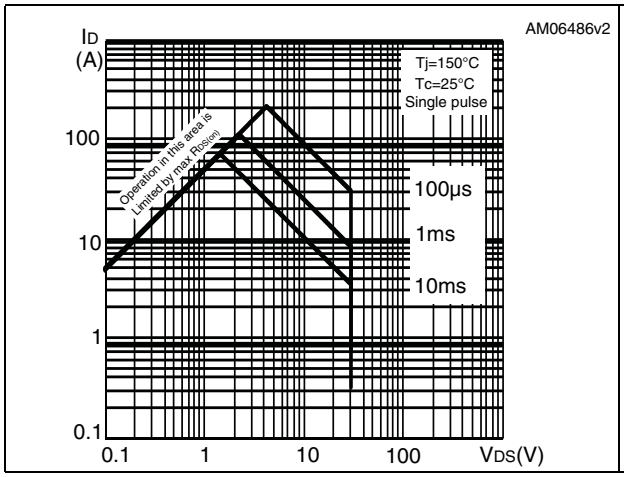


Figure 3. Thermal impedance

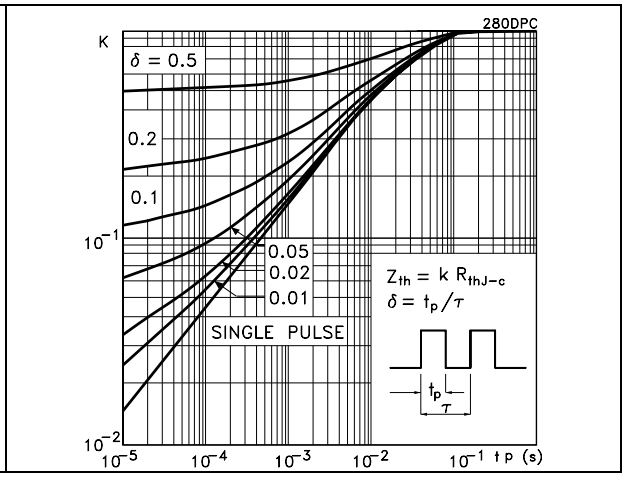


Figure 4. Output characteristics

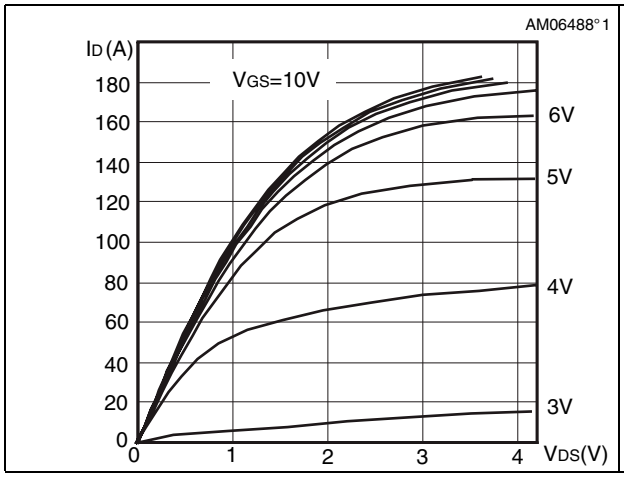


Figure 5. Transfer characteristics

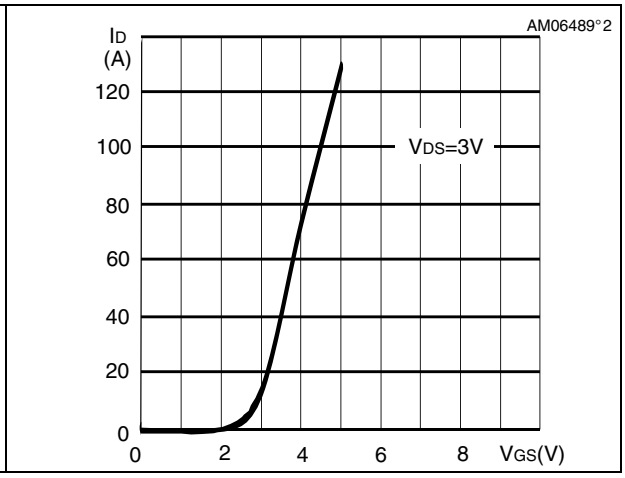


Figure 6. Normalized B_{VDSS} vs temperature

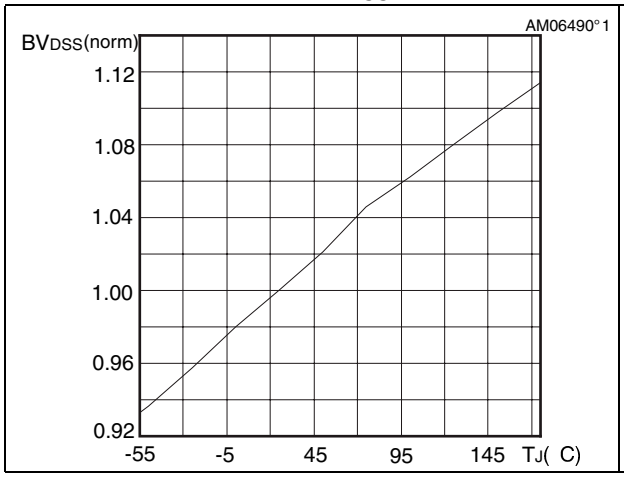


Figure 7. Static drain-source on resistance

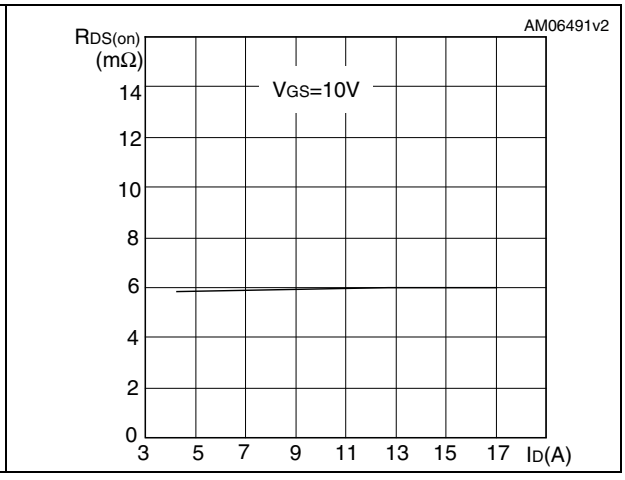


Figure 8. Gate charge vs gate-source voltage

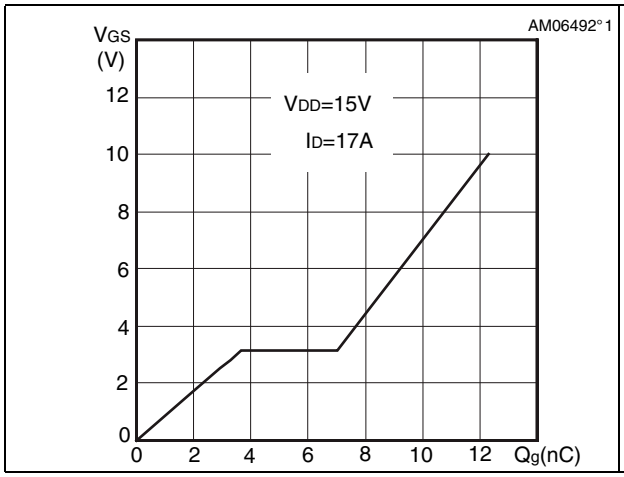


Figure 9. Capacitance variations

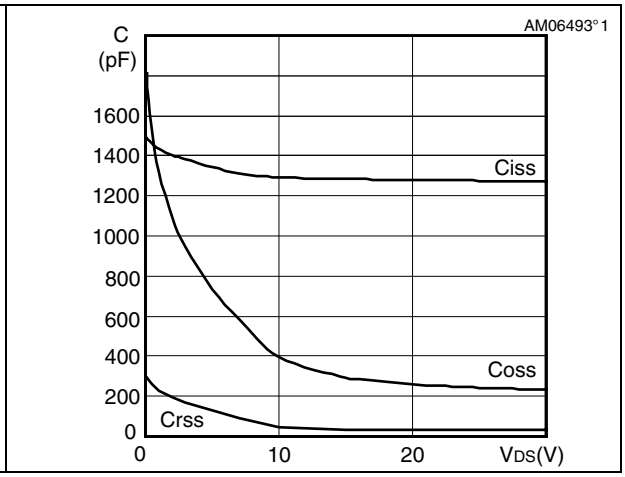


Figure 10. Normalized gate threshold voltage vs temperature

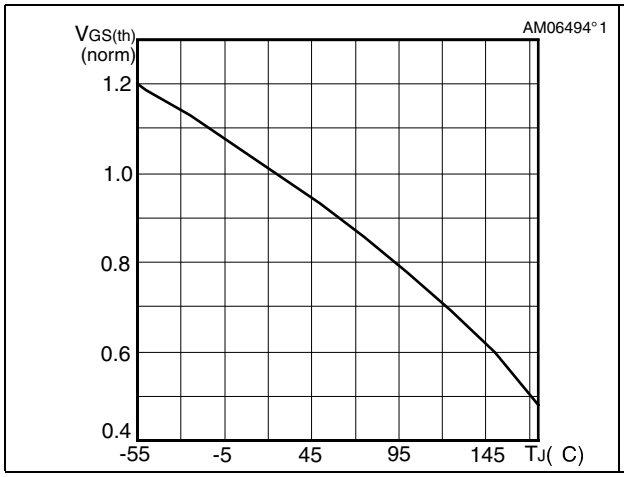


Figure 11. Normalized on resistance vs temperature

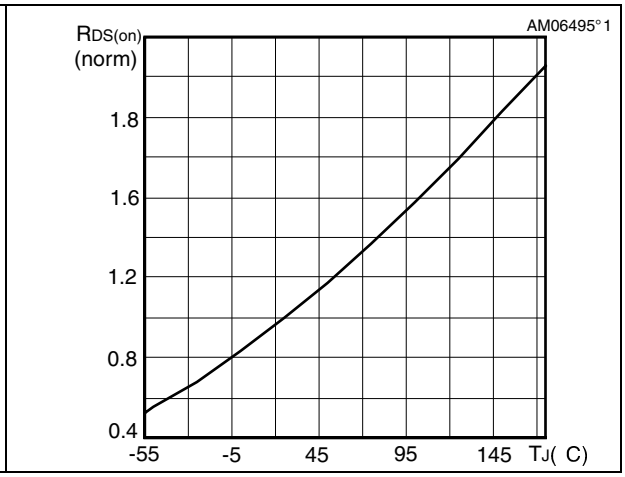
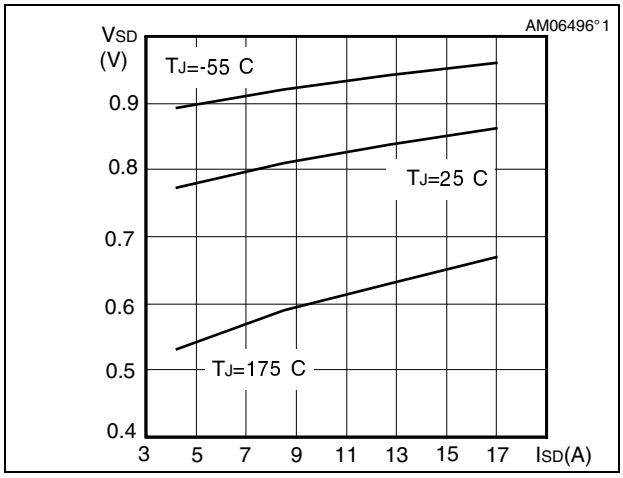


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

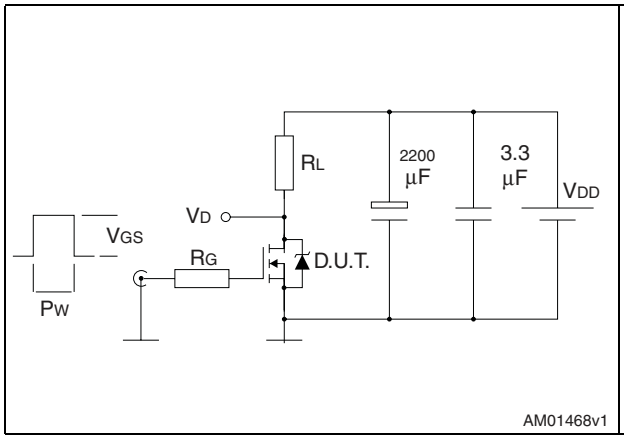


Figure 14. Gate charge test circuit

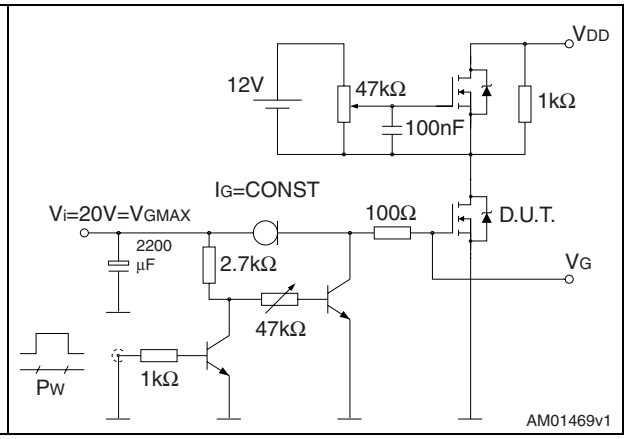


Figure 15. Test circuit for inductive load switching and diode recovery times

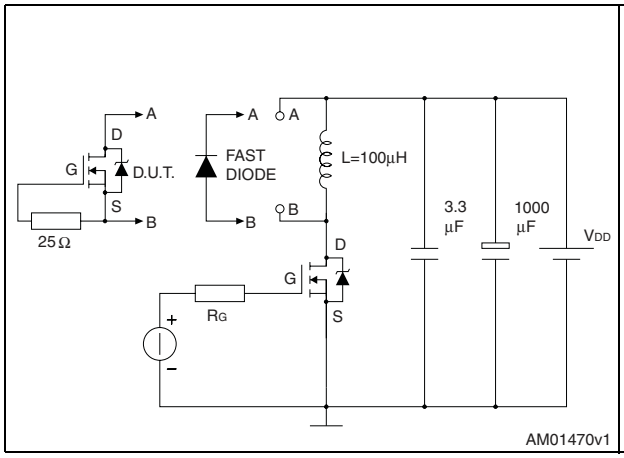


Figure 16. Unclamped inductive load test circuit

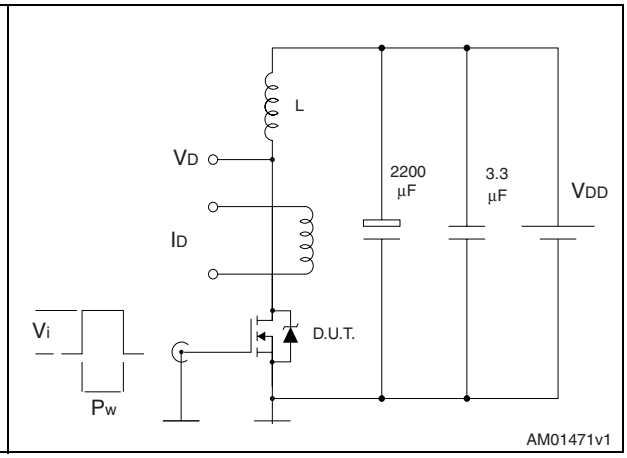


Figure 17. Unclamped inductive waveform

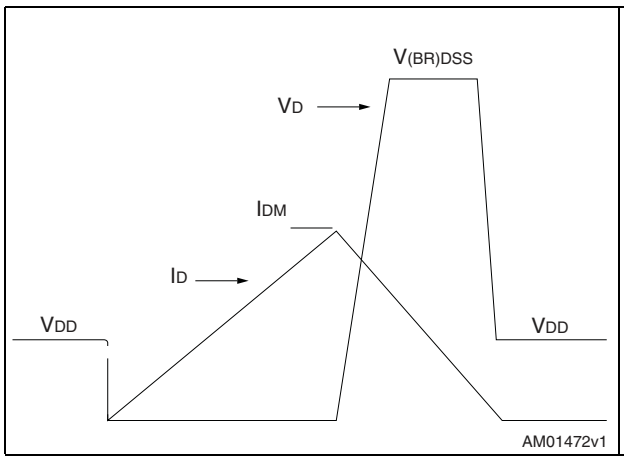
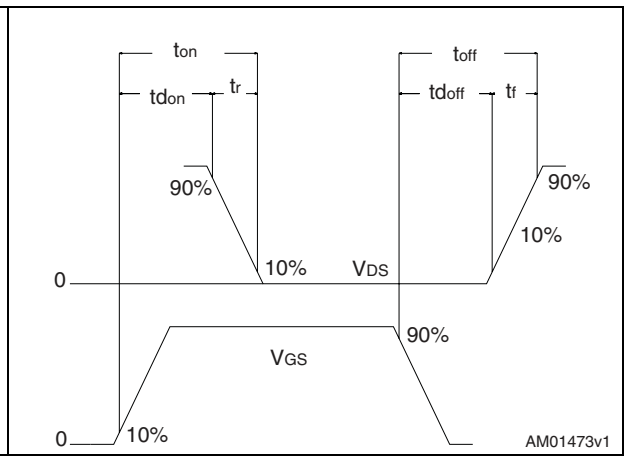


Figure 18. Switching time waveform



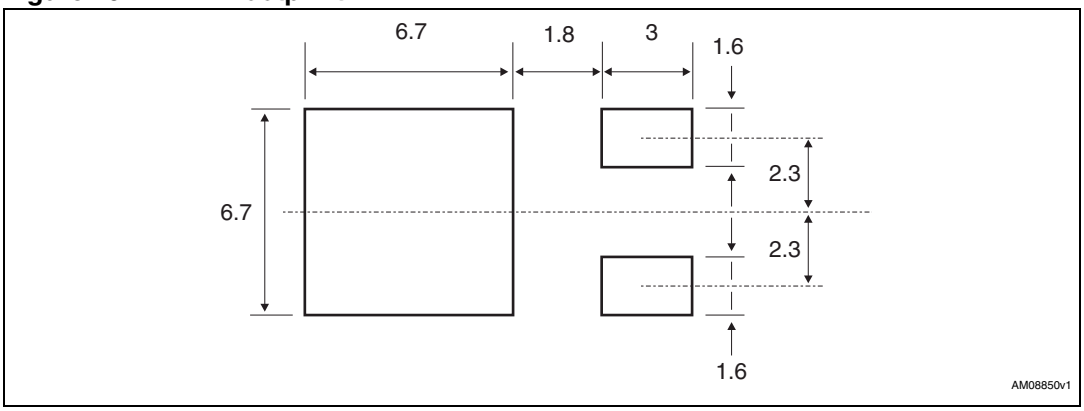
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 19. DPAK footprint[a]



a. All dimension are in millimeters

Figure 20. DPAK (TO-252) drawing

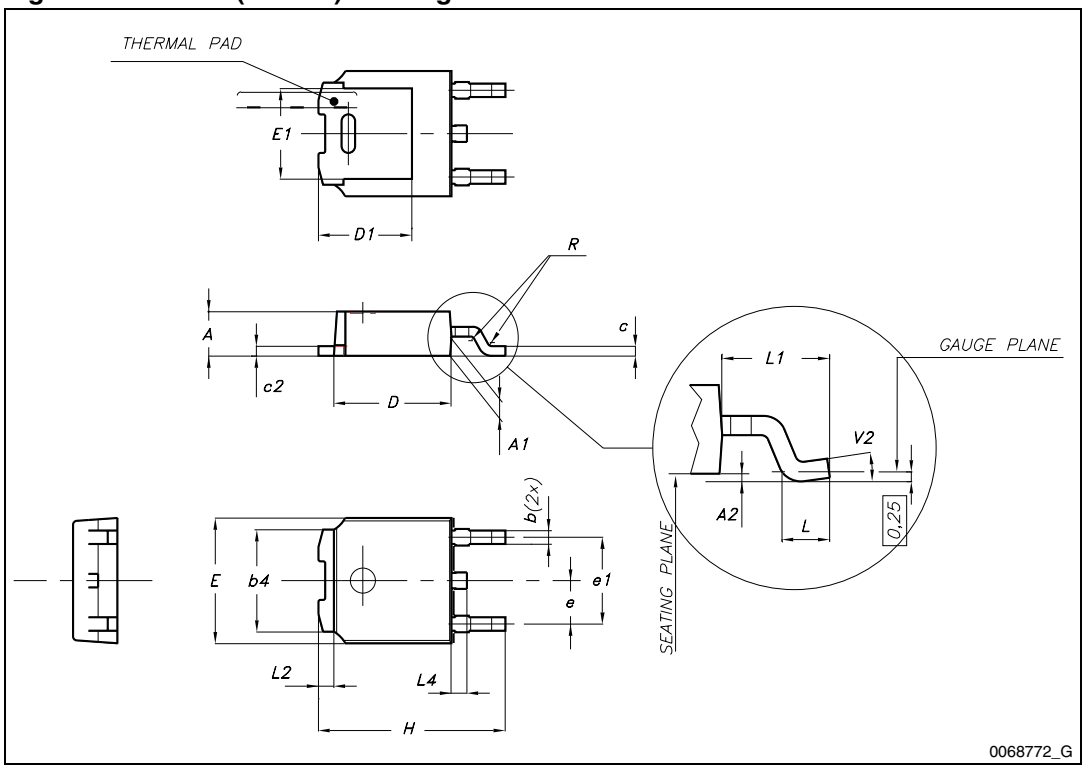
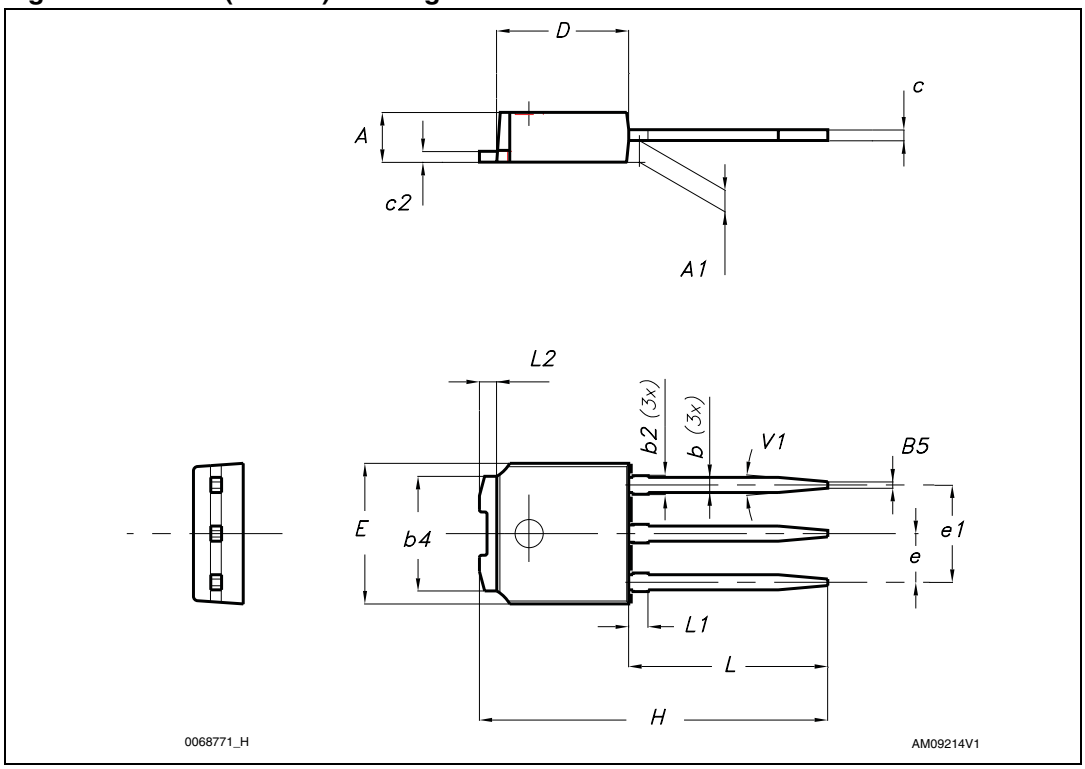


Table 9. IPAK (TO-251) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10^{o}	

Figure 21. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape for DPAK (TO-252)

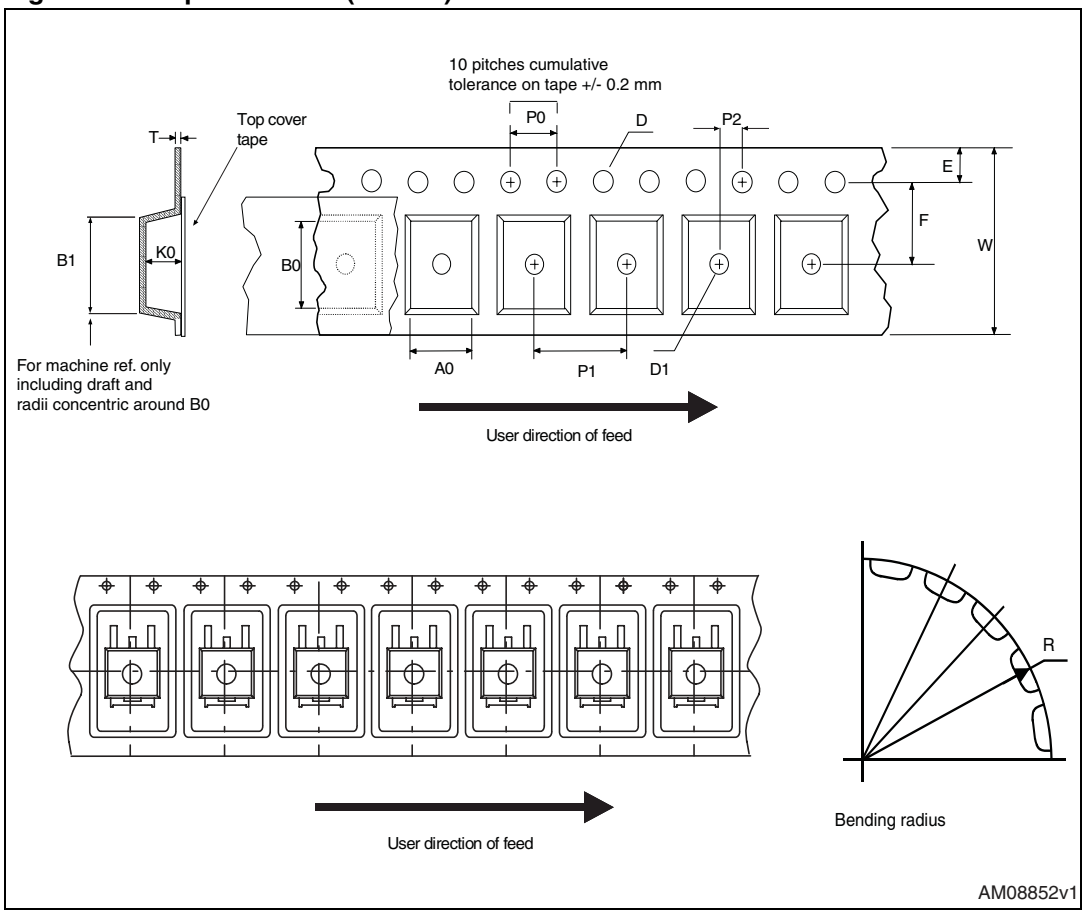
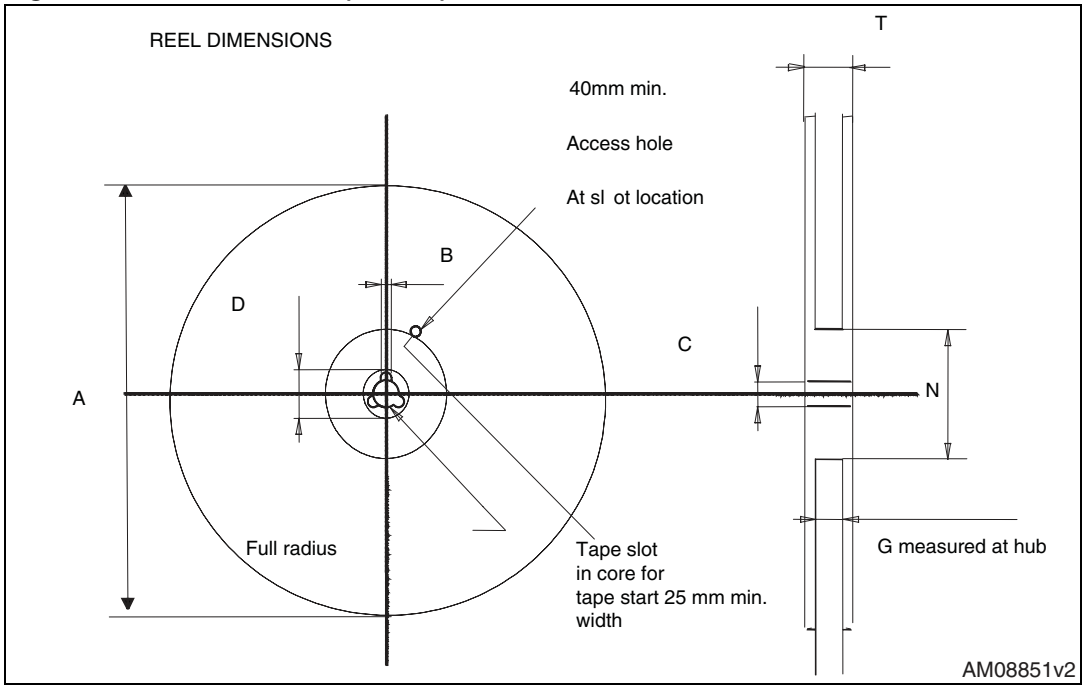


Figure 23. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-May-2011	1	First release.