EVALUATION KIT AVAILABLE

MAXIM

Dual, High-Efficiency, Step-Down Controller with Accurate Current Limit

MAX1845

General Description

The MAX1845 is a dual PWM controller configured for step-down (buck) topologies that provides high efficiency, excellent transient response, and high DC output accuracy necessary for stepping down high-voltage batteries to generate low-voltage chipset and RAM power supplies in notebook computers. The CS_ inputs can be used with low-side sense resistors to provide accurate current limits or can be connected to LX_, using low-side MOSFETs as current-sense elements.

The on-demand PWM controllers are free running, constant on-time with input feed-forward. This configuration provides ultra-fast transient response, wide input-output differential range, low supply current, and tight load-regulation characteristics. The MAX1845 is simple and easy to compensate.

Single-stage buck conversion allows the MAX1845 to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery at a higher switching frequency) allows the minimum possible physical size.

The MAX1845 is intended for generating chipset, DRAM, CPU I/O, or other low-voltage supplies down to 1V. For a single-output version, refer to the MAX1844 data sheet. The MAX1845 is available in 28-pin QSOP and 36-pin thin QFN packages.

Applications

Notebook Computers

CPU Core Supplies

Chipset/RAM Supply as Low as 1V

1.8V and 2.5V I/O Supplies

Pin Configurations appear at end of data sheet.

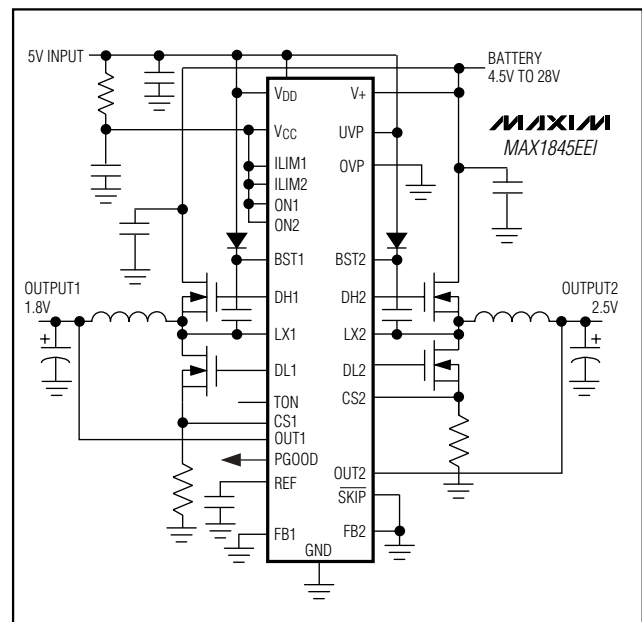*Quick-PWM and Dual Mode are trademarks of Maxim Integrated Products.*

Features

♦ **Ultra-High Efficiency**

♦ **Accurate Current-Limit Option**

♦ **Quick-PWM™ with 100ns Load-Step Response**

♦ **1% V_{OUT} Accuracy over Line and Load**

♦ **Dual Mode™ Fixed 1.8V/1.5V/Adj or 2.5V/Adj Outputs**

♦ **Adjustable 1V to 5.5V Output Range**

♦ **2V to 28V Battery Input Range**

♦ **200/300/420/540kHz Nominal Switching Frequency**

♦ **Adjustable Overvoltage Protection**

♦ **1.7ms Digital Soft-Start**

♦ **Drives Large Synchronous-Rectifier FETs**

♦ **Power-Good Window Comparator**

♦ **2V ±1% Reference Output**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1845EEI	-40°C to +85°C	28 QSOP
MAX1845ETX	-40°C to +85°C	36 Thin QFN 6mm × 6mm

Minimal Operating Circuit

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MAX1845EEI

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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual, High-Efficiency, Step-Down Controller with Accurate Current Limit

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ to AGND..-0.3 to +30V
VCC to AGND..-0.3V to +6V
VDD to PGND..-0.3V to +6V
AGND to PGND...-0.3V to +0.3V
PGOOD, OUT_ to AGND..-0.3V to +6V
OVP, UVP, ILIM_, FB_, REF,
  $\overline{SKIP}$, TON, ON_ to AGND.....................-0.3V to (VCC + 0.3V)
DL_ to PGND.......................................-0.3V to (VDD + 0.3V)
BST_ to AGND..-0.3V to +36V
CS_ to AGND..-6V to +30V
DH1 to LX1 ....-0.3V to (VBST1 + 0.3V)

LX_ to BST_ ....-6V to +0.3V
DH2 to LX2 ....-0.3V to (VBST2 + 0.3V)
REF Short Circuit to GND ....Continuous
Continuous Power Dissipation (TA = +70°C)
  28-Pin QSOP (derate 10.8mW/°C above +70°C)........860mW
  36-Pin 6mm × 6mm Thin QFN
  (derate 26.3mW/°C above +70°C)...........................2105mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: For the MAX1845EEI, AGND and PGND refer to a single pin designated GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, VDD = VCC = 5V, $\overline{SKIP}$ = AGND, V+ = 15V, **TA = 0°C to +85°C**, typical values are at +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLERS							
Input Voltage Range	V+	Battery voltage, V+		2		28	V
	VCC/VDD	VCC, VDD		4.5		5.5	
DC Output Voltage OUT1 (Note 2)	VOUT1	V+ = 2V to 28V, ILOAD = 0 to 8A, $\overline{SKIP}$ = VCC, +25°C to +85°C	FB1 to AGND	1.782	1.8	1.818	V
			FB1 to VCC	1.485	1.5	1.515	
			FB1 to OUT1	0.99	1	1.01	
		V+ = 2V to 28V, ILOAD = 0 to 8A, $\overline{SKIP}$ = VCC, 0°C to +85°C	FB1 to AGND	1.773	1.8	1.827	
			FB1 to VCC	1.477	1.5	1.523	
			FB1 to OUT1	0.985	1	1.015	
DC Output Voltage OUT2 (Note 2)	VOUT2	V+ = 4.5V to 28V, ILOAD = 0 to 4A, $\overline{SKIP}$ = VCC, +25°C to +85°C	FB2 to AGND	2.475	2.5	2.525	V
			FB2 to OUT2	0.99	1	1.01	
		V+ = 4.5V to 28V, ILOAD = 0 to 4A, $\overline{SKIP}$ = VCC, 0°C to +85°C	FB2 to AGND	2.463	2.5	2.537	
			FB2 to OUT2	0.985	1	1.015	
Output Voltage Adjust Range		OUT1, OUT2		1		5.5	V
Dual-Mode Threshold, Low		OVP, FB_		0.05	0.1	0.15	V
Dual-Mode Threshold, High		OVP, ILIM_		VCC - 1.5		VCC - 0.4	V
		FB1		1.9	2.0	2.1	
OUT_ Input Resistance	ROUT1	VOUT1 = 1.5V		75			kΩ
	ROUT2	VOUT2 = 2.5V		100			
FB_ Input Bias Current	IFB			-0.1		0.1	µA
Soft-Start Ramp Time		Zero to full ILIM			1700		µs

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{DD} = V_{CC} = 5V$, $\overline{SKIP}$ = AGND, V+ = 15V, **T_A = 0°C to +85°C**, typical values are at +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time, Side 1 (Note 3)	t_{ON1}	V+ = 24V, V_{OUT1} = 2V	TON = AGND	120	137	153	ns
			TON = REF	153	174	195	
			TON = float	222	247	272	
			TON = V_{CC}	316	353	390	
On-Time, Side 2 (Note 3)	t_{ON2}	V+ = 24V, V_{OUT2} = 2V	TON = AGND	160	182	204	ns
			TON = REF	205	234	263	
			TON = float	301	336	371	
			TON = V_{CC}	432	483	534	
On-Time Tracking (Note 3)		On-time 2 with respect to on-time 1	TON = AGND	125	135	145	%
			TON = REF	125	135	145	
			TON = float	125	135	145	
			TON = V_{CC}	125	135	145	
Minimum Off-Time (Note 3)	t_{OFF}				400	500	ns
Quiescent Supply Current (V_{CC})	I_{CC}	FB_ forced above the regulation point			1100	1500	µA
Quiescent Supply Current (V_{DD})	I_{DD}	FB_ forced above the regulation point			<1	5	µA
Quiescent Supply Current (V+)	I+	Measured at V+			25	70	µA
Shutdown Supply Current (V_{CC})		ON1 = ON2 = AGND, OVP = V_{CC} or AGND			<1	5	µA
		ON1 = ON2 = AGND, V_{OVP} = 1.8V			1	5	
Shutdown Supply Current (V_{DD})		ON1 = ON2 = AGND			<1	5	µA
Shutdown Supply Current (V+)		ON1 = ON2 = AGND, measured at V+, V_{CC} = AGND or 5V			<1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no external REF load		1.98	2	2.02	V
Reference Load Regulation		I_{REF} = 0 to 50µA				0.01	V
REF Sink Current		REF in regulation		10			µA
REF Fault Lockout Voltage		Falling edge, hysteresis = 40mV			1.6		V
Overvoltage Trip Threshold (Fixed-Threshold Mode)		OVP = AGND, with respect to error-comparator trip threshold		112	114	117	%
Overvoltage Comparator Offset (Adjustable-Threshold Mode)		1V < V_{OVP} < 1.8V, external feedback, measured at FB_ with respect to V_{OVP}		-28	0	28	mV
		1V < V_{OVP} < 1.8V, internal feedback, measured at OUT_ with respect to OUT_ regulation point		-3.5	0	+3.5	%
OVP Input Leakage Current		1V < V_{OVP} < 1.8V		-100	<1	100	nA
Overvoltage Fault Propagation Delay		FB_ forced 2% above trip threshold			1.5		µs
Output Undervoltage Threshold		UVP = V_{CC}, with respect to error-comparator trip threshold		65	70	75	%
Output Undervoltage Protection Blanking Time		From ON_ signal going high		10		30	ms

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{DD} = V_{CC} = 5V$, $\overline{SKIP}$ = AGND, V+ = 15V, **T_A = 0°C to +85°C**, typical values are at +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Limit Threshold (Fixed)		AGND - $V_{CS\_}$, ILIM_ = V_{CC}		40	50	60	mV
Current-Limit Threshold (Adjustable)		AGND - $V_{CS\_}$, ILIM_ = 0.5V		40	50	60	mV
		AGND - $V_{CS\_}$, ILIM_ = 1V		85	100	115	
ILIM_ Adjustment Range	$V_{ILIM\_}$			0.3		2.5	V
Negative Current-Limit Threshold (Fixed)		$V_{CS\_}$ - AGND, ILIM_ = V_{CC}, T_A = +25°C		-75	-60	-45	mV
Thermal Shutdown Threshold		Hysteresis = 15°C			160		°C
V_{CC} Undervoltage Lockout Threshold		Rising edge, hysteresis = 20mV, PWMs disabled below this level		4.05		4.4	V
DH Gate-Driver On-Resistance (Note 4)		BST - LX forced to 5V	MAX1845EEI		1.5	5	Ω
			MAX1845ETX		1.5	6	Ω
DL Gate-Driver On-Resistance (Note 4)		DL, high state	MAX1845EEI		1.5	5	Ω
			MAX1845ETX		1.5	6	Ω
DL Gate-Driver On-Resistance (Note 4)		DL, low state	MAX1845EEI		0.5	1.7	Ω
			MAX1845ETX		0.5	2.7	Ω
DH_ Gate Driver Source/Sink Current		$V_{DH\_}$ = 2.5V, $V_{BST\_}$ = $V_{LX\_}$ = 5V			1		A
DL_ Gate Driver Sink Current		$V_{DL\_}$ = 2.5V			3		A
DL_ Gate Driver Source Current		$V_{DL\_}$ = 2.5V			1		A
Logic Input High Voltage	V_{IH}	ON_, $\overline{SKIP}$		2.4			V
		UVP		V_{CC} - 0.4			
Logic Input Low Voltage	V_{IL}	ON_, $\overline{SKIP}$				0.8	V
		UVP				0.05	
TON Input Logic level		V_{CC} level		V_{CC} - 0.4			V
		Float level		3.15		3.85	
		REF level		1.65		2.35	
		AGND level				0.5	
Logic Input Current		TON (AGND or V_{CC})		-3		3	µA
Logic Input Current		ON_, $\overline{SKIP}$, UVP		-1		1	µA
PGOOD Trip Threshold (Lower)		With respect to error-comparator trip threshold, falling edge		-12.5	-10	-7.5	%
PGOOD Trip Threshold (Upper)		With respect to error-comparator trip threshold, rising edge		+7.5	+10	+12.5	%
PGOOD Propagation Delay		Falling edge, FB_ forced 2% below PGOOD trip threshold			1.5		µs
PGOOD Output Low Voltage		I_{SINK} = 1mA				0.4	V
PGOOD Leakage Current		High state, forced to 5.5V				1	µA

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ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = AGND, V+ = 15V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLERS							
Input Voltage Range	V+	Battery voltage, V+		2		28	V
	V_{CC}/V_{DD}	V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage, OUT1 (Note 2)	V_{OUT1}	V+ = 2V to 28V, $\overline{SKIP}$ = V_{CC}, I_{LOAD} = 0 to 10A	FB1 to AGND	1.773		1.827	V
			FB1 to V_{CC}	1.477		1.523	
			FB1 to OUT1	0.985		1.015	
DC Output Voltage, OUT2 (Note 2)	V_{OUT2}	V+ = 2V to 28V, $\overline{SKIP}$ = V_{CC}, I_{LOAD} = 0 to 10A	FB2 to AGND	2.463		2.537	V
			FB2 to OUT2	0.985		1.015	
Output Voltage Adjust Range		OUT1, OUT2		1		5.5	V
Dual-Mode Threshold (Low)		OVP, FB_		0.05		0.15	V
Dual-Mode Threshold (High)		OVP, ILIM_		V_{CC} - 1.5		V_{CC} - 0.4	V
		FB_		1.9		2.1	
OUT_ Input Resistance	R_{OUT1}	V_{OUT1} = 1.5V		75			kΩ
	R_{OUT2}	V_{OUT2} = 2.5V		100			
FB_ Input Bias Current	I_{FB}			-0.1		0.1	µA
On-Time, Side 1 (Note 3)	t_{ON1}	V+ = 24V, V_{OUT1} = 2V	TON = AGND	120		153	ns
			TON = REF	153		195	
			TON = float	217		272	
			TON = V_{CC}	308		390	
On-Time, Side 2 (Note 3)	t_{ON2}	V+ = 24V, V_{OUT2} = 2V	TON = AGND	160		204	ns
			TON = REF	205		263	
			TON = float	295		371	
			TON = V_{CC}	422		534	
On-Time Tracking (Note 3)		On-time 2, with respect to on-time 1	TON = AGND	125		145	%
			TON = REF	125		145	
			TON = float	125		145	
			TON = V_{CC}	125		145	
Minimum Off-Time (Note 3)	t_{OFF}					500	ns
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above the regulation point				1500	µA
Quiescent Supply Current (V_{DD})	I_{DD}	FB forced above the regulation point				5	µA
Quiescent Supply Current (V+)	I+	Measured at V+				70	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no external REF load		1.98		2.02	V
Reference Load Regulation		I_{REF} = 0 to 50uA				0.01	V
Overvoltage Trip Threshold (Fixed-Threshold Mode)		OVP = GND, with respect to FB_ regulation point, no load		112		117	%
Output Undervoltage Threshold		UVP = V_{CC}, with respect to FB_ regulation point, no load		65		75	%
Current-Limit Threshold (Fixed)		AGND - $V_{CS\_}$, ILIM_ = V_{CC}		35		65	mV

Dual, High-Efficiency, Step-Down Controller with Accurate Current Limit

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = AGND, V+ = 15V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Threshold (Adjustable)		AGND - $V_{CS\_}$, ILIM_ = 0.5V	35		65	mV
		AGND - $V_{CS\_}$, ILIM_ = 1V	80		120	
V_{CC} Undervoltage Lockout Threshold		Rising edge, hysteresis = 20mV, PWMs disabled below this level	4.05		4.4	V
Logic Input High Voltage	V_{IH}	ON_, $\overline{SKIP}$	2.4			V
		UVP	V_{CC} - 0.4			
Logic Input Low Voltage	V_{IL}	ON_, $\overline{SKIP}$			0.8	V
		UVP			0.05	
Logic Input Current		TON (AGND or V_{CC})	-3		3	µA
		ON_, $\overline{SKIP}$, UVP	-1		1	

Note 2: When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the error comparator threshold by 50% of the output voltage ripple. In discontinuous conduction ($\overline{SKIP}$ = AGND, light load), the output voltage will have a DC regulation higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Note 3: On-time and off-time specifications are measured from 50% point to 50% point at DH_ with LX_ = GND, BST_ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 4: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the QFN package. The MAX1845EEI and MAX1845ETX contain the same die, and the QFN package imposes no additional resistance in-circuit.

Note 5: Specifications to -40°C are guaranteed by design, not production tested.

_____*Typical Operating Characteristics*

(Circuit of Figure 1, components from Table 1, V_{IN} = 15V, $\overline{SKIP}$ = GND, TON = unconnected, T_A = +25°C, unless otherwise noted.)
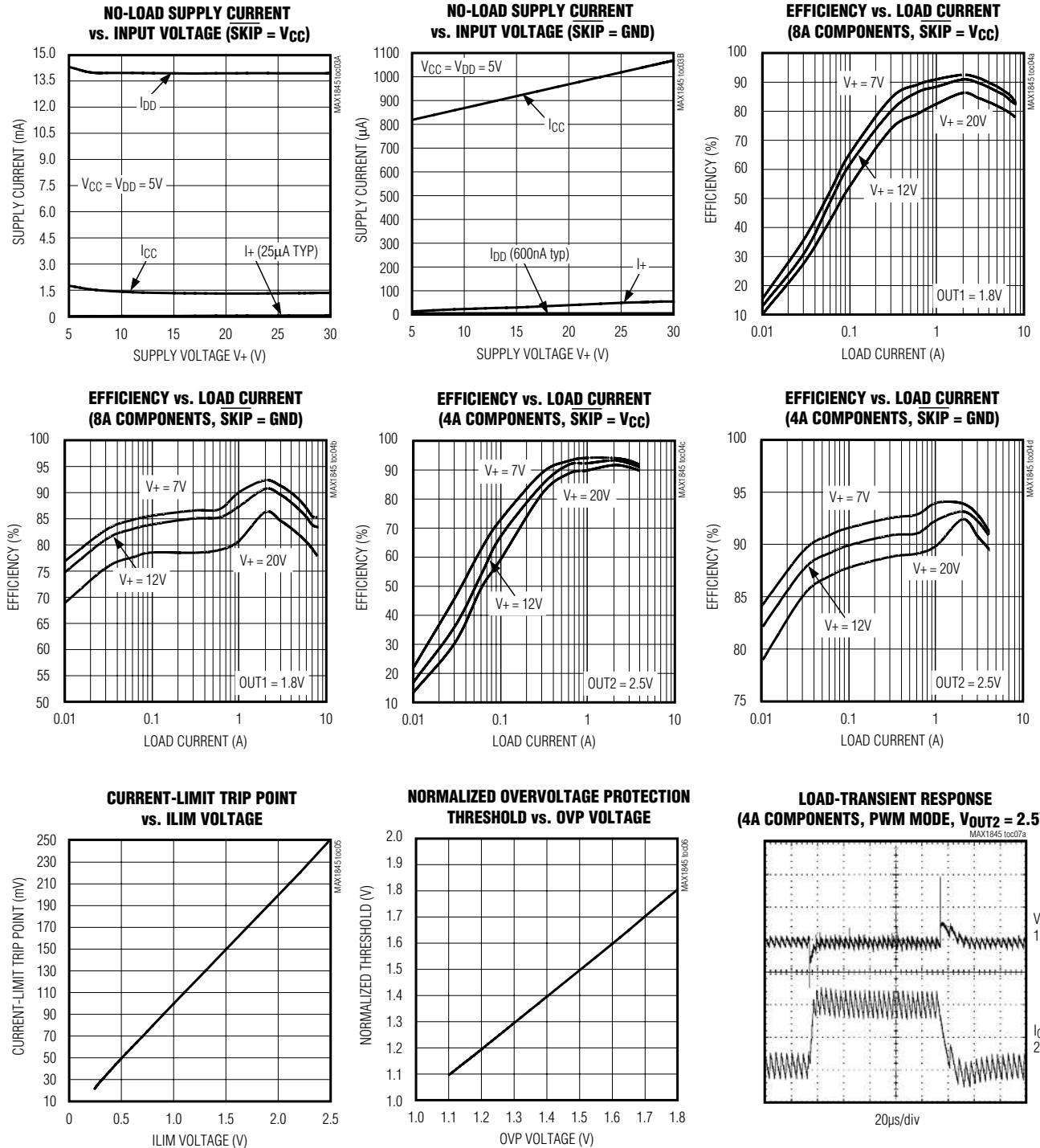

FREQUENCY vs. LOAD CURRENT


FREQUENCY vs. INPUT VOLTAGE
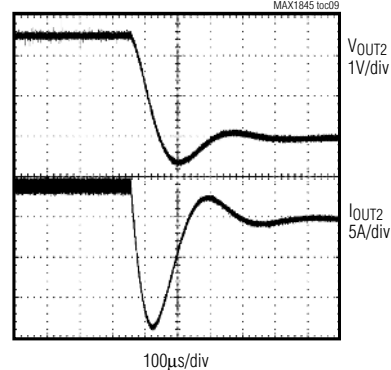(TON = FLOAT, $\overline{SKIP}$ = V_{CC})

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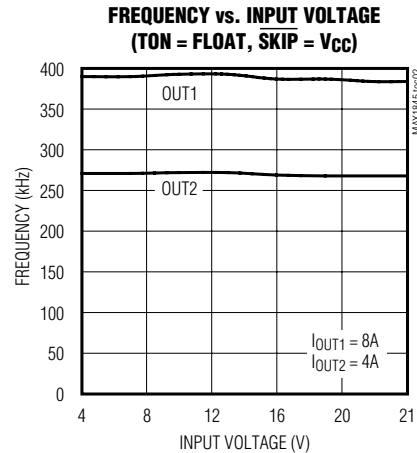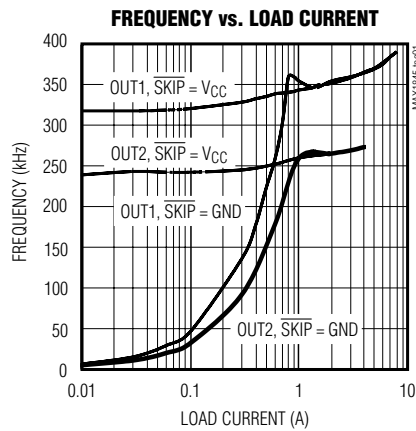
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Typical Operating Characteristics (continued)

(Circuit of Figure 1, components from Table 1, V_{IN} = 15V, $\overline{SKIP}$ = GND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE ($\overline{SKIP}$ = V_{CC})

NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE ($\overline{SKIP}$ = GND)

EFFICIENCY vs. LOAD CURRENT (8A COMPONENTS, $\overline{SKIP}$ = V_{CC})

EFFICIENCY vs. LOAD CURRENT (8A COMPONENTS, $\overline{SKIP}$ = GND)

EFFICIENCY vs. LOAD CURRENT (4A COMPONENTS, $\overline{SKIP}$ = V_{CC})

EFFICIENCY vs. LOAD CURRENT (4A COMPONENTS, $\overline{SKIP}$ = GND)

CURRENT-LIMIT TRIP POINT vs. ILIM VOLTAGE

NORMALIZED OVERVOLTAGE PROTECTION THRESHOLD vs. OVP VOLTAGE

LOAD-TRANSIENT RESPONSE (4A COMPONENTS, PWM MODE, V_{OUT2} = 2.5V)

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Dual, High-Efficiency, Step-Down
Controller with Accurate Current Limit

_____ ***Typical Operating Characteristics (continued)***

(Circuit of Figure 1, components from Table 1, V_{IN} = 15V, $\overline{SKIP}$ = GND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE
(8A COMPONENTS, PWM MODE, V_{OUT1} = 1.8V)
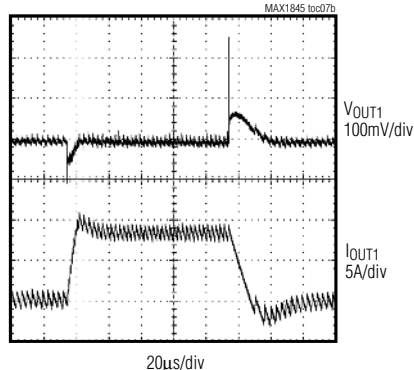
STARTUP WAVEFORM
(4A COMPONENTS, $\overline{SKIP}$ = GND, V_{OUT2} = 2.5V)
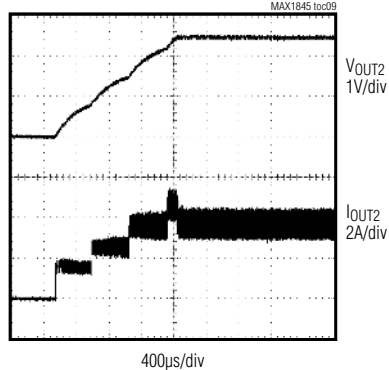
SHUTDOWN WAVEFORM
(4A COMPONENTS, $\overline{SKIP}$ = GND, V_{OUT2} = 2.5V)

_____ ***Pin Description***

PIN		NAME	FUNCTION		
QSOP	**QFN**				
1	32	OUT1	Output Voltage Connection for the OUT1 PWM. Connect directly to the junction of the external inductor and output filter capacitors. OUT1 senses the output voltage to determine the on-time and also serves as the feedback input in fixed-output modes.		
2	33	FB1	Feedback Input for OUT1. Connect to GND for 1.8V fixed output or to V_{CC} for 1.5V fixed output, or connect to a resistor-divider network from OUT1 for an adjustable output between 1V and 5.5V.		
3	34	ILIM1	Current-Limit Threshold Adjustment for OUT1. The current-limit threshold at CS1 is 0.1 times the voltage at ILIM1. Connect a resistor-divider network from REF to set the current-limit threshold between 25mV and 250mV (with 0.25V to 2.5V at ILIM). Connect to V_{CC} to assert 50mV default current-limit threshold.		
4	35	V+	Battery Voltage-Sense Connection. Connect to input power source. V+ is only used to adjust the DH_ on-time for pseudofixed-frequency operation.		
5	1	TON	On-Time Selection Control Input. This four-level input pin sets the DH_ on-time to determine the operating frequency.		
			TON	**FREQUENCY (OUT1) (kHz)**	**FREQUENCY (OUT2) (kHz)**
			AGND	620	460
			REF	485	355
			Open	345	255
			V_{CC}	235	170
6	2	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect to V_{CC} for low-noise forced-PWM mode. Connect to AGND to enable pulse-skipping operation.		

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PIN		NAME	FUNCTION
QSOP	QFN		
7	3	PGOOD	Power-Good Open-Drain Output. PGOOD is low when either output voltage is off or is more than 10% above or below the normal regulation point.
8	4	OVP	Overvoltage Protection Threshold. An overvoltage fault occurs if the voltage on FB1 or FB2 is greater than the programmed overvoltage trip threshold. Adjustment range is 1V (100%) to 1.8V (180%). Connect OVP to GND to set the default overvoltage threshold of 114% of nominal. Connect to V_{CC} to disable OVP and clear the OVP latch.
9	5	UVP	Undervoltage Protection Threshold. An undervoltage fault occurs if the voltage on FB1 or FB2 is less than the undervoltage trip threshold (70% of nominal). Connect UVP to V_{CC} to enable undervoltage protection. Connect to GND to disable undervoltage protection and clear the UVP latch.
10	7	REF	+2.0V Reference Voltage Output. Bypass to GND with 0.22µF (min) capacitor. Can supply 50µA for external loads.
11	8	ON1	OUT1 ON/$\overline{\text{OFF}}$ Control Input. Connect to AGND to turn OUT1 off. Connect to V_{CC} to turn OUT1 on.
12	11	ON2	OUT2 ON/$\overline{\text{OFF}}$ Control Input. Connect to AGND to turn OUT2 off. Connect to V_{CC} to turn OUT2 on.
13	12	ILIM2	Current-Limit Threshold Adjustment for OUT2. The current-limit threshold at CS2 is 0.1 times the voltage at ILIM2. Connect a resistor-divider network from REF to set the current-limit threshold between 25mV and 250mV (with 0.25V to 2.5V at ILIM). Connect to V_{CC} to assert 50mV default current-limit threshold.
14	13	FB2	Feedback Input for OUT2. Connect to GND for 2.5V fixed output, or connect to a resistor-divider network from OUT2 for an adjustable output between 1V and 5.5V.
15	14	OUT2	Output Voltage Connection for the OUT2 PWM. Connect directly to the junction of the external inductor and output filter capacitors. OUT2 senses the output voltage to determine the on-time and also serves as the feedback input in fixed-output modes.
16	15	CS2	Current-Sense Input for OUT2. CS2 is the input to the current-limiting circuitry for valley current limiting. For lowest cost and highest efficiency, connect to LX2. For highest accuracy, use a sense resistor. See the _Current-Limit Circuit (ILIM_)_ section.
17	16	LX2	External Inductor Connection for OUT2. Connect to the switched side of the inductor. LX2 serves as the internal lower supply voltage rail for the DH2 high-side gate driver.
18	18	DH2	High-Side Gate Driver Output for OUT2. Swings from LX2 to BST2.
19	19	BST2	Boost Flying Capacitor Connection for OUT2. Connect to an external capacitor and diode according to the standard application circuit in Figure 1. See _MOSFET Gate Drivers (DH_, DL_)_ section.
20	20	DL2	Low-Side Gate-Driver Output for OUT2. DL2 swings from PGND to V_{DD}.
21	21	V_{DD}	Supply Input for the DL Gate Drivers. Connect to system supply voltage, +4.5V to +5.5V. Bypass to PGND with a low-ESR 4.7µF capacitor.
22	22	V_{CC}	Analog Supply Input. Connect to system supply voltage, +4.5V to +5.5V, with a 20Ω series resistor. Bypass to AGND with a 1µF capacitor.
23	—	GND	Ground. Combined analog and power ground. Serves as negative input for CS_ amplifiers.

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PIN QSOP	PIN QFN	NAME	FUNCTION
—	23	AGND	Analog Ground. Serves as negative input for CS_ amplifiers. Connect backside pad to AGND.
—	24	PGND	Power Ground
24	26	DL1	Low-Side Gate-Driver Output for OUT1. DL1 swings from PGND to V$_{DD}$.
25	27	BST1	Boost Flying Capacitor Connection for OUT1. Connect to an external capacitor and diode according to the standard application circuit in Figure 1. See the *MOSFET Gate Drivers (DH_, DL_)* section.
26	28	DH1	High-Side Gate Driver Output for OUT1. Swings from LX1 to BST1.
27	30	LX1	External Inductor Connection for OUT1. Connect to the switched side of the inductor. LX1 serves as the internal lower supply voltage rail for the DH1 high-side gate driver.
28	31	CS1	Current-Sense Input for OUT1. CS1 is the input to the current-limiting circuitry for valley current limiting. For lowest cost and highest efficiency, connect to LX1. For highest accuracy, use a sense resistor. See the *Current-Limit Circuit (ILIM_)* section.
—	6, 9, 10, 17, 25, 29, 36	N.C.	No Connection

Standard Application Circuit

The standard application circuit (Figure 1) generates a 1.8V and a 2.5V rail for general-purpose use in notebook computers.

See Table 1 for component selections. Table 2 lists component manufacturers.

Detailed Description

The MAX1845 buck controller is designed for low-voltage power supplies for notebook computers. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX1845 (Figure 2) is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

5V Bias Supply (V$_{CC}$ and V$_{DD}$)

The MAX1845 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615.

The power input and 5V bias inputs can be connected together if the input source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal (ON1, ON2) must be delayed until the battery voltage is present to ensure startup. The 5V bias supply must provide V$_{CC}$ and gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f(Q_{G1} + Q_{G2}) = 5mA \text{ to } 30mA \text{ (typ)}$$

where I$_{CC}$ is 1mA typical, f is the switching frequency, and Q$_{G1}$ and Q$_{G2}$ are the MOSFET data sheet total gate-charge specification limits at V$_{GS}$ = 5V.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time current-mode type with voltage feed-forward (Figure 3). This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-

time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out (Table 3).

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time for both controllers. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: First, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point

remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-times for side 1 are set 35% higher than the on-times for side 2. This is done to prevent audio-frequency "beating" between the two sides, which switch asynchronously for each side. The on-time is given by:

$$\text{On-Time} = K \,(V_{OUT} + 0.075V) \,/\, V_{IN}$$

where K is set by the TON pin-strap connection (Table 4), and 0.075V is an approximation to accommodate for the expected drop across the low-side MOSFET switch. One-shot timing error increases for the shorter on-time settings due to fixed propagation delays; it is approximately ±12.5% at higher frequencies and ±10% at lower frequencies. This translates to reduced switching-frequency accuracy at higher frequencies (Table 4). Switching frequency increases as a function of load current due to the increasing drop across the low-side MOSFET, which causes a faster inductor-current discharge ramp. The on-times guaranteed in the *Electrical Characteristics* tables are influenced by switching delays in the external high-side power MOSFET.
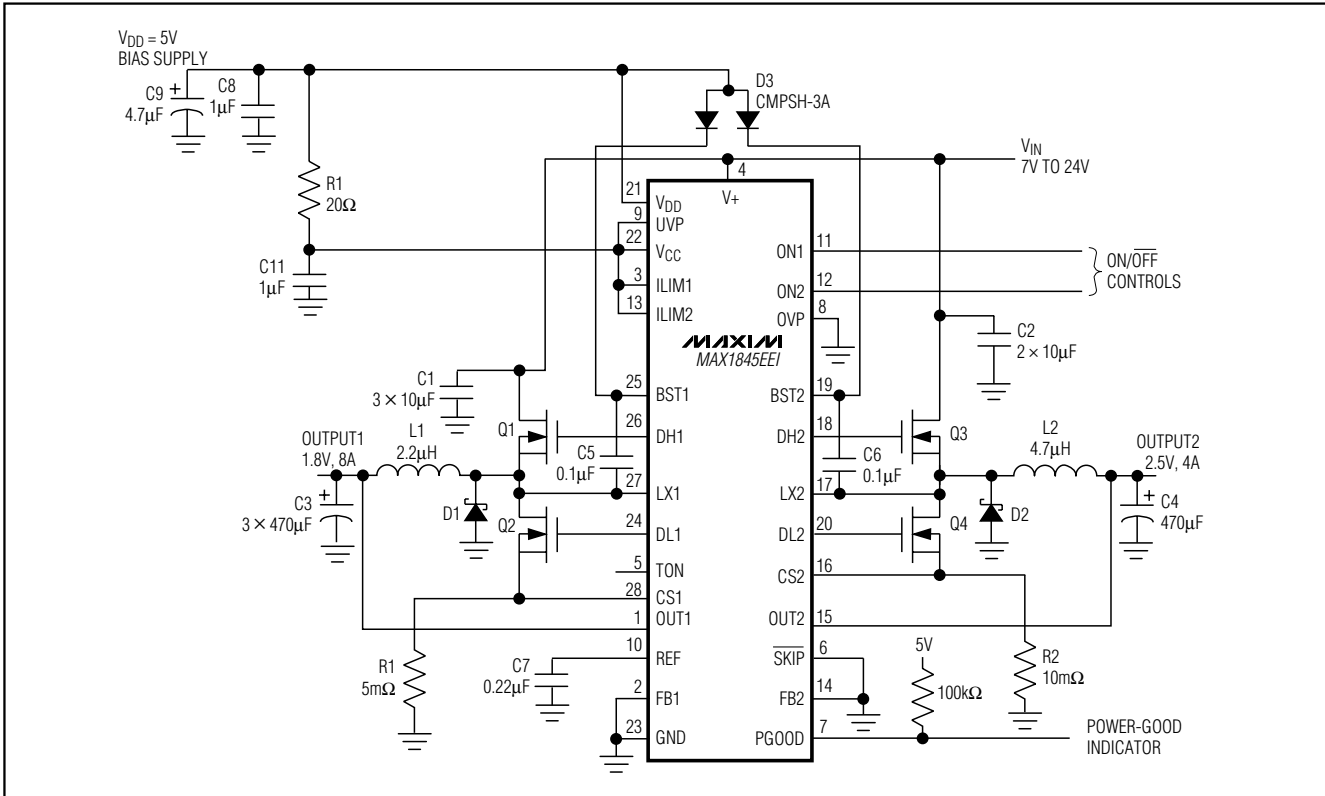

Figure 1. Standard Application Circuit

Dual, High-Efficiency, Step-Down Controller with Accurate Current Limit

Table 1. Component Selection for Standard Applications

COMPONENT	SIDE 1: 1.8V AT 8A/ SIDE 2: 2.5V AT 4A
Input Range	4.5V to 28V
Q1 High-Side MOSFET	Fairchild Semiconductor FDS6612A or International Rectifier IRF7807
Q2 Low-Side MOSFET	Fairchild Semiconductor FDS6670A or International Rectifier IRF7805
Q3, Q4 High/Low-Side MOSFETs	Fairchild Semiconductor FDS6982A
D1, D2 Rectifier	Nihon EP10QY03
D3 Rectifier	Central Semiconductor CMPSH-3A
L1 Inductor	2.2μH Panasonic ETQP6F2R2SFA or Sumida CDRH127-2R4
L2 Inductor	4.7μH Sumida CDRH124-4R7MC
C1 (3), C2 (2) Input Capacitor	10μF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
C3 (3), C4 Output Capacitor	470μF, 6V Kemet T510X477M006AS or Sanyo 6TPB330M
R$_{SENSE1}$	5mΩ, ±1%, 1W IRC LR2512-01-R005-F or D$_{ALE}$ WSL-2512-R005F
R$_{SENSE2}$	10mΩ, ±1%, 0.5W IRC LR2010-01-R010-F or D$_{ALE}$ WSL-2010-R010F

Two external factors that influence switching-frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead-time effect increases the effective on-time, reducing the switching frequency as one or

Table 2. Component Suppliers

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
Central Semiconductor	516-435-1110	[1] 516-435-1824
Dale/Vishay	203-452-5664	[1] 203-452-5670
Fairchild Semiconductor	408-822-2181	[1] 408-721-1635
International Rectifier	310-322-3331	[1] 310-322-3332
IRC	800-752-8708	[1] 828-264-7204
Kemet	408-986-0424	[1] 408-986-1442
NIEC (Nihon)	805-867-2555*	[81] 3-3494-7414
Sanyo	619-661-6835	[81] 7-2070-1174
Siliconix	408-988-8000 800-554-5565	[1] 408-970-3950
Sumida	847-956-0666	[81] 3-3607-5144
Taiyo Yuden	408-573-4150	[1] 408-573-4159
TDK	847-390-4461	[1] 847-390-4405

*Distributor

both dead times. It occurs only in PWM mode ($\overline{SKIP}$ = high) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time.

For loads above the critical conduction point, the actual switching frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

where V$_{DROP1}$ is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V$_{DROP2}$ is the sum of the resistances in the charging path; and t$_{ON}$ is the on-time calculated by the MAX1845.

Automatic Pulse-Skipping Switchover

In skip mode ($\overline{SKIP}$ = GND), an inherent automatic switchover to PFM takes place at light loads. This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). For a 7V to 24V battery range, of this threshold is relatively constant, with only a minor dependence on battery voltage:

$$I_{LOAD(SKIP)} \approx \frac{K \times V_{OUT\_}}{2L} \left(\frac{V_{IN} - V_{OUT\_}}{V_{IN}} \right)$$
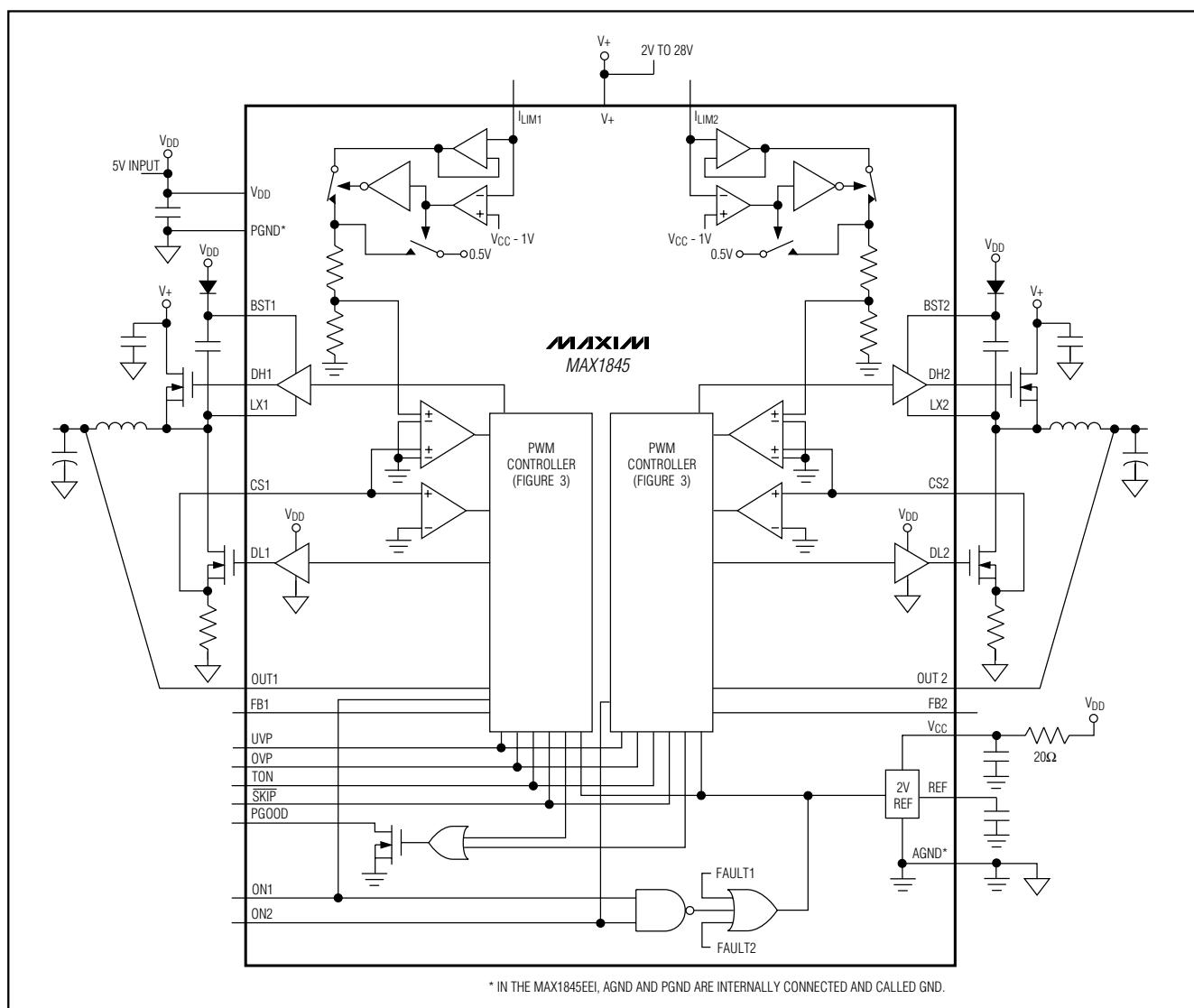
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Figure 2. Functional Diagram

where K is the on-time scale factor (Table 4). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 4). For example, in the standard application circuit with V_{OUT1} = 2.5V, V_{IN} = 15V, and K = 2.96µs (Table 4), switchover to pulse-skipping operation occurs at I_{LOAD} = 0.7A or about 1/6 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values

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Figure 3. PWM Controller (One Side Only)

include larger physical size and degraded load-transient response (especially at low input voltage levels).

DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the output voltage will have a DC regulation higher than the trip level by 50% of the ripple. In discontinuous conduction ($\overline{\text{SKIP}}$ = GND, light-load), the output voltage will have a DC regulation higher than the trip level by approximately 1.5% due to slope compensation.

Forced-PWM Mode ($\overline{\text{SKIP}}$ = High)

The low-noise, forced-PWM mode ($\overline{\text{SKIP}}$ = high) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop strives to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: The no-load battery current can be 10mA to 40mA, depending on the external MOSFETs.

Forced-PWM mode is most useful for reducing audiofrequency noise, improving load-transient response, providing sink-current capability for dynamic output voltage adjustment, and improving the cross-regulation

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Table 3. Operating Mode Truth Table

ON1	ON2	$\overline{\text{SKIP}}$	DL1/DL2	MODE	COMMENTS
GND	GND	X	High*/High*	Shutdown	Low-power shutdown state. If overvoltage protection is enabled, DL1 and DL2 are forced to V_{DD}, ensuring overvoltage protection, I_{CC} < 1µA (typ).
V_{CC}	GND	V_{CC}	Switching/High*	Run (PWM), Low Noise, Side 1 Only	Low-noise, fixed frequency PWM at all load conditions. Low noise, high I_Q.
GND	V_{CC}	V_{CC}	High*/Switching	Run (PWM), Low Noise, Side 2 Only	
V_{CC}	V_{CC}	V_{CC}	Switching/ Switching	Run (PWM), Low Noise, Both Sides Active	
V_{CC}	GND	GND	Switching/High*	Run (PWM/PFM), Skip Mode, Side 1 Only	Normal operation with automatic PWM/PFM switchover for pulse skipping at light loads. Best light-load efficiency.
GND	V_{CC}	GND	High*/Switching	Run (PWM/PFM), Skip Mode, Side 2 Only	
V_{CC}	V_{CC}	GND	Switching/ Switching	Run (PWM/PFM), Skip Mode, Both Sides Active	
V_{CC}	V_{CC}	X	High*/High*	Fault	Fault latch has been set by overvoltage protection circuit, undervoltage protection circuit, or thermal shutdown. Device will remain in fault mode until V_{CC} power is cycled or ON1/ON2 is toggled.

*DL_ high only if overvoltage protection enabled (see Output Overvoltage Protection section).

of multiple-output applications that use a flyback transformer or coupled inductor.

Current-Limit Circuit (ILIM_)

The current-limit circuit employs a unique "valley" current-sensing algorithm. If the magnitude of the current-sense signal at CS_ is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 5). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery voltage.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and therefore tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an internal 5µA current source and an external resistor at ILIM. The current-limit threshold adjustment range is from 25mV to 250mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10 the voltage seen at ILIM. The threshold defaults to 50mV when ILIM is con-

nected to V_{CC}. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by CS_ and GND. Mount or place the IC close to the low-side MOSFET and sense resistor with short, direct traces, making a Kelvin sense connection to the sense resistor. In Figure 1, the Schottky diodes (D1 and D2) provide current paths parallel to the Q2/R_{SENSE} and Q4/R_{SENSE} current paths, respectively. Accurate current sensing requires D1/D2 to be off while Q2/Q4 conducts. Avoid large current-sense voltages that, combined with the voltage across Q2/Q4, would allow D1/D2 to conduct. If very large sense voltages are used, connect D1/D2 in parallel with Q2/Q4 only.

MOSFET Gate Drivers (DH_, DL_)

The DH and DL drivers are optimized for driving moderate-size, high-side and larger, low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{BATT} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must
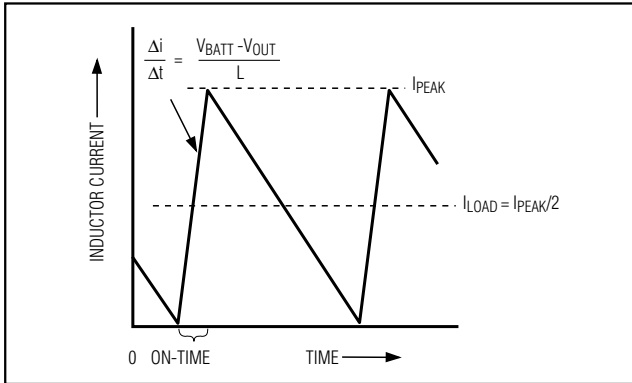
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Figure 4. Pulse-Skipping/Discontinuous Crossover Point

Figure 5. "Valley" Current-Limit Threshold Point

be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1845 will interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the MAX1845).

The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.5Ω typical on-resistance. This helps prevent DL from being pulled up during the fast rise-time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, some combinations of high- and low-side FETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 6).

POR, UVLO, and Soft-Start
Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching. DL is low if the overvoltage protection (OVP) is disabled. DL is high if the overvoltage protection is enabled (see the *Output Overvoltage Protection* section) when V_{CC} rises above 4.2V, whereupon an internal digital soft-start timer begins to ramp up the maximum allowed current limit. The ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%; 100% current is available after 1.7ms ±50%.

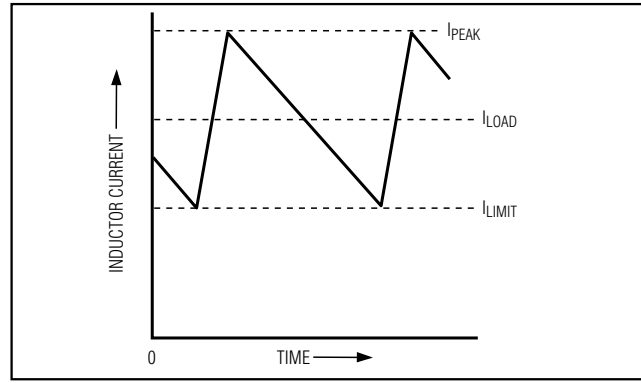A continuously adjustable analog soft-start function can be realized by adding a capacitor in parallel with the ILIM external resistor-divider network. This soft-start method requires a minimum interval between power-down and power-up to discharge the capacitor.

Power-Good Output (PGOOD)
The PGOOD window comparator continuously monitors the output voltage for both overvoltage and undervoltage conditions. In shutdown, standby, and soft-start, PGOOD is actively held low. After a digital soft-start has terminated, PGOOD is released when the output is within 10% of the error-comparator threshold. The PGOOD output is a true open-drain type with no parasitic ESD diodes. Note that the PGOOD window detector is independent of the output overvoltage and undervoltage protection (UVP) thresholds.

Output Overvoltage Protection
The output voltage can be continuously monitored for overvoltage. When overvoltage protection is enabled, if the output exceeds the overvoltage threshold, overvoltage protection is triggered and the DL low-side gate-drivers are forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and reduces the input voltage.

Note that DL latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

Connect OVP to GND to enable the default trip level of 114% of the nominal output. To adjust the overvoltage protection trip level, apply a voltage from 1V (100%) to 1.8V (180%) at OVP. Disable the overvoltage protection by connecting OVP to V_{CC}.
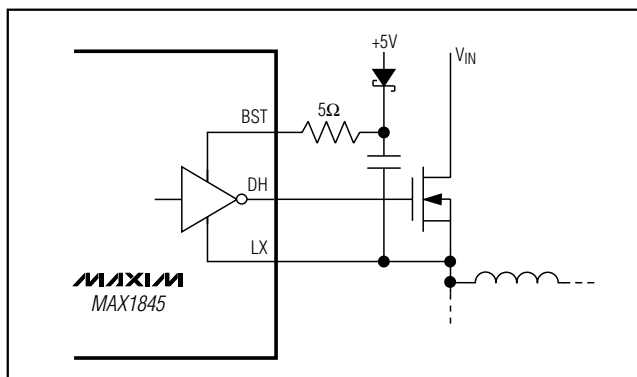
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Figure 6. Reducing the Switching-Node Rise Time

The overvoltage trip level depends on the internal or external output voltage feedback divider and is restricted by the output voltage adjustment range (1V to 5.5V) and by the absolute maximum rating of OUT_. Setting the overvoltage threshold higher than the output voltage adjustment range is not recommended.

Output Undervoltage Protection

The output voltage can be continuously monitored for undervoltage. When undervoltage protection is enabled (UVP = V_{CC}), if the output is less than 70% of the error-amplifier trip voltage, undervoltage protection is triggered. If an overvoltage protection threshold is set, the DL low-side gate driver is forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor, reduces the input voltage, and grounds the outputs. If the overvoltage protection is disabled (OVP = V_{CC}) and an undervoltage event occurs, the gate drivers are turned off and the outputs float. Connect UVP to GND to disable undervoltage protection.

Note that DL latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp. Also, note the nonstandard logic levels if actively driving UVP (see the *Electrical Characteristics*).

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

1) **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. Lower input voltages result in better efficiency.

2) **Maximum Load Current.** There are two values to consider. The *peak load current* ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The *continuous load current* (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

3) **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2.

4) **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

The MAX1845's pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load-current value at which PFM/PWM switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)} = 8A$, $V_{IN} = 15V$, $V_{OUT} = 1.8V$, f = 300kHz, 25% ripple current or LIR = 0.25:

$$L = \frac{1.8V(15V - 1.8V)}{15V \times 345kHz \times 0.25 \times 8A} = 2.3\mu H$$

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Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + [(LIR / 2) \times I_{LOAD(MAX)}]$$

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L}{2 \times C_F \times DUTY\ (V_{IN(MIN)} - V_{OUT})}$$

where:

$$DUTY = \frac{K\ (V_{OUT} + 0.075V)\ V_{IN}}{K\ (V_{OUT} + 0.075V)\ V_{OUT} + min\ off\text{-}time}$$

where minimum off-time = 400ns typ (Table 4).

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} = L \times I_{PEAK}^2 / (2\ C_{OUT}\ V_{OUT})$$

where I_{PEAK} is the peak inductor current.

Determining the Current Limit

For most applications, set the MAX1845 current limit by the following procedure:

1) Determine the minimum (valley) inductor current ($I_{L(MIN)}$) under conditions when V_{IN} is small, V_{OUT} is large, and load current is maximum. The minimum inductor current is I_{LOAD} minus half the ripple current (Figure 4).

2) The sense resistor determines the achievable current-limit accuracy. There is a trade-off between current-limit accuracy and sense-resistor power dissipation. Most applications employ a current-sense voltage of 50mV to 100mV. Choose a sense resistor such that:

R_{SENSE} = Current-Limit Threshold Voltage / $I_{L(MIN)}$

Extremely cost-sensitive applications that do not require high-accuracy current sensing can use the on-resistance of the low-side MOSFET switch in place of the sense resistor by connecting CS_ to LX_ (Figure

7a). Use the worst-case value for $R_{DS(ON)}$ from the MOSFET data sheet, and add a margin of 0.5%/°C for the rise in $R_{DS(ON)}$ with temperature. Use the calculated $R_{DS(ON)}$ and $I_{L(MIN)}$ from step 1 above to determine the current-limit threshold voltage. If the default 50mV threshold is unacceptable, set the threshold value as in step 2 above.

In all cases, ensure an acceptable current limit considering current-sense and resistor accuracies.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

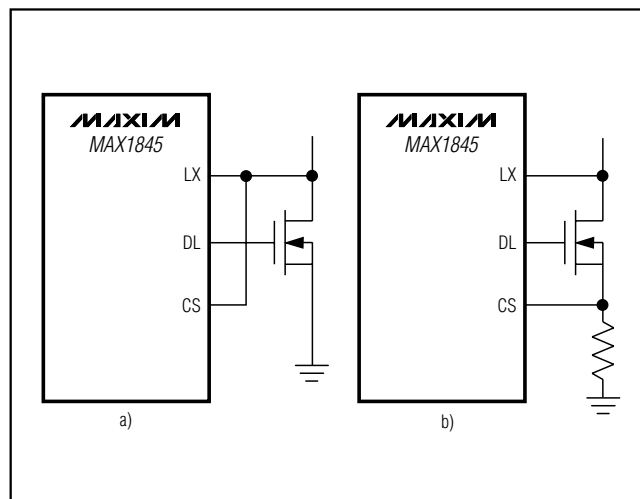$$R_{ESR} \leq \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

Figure 7. Current-Sense Configurations

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Table 4. Frequency Selection Guidelines

TON SETTING	SIDE 1 FREQUENCY (kHz)	SIDE 1 K-FACTOR (µs)	SIDE 2 FREQUENCY (kHz)	SIDE 2 K-FACTOR (µs)	APPROXIMATE K-FACTOR ERROR (%)
V_{CC}	235	4.24	170	5.81	±10
FLOAT	345	2.96	255	4.03	±10
REF	485	2.08	355	2.81	±12.5
AGND	620	1.63	460	2.18	±12.5

The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs™, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Also, the capacitance must be great enough to prevent the inductor's stored energy from launching the output above the overvoltage protection threshold. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} \leq \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_F}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 15kHz. In the design example used for inductor selection, the ESR needed to support 20mV$_{P-P}$ ripple is 20mV/2A = 10mΩ. Three 470µF/6V Kemet T510 low-ESR tantalum capacitors in parallel provide

10mΩ (max) ESR. Their typical combined ESR results in a zero at 11.3kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting OUT_ or the FB_ divider close to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback-loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient (refer to the MAX1845 EV kit manual) and carefully observe the output voltage ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or overshoot.

OS-CON is a trademark of Sanyo.

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Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>5A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses equal to the switching losses at the optimum battery voltage (15V). Check to ensure that the conduction losses at the **minimum** input voltage do not exceed the package thermal limits or violate the overall thermal budget. Check to ensure that conduction losses plus switching losses at the **maximum** input voltage do not exceed the package ratings or violate the overall thermal budget.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate to small package (i.e., SO-8), and is reasonably priced. Ensure that the MAX1845 DL gate driver can drive Q2; in other words, check that the gate is not pulled up by the high-side switch turning on due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses are not an issue for the low-side MOS-FET since it is a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty cycle extremes. For the high-side MOSFET, the worst-case-power dissipation (PD) due to resistance occurs at minimum battery voltage:

$$PD(\text{Q1 resistance}) = \left(\frac{V_{OUT}}{V_{IN(MIN)}}\right)I_{LOAD}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired in order to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOS-FET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually

become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2f switching loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, reconsider the choice of MOSFET.

Calculating the power dissipation in Q1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for bench evaluation, preferably including a verification using a thermocouple mounted on Q1:

$$PD(\text{Q1 switching}) = \frac{C_{RSS} \times V_{IN(MAX)}^2 \times f \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

For the low-side MOSFET, Q2, the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(\text{Q2}) = \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]I_{LOAD}^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + (LIR / 2) \times I_{LOAD(MAX)}$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. If short-circuit protection without overload protection is adequate, enable overvoltage protection, and use $I_{LOAD(MAX)}$ to calculate component stresses.

Choose a Schottky diode (D1) having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional and can be removed if efficiency is not critical.

Applications Information

Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. For best dropout performance, use the slower on-time settings. When working with low input voltages, the duty-cycle limit must be calculated using the worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 4). Also, keep in mind that transient response performance of buck regulators operating close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP} / \Delta I_{DOWN}$ is an indicator of ability to slew the inductor current higher in response to increased load and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current will be less able to increase during each switching cycle, and V_{SAG} will greatly increase unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but this may be adjusted up or down to allow trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, calculate the minimum operating voltage as follows:

$$V_{IN(MIN)} = [(V_{OUT} + V_{DROP1}) / \{1 - (t_{OFF(MIN)} \times h / K)\}] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see the *On-Time One-Shot (TON)* section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics*, and K is taken from Table 4. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to ensure adequate transient response.

Dropout Design Example:

V_{OUT} = 1.8V

fsw = 600kHz

K = 1.63µs, worst-case K = 1.4175µs

$t_{OFF(MIN)}$ = 500ns

V_{DROP1} = V_{DROP2} = 100mV

h = 1.5

$$V_{IN(MIN)} = (1.8V + 0.1V) / [1 - (0.5µs \times 1.5) / 1.4175µs] + 0.1V - 0.1V = 3.8V$$

Calculating again with h = 1 gives an absolute limit of dropout:

$$V_{IN(MIN)} = (1.8V + 0.1V) / [1 - (0.5µs \times 1) / 1.4175µs] + 0.1V - 0.1V = 2.8V$$

Therefore, V_{IN} must be greater than 2.8V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.8V.

Fixed Output Voltages

The MAX1845's dual-mode operation allows the selection of common voltages without requiring external components (Figure 8). Connect FB1 to GND for a fixed 1.8V output or to V_{CC} for a 1.5V output, or connect FB1 directly to OUT1 for a fixed 1V output.

Connect FB2 to GND for a fixed 2.5V output or to OUT2 for a fixed 1V output.

Setting $V_{OUT\_}$ with a Resistor-Divider

The output voltage can be adjusted from 1V to 5.5V with a resistor-divider network (Figure 9). The equation for adjusting the output voltage is:

$$V_{OUT\_} = V_{FB\_}\left(1 + \frac{R1}{R2}\right)$$

where $V_{FB\_}$ is 1.0V and R2 is about 10kΩ.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. This is especially true for dual converters, where one channel can affect the other. The switching power stages require particular attention (Figure 10). Refer to the MAX1845 evaluation kit data sheet for a specific layout example.

Use a four-layer board. Use the top side for power components and the bottom side for the IC and the sensitive ground components. Use the two middle layers as ground planes, with interconnections between the top and bottom layers as needed. If possible,

Dual, High-Efficiency, Step-Down Controller with Accurate Current Limit
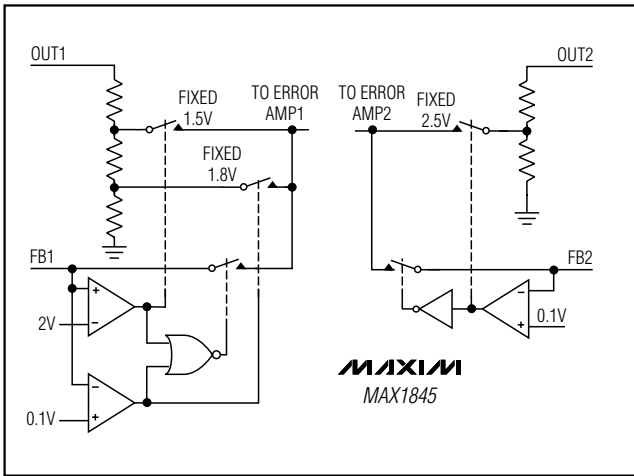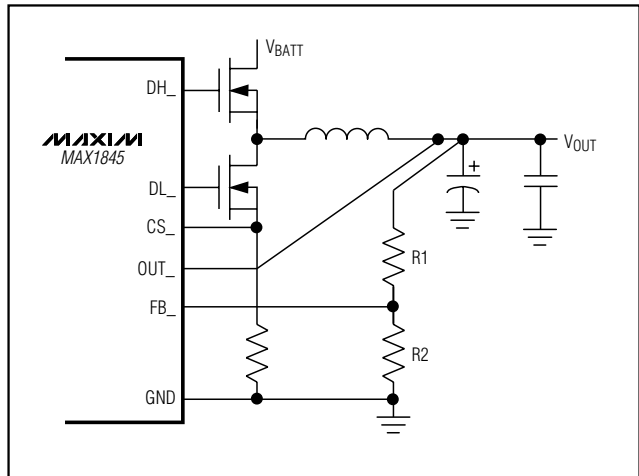

Figure 8. Feedback Mux

Figure 9. Setting V_{OUT} with a Resistor-Divider

mount all of the power components on the top side of the board, with connecting terminals flush against one another.

Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Short power traces and load connections are essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.

Place the current-sense resistors close to the top-side star-ground point (where the IC ground connects to the top-side ground plane) to minimize current-sensing errors. Avoid additional current-sensing errors by using a Kelvin connection from CS_ pins to the sense resistors.

The following guidelines are in order of importance:

• Keep the space between the ground connection of the current-sense resistors short and near the via to the IC ground pin.

• Minimize the resistance on the low-side path. The low-side path starts at the ground of the low-side FET, goes through the low-side FET, through the inductor, through the output capacitor, and returns to the ground of the low-side FET. Minimize the resistance by keeping the components close together and the traces short and wide.

• Minimize the resistance in the high-side path. This path starts at V_{IN}, goes through the high-side FET,
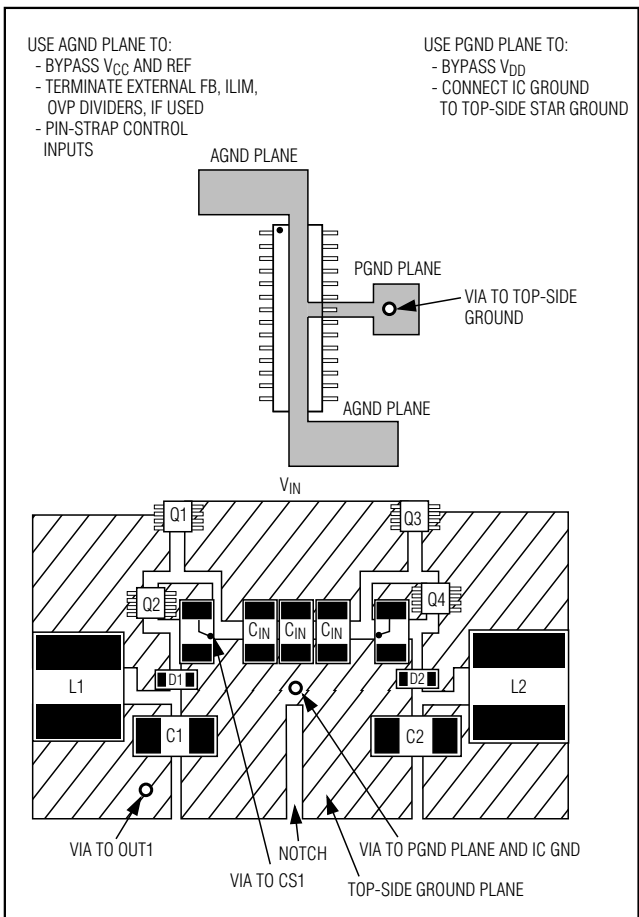

Figure 10. PC Board Layout Example

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through the inductor, through the input capacitor, and back to the input.

- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, ILIM_, FB_).
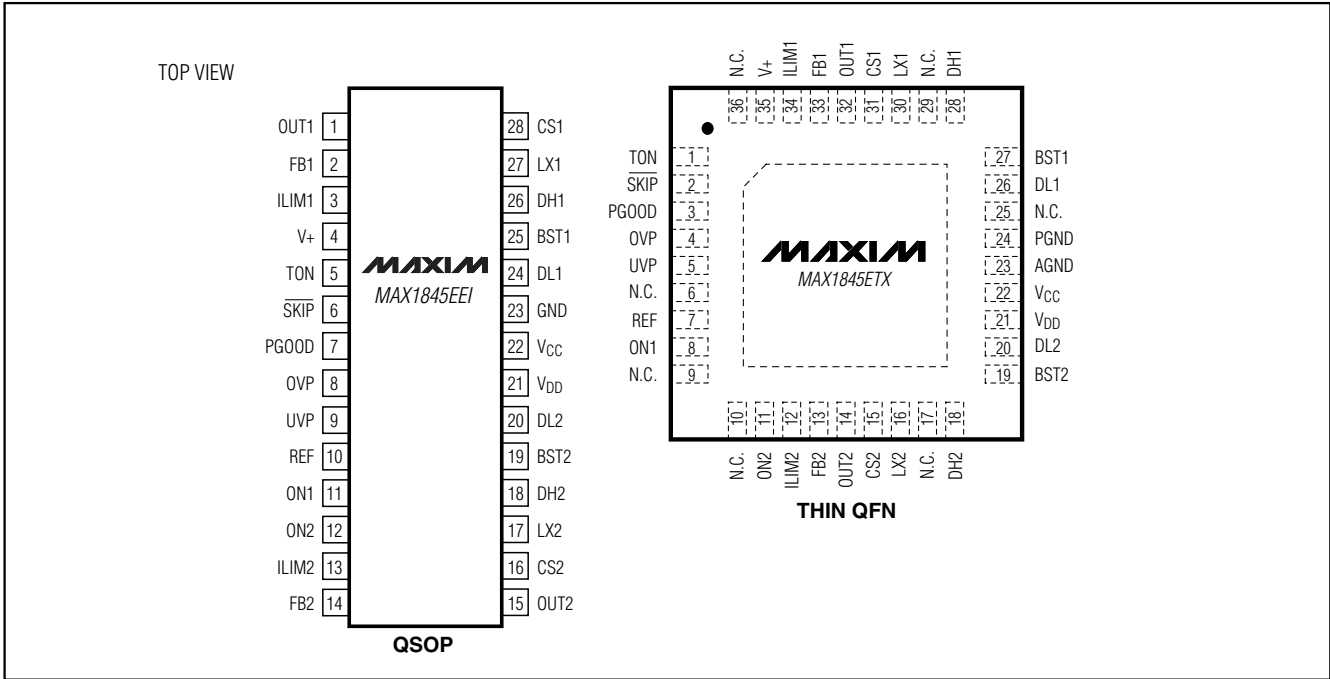
Layout Procedure

1) Place the power components first, with ground terminals adjacent (sense resistor, C_{IN}-, C_{OUT}-, D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.

2) Mount the controller IC adjacent to the synchronous rectifiers MOSFETs, preferably on the back side in order to keep CS_, GND, and the DL_ gate-drive line short and wide. The DL_ gate trace must be short and wide, measuring 10 squares to 20 squares (50mils to 100mils wide if the MOSFET is 1 inch from the controller IC).

3) Group the gate-drive components (BST_ diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.

4) Make the DC-DC controller ground connections as follows: Create a small analog ground plane (AGND) near the IC. Connect this plane directly to GND under the IC, and use this plane for the ground connection for the REF and V_{CC} bypass capacitors, FB_, OVP, and ILIM_ dividers (if any). Do not connect the AGND plane to any ground other than the GND pin. Create another small ground island (PGND), and use it for the V_{DD} bypass capacitor, placed very close to the IC. Connect the PGND plane directly to GND from the outside of the IC.

5) On the board's top side (power planes), make a star ground to minimize crosstalk between the two sides. The top-side star ground is a star connection of the input capacitors, side 1 low-side MOSFET, and side 2 low-side MOSFET. Keep the resistance low between the star ground and the source of the low-side MOSFETs for accurate current limit. Connect the top-side star ground (used for MOSFET, input, and output capacitors) to the small PGND island with a short, wide connection (preferably just a via).

Minimize crosstalk between side 1 and side 2 by directing their switching ground currents into the star ground with a notch as shown in Figure 10. If multiple layers are available (highly recommended), create PGND1 and PGND2 islands on the layer just below the top-side layer (refer to the MAX1845 EV kit for an example) to act as an EMI shield. Connect each of these individually to the star-ground via, which connects the top side to the PGND plane. Add one more solid ground plane under the IC to act as an additional shield, and also connect that to the star-ground via.

6) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias.

_____Chip Information

TRANSISTOR COUNT: 4795
PROCESS: BiCMOS

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Pin Configurations

TOP VIEW

QSOP

```
MAX1845EEI

OUT1   1           28  CS1
FB1    2           27  LX1
ILIM1  3           26  DH1
V+     4           25  BST1
TON    5           24  DL1
SKIP   6           23  GND
PGOOD  7           22  VCC
OVP    8           21  VDD
UVP    9           20  DL2
REF   10           19  BST2
ON1   11           18  DH2
ON2   12           17  LX2
ILIM2 13           16  CS2
FB2   14           15  OUT2
```

THIN QFN

```
MAX1845ETX

         N.C.  V+  ILIM1  FB1  OUT1  CS1  LX1  N.C.  DH1
          36   35   34    33    32   31   30   29    28

TON    1                                            27  BST1
SKIP   2                                            26  DL1
PGOOD  3                                            25  N.C.
OVP    4                                            24  PGND
UVP    5                                            23  AGND
N.C.   6                                            22  VCC
REF    7                                            21  VDD
ON1    8                                            20  DL2
N.C.   9                                            19  BST2

         10   11   12   13   14   15   16   17   18
         N.C. ON2 ILIM2 FB2 OUT2 CS2  LX2  N.C. DH2
```

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)
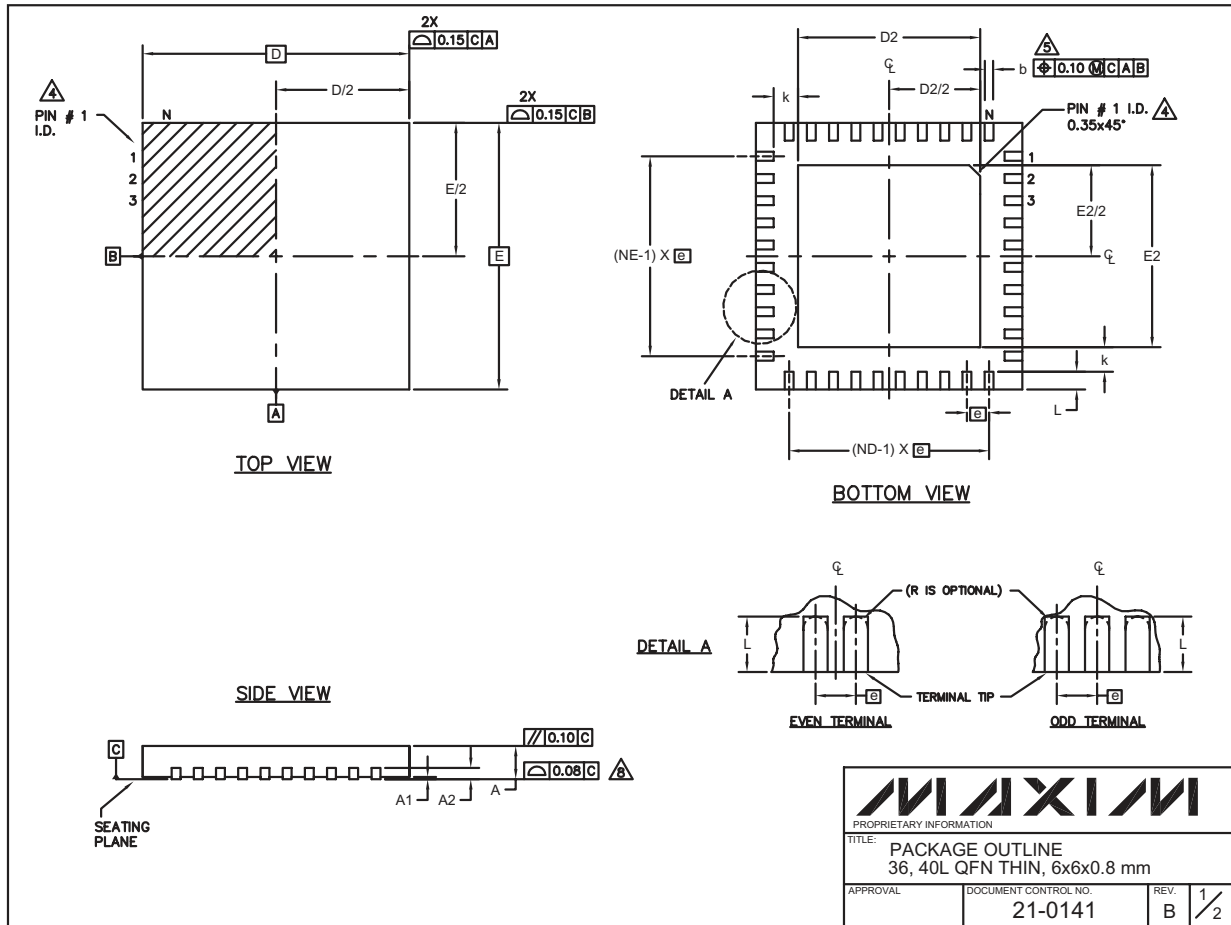
MAX1845

QSOP.EPS

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	N
D	.189	.196	4.80	4.98	16 AA
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20 AB
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24 AC
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28 AD
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28
   LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

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PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025' LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Note: *The MAX1845EEI does not have a heat slug.*

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(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TOP VIEW

BOTTOM VIEW

DETAIL A

SIDE VIEW

QFN THIN 6x6x0.8.EPS

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PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40L QFN THIN, 6x6x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	B	1/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05
A3		0.20 REF.			0.20 REF.	
b	0.20	0.25	0.30	0.20	0.25	0.30
D	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10
e		0.50 BSC.			0.50 BSC.	
k	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.30	0.40	0.50
N		36			40	
ND		9			10	
NE		9			10	
JEDEC		WJJD-1			WJJD-2	

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3. N IS THE TOTAL NUMBER OF TERMINALS.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC MO220.

10. WARPAGE SHALL NOT EXCEED 0.10 mm.

/VI /IXI /VI

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 36, 40L QFN THIN, 6x6x0.8 mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0141	REV. B / 2/2

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Part Number Table

Notes:

1. See the MAX1845 QuickView Data Sheet for further information on this product family or download the MAX1845 full data sheet (PDF, 548kB).
2. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
3. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See full data sheet or Part Naming Conventions.
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX1845EEI			QSOP;28 pin;.150" Dwg: 21-0055F (PDF) Use pkgcode/variation: E28-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX1845EEI-T			QSOP;28 pin;.150" Dwg: 21-0055F (PDF) Use pkgcode/variation: E28-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX1845EEI+			QSOP;28 pin;.150" Dwg: 21-0055F (PDF) Use pkgcode/variation: E28+1*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX1845EEI+T			QSOP;28 pin;.150" Dwg: 21-0055F (PDF) Use pkgcode/variation: E28+1*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX1845ETX			THIN QFN;36 pin;6x6x0.8mm Dwg: 21-0141H (PDF) Use pkgcode/variation: T3666-3*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX1845ETX-T			THIN QFN;36 pin;6x6x0.8mm Dwg: 21-0141H (PDF) Use pkgcode/variation: T3666-3*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX1845ETX+			THIN QFN;36 pin;6x6x0.8mm Dwg: 21-0141H (PDF) Use pkgcode/variation: T3666+3*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis

| MAX1845ETX+T | | | THIN QFN;36 pin;6x6x0.8mm
Dwg: 21-0141H (PDF)
Use pkgcode/variation: T3666+3* | -40C to +85C | RoHS/Lead-Free: Yes
Materials Analysis |

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