MP86998

Intelli-Phase™ Solution with Integrated HS-/LS-FETs and Driver in TLGA (5mmx6mm) Package

DESCRIPTION

The MP86998 is a monolithic half-bridge driver with built-in internal power MOSFETs and gate drivers. The MP86998 achieves 80A of continuous output current across a wide input supply range.

The devices utilizes a monolithic IC approach that drives up to 80A of current per phase. The integration of drivers and MOSFETs results in high efficiency due to an optimal dead time and parasitic inductance reduction. The MP86998 can operate at frequencies from 100kHz to 3MHz.

The MP86998 offers many features to simplify system design, and works with controllers with a tri-state PWM signal. It also comes with accurate current sense to monitor the inductor current, and temperature sense to report the junction temperature.

The device is ideal for server applications where efficiency and small size are at a premium. The MP86998 is available in a TLGA (5mmx6mm) package.

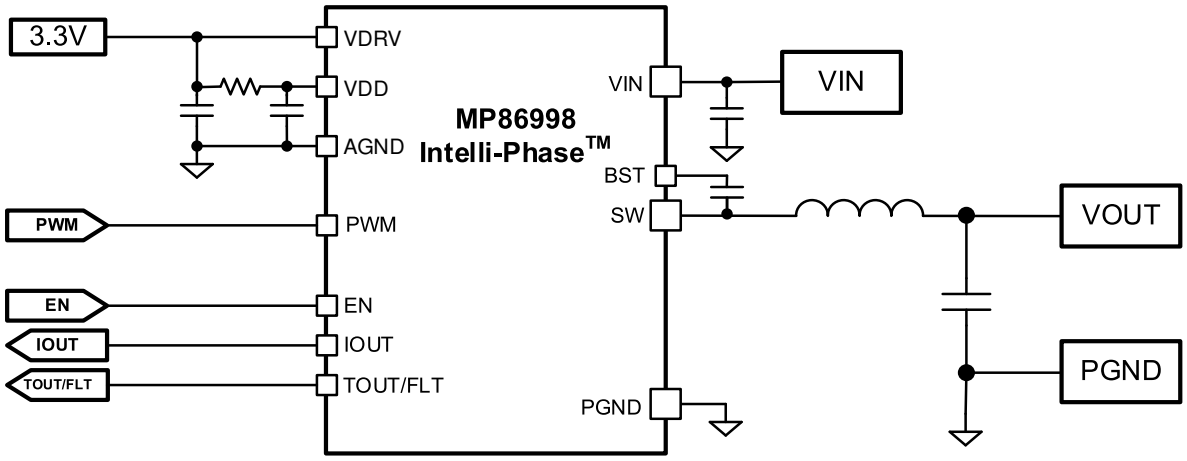
FEATURES

- Wide 3V to 16V Operating Input Range
- 80A Output Current
- Accu-Sense™ Current Sense
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a TLGA (5mmx6mm) Package

APPLICATIONS

- Server Core Voltages
- Graphics Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP86998GMJT	TLGA-41 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix –Z (e.g. MP86998GMJT–Z).

TOP MARKING

MPSYYWW

MP86998

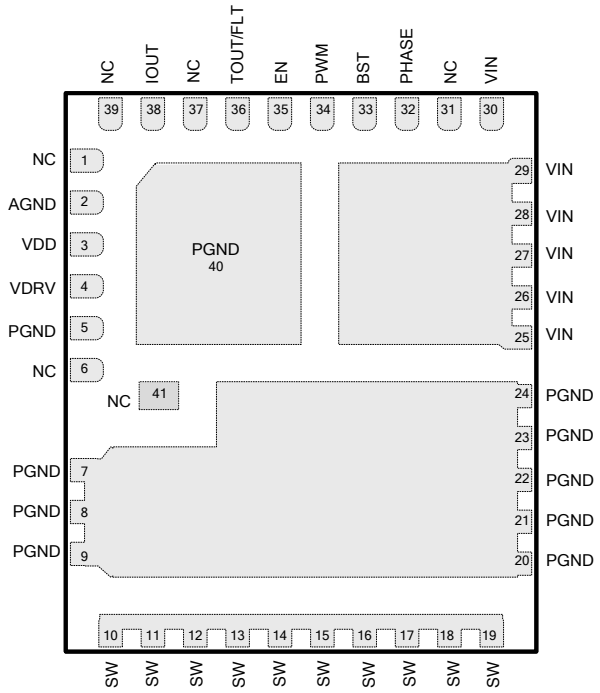
LLLLLLL

T

MPS: MPS prefix
YY: Year code
WW: Week code
MP86998: Part number
LLLLLLL: Lot number
T: Thin

PACKAGE REFERENCE

TOP VIEW



TLGA-41 (5mmx6mm)

PIN FUNCTIONS

Pin #	Pin Name	Description
1, 6, 31, 37, 39, 41	NC	**No connection.**
2	AGND	**Analog ground.**
3	VDD	**Supply voltage for internal circuitry.** Connect VDD to VDRV through a 2.2Ω resistor. Decouple VDD with a 1µF capacitor to AGND. Connect AGND and PGND at the VDD capacitor.
4	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply. Decouple VDRV with a 1µF to 4.7µF ceramic capacitor.
5, 7, 8, 9, 20–24, 40	PGND	**Power ground.**
10–19	SW	**Phase node.**
25–30	VIN	**Input supply voltage.** Place input ceramic capacitors (C_{IN}) close to the device to support the switching current with minimal parasitic inductance.
32	PHASE	**Switching node for the bootstrap capacitor connection.** The PHASE pin is connected to SW internally.
33	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.22µF capacitor to drive the power switch's gate above the supply voltage. Connect the capacitor between the PHASE and BST pins to form a floating supply across the power switch driver.
34	PWM	**Pulse-width modulation input.** Leave PWM floating or drive PWM to a middle-state voltage to put SW in a high-impedance state.
35	EN	**Enable.** Pull EN low to disable the MP86998 and place SW in a high-impedance state.
36	TOUT/FLT	**Single-pin temperature sense and fault reporting.** TOUT/FLT is pulled up to the VDD voltage if a fault occurs.
38	IOUT	**Current-sense output.** Use an external resistor to adjust the voltage proportional to the inductor current.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{IN} - $V_{SW\ (DC)}$ .....-0.3V to +25V
V_{IN} - $V_{SW\ (10ns)}$.....-5V to +32V
$V_{SW\ (DC)}$ .....-0.3V to V_{IN} + 0.3V
$V_{SW\ (25ns)}$.....-5V to +25V
V_{BST} ..... V_{SW} + 4V
V_{BST} - V_{PHASE} .....-0.3V to +4V
V_{DD}, V_{DRV} .....-0.3V to +4V
All other pins .....-0.3V to VDD + 0.3V
Instantaneous current 125A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....2000V

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) .....3.0V to 16V
Driver voltage (VDRV) .....3.0V to 3.6V
Logic voltage (VDD).....3.0V to 3.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TLGA-41 (5mmx6mm)..... 2.7..... 12.4... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB}: Thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical value, T_J = -40°C to 125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown		EN = low		90	180	μA
V_{IN} under-voltage lockout (UVLO) rising threshold				2.5	3.0	V
V_{IN} UVLO threshold hysteresis				450		mV
I_{VDRV} quiescent current		PWM = low		250	350	μA
I_{VDD} quiescent current		PWM = low		3		mA
I_{VDRV} operation current (4)		f_{SW} = 500kHz		19.8		mA
		f_{SW} = 800kHz		31.7		mA
VDD voltage UVLO rising threshold				2.75	2.95	V
VDD voltage UVLO threshold hysteresis				300		mV
High-side current limit (4)	I_{LIM_FLT}	Cycle-by-cycle up to 8 cycles		110		A
Low-side current limit (4)		Negative current limit, cycle-by-cycle, no fault report		-35		A
Negative current limit low-side off time (4)				200		ns
High-side current limit shutdown counter (4)				8		times
Dead time at SW rising (4)				2		ns
Dead time at SW falling (4)		Positive inductor current		6		ns
		Negative inductor current		28		ns
EN input high threshold voltage			2.30			V
EN input low threshold voltage					0.8	V
PWM high to SW rising delay (4)	t_{RISING}			20		ns
PWM low to SW falling delay (4)	$t_{FALLING}$			20		ns
PWM tri-state to SW Hi-Z delay (4)	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			30		ns
Minimum PWM pulse width (4)				20		ns
IOUT sense gain accuracy (4)		20A ≤ I_{SW} ≤ 80A, T_J = 25°C	-2	0	+2	%
IOUT sense gain	G_{IOUT}			5		μA/A
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V, T_J = 25°C	-2	0	+2	μA
		PWM = Hi-Z, V_{IOUT} = 1.2V	-1	0	+1	μA
IOUT pin voltage range (4)	V_{IOUT}		0.7		2.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

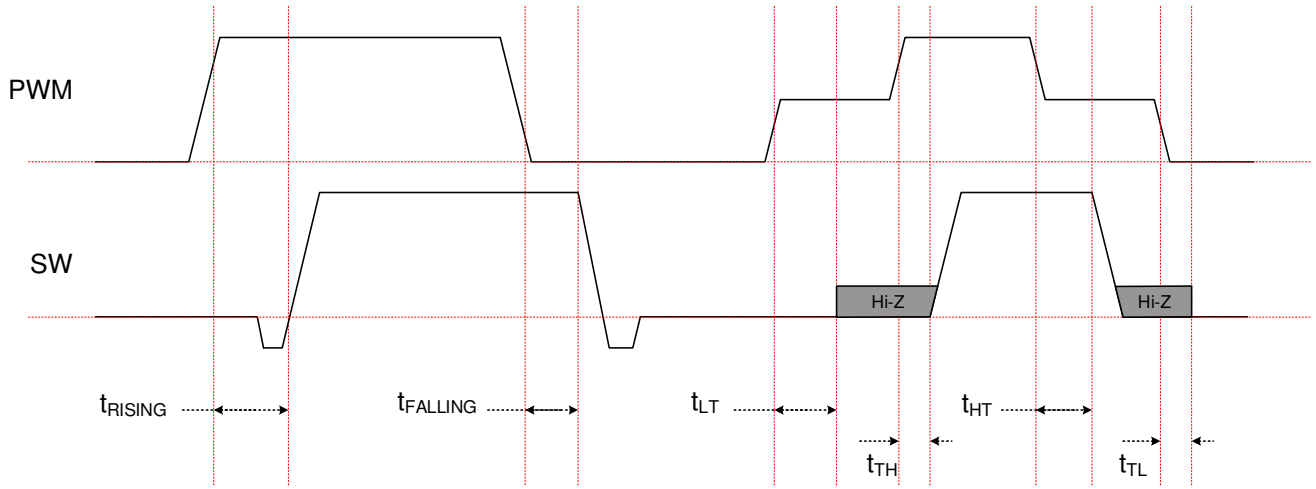
V_{IN} = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical value and T_J = -40°C to 125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
TOUT/FLT sense gain (4)				8		mV/℃
TOUT/FLT sense offset (4)		T_J = 25°C		800		mV
Over-temperature shutdown and fault flag (4)				160		°C
TOUT/FLT if a fault occurs (4)			3.0	3.3		V
PWM resistor		Pull up, EN = high		6		kΩ
		Pull down, EN = high		5		kΩ
PWM logic high voltage			2.30			V
PWM tri-state region			1.10		1.8	V
PWM logic low voltage					0.80	V

Note:

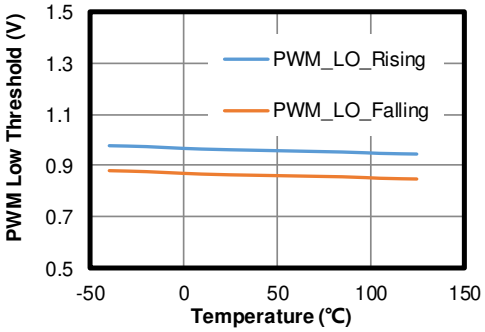
4) Not tested in production.

PWM TIMING DIAGRAM

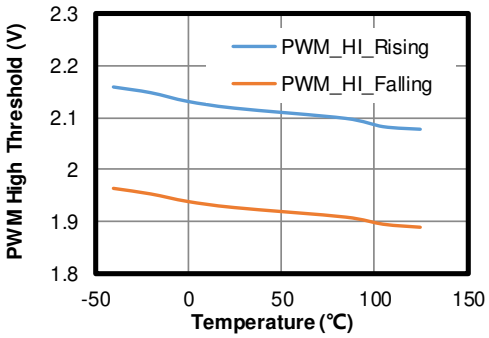


TYPICAL CHARACTERISTICS

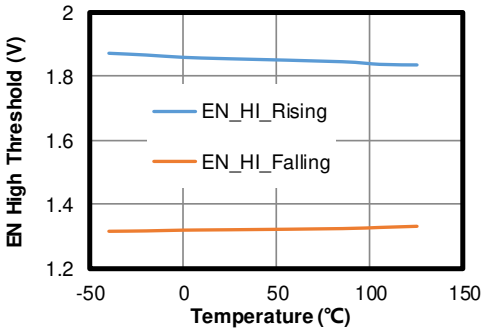
PWM Low



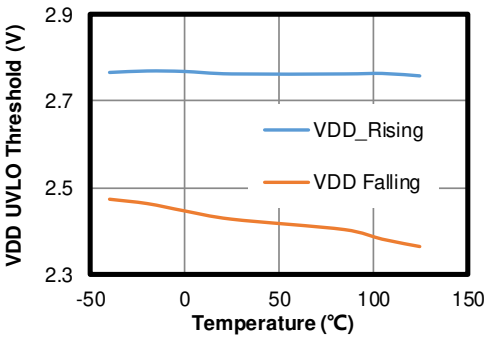
PWM High



EN High

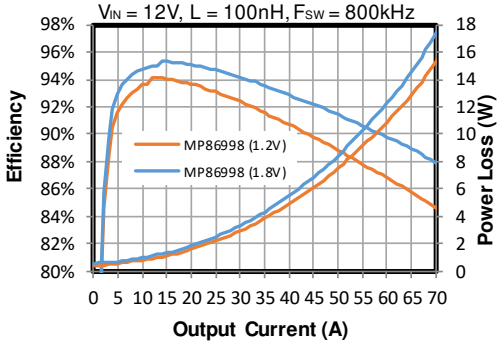


VDD UVLO



Efficiency vs. Output Current vs Power Loss

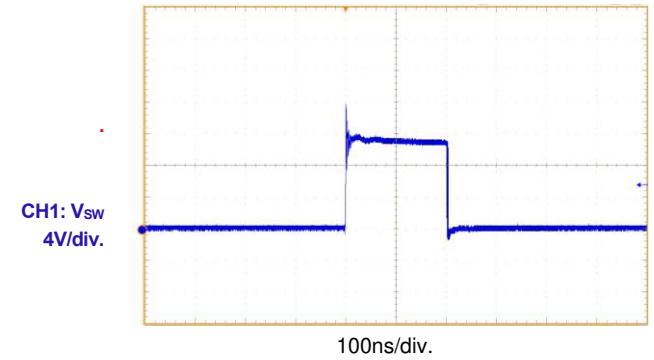
V_{IN} = 12V, L = 100nH, F_{SW} = 800kHz



TYPICAL PERFORMANCE CHARACTERISTICS

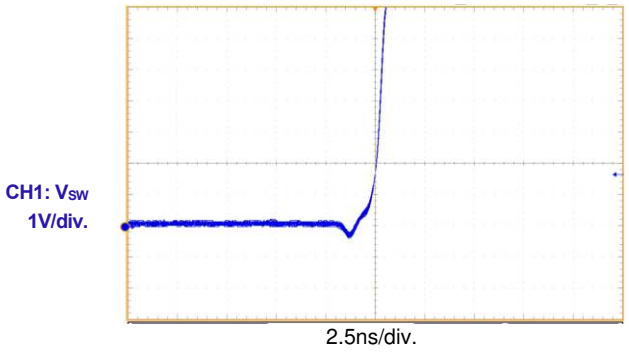
Switching

V_{IN} = 12V, L = 120nH, load = 30A



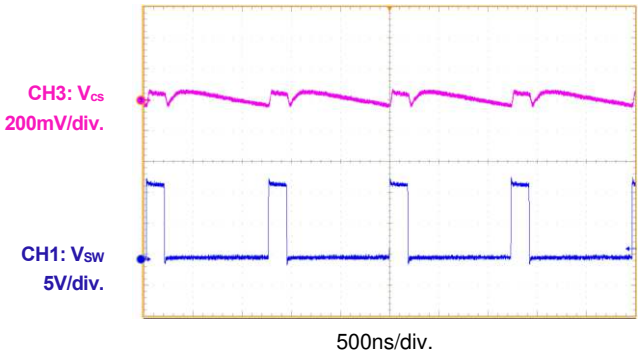
Dead Time when SW Ringing

Load = 30A



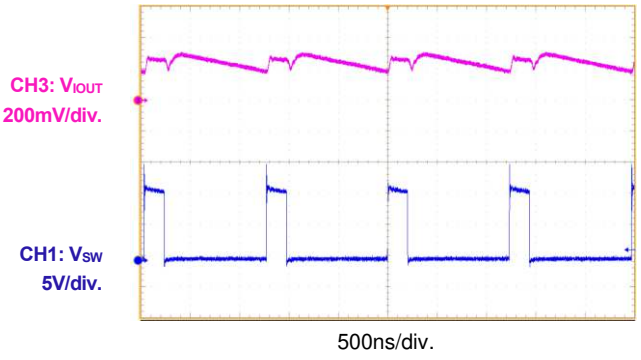
IOUT Output

Load = 0A

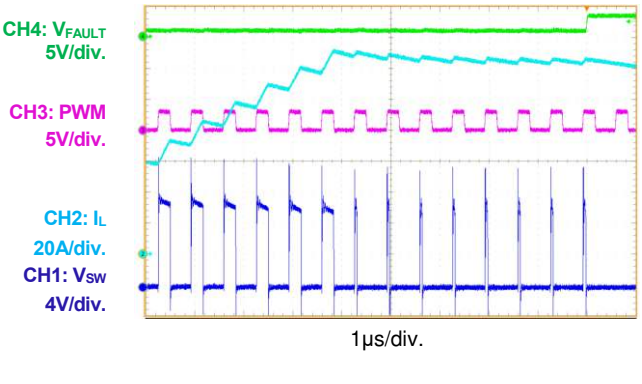


IOUT Output

Load = 30A



HS Current Limit



FUNCTIONAL BLOCK DIAGRAM

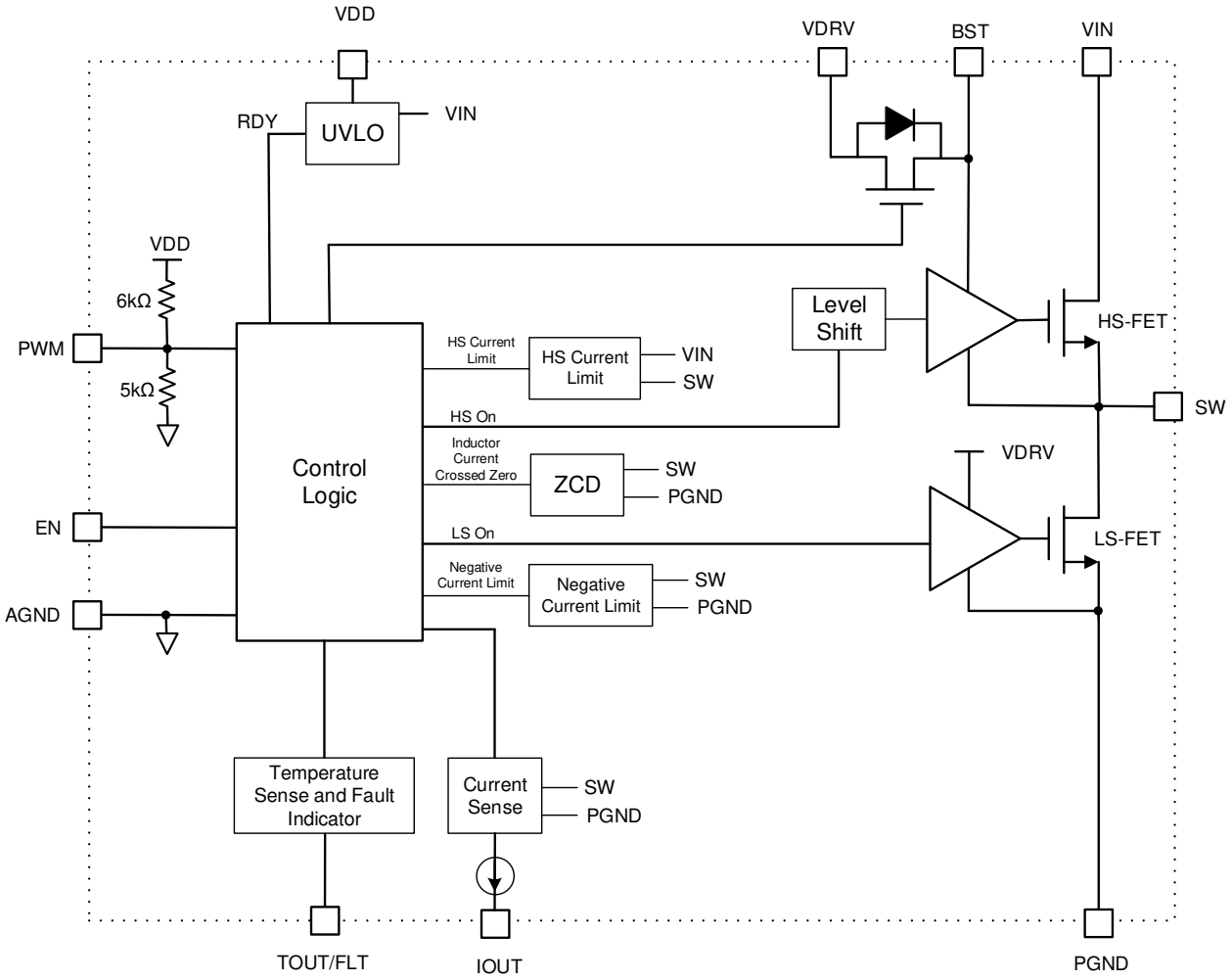


Figure 1: Functional Block Diagram

OPERATION

The MP86998 is an 80A, monolithic half-bridge driver with internal MOSFETs. It is well-suited for multi-phase buck regulators. An external 3.3V supply is required to supply both VDD and VDRV. When EN transitions from low to high and the VDRV signals are sufficiently high, the device begins operating.

Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) input pin is capable of tri-state input. If the PWM input signal is within the tri-state threshold window for 40ns (t_{HT} or t_{LT}), the high-side MOSFET (HS-FET) turns off immediately. Then the low-side MOSFET (LS-FET) enters diode emulation mode and remains on until zero-current detection (ZCD).

The tri-state PWM input is enabled by forcing a middle-voltage PWM signal, or by floating the PWM input. The internal current source charges the signal to a middle voltage. See the PWM Timing Diagram on page 5 for the propagation delay definition from PWM to the SW node.

Diode Emulation Mode

If PWM is either low or in tri-state while operating in diode emulation mode, the LS-FET turns on when the inductor current is positive. The LS-FET turns off if the inductor current is negative or if it crosses the ZCD threshold. Diode emulation mode can be enabled by driving PWM to a middle state or floating PWM.

Current Sense

When EN is high, the IOUT pin is a bidirectional current source that is proportional to the inductor current. The current-sense gain is 5μA/A. If required, a resistor can be used to configure the voltage gain proportional to the inductor current.

The IOUT output has two states (see Table 1). In disable mode (EN = low), the current-sense circuit is disabled, and IOUT is in a Hi-Z (high impedance) state.

Table 1: IOUT Output States

PWM	EN	IOUT
PWM	High	Active
-	Low	Hi-Z

The IOUT pin's voltage should range between 0.7V and 2.1V to achieve an accurate IOUT current output of up to +400μA/-200μA (e.g. +80A/-40A). Generally, there is a resistor (R_{IOUT}) connected from IOUT to an external voltage that is capable of sinking small currents. This provides a sufficient voltage to meet the required operating voltage range. Calculate the reference voltage (V_{CM}) and R_{IOUT} values with Equation (1):

$$0.7V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.1V \quad (1)$$

Where V_{CM} is a reference voltage connected to R_{IOUT}.

I_{OUT} can be estimated with Equation (2):

$$I_{IOUT} = I_{SW} \times G_{IOUT} \quad (2)$$

The Intelli-Phase's™ current-sense output can be used by the controller to monitor the output current accurately. The cycle-by-cycle current information from IOUT can be used for phase current balancing, over-current protection (OCP), and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current Limit

If an HS-FET over-current (OC) condition is detected, the HS-FET turns off for that PWM cycle. If the OC condition remains for eight consecutive cycles, the HS-FET latches off, TOUT/FLT pulls high to VDD, and the LS-FET turns on until ZCD. To release the latch and restart the device, toggle EN, or cycle the power on VIN or VDD.

When the LS-FET detects a -35A valley current, the MP86998 turns off the LS-FET and turns on the HS-FET for 200ns to limit the negative current. The LS-FET negative current limit does not trigger a fault report.

Temperature-Sense Output with Fault Indication (TOUT/FLT)

The TOUT/FLT pin senses the junction temperature and indicates whether a fault has occurred.

When VDD exceeds its under-voltage lockout (UVLO) threshold and the part is active, TOUT/FLT is a voltage output proportional to the junction temperature.

The gain is 8mV/°C and has an 800mV offset at 25°C. For example the voltage is 0.8V when T_J = 25°C, and 1.6V when T_J = 125°C.

If a fault occurs, TOUT/FLT is pulled to the VDD voltage to report the fault event, regardless of the temperature. 200ns after the fault occurrs, the PWM impedance changes accordingly to indicate the fault type. Table 2 shows the PWM status regarding each fault event.

Table 2: PWM Resistance when a Fault Occurs

Fault Type	PWM
HS-FET current limit protection	10kΩ to AGND
Over-temperature protection	20kΩ to AGND
SW-to-PGND short protection	1kΩ to VDD

TOUT/FLT can monitor three fault events.

1. Over-current limit (HS-FET): To trigger an over-current fault, the current limit must be exceeded eight consecutive times. If this fault occurs, the MP86998 latches off to turn off the HS-FET. The LS-FET turns on and stays on until the inductor current reaches 0A. PWM uses a 10kΩ resistor connected to AGND to indicate the fault type.
2. Over-temperature fault at T_J > 160°C: If this fault occurs, the MP86998 latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches 0A. PWM uses a 20kΩ resistor connected to AGND to indicate the fault type.
3. SW-to-PGND short: If this fault occurs, the MP86998 latches off to turn off the HS-FET. PWM is pulled high (1kΩ to VDD) to indicate the fault type.

The fault latch can be released by toggling EN or by recycling power on VIN or VDD.

For multi-phase operation, connect the TOUT/FLT pins of each Intelli-Phase™ together (see Figure 2).

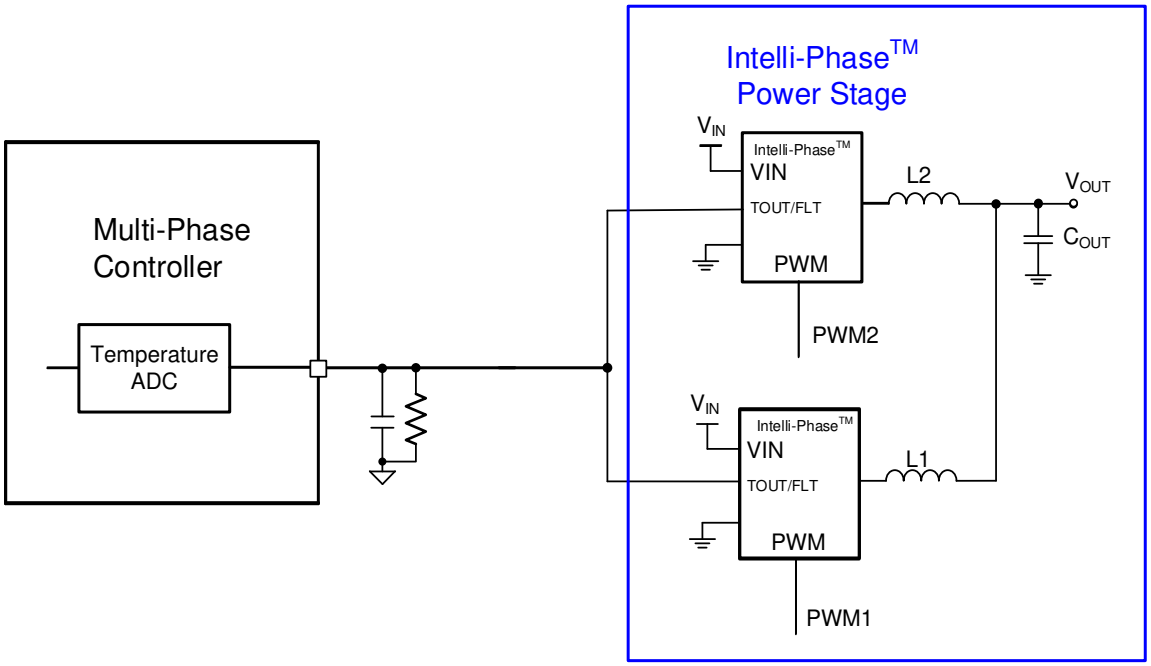


Figure 2: Multi-Phase Temperature-Sense Utilization

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86998.
3. Place as many VIN and PGND vias underneath the package as possible.
4. Place the vias between the VIN or PGND long pads.
5. Place a VIN copper plane on the second inner layer to form the PCB stack as positive/negative/positive, which reduces the parasitic impedance from the input MLCC capacitor to the MP86998. Ensure that the copper plane on the inner layer covers the VIN vias underneath the package, as well as the input MLCC capacitors.
6. Place more PGND vias close to the PGND pin/pad to minimize both thermal resistance and parasitic resistance/impedance.
7. Place the BST capacitor and VDRV capacitor as close to the MP86998's pins as possible.
8. Use a trace width of 20mils or longer to route the path.
9. Avoid placing vias on the BST driving path.
10. Use a 0.1μF to 0.22μF bootstrap capacitor.
11. Place the VDD decoupling capacitor close to the device.
12. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
13. Keep the IOUT signal trace away from high-current paths, such as SW and PWM.

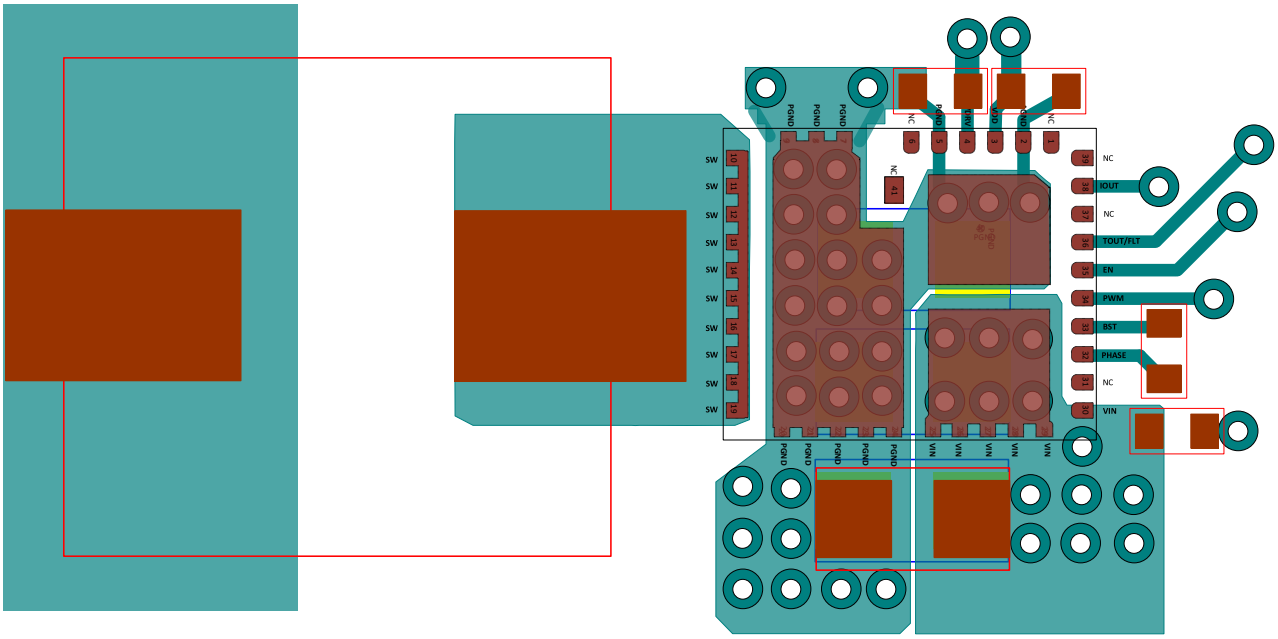


Figure 3: Example of PCB Layout (Placement and Top Layer PCB)

Input Capacitor: 0805 Package (Top and Bottom Sides) and 0402 Package (Top Side)

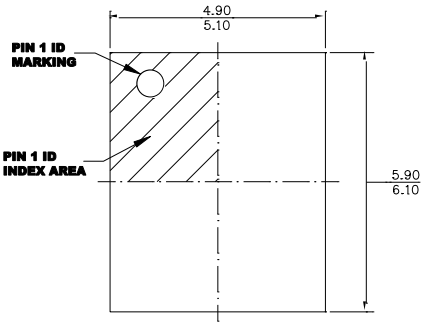
Inductor: 11mmx8mm Package

VDD/BST/VDRV Capacitor: 0402 Package

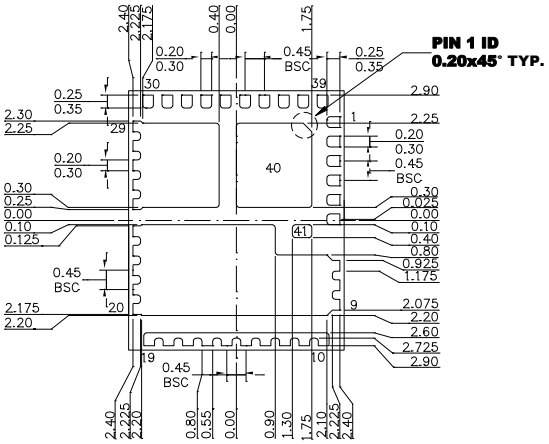
Via Size: 20mils/10mils

PACKAGE INFORMATION

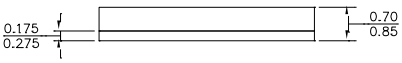
TLGA-41 (5mmx6mm)



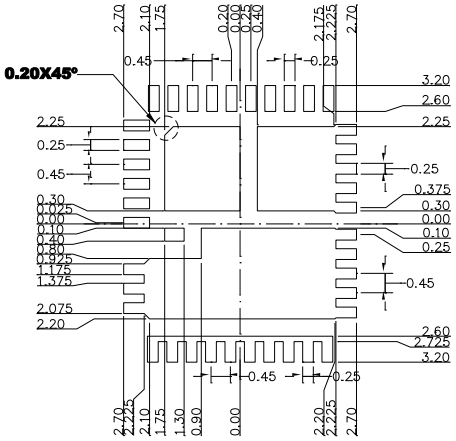
TOP VIEW



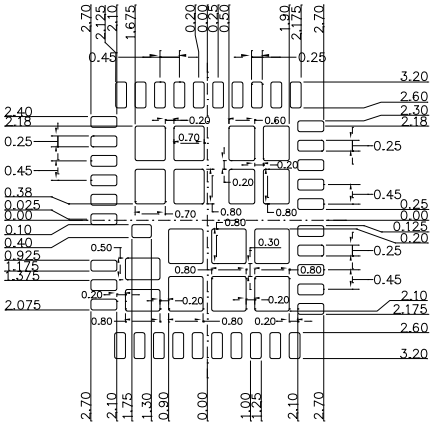
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

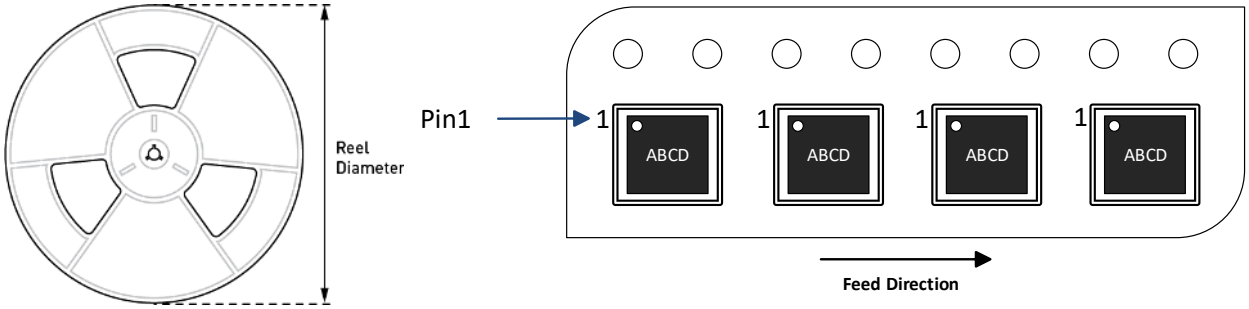


RECOMMENDED STENCIL DESIGN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86998GMJT–Z	TLGA-41 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	11/3/2020	Initial Release	-