

# FDMS8662

## N-Channel PowerTrench® MOSFET

30V, 49A, 2.0mΩ

### Features

- Max  $r_{DS(on)}$  = 2.0mΩ at  $V_{GS} = 10V$ ,  $I_D = 28A$
- Max  $r_{DS(on)}$  = 3.0mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 24A$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- RoHS Compliant

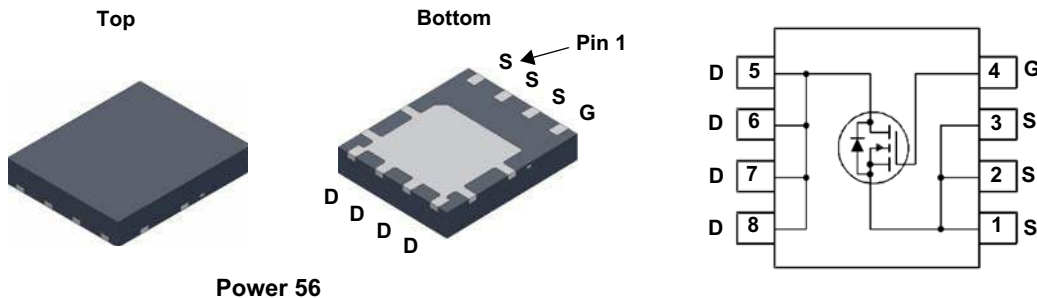


### General Description

The FDMS8662 has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance.

### Applications

- Low Side for Synchronous Buck to Power Core Processor
- Secondary Side Synchronous Rectifier
- Low Side Switch in POL DC/DC Converter
- Oring FET/ Load Switch



Power 56

### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	49	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	159	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	28	
	-Pulsed	200	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	726	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	83	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8662	FDMS8662	Power 56	13"	12mm	3000units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		18		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 28\text{A}$		1.6	2.0	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 24\text{A}$		2.2	3.0	
		$V_{GS} = 10\text{V}, I_D = 28\text{A}, T_J = 125^\circ\text{C}$		2.2	3.0	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{V}, I_D = 28\text{A}$		207		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		4825	6420	pF
$C_{oss}$	Output Capacitance			2365	3145	pF
$C_{rss}$	Reverse Transfer Capacitance			290	435	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		1.1		$\Omega$

**Switching Characteristics**

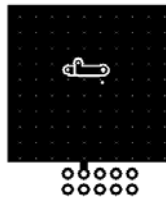
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 28\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		17	31	ns
$t_r$	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			45	72	ns
$t_f$	Fall Time			7	14	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } 10\text{V}$		71	100
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V to } 4.5\text{V}$	$V_{DD} = 15\text{V},$ $I_D = 28\text{A}$	33	47	nC
$Q_{gs}$	Gate to Source Charge			13		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			9		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.1\text{A}$ (Note 3)		0.7	1.2	V
		$V_{GS} = 0\text{V}, I_S = 28\text{A}$		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 28\text{A}, di/dt = 100\text{A}/\mu\text{s}$		55	88	ns
$Q_{rr}$	Reverse Recovery Charge			42	68	nC

## NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



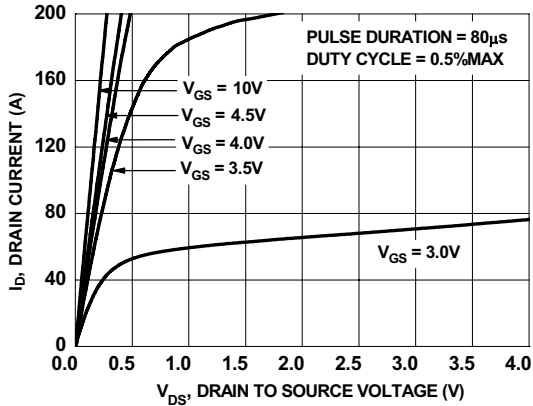
a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.



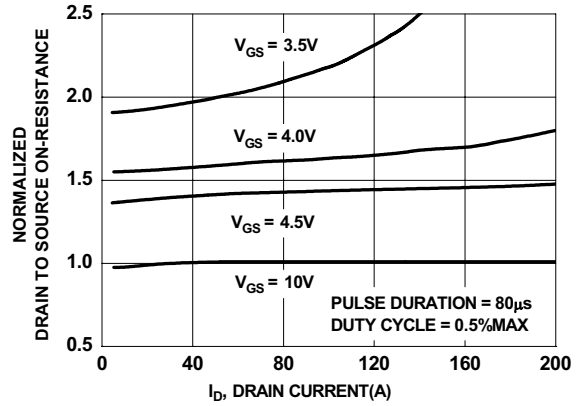
b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 22\text{A}$ ,  $V_{DD} = 30\text{V}$ ,  $V_{GS} = 10\text{V}$ .
- Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

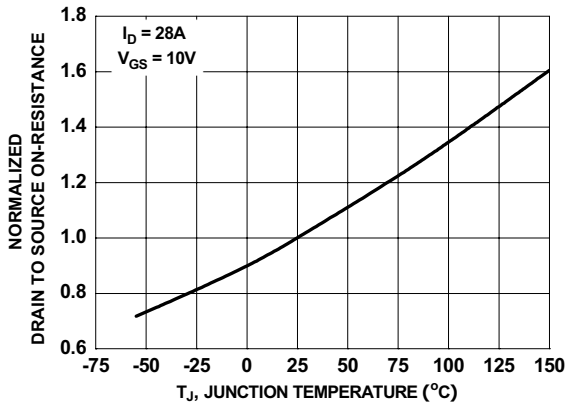
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



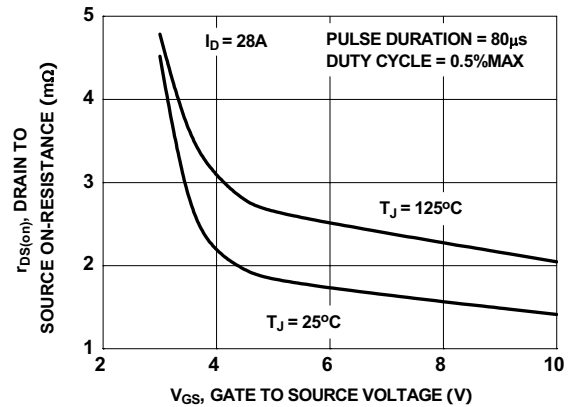
**Figure 1. On-Region Characteristics**



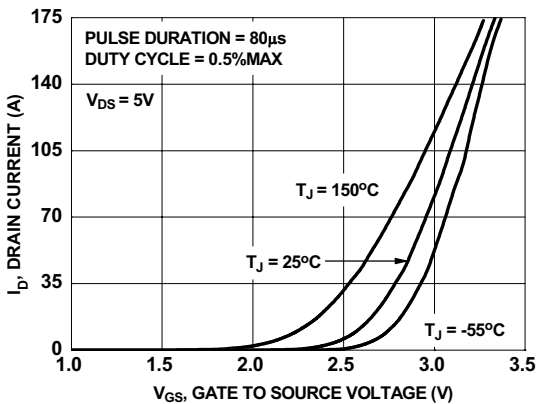
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



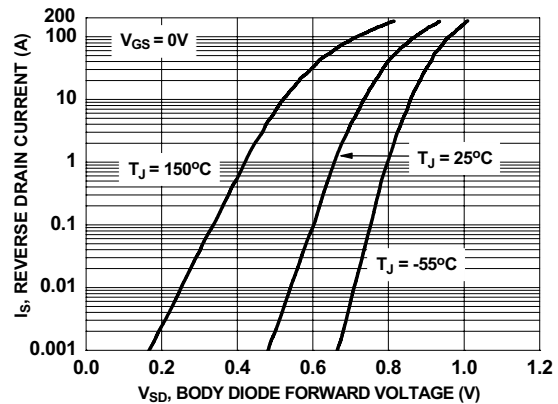
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

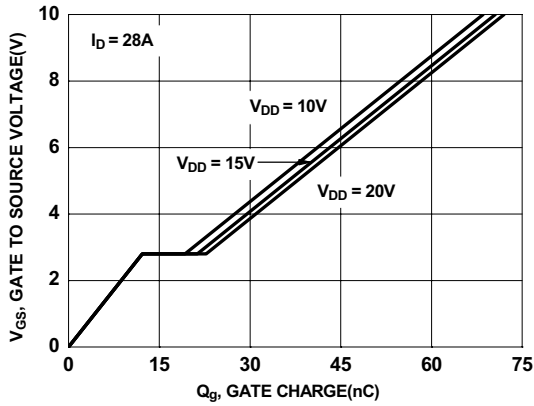


**Figure 5. Transfer Characteristics**

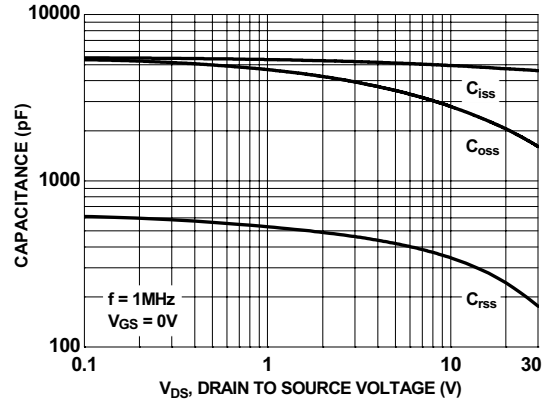


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

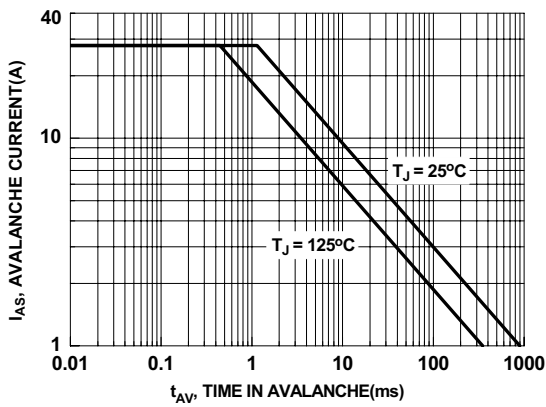
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



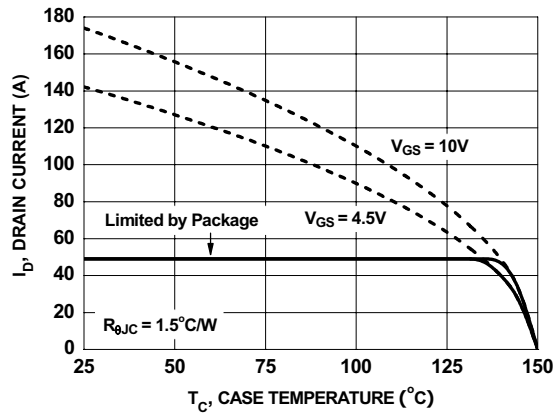
**Figure 7. Gate Charge Characteristics**



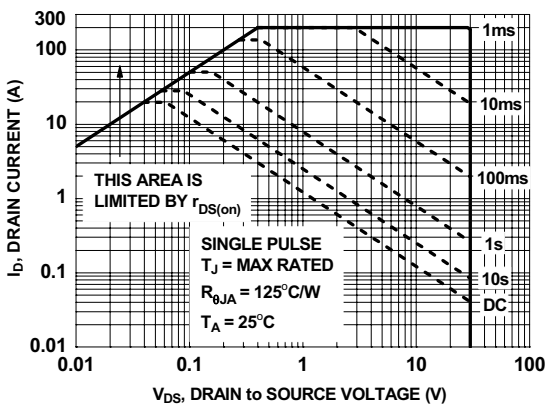
**Figure 8. Capacitance vs Drain to Source Voltage**



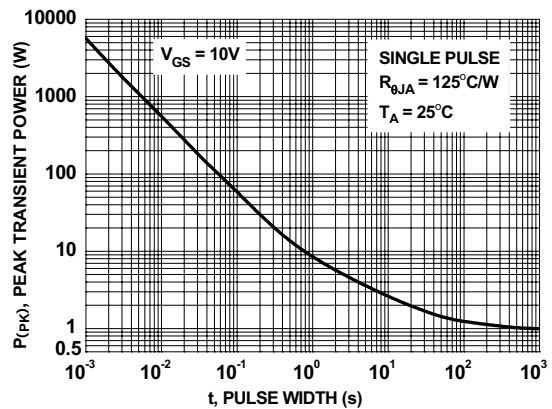
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

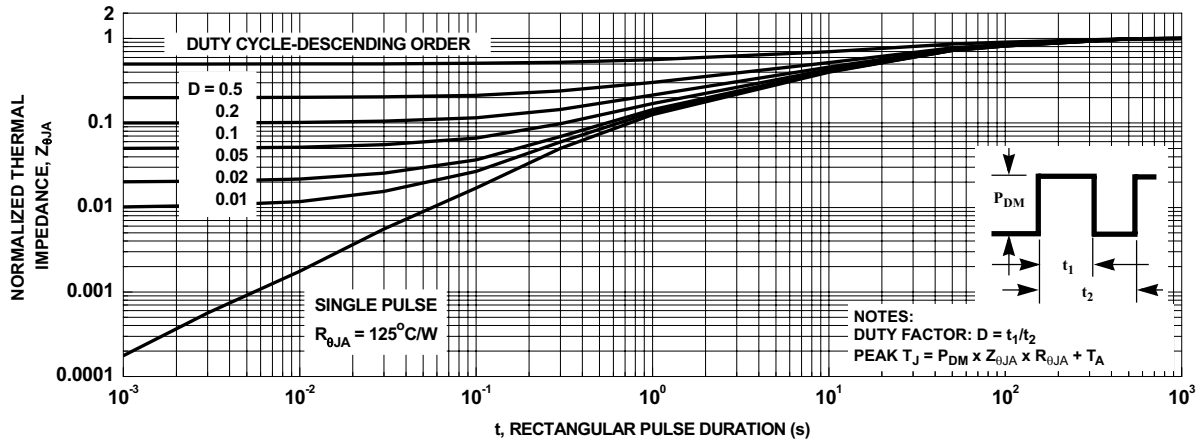


**Figure 11. Forward Bias Safe Operating Area**



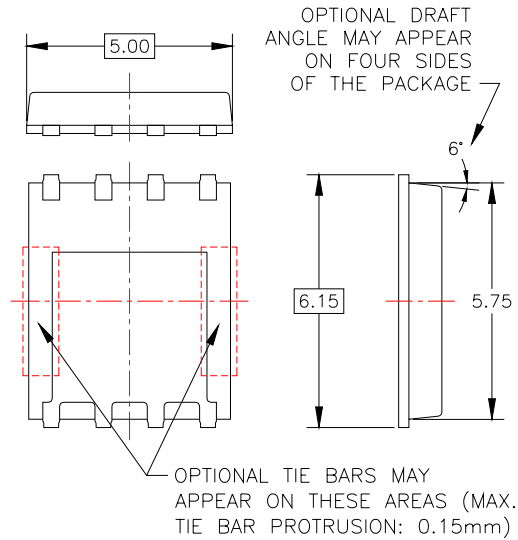
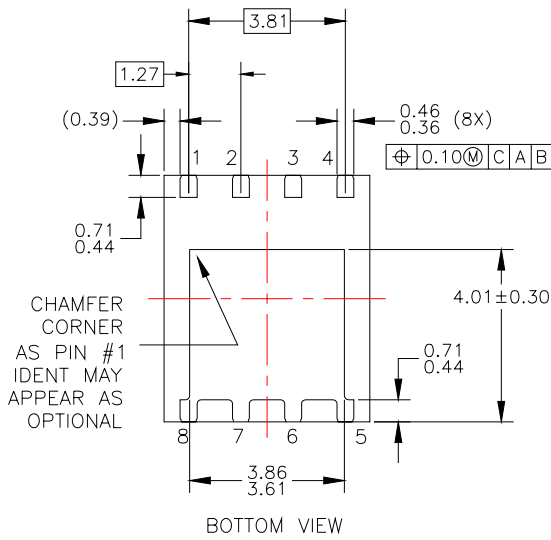
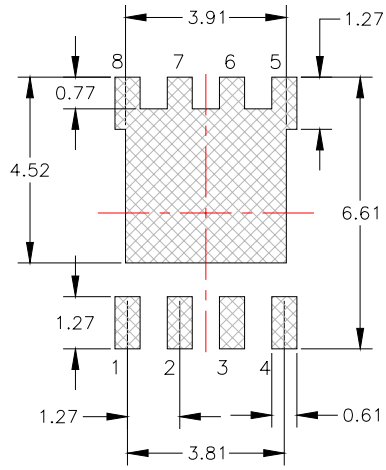
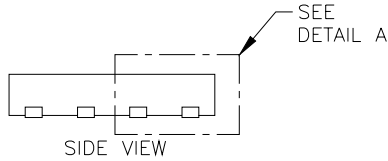
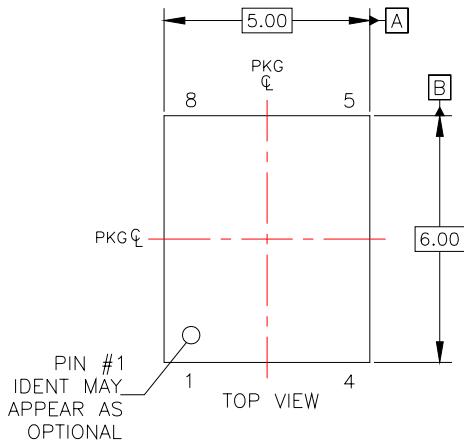
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



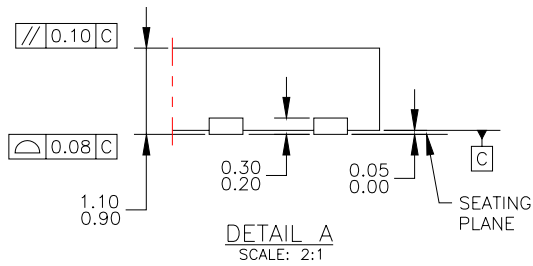
**Figure 13. Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED






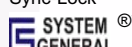
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4





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