Integrated Device Technology, Inc.

# 128K x 64 FLOW THRU ZBT SRAM
# 128K x 64 PIPELINE ZBT SRAM

**ADVANCE INFORMATION**
**IDT7MBV4153**
**IDT7MBV4154**

## FEATURES:

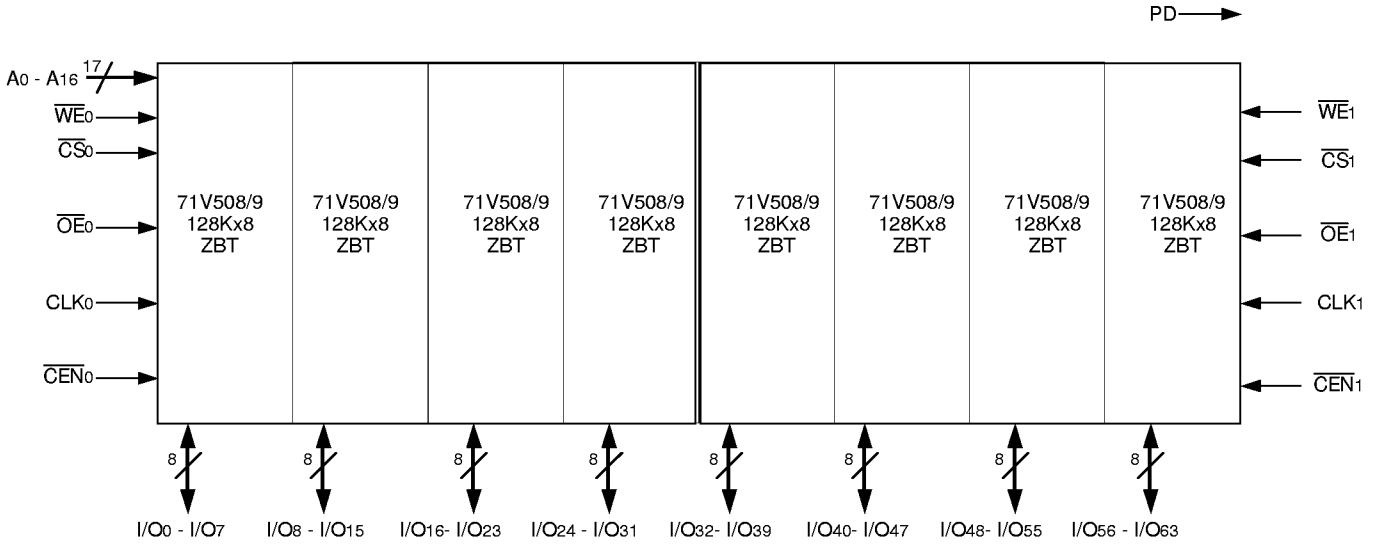
- Low profile 160-lead AMP Free Height Surface Mount Board-to-Board Connector family (5mm-8mm plug options)
- High speed – 50 MHz flow thru, 100 MHz pipeline
- ZBT advantage – no dead cycles between Write and Read Cycles
- Low power deselect mode
- Single 3.3V power supply (±5%)

## DESCRIPTION:

The IDT7MBV4153/54 are ZBT SRAM 3.3V synchronous SRAM modules constructed on an epoxy laminate (FR-4) substrate using 8 static RAMs in plastic ZBT packages and a 160-lead board-to-board connector receptacle. The ZBT SRAM is designed to eliminate dead cycles when turning the bus around between reads and writes, or writes and reads. Thus, it has been given the name ZBT™, or Zero Bus Turn-around.

The 160-lead AMP Free Height Surface Mount Board-to-Board Connector configuration allows 160 leads to be mated to a plug on the board which is 2.80 inches long and 1.50 inches wide. The maximum height (with an 8mm plug) from the base board to the top of the module is 0.535 inches.

## FUNCTIONAL BLOCK DIAGRAM




4261 dwg 01

## MODULE PINOUT

| | | | |
|---|---|---|---|
| $V_{CC}$ | 81 | 1 | $I/O_0$ |
| $I/O_1$ | 82 | 2 | $I/O_2$ |
| $I/O_3$ | 83 | 3 | GND |
| $I/O_5$ | 84 | 4 | $I/O_4$ |
| $V_{CC}$ | 85 | 5 | $I/O_6$ |
| $I/O_7$ | 86 | 6 | NC |
| $I/O_9$ | 87 | 7 | GND |
| $I/O_{11}$ | 88 | 8 | $I/O_8$ |
| $V_{CC}$ | 89 | 9 | $I/O_{10}$ |
| $I/O_{13}$ | 90 | 10 | $I/O_{12}$ |
| $I/O_{15}$ | 91 | 11 | GND |
| NC | 92 | 12 | $I/O_{14}$ |
| $V_{CC}$ | 93 | 13 | $I/O_{16}$ |
| $I/O_{17}$ | 94 | 14 | $I/O_{18}$ |
| $I/O_{19}$ | 95 | 15 | GND |
| $I/O_{21}$ | 96 | 16 | $I/O_{20}$ |
| $V_{CC}$ | 97 | 17 | $I/O_{22}$ |
| $I/O_{23}$ | 98 | 18 | NC |
| $I/O_{25}$ | 99 | 19 | GND |
| $I/O_{27}$ | 99 | 20 | $I/O_{24}$ |
| $V_{CC}$ | 101 | 21 | $I/O_{26}$ |
| $I/O_{29}$ | 102 | 22 | $I/O_{28}$ |
| $I/O_{31}$ | 103 | 23 | GND |
| NC | 104 | 24 | $I/O_{30}$ |
| $V_{CC}$ | 105 | 25 | $\overline{WE_0}$ |
| NC | 106 | 26 | $\overline{WE_1}$ |
| NC | 107 | 27 | GND |
| $\overline{CEN_0}$ | 108 | 28 | $PD_0$ |
| $V_{CC}$ | 109 | 29 | $PD_1$ |
| $\overline{CEN_1}$ | 110 | 30 | $PD_2$ |
| $A_0$ | 111 | 31 | GND |
| $A_2$ | 112 | 32 | $A_1$ |
| $V_{CC}$ | 113 | 33 | $A_3$ |
| $A_4$ | 114 | 34 | $A_5$ |
| $A_6$ | 115 | 35 | GND |
| $V_{CC}$ | 116 | 36 | $A_7$ |
| $A_8$ | 117 | 37 | $A_9$ |
| $A_{10}$ | 118 | 38 | $A_{11}$ |
| GND | 119 | 39 | GND |
| $CLK_0$ | 120 | 40 | $CLK_1$ |
| GND | 121 | 41 | GND |
| $A_{12}$ | 122 | 42 | $A_{13}$ |
| $A_{14}$ | 123 | 43 | GND |
| $V_{CC}$ | 124 | 44 | $A_{15}$ |
| $A_{16}$ | 125 | 45 | $A_{17}$ (1) |
| (1) $A_{18}$ | 126 | 46 | GND |
| (1) $A_{20}$ | 127 | 47 | $A_{19}$ (1) |
| $V_{CC}$ | 128 | 48 | $A_{21}$ (1) |
| (1) $A_{22}$ | 129 | 49 | $\overline{CS_1}$ |
| $\overline{CS_0}$ | 130 | 50 | GND |
| $\overline{OE_0}$ | 131 | 51 | $\overline{OE_1}$ |
| $V_{CC}$ | 132 | 52 | RES (1) |
| (1) RES | 133 | 53 | RES (1) |
| NC | 134 | 54 | GND |
| NC | 135 | 55 | NC |
| $V_{CC}$ | 136 | 56 | NC |
| $I/O_{33}$ | 137 | 57 | $I/O_{32}$ |
| $I/O_{35}$ | 138 | 58 | GND |
| $I/O_{37}$ | 139 | 59 | $I/O_{34}$ |
| $V_{CC}$ | 140 | 50 | $I/O_{36}$ |
| $I/O_{39}$ | 141 | 61 | $I/O_{38}$ |
| NC | 142 | 62 | GND |
| $I/O_{41}$ | 143 | 63 | $I/O_{40}$ |
| $V_{CC}$ | 144 | 64 | $I/O_{42}$ |
| $I/O_{43}$ | 145 | 65 | $I/O_{44}$ |
| $I/O_{45}$ | 146 | 66 | GND |
| $I/O_{47}$ | 147 | 67 | $I/O_{46}$ |
| $V_{CC}$ | 148 | 68 | NC |
| $I/O_{49}$ | 149 | 69 | $I/O_{48}$ |
| $I/O_{51}$ | 150 | 70 | GND |
| $I/O_{53}$ | 151 | 71 | $I/O_{50}$ |
| $V_{CC}$ | 152 | 72 | $I/O_{52}$ |
| $I/O_{55}$ | 153 | 73 | $I/O_{54}$ |
| NC | 154 | 74 | GND |
| $I/O_{57}$ | 155 | 75 | $I/O_{56}$ |
| $V_{CC}$ | 156 | 76 | $I/O_{58}$ |
| $I/O_{59}$ | 157 | 77 | $I/O_{60}$ |
| $I/O_{61}$ | 158 | 78 | GND |
| $I/O_{63}$ | 159 | 79 | $I/O_{62}$ |
| $V_{CC}$ | 160 | 80 | NC |

4261 dwg 02

**TOP VIEW**

**NOTES:**
1. These pins are No Connects; they are reserved for future modules.

## PIN NAMES

| | |
|---|---|
| $A_0 – A_{22}$ | Address Inputs |
| $I/O_0 – I/O_{63}$ | Data Inputs/Outputs |
| $\overline{CS_0}$, $\overline{CS_1}$ | Chip Select Inputs |
| $\overline{OE_0}$, $\overline{OE_1}$ | Data Output Enable Inputs |
| $\overline{WE_0}$, $\overline{WE_1}$ | Write Enable Inputs |
| $CLK_0$ , $CLK_1$ | Clock Inputs |
| $\overline{CEN_0}$, $\overline{CEN_1}$ | Clock Enable Inputs |
| $PD_0$-$PD_2$ | Presence Detect Pins |
| RES | Reserved Pins |
| NC | No Connect |
| GND | Ground |
| $V_{CC}$ | 3.3 Volt Power Supply |

4261 tbl 01

## PRESENCE DETECT TABLE

| $PD_0$ | $PD_1$ | $PD_2$ | |
|---|---|---|---|
| NC | NC | NC | No Module Present |
| GND | NC | $V_{CC}$ | 128Kx64 FT ZBT |
| GND | NC | GND | 128Kx64 PIPE ZBT |

4261 tbl 02

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ for $V_{CC}$ | Terminal Voltage with Respect to GND | –0.5 to +4.6 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –10 to +85 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | °C |
| $I_{OUT}$ | DC Output Current | 50 | mA |

4261 tbl 03

**NOTE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 3.3V –5%/+5% |

4261 tbl 04

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.15 | 3.3 | 3.45 | V |
| GND | Supply Voltage | 0 | 0 | 0.0 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | — | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | –0.5(1) | — | 0.8 | V |

**NOTE:**
1. $V_{IL}$ = –1.0V for pulse width less than $t_{CYC}/2$, once per cycle.

4261 tbl 05

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ($V_{DD}$ = 3.3V ±5%)

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current-Address | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 40 | µA |
| $\|I_{LI}\|$ | Input Leakage Current-Clock, Control | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 20 | µA |
| $\|I_{LI}\|$ | Input Leakage Current-Data | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{OE} \geq V_{IH}$, $V_{OUT}$ = 0V to $V_{DD}$, $V_{DD}$ = Max. | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 5 mA, $V_{DD}$ = Min. | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –5 mA, $V_{DD}$ = Min. | 2.4 | — | V |

4261 tbl 06

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) ($V_{DD}$ = 3.3V ±5%, $V_{HD}$ = $V_{DD}$ - 0.2V, $V_{LD}$ = 0.2V)

| Symbol | Parameter | Test Condition | 7MBV4153 | 7MBV4154 | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Operating Power Supply Current | $\overline{CS} \leq V_{IL}$, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = $f_{MAX}$(2) | 960 | 1760 | mA |
| $I_{SB}$ | Standby Power Supply Current | $\overline{CS} \geq V_{IH}$, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = $f_{MAX}$(2) | 360 | 640 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current | $\overline{CS} \geq V_{HD}$, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2) | 160 | 160 | mA |

**NOTES:**
1. All values are maximum guaranteed values.
2. At f = $f_{MAX}$, address inputs are switching at $1/t_{CYC}$ and CLK is cycling at $1/t_{CYC}$; at f=0, no input signals are changing.

4261 tbl 07

## CAPACITANCE

($T_A$ = +25°C, f = 1.0MHz, SOJ package)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN1}$ | Input Capacitance-Address | $V_{IN}$ = 3dV | 60 | pF |
| $C_{IN2}$ | Input Capacitance-Control, Clock | $V_{in}$ = 3dV | 30 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 10 | pF |

**NOTE:**
1. This parameter is guaranteed by design, but not production tested.

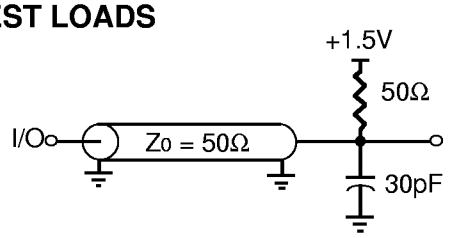
4261 tbl 08

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | 0 to 3V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

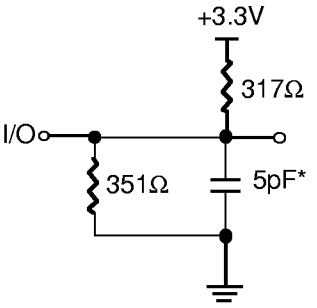
4261 tbl 09

## AC TEST LOADS




4261 dwg 03

**Figure 1. AC Test Load**




4261 dwg 04

**Figure 2. AC Test Load**
**(for $t_{OHZ}$, $t_{CHZ}$, $t_{OLZ}$, and $t_{DC1}$)**

*** Including scope and jig**

## AC ELECTRICAL CHARACTERISTICS(1)

($V_{DD}$ = 3.3V ±5%, $T_A$ = 0 to 70°C)

| Symbol | Parameter | 7MBV4154S100 | | 7MBV4154S80 | | |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Unit |
| **Clock Times** | | | | | | |
| $f_{MAX}$ | Clock Frequency | — | 100 | — | 80 | MHz |
| $t_{CYC}$ | Clock Cycle Time | 10 | — | 12.5 | — | ns |
| $t_{CH}$ | Clock High Pulse Width | 4 | — | 4 | — | ns |
| $t_{CL}$ | Clock Low Pulse Width | 4 | — | 4 | — | ns |
| **Output Times** | | | | | | |
| $t_{CD}$ | Clock High to Valid Data | — | 5 | — | 7 | ns |
| $t_{CDC}$ | Clock High to Data Change | 2 | — | 2 | — | ns |
| $t_{CLZ}$ | Clock High to Output Active | 2 | — | 2 | — | ns |
| $t_{CHZ}$ | Clock High to Data High-Z | 2 | — | 2 | — | ns |
| $t_{OE}$ | Output Enable Access Time | — | 5 | — | 6 | ns |
| $t_{OLZ}$ | Output Enable Low to Data Active | 0 | — | 0 | — | ns |
| $t_{OHZ}$ | Output Enable High to Data High-Z | — | 5 | — | 6 | ns |
| **Set Up Times** | | | | | | |
| $t_{SE}$ | Clock Enable Setup Time | 1.5 | — | 2 | — | ns |
| $t_{SA}$ | Address Setup Time | 1.5 | — | 2 | — | ns |
| $t_{SD}$ | Data In Setup Time | 1.5 | — | 2 | — | ns |
| $t_{SW}$ | Write Enable Setup Time | 1.5 | — | 2 | — | ns |
| $t_{SC}$ | Chip Select Setup Time | 1.5 | — | 2 | — | ns |
| **Hold Times** | | | | | | |
| $t_{HE}$ | Clock Enable Hold Time | 1 | — | 1 | — | ns |
| $t_{HA}$ | Address Hold Time | 2.5 | — | 2.5 | — | ns |
| $t_{HD}$ | Data In Hold Time | 1 | — | 1 | — | ns |
| $t_{HW}$ | Write Enable Hold Time | 1 | — | 1 | — | ns |
| $t_{HC}$ | Chip Select Hold Time | 1 | — | 1 | — | ns |

**NOTES:**

4261 tbl 09

1. Parameters shown reflect component specifications, and they do not necessarily reflect module tester limits.

## AC ELECTRICAL CHARACTERISTICS(1)

($V_{DD}$ = 3.3V ±5%, $T_A$ = 0 to 70°C)

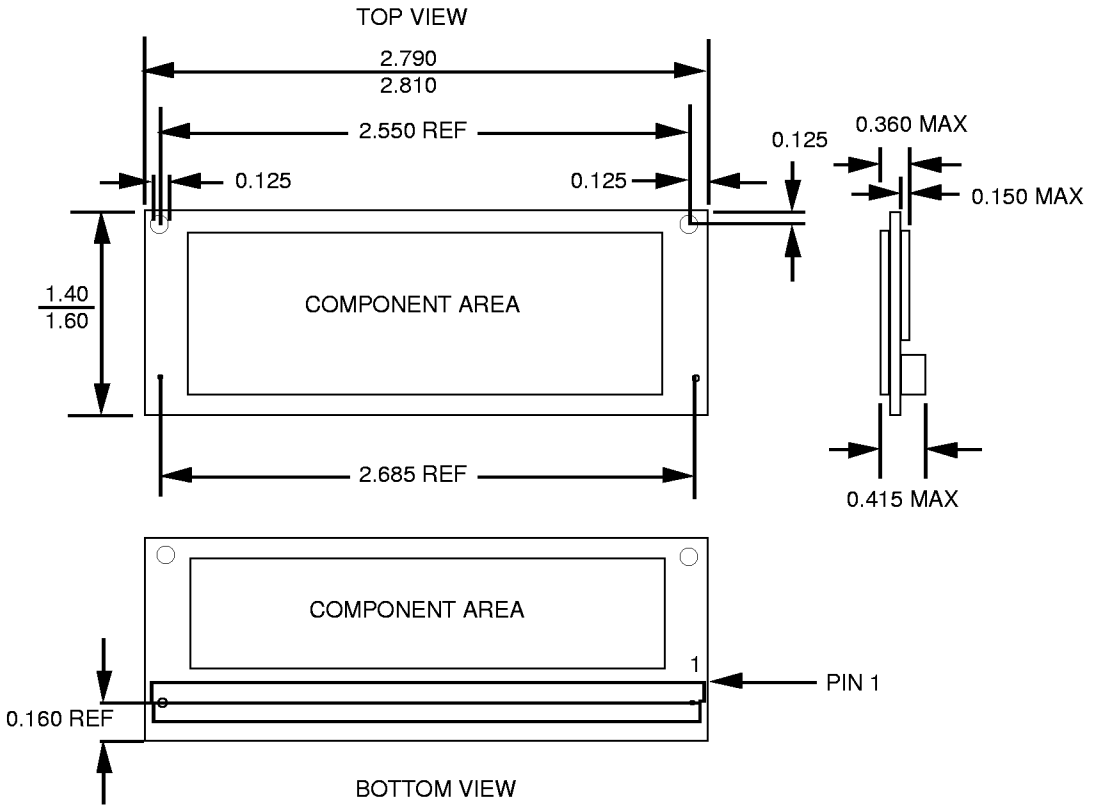
| Symbol | Parameter | IDT7MBV4153S50 | | |
|---|---|---|---|---|
| | | Min. | Max. | Unit |
| **Clock Times** | | | | |
| $f_{MAX}$ | Clock Frequency | — | 50 | MHz |
| $t_{CYC}$ | Clock Cycle Time | 20 | — | ns |
| $t_{CH}$ | Clock High Pulse Width | 6 | — | ns |
| $t_{CL}$ | Clock Low Pulse Width | 6 | — | ns |
| **Output Times** | | | | |
| $t_{CD}$ | Clock High to Valid Data | — | 10 | ns |
| $t_{CDC}$ | Clock High to Data Change | 2 | — | ns |
| $t_{CLZ}$ | Clock High to Output Active | 2 | — | ns |
| $t_{CHZ}$ | Clock High to Data High-Z | 2 | 6 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 7 | ns |
| $t_{OLZ}$ | Output Enable Low to Data Active | 0 | — | ns |
| $t_{OHZ}$ | Output Enable High to Data High-Z | — | 6 | ns |
| **Set Up Times** | | | | |
| $t_{SE}$ | Clock Enable Setup Time | 2.5 | — | ns |
| $t_{SA}$ | Address Setup Time | 2.5 | — | ns |
| $t_{SD}$ | Data In Setup Time | 2.5 | — | ns |
| $t_{SW}$ | Write Enable Setup Time | 2.5 | — | ns |
| $t_{SC}$ | Chip Select Setup Time | 2.5 | — | ns |
| **Hold Times** | | | | |
| $t_{HE}$ | Clock Enable Hold Time | 1 | — | ns |
| $t_{HA}$ | Address Hold Time | 2.5 | — | ns |
| $t_{HD}$ | Data In Hold Time | 1 | — | ns |
| $t_{HW}$ | Write Enable Hold Time | 1 | — | ns |
| $t_{HC}$ | Chip Select Hold Time | 1 | — | ns |

**NOTES:**

4261 tbl 10

1. Parameters shown reflect component specifications, and they do not necessarily reflect module tester limits.

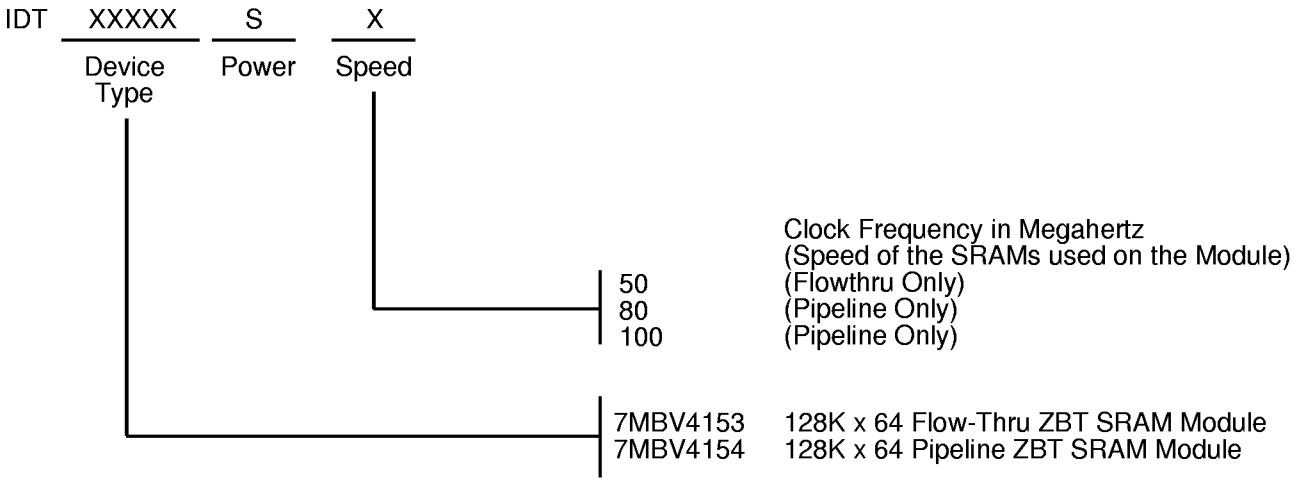
## PACKAGE DRAWING




4261 dwg 05

**NOTES:**
1. Specified dimension are in inches.
2. The receptable used on the module is AMP part number 177983-8..

## ORDERING INFORMATION




4261 dwg 06



Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (800) 544-SRAM FAX: (408) 754-4547