TPS65154 LCD Bias IC with Integrated WLED Driver

1 Device Overview

1.1 Features

- 2.0 V to 5.5 V Input Voltage Range
- Synchronous Boost Converter (AV_{DD})
- Non-Synchronous Boost Converter (V_{GH})
- Low Dropout Linear Regulator (V_{CC})
- Programmable V_{COM} Calibrator with Integrated Buffer Amplifier
- 6-Channel WLED Driver with Direct Dimming and Phase-Shift Dimming Modes
- Gate Voltage Shaping
- Panel Reset Signal ($\overline{XAO}$)
- T-CON Reset Signal ($\overline{RST}$)
- On-Chip EEPROM with Write Protect
- I^2C Interface
- Thermal Shutdown
- 48-Pin, 6 mm × 6 mm, 0.4 mm Pitch VQFN

1.2 Applications

- Notebook PCs
- Tablet PCs

1.3 Description

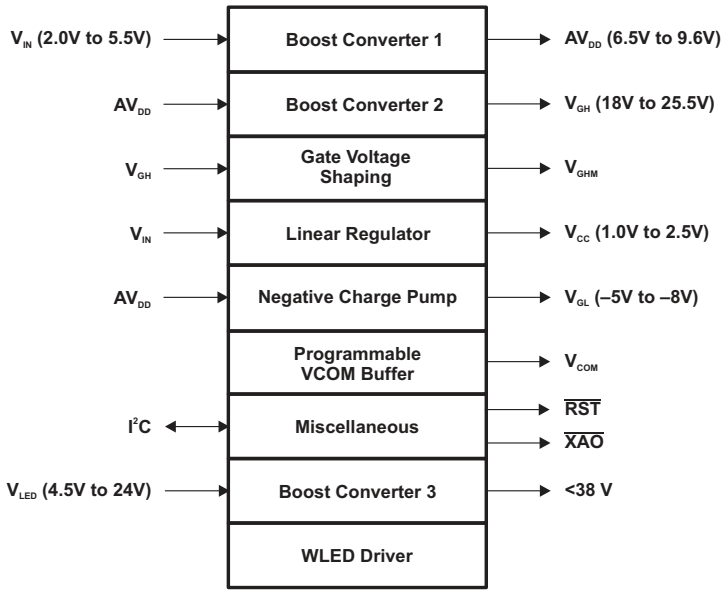
The TPS65154 is a compact LCD bias solution primarily intended for use in Notebook and Tablet PCs. The device comprises two boost converters to supply the LCD panel's source driver and gate driver; a linear regulator to supply the system's logic voltage; a programmable V_{COM} with high-speed amplifier; and a gate voltage shaping function; and a 6-channel WLED driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65154	VQFN (48)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data manual.

1.4 Simplified System Diagram



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2 Revision History

Changes from Original (September 2013) to Revision A	Page
• Changed from data sheet to data manual format	1
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

3 Pin Configuration and Functions

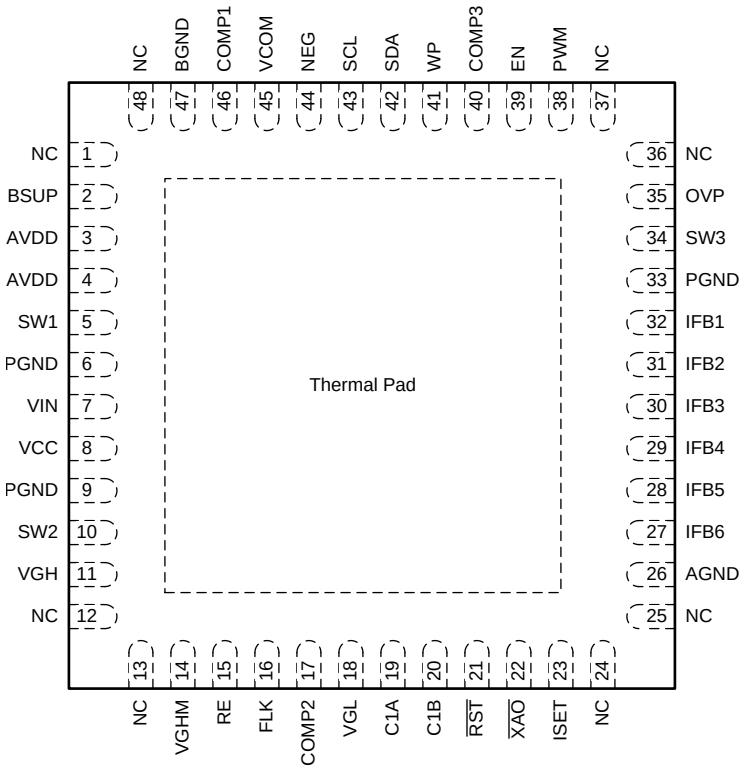


Figure 3-1. RSL Package, 48-Pin VQFN (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1	N/A	No internal connection.
BSUP	2	P	Positive supply for the VCOM buffer.
AVDD	3	P	Boost converter 1 output voltage sense.
AVDD	4	P	Boost converter 1 rectifier output.
SW1	5	P	Boost converter 1 switch pin.
PGND	6	P	Ground.
VIN	7	P	Positive supply.
VCC	8	P	Linear regulator output.
PGND	9	P	Ground.
SW2	10	P	Boost converter 2 switch pin.
VGH	11	P	V_{GH} regulation point and positive supply for gate voltage shaping function.
NC	12	N/A	No internal connection.
NC	13	N/A	No internal connection.
VGHM	14	P	Gate voltage shaping output.
RE	15	I/O	Gate votlage shaping discharge resistor connection.
FLK	16	I/O	Gate votlage shaping flicker clock input.
COMP2	17	I/O	Internal linear regulator compensation network connection.
VGL	18	P	Negative charge pump output and V_{GL} regulation point.
C1A	19	P	Negative charge pump flying capacitor connection.
C1B	20	P	Negative charge pump flying ccapacitor connection.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{RST}$	21	I/O	Reset generator output.
$\overline{XAO}$	22	I/O	Panel discharge generator output.
ISET	23	I/O	WLED driver current-setting resistor connection.
NC	24	N/A	No internal connection.
NC	25	N/A	No internal connection.
AGND	26	P	Ground.
IFB6	27	I/O	WLED driver channel 6 output.
IFB5	28	I/O	WLED driver channel 5 output.
IFB4	29	I/O	WLED driver channel 4 output.
IFB3	30	I/O	WLED driver channel 3 output.
IFB2	31	I/O	WLED driver channel 2 output.
IFB1	32	I/O	WLED driver channel 1 output.
PGND	33	P	Ground.
SW3	34	P	WLED driver boost converter switch pin.
OVP	35	I/O	WLED driver boost converter output voltage sensing pin.
NC	36	N/A	No internal connection.
NC	37	N/A	No internal connection.
PWM	38	I/O	WLED driver PWM input.
EN	39	I/O	WLED driver enable input.
COMP3	40	I/O	WLED driver boost converter compensation network connection.
WP	41	I/O	EEPROM write protect input.
SDA	42	I/O	I^2C data.
SCL	43	I/O	I^2C clock.
NEG	44	I/O	VCOM buffer inverting input.
VCOM	45	I/O	VCOM buffer output.
COMP1	46	I/O	Boost converter 1 compensation network connection.
BGND	47	P	Ground.
NC	48	N/A	No internal connection.
GND	Pad	P	Ground.

4 Specifications

4.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage	VIN, VCC, SCL, SDA, FLK, WP, $\overline{XAO}$, COMP1	–0.3	7	V
	AVDD, SW1, VCOM, NEG, BSUP, $\overline{RST}$	–0.3	12	V
	EN, PWM	–0.3	20	V
	COMP2, COMP3, ISET	–0.3	3.6	V
	C1A, C1B	–10	12	V
	VGL	–10	0.3	V
	SW3, OVP	–0.3	40	V
	IFB1, IFB2, IFB3, IFB4, IFB5, IFB6, VGH, VGHM, RE, SW2	–0.3	30	V
Pin current	SW2		TBD	A
Ambient temperature, T_A		–40	85	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	Normal operation	2.0		5.5	V
		EEPROM programming	2.6		5.5	
dV_{IN}/dt	V_{IN} rise time		0.45		11	ms
V_{BSUP}	Input voltage range		6.5		9.6	V
V_{BAT}	Input voltage range		4.5		24	V
dV_{BAT}/dt	V_{BAT} rise time		0.45		11	ms
LINEAR REGULATOR (V_{CC})						
V_{CC}	Output voltage		1.0		2.5	V
I_{ICC}	Output current				300	mA
C_{OUT}	Output capacitance		4.7	10	22	µF
BOOST CONVERTER 1 (AV_{DD})						
AV_{DD}	Boost converter 1 output voltage range		6.5		9.6	V
IAV_{DD}	Boost converter 1 output current at V_{IN} = 3.7 V				400	mA
L	Inductance		4.7	10	15	µH
C_{OUT}	Boost converter 1 output capacitance		4.7	10	22	µF
BOOST CONVERTER 2 (V_{GH})						
AV_{DD}	Input voltage range		6.5		9.6	V
V_{GH}	Output voltage range		18		25.5	V
I_{GH}	Output current				25	mA

Recommended Operating Conditions *(continued)*

		MIN	NOM	MAX	UNIT
L	Inductance	4.7	10	15	µH
C_{OUT}	Output capacitance	1	4.7	10	µF
NEGATIVE CHARGE PUMP (V_{GL})					
V_{GL}	Output voltage	–5		–8	V
I_{GL}	Output current			25	mA
C_{FLY}	Flying capacitance		0.5		µF
C_{OUT}	Output capacitance	0.5		5	µF
BOOST CONVERTER 3 (WLED)					
V_{OUT}	Output voltage			38	V
I_{OUT}	Output current			250	mA
L	Inductance	4.7	10	15	µH
C_{OUT}	Output capacitance	2.2	4.7	10	µF
INTERNAL REGULATOR					
C_{OUT}	Capacitance connected to the TCOMP pin	1			µF

4.4 Thermal Information

THERMAL METRIC[1]		TPS65154 RSL (VQFN) 48 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Electrical Characteristics

V_{IN} = 3.3 V, V_{LED} = 12 V, V_{CC} = 2.5 V, AV_{DD} = 8 V, V_{GL} = –6.8 V, V_{GH} = 20 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{IN}	Supply current into VIN pin	Converters not switching			0.1	1	mA
I_{AVDD}	Supply current into AVDD pins	Pins 2 and 3 connected together			0.75	2.5	mA
I_{BSUP}	Supply current into BSUP pin				2.5	5	mA
I_{GH}	Supply current into VGH pin	No load on VGHM			0.1	1	mA
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		1.75			V
		V_{IN} rising				2.2	
	Hysteresis			90			mV
LINEAR REGULATOR (V_{CC})							
V_{CC}	Linear regulator output voltage range			1.0		2.5	V
	Tolerance	I_{CC} = 10 mA		–3%		+3%	
V_{UVP}	Undervoltage protection threshold	V_{CC} falling		60%	70%	75%	
V_{SCP}	Short circuit protection threshold	V_{CC} falling		25%	30%	40%	
I_{LIM}	Current limit	V_{CC} = 5% below value at 10 mA.	T_J = 25°C to 125°C	300			mA
			T_J = –40°C	250			
$r_{DS(ON)}$	Active pull-down resistance			10	21	35	Ω
BOOST CONVERTER 1 (AV_{DD})							
AV_{DD}	Output voltage range			6.5		9.6	V
	Tolerance			–2%		+2%	
V_{UVP}	Undervoltage protection threshold			60%	70%	75%	
V_{SCP}	Short-circuit protection threshold			25%	30%	35%	
$r_{DS(ON)}$	Switch ON resistance	I_{SW} = 1 A			0.1	0.25	Ω
I_{LIM}	Switch current limit			2.4	3.0	3.6	A
$r_{DS(ON)}$	Rectifier ON resistance	I_{SW} = 1 A			0.25	0.4	Ω
f_{SW}	Switching frequency			400		1000	kHz
	Tolerance			–20%		+20%	
NEGATIVE CHARGE PUMP (V_{GL})							
V_{GL}	Output voltage range			–5		–8	V
	Output voltage tolerance			–3%		3.5%	
V_{UVP}	Undervoltage protection threshold	V_{GL} rising		65%	70%	75%	
V_{SCP}	Short-circuit protection threshold	V_{GL} rising		25%	30%	35%	
I_{DRVN}	Maximum drive current	C1B sinking		50		150	mA
		C1B sourcing		60		160	
V_{DO}	Dropout voltage	f_{SW} = 500 kHz, C_{FLY} = 0.5 µF, I_{GL} = 10 mA			0.6	1.0	V
f_{SW}	Switching frequency			400	500	600	kHz
$r_{DS(ON)}$	Discharge ON resistance	I_{MEAS} = 2 mA		2.1	3	3.9	kΩ
BOOST CONVERTER 2 (V_{GH})							
V_{GH}	Output voltage range			18		25.5	V
	Tolerance			–3%		3%	
V_{UVP}	Undervoltage protection threshold	V_{GH} falling		65%	70%	75%	
V_{SCP}	Short-circuit protection threshold	V_{GH} falling		25%	30%	35%	
$r_{DS(ON)}$	Switch ON resistance	I_{SW} = 1 A			0.3	1.0	Ω
$t_{ON(MAX)}$	Maximum t_{ON} time			1	2	2.5	µs
t_{OFF}	t_{OFF} time			2	2.7	4	µs
BOOST CONVERTER 3							
V_{OUT}	Output voltage range			V_{LED}+2		38	V
I_{LIM}	Switch current limit			2.0	2.7	3.7	A
$r_{DS(ON)}$	Switch ON resistance	I_{SW} = 1 A			0.2	0.35	Ω

Electrical Characteristics *(continued)*

V_{IN} = 3.3 V, V_{LED} = 12 V, V_{CC} = 2.5 V, AV_{DD} = 8 V, V_{GL} = –6.8 V, V_{GH} = 20 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OVP}	OVP range			30		39	V
	Tolerance			-5%		+5%	
V_{IL}	EN low input voltage	EN falling				0.6	V
V_{IH}	EN high input voltage	EN rising		1.5			V
$V_{IH} – V_{IL}$	EN input hysteresis			0.09	0.16	0.27	V
$R_{PULL-DOWN}$	EN pull-down resistance			450	750	1250	kΩ
WLED DIMMING							
I_{FB}	Maximum current			40			mA
	Channel-to-channel current matching			–3%		+3%	
	Output dimming resolution				10		bits
D_{MIN}	Minimum output duty cycle					1%	
D_{HYS}	Input PWM jitter hysteresis			–0.048 %		0.048 %	
V_{SET}	ISET regulation voltage			–3%	1.0	+3%	V
K_{SET}	ISET multiplication constant			1260	1296	1332	
V_{IL}	PWM low input voltage	PWM falling				0.6	V
V_{IH}	PWM high input voltage	PWM rising		1.2			V
$V_{IH} – V_{IL}$	PWM input voltage hysteresis			0.09	0.16	0.27	V
$R_{PULL-DOWN}$	PWM pull-down resistance			450	750	1250	kΩ
RESET ($\overline{RST}$)							
V_{OL}	Output voltage	$I_{\overline{RST}}$ = 1 mA (sinking)			0.2	0.5	V
I_{OH}	Leakage current	$V_{\overline{RST}}$ = 1.8 V				1	µA
PROGRAMMABLE VCOM							
SET_{ZSE}	VCOM DAC set zero-scale error	V_{MIN} = 07h, V_{MAX} = 07h		−7		7	LSB
	VMAX DAC set zero-scale error			–1		1	
	VMIN DAC set zero-scale error			–1		1	
SET_{FSE}	VCOM set full-scale error	V_{MIN} = 07h, V_{MAX} = 07h		−7		7	LSB
	VMAX set full-scale error			–1		1	
	VMIN set full-scale error			−1		1	
DNL	Differential nonlinearity	V_{COM}				1	LSB
		V_{MAX}				1	
		V_{MIN}				1	
BW	Small-signal bandwidth	Closed-loop; A_V = –1; R_F = 1 kΩ, R_{IN} = 1 kΩ, V_{CM} = 4 V; V_{SIGNAL} = 63 mV_{pp}; R_L = ∞			21		MHz
I_{OUT}	Peak output current	Open-loop; V_{POS} = 4 V, V_{NEG} = 3 V			400		mA
		Open-loop; V_{POS} = 4 V, V_{NEG} = –5 V			330		
SR	Slew rate	Open-loop; V_{POS} = 4 V, V_{NEG} = 5 V			36		V/µs
		Open-loop; V_{POS} = 4 V, V_{NEG} = 3 V			33		
$I_{IB–}$	Input bias current (inverting input)	Closed-loop; A_V = +1; R_F = 1 MΩ; V_{POS} = 4 V		−1		1	µA
V_{DROP}	Output voltage drop	Open-loop; V_{POS} = 4 V; I_{MEAS} = 10 mA	V_{NEG} = 3 V		0.06	0.1	V
			V_{NEG} = 5 V		0.03	0.1	
GATE VOLTAGE SHAPING							
$r_{DS(ON)H}$	VGH to VGHM ON resistance	V_{GH} = 20 V, I_{GHM} = 10 mA, V_{FLK} = 1.8 V			13	25	Ω
$r_{DS(ON)L}$	VGHM to RE ON resistance	V_{GHM} = 20 V, I_{GHM} = 10 mA, V_{FLK} = 0 V			26	50	Ω
		V_{GHM} = 6 V, I_{GHM} = 10 mA, V_{FLK} = 0 V			26	50	
V_{IL}	FLK low input voltage threshold	V_{FLK} falling		0.6			V
V_{IH}	FLK high input voltage threshold	V_{FLK} rising				1.2	V
$V_{IH} – V_{IL}$	FLK input hysteresis			0.09	0.15	0.27	V

Electrical Characteristics *(continued)*

V_{IN} = 3.3 V, V_{LED} = 12 V, V_{CC} = 2.5 V, AV_{DD} = 8 V, V_{GL} = –6.8 V, V_{GH} = 20 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	FLK low input current	V_{FLK} = 0 V	–100		100	nA
I_{IH}	FLK high input current	V_{FLK} = 1.8 V	–100		100	nA
PANEL RESET ($\overline{XAO}$)						
$V_{OL(\overline{XAO})}$	Output voltage	$I_{\overline{XAO}}$ = 1 mA (sinking)		0.16	0.5	V
$I_{LK(\overline{XAO})}$	Leakage current	$V_{\overline{XAO}}$ = 1.8 V			1	µA
V_{DET}	$\overline{XAO}$ Threshold voltage range	V_{IN} falling	V_{UVLO}		3.0	V
	Tolerance		–3%		+3%	
	Hysteresis	V_{IN} rising	0.05		0.3	V
I²C INTERFACE						
ADDR	Configuration parameters slave address			74h		
	Programmable VCOM slave address			28h		
V_{IL}	Low level input voltage	SCL or SDA falling, standard and fast modes			0.6	V
V_{IH}	High level input voltage	SCL or SDA rising, standard and fast modes	1.0			V
$V_{IH} – V_{IL}$	Input hysteresis		0.05			V
V_{OL}	Low level output voltage	Sinking 3 mA			0.36	V
C_I	Input capacitance				10	pF
C_B	Capacitive load on SDA and SCL	Standard mode			400	pF
		Fast mode			400	
EEPROM						
V_{IL}	WP low input voltage threshold	V_{WP} falling	0.8			V
V_{IH}	WP high input voltage threshold	V_{WP} rising			1.2	V
$V_{IH} – V_{IL}$	WP input voltage hysteresis		0.03	0.05	0.1	V
$R_{PULL-UP}$	WP internal pull-up resistor		20	60	100	kΩ
N_{WRITE}	Number of write cycles		1000			
	Data retention	Storage temperature = 150 °C	100			1000 hrs
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			150		°C
	Thermal shutdown hysteresis			10		

4.6 Timing Requirements

V_{IN} = 3.3 V, V_{LED} = 12 V, V_{CC} = 2.5 V, AV_{DD} = 8 V, V_{GL} = –6.8 V, V_{GH} = 20 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

		MIN	TYP	MAX	UNIT
LINEAR REGULATOR (V_{CC})					
t_{DLY1}	Linear regulator start-up delay time	0		75	ms
	Tolerance	–20%		30%	
BOOST CONVERTER 1 (AV_{DD})					
t_{SS2}	Boost converter 1 soft-start duration range	0.5		75	ms
	Tolerance	–20%		30%	
t_{DLY2}	Boost converter 1 start-up delay range	0		75	ms
	Tolerance	–20%		30%	
NEGATIVE CHARGE PUMP (V_{GL})					
t_{SS3}	Negative charge pump soft-start duration	0		35	ms
	Tolerance	–20%		30%	
t_{DLY3}	Negative charge pump start-up delay	0		35	ms
	Tolerance	–20%		30%	
BOOST CONVERTER 2 (V_{GH})					

Timing Requirements *(continued)*

V_{IN} = 3.3 V, V_{LED} = 12 V, V_{CC} = 2.5 V, AV_{DD} = 8 V, V_{GL} = –6.8 V, V_{GH} = 20 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

			MIN	TYP	MAX	UNIT
t_{SS4}	Boost converter 2 soft-start duration range		0		35	ms
	Tolerance		–20%		30%	
BOOST CONVERTER 3						
f_{SW}	Switching frequency range		400		1000	kHz
	Tolerance		–20%		20%	
WLED DIMMING						
t_{PWMIN}	Input pulse width		500			ns
f_{OUT}	Output frequency range	Direct dimming	0.1		15	kHz
		DPWM dimming	15		22	
	Tolerance		–20%		20%	
f_{IN}	Input frequency range	PWM and direct dimming modes	0.1		15	kHz
RESET ($\overline{RST}$)						
t_{RST}	Reset pulse duration range		0		15	ms
	Tolerance	Measured from end of V_{CC}'s ramp to 50% of $\overline{RST}$'s rising edge with a 10 kΩ pull-up resistor.	–20%		20%	
GATE VOLTAGE SHAPING						
t_{PLH}	Propagation delay	V_{GHM} rising, V_{FLK} = 0 V/1.8 V, 50% thresholds, C_{VGHM} = 150 pF, R_E = 0 Ω		92	200	ns
t_{PHL}		V_{GHM} falling, V_{FLK} =0 V/1.8 V, 50% thresholds, C_{VGHM} = 150 pF, R_E = 0 Ω		88	200	
t_{DLY4}	Gate voltage shaping start-up delay range		0		35	ms
	Tolerance		–20%		30%	
PANEL RESET ($\overline{XAO}$)						
t_{DLY6}	Panel reset duration range		0		35	ms
	Tolerance	Measured from V_{IN} = V_{DET} to 50% of $\overline{XAO}$'s rising edge with a 10-kΩ pull-up resistor.	–20%		30%	
TIMING						
t_{UVP}	Undervoltage protection timeout		40	50	60	ms
I^2C INTERFACE						
f_{SCL}	Clock frequency	Standard mode			100	kHz
		Fast mode			400	
t_{LOW}	Clock low period	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HIGH}	Clock high period	Standard mode	4.0			µs
		Fast mode	0.6			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
$t_{hd:STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	0.6			
$t_{su:STA}$	Set-up time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	0.6			
$t_{su:DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
$t_{hd:DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	

Timing Requirements *(continued)*

V_{IN} = 3.3 V, V_{LED} = 12 V, V_{CC} = 2.5 V, AV_{DD} = 8 V, V_{GL} = –6.8 V, V_{GH} = 20 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

			MIN	TYP	MAX	UNIT
t_{RCL1}	Rise time of SCL after a repeated START condition and after an ACK bit	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		1000	
t_{RCL}	Rise time of SCL	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		300	
t_{FCL}	Fall time of SCL	Standard mode	$20+0.1C_B$		300	ns
		Fast mode	$20+0.1C_B$		300	
t_{RDA}	Rise time of SDA	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		300	
t_{FDA}	Fall time of SDA	Standard mode	$20+0.1C_B$		300	ns
		Fast mode	$20+0.1C_B$		300	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
EEPROM						
t_{WRITE}	Write time				100	ms

5 Detailed Description

5.1 Overview

The TPS65154 device integrates the bias and backlight functions needed by an active matrix liquid crystal display.

The LCD bias functions comprise

- A synchronous boost converter to generate AV_{DD}
- A non-synchronous boost converter to generate V_{GH}
- An inverting charge pump to generate V_{GL}
- An low dropout linear regulator to generate V_{CC}
- A gate-voltage shaping function
- A programmable VCOM buffer
- $\overline{XAO}$ and $\overline{RST}$ signals
- An I^2C programming interface

The backlight driver functions comprise

- A non-synchronous boost converter
- A six-channel WLED driver with PWM dimming

The device configuration is stored in an on-chip nonvolatile memory, which can be programmed via an I^2C interface.

5.2 Functional Block Diagram

Figure 5-1 shows a top-level block diagram of the TPS65154.

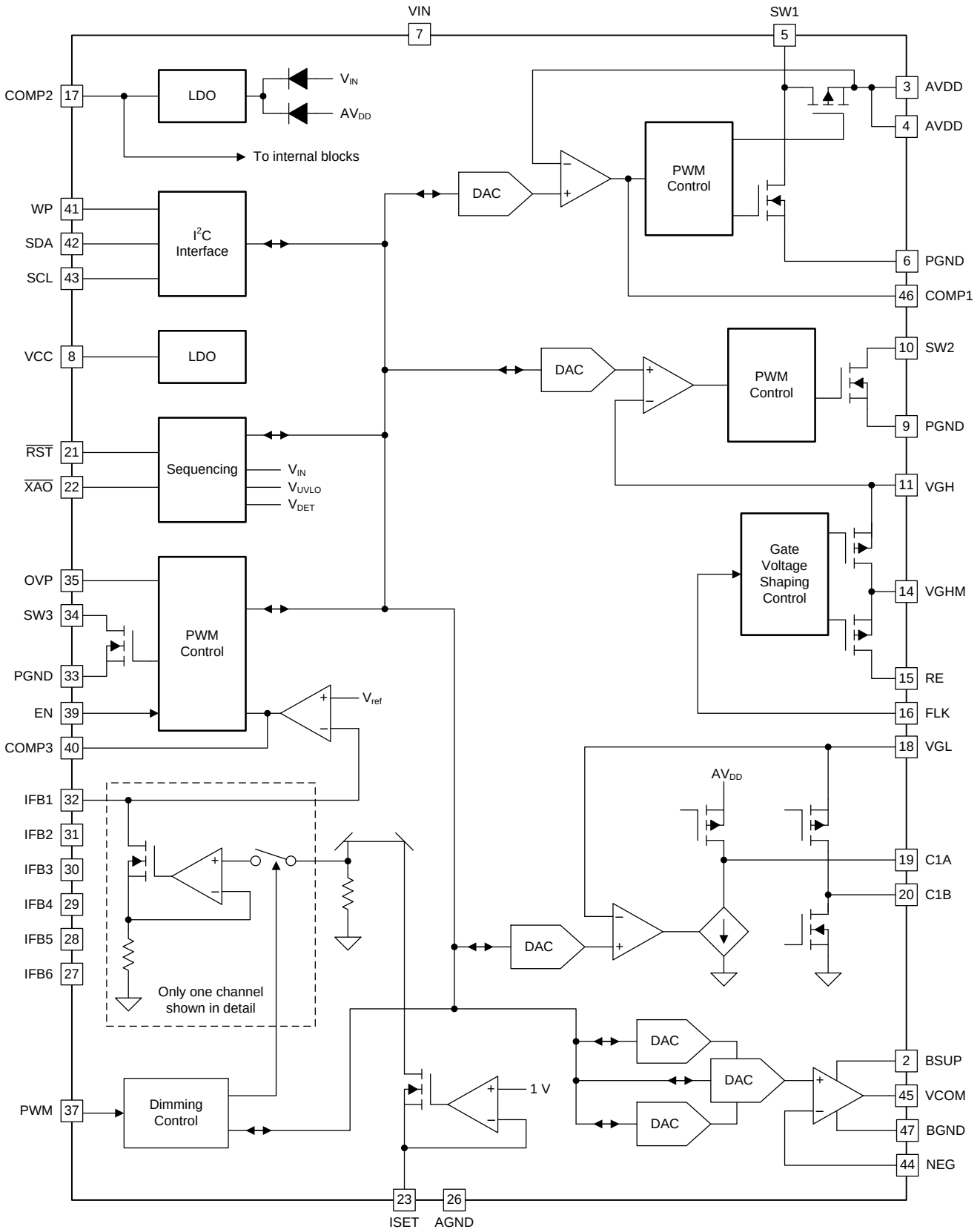


Figure 5-1. Top-Level Block Diagram

5.3 Feature Description

The following sections describe the features of the TPS65154.

5.3.1 Linear Regulator (V_{CC})

The linear regulator is supplied directly from the VIN pin, and its output voltage can be programmed to 1.0 V, 1.2 V, 1.89 V, or 2.5 V using the VCC register.

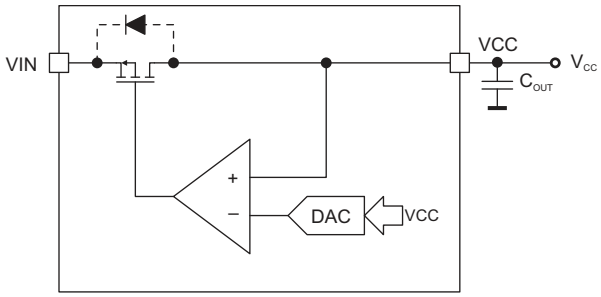


Figure 5-2. Linear Regulator Block Diagram

5.3.1.1 Power-Up (Linear Regulator)

The linear regulator starts t_{DLY1} milliseconds after the supply voltage exceeds the undervoltage lockout threshold ($V_{IN} > V_{UVLO}$). It does not have a soft-start function, and its output ramps up as fast as the supply voltage slew rate and the linear regulator's output capacitance allow.

5.3.1.2 Power-Down (Linear Regulator)

The linear regulator is turned off as soon as the supply voltage falls below the undervoltage lockout threshold ($V_{IN} < V_{UVLO}$). V_{CC} is actively discharged during power-down.

5.3.1.3 Protection (Linear Regulator)

The linear regulator is protected against short-circuits and undervoltage conditions. An undervoltage condition is detected if the linear regulator's output falls below 70% of its programmed voltage for longer than 50 ms, in which case the IC is disabled. A short-circuit condition is detected if the linear regulator's output falls below 30% of its programmed voltage, in which case the IC is disabled immediately (short-circuit detection has no time delay associated with it). To recover normal operation following either an undervoltage condition or short-circuit condition, the cause of the error must be removed and a POR applied.

5.3.2 Boost Converter 1 (AV_{DD})

Boost converter 1 is synchronous and uses a virtual current mode topology that:

- achieves high efficiencies;
- allows the converter to work in continuous conduction mode under all operating conditions, simplifying compensation; and
- provides true input-output isolation when the boost converter is disabled.

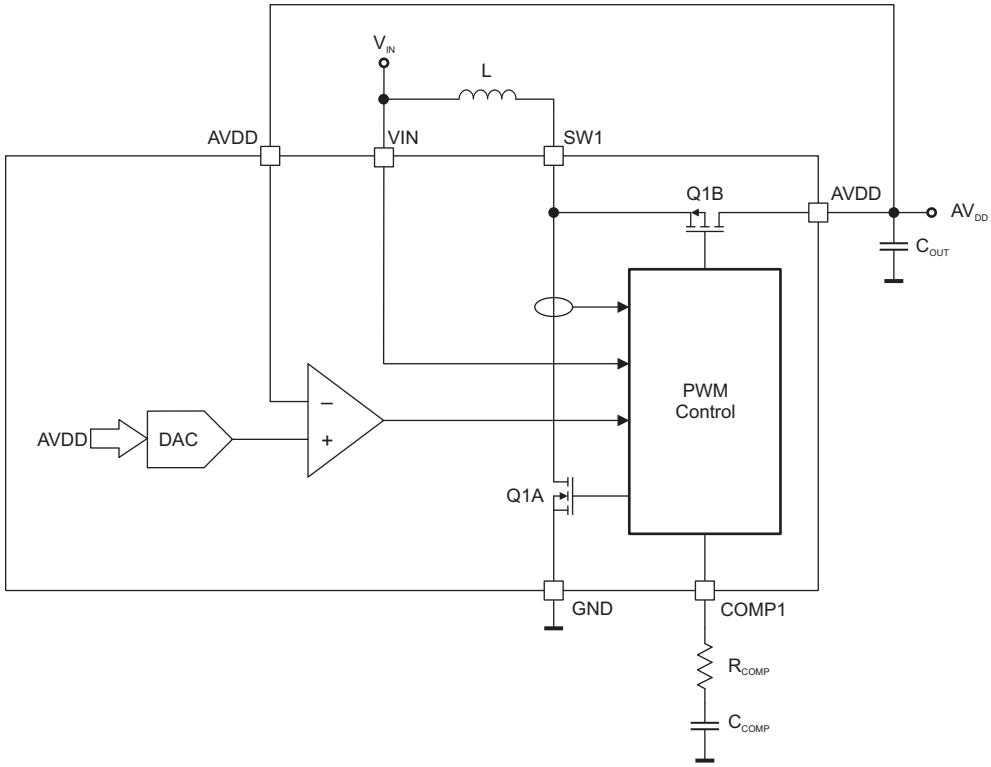


Figure 5-3. Boost Converter 1 Internal Block Diagram

Boost converter 1's switching frequency can be programmed to 400 kHz, 600 kHz, 800 kHz, or 1 MHz using the FSW1 register. Its output voltage can be programmed from 6.5 V to 9.6 V in 100 mV steps using the AVDD register.

Boost converter 1 uses an external compensation network connected to the COMP1 pin to stabilize its feedback loop. A simple series R-C network connected between the COMP1 pin and ground is sufficient to achieve good performance, that is, stable and with good transient response. Good starting values, which will work for most applications, are 25 kΩ and 3.9 nF.

In some applications (for example, those using electrolytic output capacitors), it may be necessary to include a second compensation capacitor between the COMP1 pin and ground. This has the effect of adding an additional pole in the feedback loop's frequency response, which cancels the zero introduced by the output capacitor's ESR.

The synchronous topology of boost converter 1 ensures that AV_{DD} is fully isolated from V_{IN} when the converter is disabled.

5.3.2.1 Power-Up (Boost Converter 1)

Boost converter 1 starts t_{DLY2} milliseconds after $\overline{RST}$ goes high. Delay time t_{DLY2} can be programmed from 0 ms to 75 ms using the DLY2 register.

To minimize inrush current during start-up, boost converter 1 ramps its output voltage in t_{SS2} milliseconds. Start-up time t_{SS2} can be programmed from 0.5 ms to 75 ms using the SS2 register. Longer soft-start times generate lower inrush currents.

5.3.2.2 Power-Down (Boost Converter 1)

Boost converter 1 is disabled when $V_{IN}<V_{UVLO}$. When disabled, boost converter 2 actively discharges AV_{DD} by turning on Q2.

5.3.2.3 Protection (Boost Converter 1)

Boost converter 1 is protected against short-circuits and undervoltage conditions. An undervoltage condition is detected if the boost converter's output falls below 70% of its programmed voltage for longer than 50 ms, in which case the IC is disabled. A short-circuit condition is detected if the boost converter's output falls below 30% of its programmed voltage, in which case the IC is disabled immediately (short-circuit detection has no time delay associated with it). To recover normal operation following either an undervoltage condition or short-circuit condition, the cause of the error must be removed and a POR applied.

5.3.3 Boost Converter 2 (V_{GH})

Boost converter 2 is non-synchronous and uses a constant off-time topology. The converter's switching frequency is not constant but adapts itself to V_{IN} and V_{GH}. Boost converter 2 uses peak current control and is designed to operate permanently in discontinuous conduction mode (DCM), thereby allowing the internal compensation circuit to achieve stable operation over a wide range of output voltages and currents. Boost converter 2's output voltage can be programmed from 18 V to 25.5 V using the VGH register.

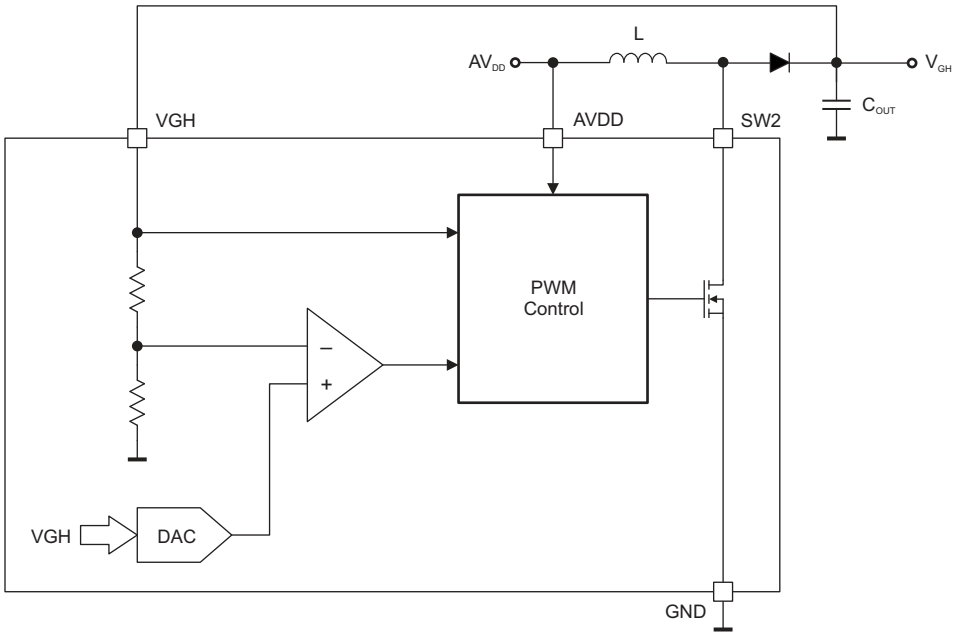


Figure 5-4. Boost Converter 2 Block Diagram

5.3.3.1 Power-Up (Boost Converter 2)

Boost converter 2 is enabled as soon as V_{GL} has finished ramping down. To minimize inrush current during start-up, boost converter 2 ramps V_{GH} linearly to its programmed value in t_{SS4} seconds. Soft-start time t_{SS4} can be programmed from 0.256 ms to 35 ms using the SS4 register. Because boost converter 2 is non-synchronous, its output is already equal to AV_{DD} (minus the voltage drop across its rectifier diode) before it starts switching, which means that the time during which V_{GH} is actually ramping during start-up is less than the actual programmed soft-start time (see Figure 5-5).

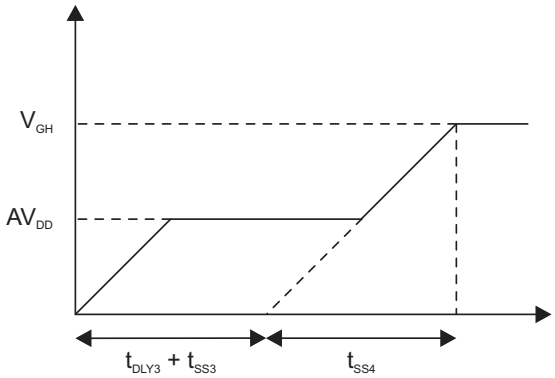


Figure 5-5. Boost Converter 2 Soft-Start

5.3.3.2 Power-Down (Boost Converter 2)

Boost converter 2 is disabled when V_{IN}<V_{UVLO}. The converter's output is not actively discharged when the converter is disabled.

5.3.3.3 Protection (Boost Converter 2)

Boost converter 2 is protected against short-circuits and undervoltage conditions. An undervoltage condition is detected if the boost converter's output falls below 70% of its programmed voltage for longer than 50 ms, in which case the IC is disabled. A short-circuit condition is detected if the boost converter's output falls below 30% of its programmed voltage, in which case the IC is disabled immediately (short-circuit detection has no time delay associated with it). To recover normal operation following either an undervoltage condition or short-circuit condition, the cause of the error must be removed and a POR applied.

5.3.4 Negative Charge Pump (V_{GL})

The negative charge pump inverts AV_{DD} and regulates its output to the voltage set by the VGL register. V_{GL} can be programmed from –5 V to –8 V in 0.2 V steps using the VGL register, however, since the negative charge pump inverts AV_{DD} to generate its output, the most negative voltage that can be generated is approximately $–AV_{DD}$+1 V. Thus, if AV_{DD} = 8.0 V, the usable range of V_{GL} is approximately –5 V to –7 V. If V_{GL} is programmed to a more negative voltage than this the charge pump may not be able to regulate its output. This will not damage the IC, but performance may be impaired.

The negative charge pump in the TPS65154 is fully integrated and requires only two external capacitors to operate (a flying capacitor connected between the C1A and C1B pins, and an output capacitor connected between the VGL pin and ground).

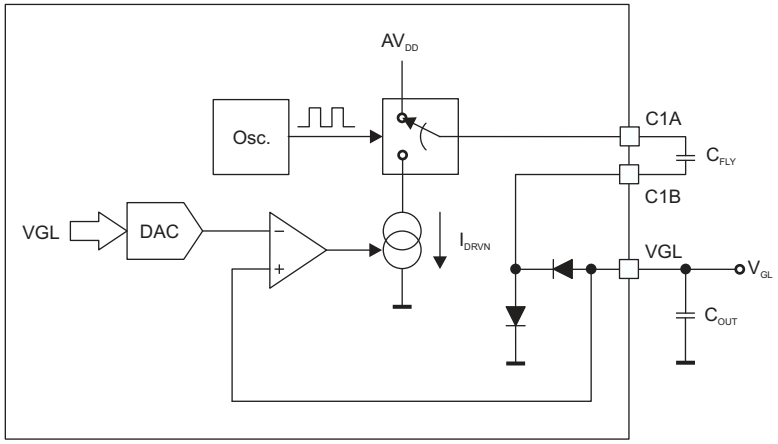


Figure 5-6. Negative Charge Pump Block Diagram

5.3.4.1 Power-Up (Negative Charge Pump)

The negative charge pump starts t_{DLY3} milliseconds after boost converter 1 (AV_{DD}) starts ramping and ramps its output linearly from zero to its programmed output voltage in t_{SS3} ms. Delay time t_{DLY3} can be programmed from 0 ms to 35 ms using the DLY3 register. Soft-start time t_{SS3} can be programmed from 0 ms to 35 ms using the SS3 register.

5.3.4.2 Power-Down (Negative Charge Pump)

The negative charge pump is disabled when the supply voltage falls below the undervoltage lockout threshold (V_{IN}<V_{UVLO}). During power-down the charge pump's output is actively discharge to GND.

5.3.4.3 Protection (Negative Charge Pump)

The negative charge pump is protected against short-circuits and undervoltage conditions. An undervoltage condition is detected if the charge pump's output falls below 70% of its programmed voltage for longer than 50 ms, in which case the IC is disabled. A short-circuit condition is detected if the charge pump's output falls below 30% of its programmed voltage, in which case the IC is disabled immediately (short-circuit detection has no time delay associated with it). To recover normal operation following either an undervoltage condition or short-circuit condition, the cause of the error must be removed and a POR applied.

5.3.5 Gate Voltage Shaping

The gate voltage shaping function can be used to reduce image sticking in LCD panels by modulating the LCD panel's gate ON voltage (V_{GH}). Figure 5-7 shows a block diagram of the gate voltage shaping function and Figure 5-8 shows the typical waveforms during operation.

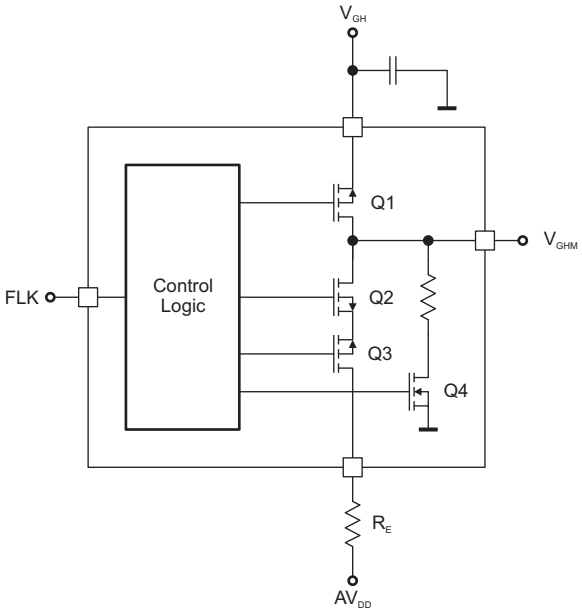


Figure 5-7. Gate Voltage Shaping Block Diagram

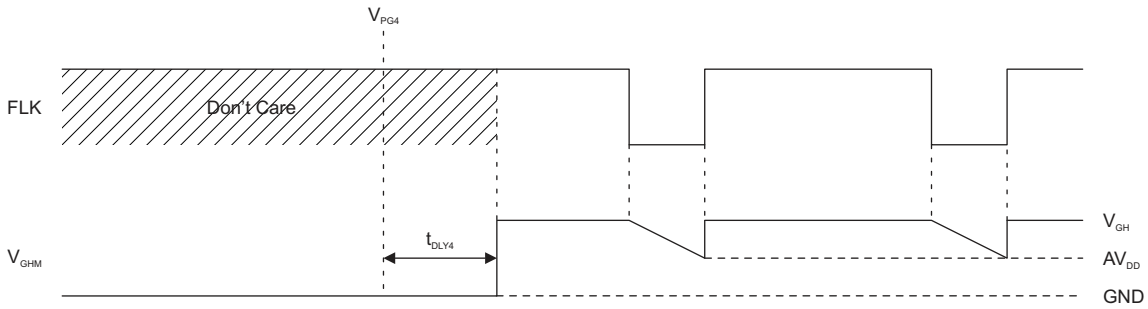


Figure 5-8. Gate Voltage Shaping Waveforms

Gate voltage shaping is controlled by the FLK input. When FLK is high, Q1 is on, Q2, Q3 and Q4 are off, and V_{GHM} is equal to V_{GH}. On the falling edge of FLK, Q1 is turned off, Q2 and Q3 are turned on, and the LCD panel load connected to the VGHM pin discharges through the external resistor connected to the RE pin.

During power-up, Q1, Q2 and Q3 are held off and Q4 is turned on, pulling the VGHM pin pulled to GND, regardless of the state of the FLK signal, until t_{DLY4} milliseconds after boost converter 2 (V_{GH}) has finished ramping. The value of t_{DLY4} can be programmed from 0 ms to 35 ms using the DLY4 register.

During power-down Q1 is held permanently on and Q2, Q3 and Q4 permanently off, regardless of the state of the FLK signal.

5.3.6 Panel Discharge ($\overline{XAO}$)

The TPS65154 provides an output signal via its $\overline{XAO}$ pin that can be used to drive the outputs of the display panel's gate driver IC high during power-down. The $\overline{XAO}$ pin is pulled low whenever $V_{IN}<V_{DET}$. The V_{DET} threshold voltage can be configured using the VDET register.

The $\overline{XAO}$ output is an open-drain type and requires an external pull-up, typically in the range 10 kΩ to 100 kΩ.

5.3.7 Reset Generator ($\overline{RST}$)

The $\overline{RST}$ pin generates an active-low reset signal for the rest of the system. During power-up, the reset timer starts when V_{CC} has finished ramping. The reset pulse duration t_{RST} can be programmed from 0 ms to 15 ms using the RESET register. The $\overline{RST}$ signal is latched when it goes high and will not be taken low again until the device is powered down (even if V_{CC} temporarily falls out of regulation). The active power-down threshold (V_{UVLO} or V_{DET}) can be selected using the RMODE bit in the CONFIG register.

The $\overline{RST}$ output is an open-drain type that requires an external pull-up resistor. Pull-up resistor values in the range 10 kΩ to 100 kΩ are recommended for most applications.

5.3.8 Programmable VCOM

The programmable VCOM uses three digital-to-analog converters (DACs) to generate a V_{COM} voltage that is subsequently buffered by a high-speed op-amp. The maximum value of V_{COM} is set by the 4-bit VMAX register, and can be programmed in the range 2.5/8×AV_{DD} to 4/8×AV_{DD}. The minimum value of V_{COM} is set by the 4-bit VMIN register, and can be programmed in the range 2/8 × AV_{DD} to 3.5/8 × AV_{DD}. **Note, for proper operation, V_{MAX} must be greater than V_{MIN}.** By programming the 7-bit VCOM parameter, users can adjust the V_{COM} voltage appearing at the OUT pin between V_{MIN} and V_{MAX} as follows:

$$V_{COM} = V_{MIN} + \frac{(V_{MAX} - V_{MIN}) \cdot VCOM}{127} \quad (1)$$

where VCOM is the value stored in the Wiper Register (see Figure 5-9).

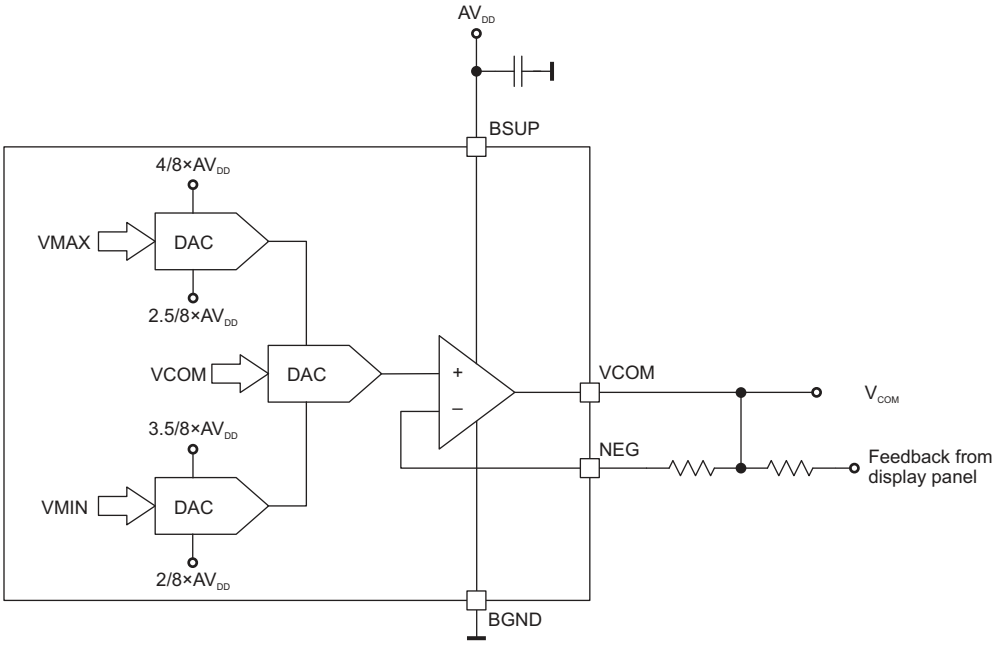


Figure 5-9. Programmable VCOM Block Diagram

The programmable VCOM function has three registers. The volatile Wiper Register (WR) contains the value currently output by the programmable VCOM DAC; this value is lost when power to the device is removed. The non-volatile Initial Value Register (IVR) contains the value loaded into the DAC every time the device is powered up. The Control Register (CR) determines whether data is written to or read from the WR, the IVR, or both. If the CR contains 00h, during write operations data is stored in the WR *and* the IVR, and during read operations data is read from the IVR. If the CR contains 80h, data is written to and read from the WR register *only*. 00h and 80h are the only valid values for the CR. Table 5-1 shows the programmable VCOM's register address map.

Table 5-1. Programmable VCOM Register Address Map

REGISTER ADDRESS	NON-VOLATILE	VOLATILE
00h	Initial Value Register (IVR)	Wiper Register (WR)
02h	Not Used	Control Register (CR)

5.3.8.1 Operational Amplifier Performance

Like most op-amps, the V_{COM} op-amp in the TPS65154 is not designed to drive purely capacitive loads, so it is not recommended to connect a capacitor directly to its output in an attempt to increase performance; however, the op-amp is capable of delivering high peak currents that make such capacitors unnecessary in most applications.

High-speed op amps such as the one in the TPS65154 require care when using them. The most common problem is when parasitic capacitance at the inverting input creates a pole with the feedback resistor, reducing amplifier stability. Two things can be done to minimize the likelihood of this happening. Both of these work by shifting the pole (which can never be completely eliminated) to a frequency outside the op amp's bandwidth, where it has no effect.

- Reduce the value of the feedback resistor. In applications where no feedback from the panel is used, the feedback resistor can be made zero. In applications where a non-zero feedback resistor has to be used, a small capacitor (between 10 pF and 100 pF) across the feedback resistor will minimize ringing.
- Minimize the parasitic capacitance at the op amp's inverting input. This is achieved by using short PCB traces between the feedback resistor and the inverting input, and by removing ground planes and other copper areas above and below this PCB trace.

5.3.8.2 Power-Up (Programmable VCOM)

The programmable V_{COM} is enabled when $AV_{DD} > V_{UVLO2}$.

5.3.8.3 Power-Down (Programmable VCOM)

During power-down, the programmable VCOM continues to operate until $AV_{DD} < V_{UVLO2}$.

5.3.9 WLED Driver

5.3.9.1 WLED Boost Converter

The WLED boost converter boosts a 4.5 V to 24 V supply V_{BAT} to a higher voltage to supply the LED strings connected to the WLED driver. It uses a fixed-frequency, current-mode topology. The converter's output voltage is automatically adjusted to maintain the lowest feedback voltage (IFB1 to IFB6) between 450 mV and 750 mV, thus ensuring sufficient headroom for the output current sinks, but without dissipating excessive power in the IC. This approach automatically compensates for changes in the LED string voltage, for example, because of temperature effects. The WLED boost converter's switching frequency can be programmed to 400 kHz, 600 kHz, 800 kHz, and 1 MHz using the FSW3 register.

The WLED boost converter features a soft-start circuit to limit inrush current when the converter starts. The duration of the soft-start ramp depends on the value of the capacitor connected to the COMP3 pin. Note, that because the converter is a non-synchronous type, its output voltage before it starts switching is equal to V_{BAT} (minus the voltage drop across its rectifier).

5.3.9.2 Current Sinks

The brightness of the LED strings is determined by the *average* current flowing through each string, which is the product of the output duty cycle and the current sink's output current. The output current of all current sinks is the same and is set by the external resistor connected between the ISET pin and ground:

$$I_{MAX} = \frac{V_{SET}}{R_{SET}} \cdot K_{SET} \quad (2)$$

where:

- V_{SET} is the voltage on the ISET pin
- R_{SET} is the resistance between the ISET pin and GND
- K_{SET} is a constant

When the TPS65154 measures zero current flowing in one of the IFB pins it determines that the string is open and automatically disables that output. The WLED boost converter's output voltage is subsequently regulated according to the remaining operational strings. If an application uses fewer than six LED strings, it is recommended to connected the unused outputs to ground; this ensures the most rapid detection of the unused strings. Once open strings have been detected, they remain disabled until a POR occurs or EN is toggled.

5.3.9.3 Protection

The WLED boost converter and dimming circuits feature a variety of protection schemes to ensure reliable operation when subjected to various failure modes. These protection schemes are listed in Table 5-2.

Table 5-2. WLED Driver Protection

ERROR	DETECTION	ACTION	RECOVERY
WLED boost converter output voltage too high	V_{OVP} exceeds programmed threshold (30 V, 33 V, 36 V or 39 V)	WLED boost converter output regulated to programmed threshold	None required
WLED boost converter switch current too high	$I_{SW} > I_{LIM}$	Switch turned off	Switch automatically re-enabled at start of next switching cycle
All LED strings open-circuit	I_{IFB} = 0 mA and $V_{OUT} = V_{OVP}$	Disable all output channels and boost converter	Output channels re-enabled following power cycle
Individual LED string(s) open-circuit	I_{IFB} = 0 mA and $V_{OUT} = V_{OVP}$	Disable affected output channel(s) Functional output channels continue operating.	Affected output channel(s) re-enabled following power cycle
Individual LED string(s) shorted-circuited to ground	I_{IFB} = 0 mA for longer than 4 ms		

5.3.9.4 Enable and Start-Up

The WLED driver is enabled and disabled by EN, however, this signal has no effect until the LCD bias functions have completed their start-up sequence. Following a POR, EN has no effect until t_{DLY4} is complete; after that the WLED driver can be enabled and disabled at any time using EN (providing nothing happens to cause the LCD bias functions to re-start) and applying a PWM signal. In applications that do not generate an EN signal, the EN pin can be tied to V_{IN}, in which case the WLED driver will start automatically at the end of t_{DLY4}. Note, that a permanently low PWM signal (0% duty cycle) will prevent boost converter 3 from starting-up.

When the WLED driver is enabled it first checks the status of IFB1 to IFB6 and shuts down any channels that it detects are disabled/unused. These channels will be subsequently ignored until a POR occurs or EN is toggled.

5.3.10 Undervoltage Lockout

An undervoltage lockout function disables the IC when the supply voltage is too low for proper operation.

5.4 Device Functional Modes

5.4.1 Dimming Modes

The TPS65154 support direct dimming and phase-shift dimming modes. The active dimming mode can be selected using the DMODE bit in the CONFIG register.

5.4.1.1 Direct Dimming

When direct dimming is selected, the output current sinks are controlled directly by the PWM signal. In this mode, they are turned on and off together, at the same frequency and duty cycle as the PWM signal (see Figure 5-10).

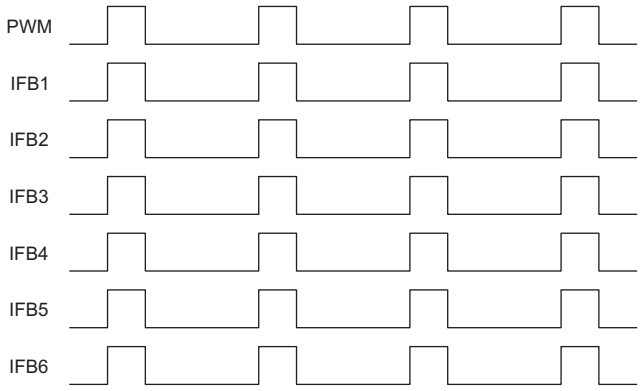


Figure 5-10. Direct Dimming

5.4.1.2 Phase-Shift Dimming

When phase-shift dimming mode is selected, the output dimming frequency does not depend on the frequency of the PWM signal but can be independently programmed from 15 kHz to 22 kHz using the FDIM register. In this mode, the duty cycle information contained in the PWM signal is extracted and re-used to generate up to six outputs, at the output frequency set by the FDIM register, and phase-shifted with respect to each other by 360°/N, where N is the number of outputs in use (see Figure 5-11). Using phase-shifted outputs, the maximum load current step is reduced by the same factor N, resulting in reduced voltage ripple on the boost converter's output and consequently lower audible noise.

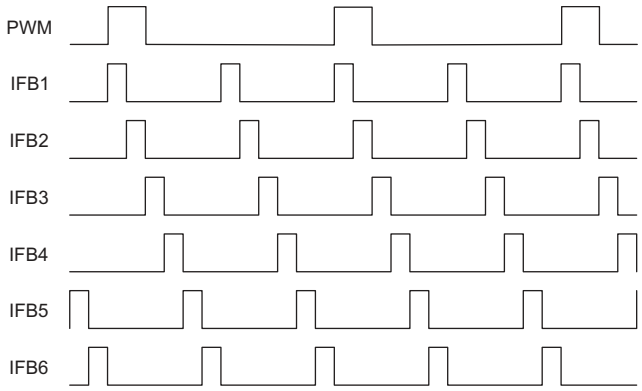


Figure 5-11. Phase-Shift Dimming

5.4.2 Power Sequencing

Figure 5-12 shows the typical power-up/down characteristic of the TPS65154.

5.4.2.1 Power-Up

V_{CC} starts ramping t_{DLY1} seconds after $V_{IN} > V_{UVLO}$.

$\overline{RST}$ is initially held low. t_{RST} seconds after V_{CC} has finished ramping $\overline{RST}$ goes high.

AV_{DD} starts ramping t_{DLY2} seconds after $\overline{RST}$ has gone high.

V_{GL} starts ramping t_{DLY3} seconds after AV_{DD} starts ramping.

V_{GH} starts ramping as soon as V_{GL} has finished ramping.

V_{GHM} is initially held low (connected to RE). t_{DLY4} seconds after V_{GH} has finished ramping, gate voltage shaping is enabled and V_{GHM} follows the state of FLK.

$\overline{XAO}$ is initially held low. t_{DLY6} seconds after $V_{IN}>V_{DET}$ $\overline{XAO}$ goes high.

The WLED driver is enabled by the logical AND of AV_{DD} (that is, AV_{DD} has finished ramping) and EN.

5.4.2.2 Power-Down

V_{CC}, AV_{DD}, V_{GH} and V_{GL} are disabled when $V_{IN}<V_{UVLO}$.

$\overline{XAO}$ goes low when V_{IN} falls below the threshold selected for it (V_{UVLO} or V_{DET}).

$\overline{RST}$ goes low when V_{IN} falls below the threshold selected for it (V_{UVLO} or V_{DET}).

The WLED driver is turned off when EN = 0 or $V_{IN} < V_{UVLO}$.

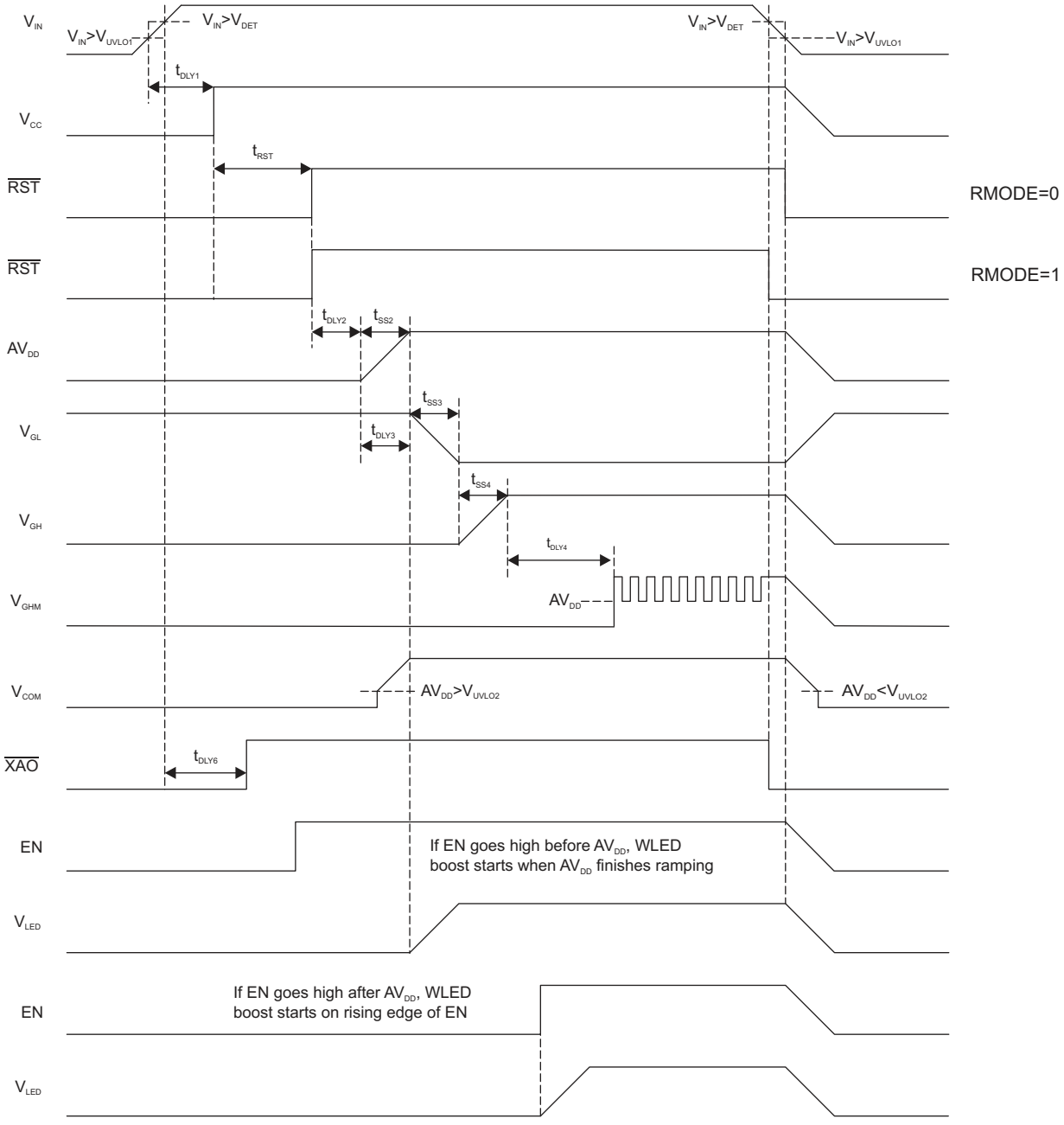


Figure 5-12. Power Up/Down Sequencing

5.5 Programming

5.5.1 Configuration

The TPS65154 divides the configuration parameters into two categories:

- Configuration parameters
- VCOM

In typical applications, all configuration parameters except VCOM are programmed by the subcontractor during PCB assembly, and VCOM is programmed by the display manufacturer during display calibration.

5.5.1.1 General

Configuration parameters can be changed by writing the desired values to the appropriate RAM register(s). The RAM registers are volatile and their contents are lost when power is removed from the device. By writing to the Control Register, it is possible to store the active configuration in non-volatile EEPROM; during power-up, the contents of the EEPROM are copied into the RAM registers and used to configure the device.

5.5.1.1.1 I^2C Interface

The TPS65154 features an industry-standard I^2C interface that supports both Standard and Fast modes of operation.

5.5.1.1.2 Slave Addresses

The configuration parameters are all accessed using slave address 74h and the VCOM is accessed using slave address 28h.

5.5.1.1.3 Write Protect

An active-high Write Protect pin (WP) prevents the configuration parameters from being changed by accident. This pin is internally pulled high and must be actively pulled low to access to the EEPROM or RAM registers. Note that the WP pin disables all I^2C traffic to the TPS65154, and must also be pulled low during read operations. This is to ensure that noise present on the I^2C lines does not erroneously overwrite the active configuration stored in RAM (which would not be protected by a simple EEPROM write-protect scheme). The write protect function can be enabled and disabled using the WPEN bit in the CONFIG register. Note that once the write protect function is enabled it is not possible to disable again it without pulling the WP pin low. For this reason, it is strongly recommended that applications include some way to pull the WP pin low (for example, a test pad), even if it is not normally used.

5.5.2 Programming Examples (Excluding VCOM)

5.5.2.1 Writing to a Single RAM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65154 acknowledges
4. Bus master sends address of RAM register (00h)
5. TPS65154 acknowledges
6. Bus master sends data to be written
7. TPS65154 acknowledges
8. Bus master sends STOP condition

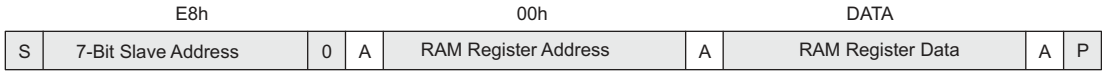


Figure 5-13. Writing to a Single RAM Register

5.5.2.2 Writing to Multiple RAM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65154 acknowledges
4. Bus master sends address of first RAM register to be written to (00h)
5. TPS65154 acknowledges
6. Bus master sends data to be written to first RAM register
7. TPS65154 acknowledges
8. Bus master sends data to be written to RAM register at next higher address (auto-increment)
9. TPS65154 acknowledges
10. Steps (8) and (9) repeated until data for final RAM register has been sent
11. TPS65154 acknowledges
12. Bus master sends STOP condition

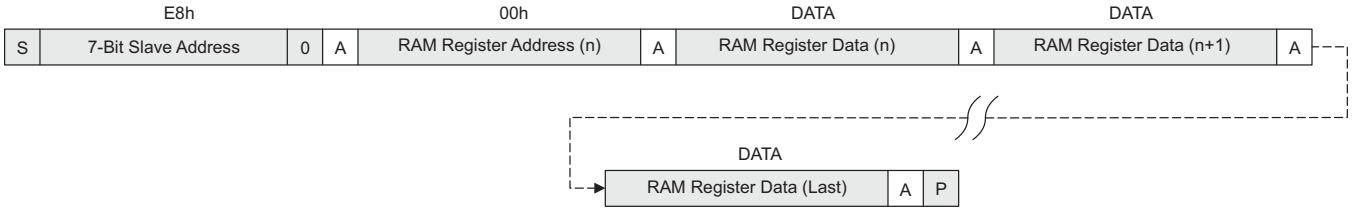


Figure 5-14. Writing to Multiple RAM Registers

5.5.2.3 Saving Contents of all RAM Registers to EEPROM

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65154 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65154 acknowledges
6. Bus master sends data to be written to the Control Register (80h)
7. TPS65154 acknowledges
8. Bus master sends STOP condition

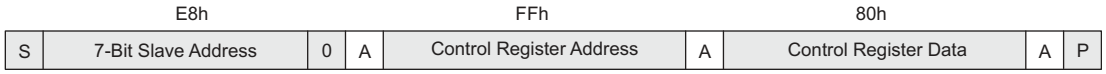


Figure 5-15. Saving Contents of all RAM Registers to EEPROM

5.5.2.4 Reading from a Single RAM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65154 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65154 acknowledges
6. Bus master sends data for Control Register (00h)
7. TPS65154 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65154 acknowledges
12. Bus master sends address of RAM register (00h)
13. TPS65154 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65154 acknowledges
17. TPS65154 sends RAM register data
18. Bus master does not acknowledge
19. Bus master sends STOP condition

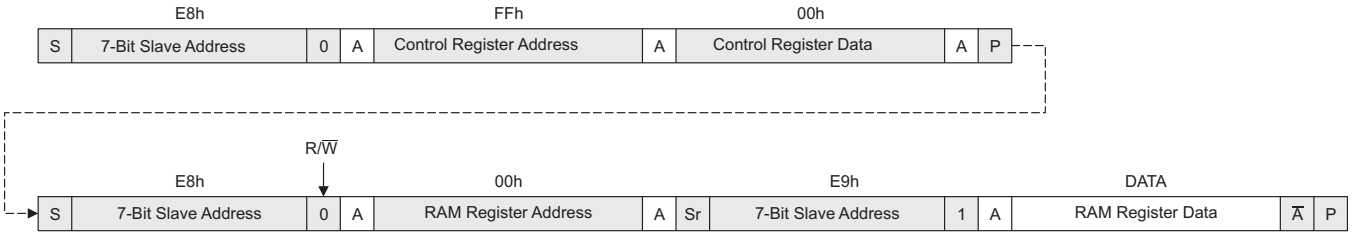


Figure 5-16. Reading from a Single RAM Register

5.5.2.5 Reading from a Single EEPROM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65154 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65154 acknowledges
6. Bus master sends data for Control Register (01h)
7. TPS65154 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65154 acknowledges
12. Bus master sends address of EEPROM register (00h)
13. TPS65154 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65154 acknowledges
17. TPS65154 sends EEPROM register data
18. Bus master does not acknowledge
19. Bus master sends STOP condition

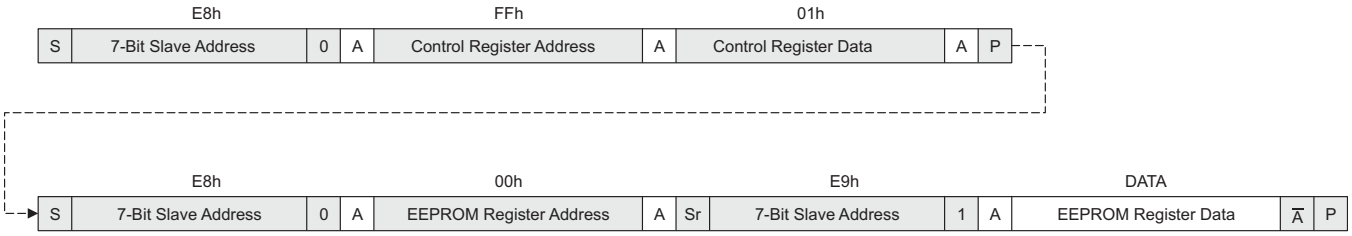


Figure 5-17. Reading from a Single EEPROM Register

5.5.2.6 Reading from Multiple RAM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65154 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65154 acknowledges
6. Bus master sends data for Control Register (00h)
7. TPS65154 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65154 acknowledges
12. Bus master sends address of first register to be read (00h)
13. TPS65154 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65154 acknowledges
17. TPS65154 sends contents of first RAM register to be read
18. Bus master acknowledges
19. TPS65154 sends contents of second RAM register to be read
20. Bus master acknowledges
21. TPS65154 sends contents of third (last) RAM register to be read
22. Bus master does not acknowledge
23. Bus master sends STOP condition

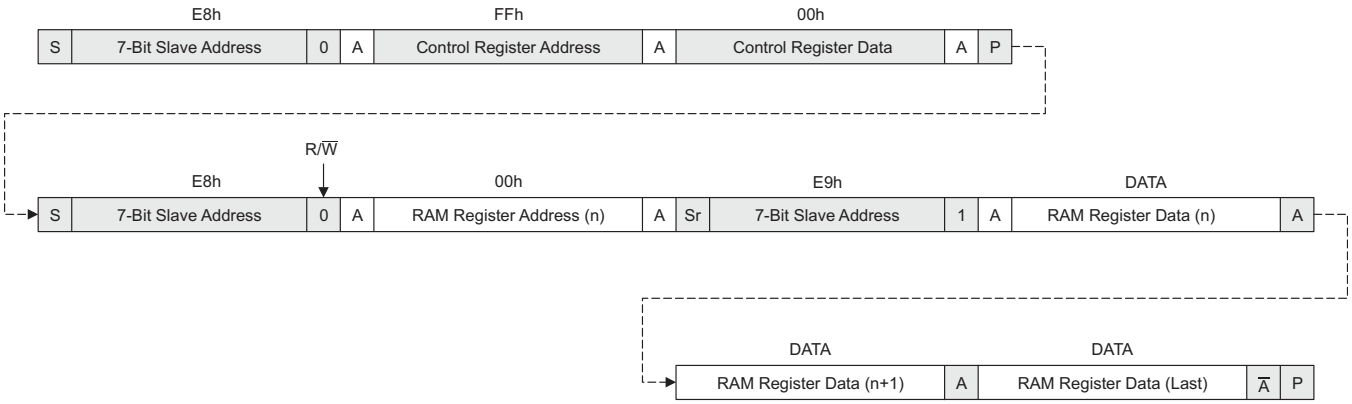


Figure 5-18. Reading from Multiple RAM Registers

5.5.2.7 Reading from Multiple EEPROM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65154 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65154 acknowledges
6. Bus master sends data for Control Register (01h)
7. TPS65154 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65154 acknowledges
12. Bus master sends address of first EEPROM register to be read (00h)
13. TPS65154 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65154 acknowledges
17. TPS65154 sends contents of first EEPROM register to be read
18. Bus master acknowledges
19. TPS65154 sends contents of second EEPROM register to be read
20. Bus master acknowledges
21. TPS65154 sends contents of third (last) EEPROM register to be read
22. Bus master does not acknowledge
23. Bus master sends STOP condition

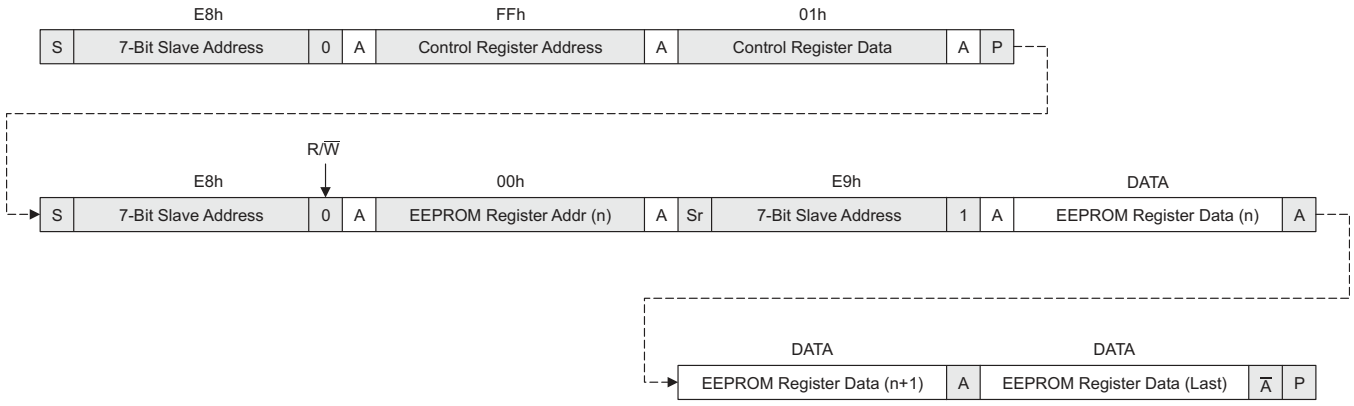


Figure 5-19. Reading from Multiple EEPROM Registers

5.5.3 Programming Examples - VCOM

5.5.3.1 Writing a VCOM Value of 77h to WR

1. The bus master sends a START condition.
2. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
3. TPS65154 slave acknowledges.
4. The bus master sends the CR address of 02h.
5. The TPS65154 acknowledges.
6. The bus master sends the CR contents of 80h.
7. The TPS65154 slave acknowledges.
8. The bus master sends a STOP condition.
9. The bus master sends a START condition.
10. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
11. TPS65154 slave acknowledges.
12. The bus master sends the WR address of 00h.
13. The TPS65154 acknowledges.
14. The bus master sends the WR contents of 77h (right-justified).
15. The TPS65154 slave acknowledges.
16. The bus master sends a STOP condition.

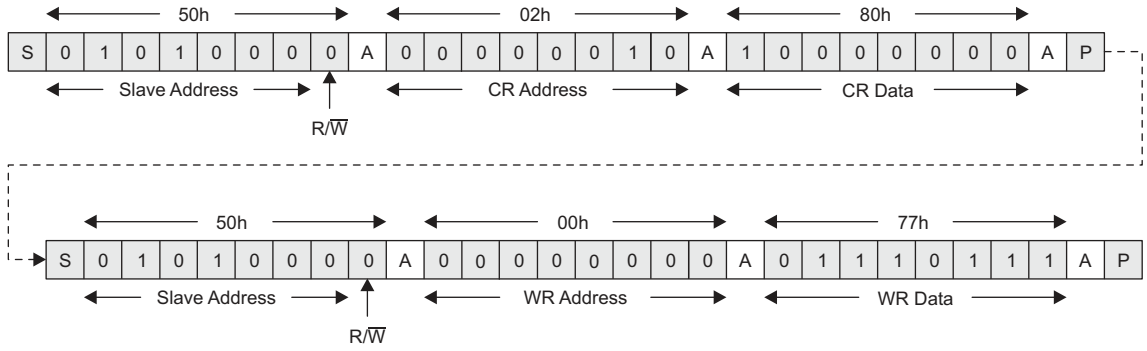


Figure 5-20. Writing a VCOM Value of 77h to WR

5.5.3.2 Writing a VCOM Value of 77h to IVR and WR

1. The bus master sends a START condition.
2. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
3. TPS65154 slave acknowledges.
4. The bus master sends the CR address of 02h.
5. The TPS65154 acknowledges.
6. The bus master sends the CR contents of 00h.
7. The TPS65154 slave acknowledges.
8. The bus master sends a STOP condition.
9. The bus master sends a START condition.
10. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
11. TPS65154 slave acknowledges.
12. The bus master sends the WR address of 00h.
13. The TPS65154 acknowledges.
14. The bus master sends the WR contents of 77h (right-justified).
15. The TPS65154 slave acknowledges.
16. The bus master sends a STOP condition.

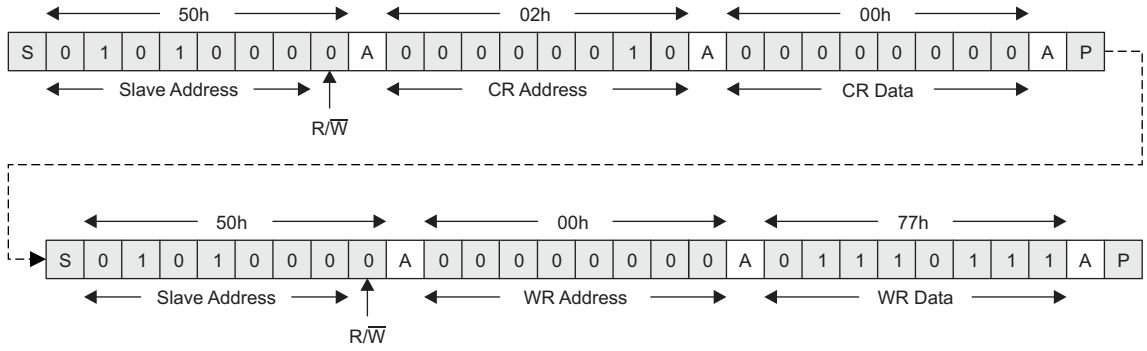


Figure 5-21. Writing a VCOM Value of 77h to IVR and WR

5.5.3.3 Reading a VCOM Value of 77h from WR

1. The bus master sends a START condition.
2. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
3. TPS65154 slave acknowledges.
4. The bus master sends the CR address of 02h.
5. The TPS65154 acknowledges.
6. The bus master sends the CR contents of 80h.
7. The TPS65154 slave acknowledges.
8. The bus master sends a STOP condition.
9. The bus master sends a START condition.
10. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
11. TPS65154 slave acknowledges.
12. The bus master sends the WR address of 00h.
13. The TPS65154 acknowledges.
14. The bus master sends a REPEATED START condition.
15. The bus master sends 7-bit slave address plus high R/$\overline{W}$ bit.
16. The TPS65154 sends the WR contents of 77h (right-justified).
17. The bus master does not acknowledge.
18. The bus master sends a STOP condition.

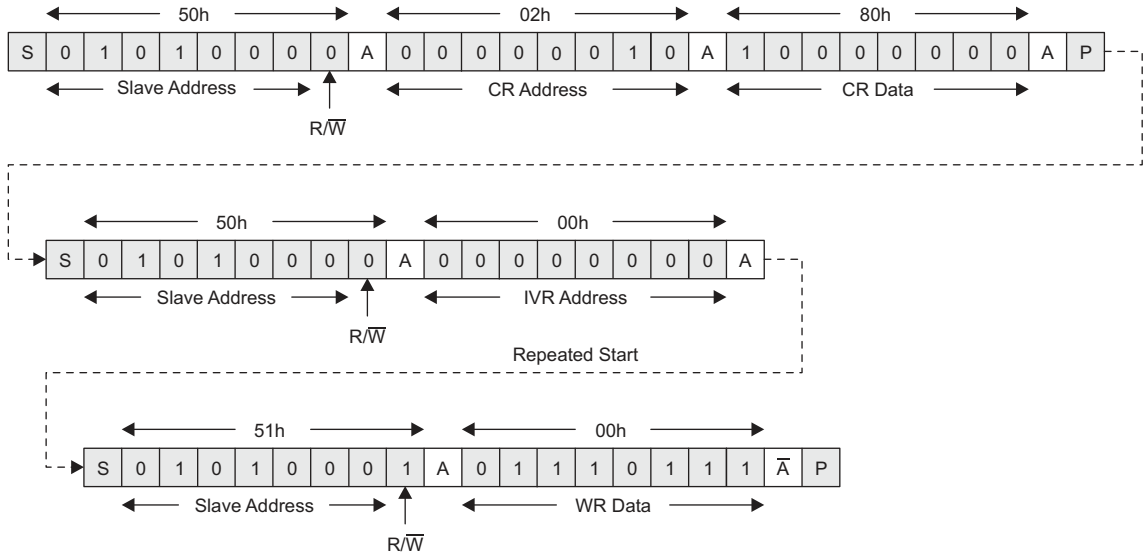


Figure 5-22. Reading 77h from WR

5.5.3.4 Reading a VCOM Value of 77h from IVR

1. The bus master sends a START condition.
2. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
3. TPS65154 slave acknowledges.
4. The bus master sends the CR address of 02h.
5. The TPS65154 acknowledges.
6. The bus master sends the CR contents of 00h.
7. The TPS65154 slave acknowledges.
8. The bus master sends a STOP condition.
9. The bus master sends a START condition.
10. The bus master sends 7-bit slave address plus low R/$\overline{W}$ bit.
11. TPS65154 slave acknowledges.
12. The bus master sends the WR address of 00h.
13. The TPS65154 acknowledges.
14. The bus master sends a REPEATED START condition.
15. The bus master sends 7-bit slave address plus high R/$\overline{W}$ bit.
16. The TPS65154 sends the WR contents of 77h (right-justified).
17. The bus master does not acknowledge.
18. The bus master sends a STOP condition.

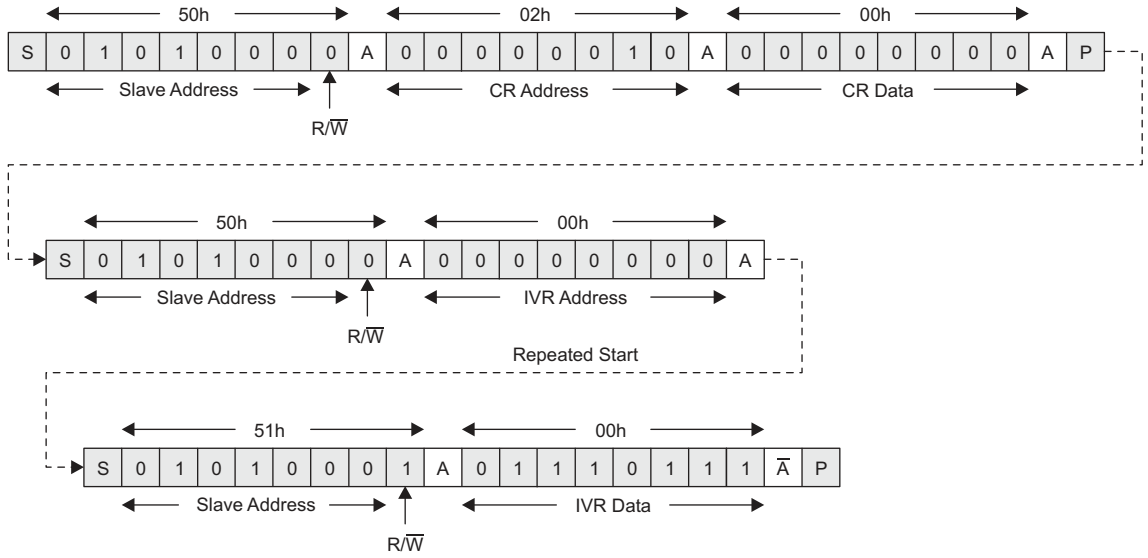


Figure 5-23. Reading 77h from IVR

5.6 Register Map

5.6.1 Configuration Registers (Excluding VCOM)

Table 5-3 shows the memory map of the configuration parameters.

Table 5-3. Configuration Memory Map

REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT		DESCRIPTION
00h	CONFIG	02h	KMODE = 0 WPEN = 0 DMODE = 1 RMODE = 0	Sets miscellaneous configuration bits
01h	VCC	03h	2.5 V	Sets the output voltage of the linear regulator (V_{CC})
02h	DLY1	02h	10 ms	Sets the start-up delay of the linear regulator (V_{CC})
03h	AVDD	0Fh	8.0 V	Sets the output voltage of boost converter 1 (AV_{DD})
04h	FSW1	01h	600 kHz	Sets the switching frequency of boost converter 1 (AV_{DD})
05h	SS2	04h	20 ms	Sets the soft-start time of boost converter 1 (AV_{DD})
06h	DLY2	02h	10 ms	Sets the start-up delay of boost converter 1 (AV_{DD})
07h	VGL	09h	–6.8 V	Sets the output voltage of the negative charge pump (V_{GL})
08h	SS3	01h	5 ms	Sets the soft-start time of the negative charge pump (V_{GL})
09h	DLY3	01h	5 ms	Sets the start-up delay of the negative charge pump (V_{GL})
0Ah	VGH	04h	20.0 V	Sets the output voltage of boost converter 2 (V_{GH})
0Bh	SS4	01h	5 ms	Sets the soft-start time of boost converter 2 (V_{GH})
0Ch	FSW3	01h	600 kHz	Sets the switching frequency of boost converter 3 (WLED)
0Dh	DLY4	02h	10 ms	Sets the start-up delay of the gate voltage shaping function (V_{GHM})
0Eh	OVP	03h	39 V	Sets the over-voltage protection threshold of boost converter 3 (WLED)
0Fh	FDIM	07h	22 kHz	Sets the output dimming frequency of the WLED driver in phase-shift dimming mode
10h	RESET	05h	5 ms	Sets the reset pulse duration
11h	VDET	00h	$V_{DET} = V_{UVLO}$	Sets the threshold of the $\overline{RST}$ and $\overline{XAO}$ signals
12h	DLY6	02h	30 ms	Sets the start-up delay of the $\overline{XAO}$ signal
13h	VMAX	07h	3.2 V	Sets the maximum V_{COM} voltage
14h	VMIN	07h	2.7 V	Sets the minimum V_{COM} voltage
15h	USER1	00h	00h	For customer use
FFh	CONTROL	00h		Controls whether read and write operations access RAM or EEPROM registers

5.6.1.1 CONFIG (00h)

The CONFIG register can be written to and read from.

Figure 5-24. CONFIG Register Bit Allocation

7	6	5	4	3	2	1	0
ADIS	Reserved			KMODE	WPEN	DMODE	RMODE
R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-4. CONFIG Register Field Descriptions

Bit	Field	Value	Description
7	ADIS		This bit can be used to disable boost converter 1 (AV_{DD}), boost converter 2 (V_{GH}) and the negative charge pump (V_{GL}) during device programming. This bit is volatile and is never stored in EEPROM. It is always reset (that is, ADIS = 0) following power-up, that is, the affected converters are always enabled following power-up.
		0	Boost converter 1 (AV_{DD}), boost converter 2 (V_{GH}), and negative charge pump (V_{GL}) enabled.
		1	Boost converter 1 (AV_{DD}), boost converter 2 (V_{GH}), and negative charge pump (V_{GL}) disabled.
6-4	Reserved	N/A	These bits are reserved for future use and should be programmed to 0 to ensure proper operation.
3	KMODE		This bit can be used to enable and disable boost converter 1's active discharge function.
		0	Boost converter 1 (AV_{DD}) active discharge enabled.
		1	Boost converter 1 (AV_{DD}) active discharge disabled.
2	WPEN		This bit can be used to enable and disable the write protect function.
		0	Disabled. WP not used and I^2C interface always active.
		1	Enabled. I^2C interface only active when WP pulled low.
1	DMODE		This bit determines which dimming mode is used by the WLED driver.
		0	Direct dimming.
		1	Phase-shift dimming.
0	RMODE		This bit determines which threshold is used to assert $\overline{RST}$ during power-down.
		0	V_{UVLO} threshold used.
		1	V_{DET} threshold used.

5.6.1.2 VCC (01h)

The VCC register can be written to and read from.

Figure 5-25. VCC Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						VCC	
						R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-5. VCC Register Field Descriptions

Bit	Field	Value	Description
7-2	Not implemented	N/A	These bits are not implemented. During write operations, data for these bits is ignored, and during read operations 0 is returned.
1-0	VCC		These bits determine the output voltage of the linear regulator (V_{CC}).
		0h	1.0 V
		1h	1.2 V
		2h	1.89 V
		3h	2.5 V

5.6.1.3 DLY1 (02h)

The DLY1 register can be written to and read from.

Figure 5-26. DLY1 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				DLY1			
				R/W-*0*	R/W-*0*	R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-6. DLY1 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during write operations 0 is returned.
3-0	DLY1		These bits determine how soon after V_{IN}>V_{UVLO} the linear regulator (V_{CC}) starts.
		0h	0 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms
		8h	40 ms
		9h	45 ms
		Ah	50 ms
		Bh	55 ms
		Ch	60 ms
		Dh	65 ms
		Eh	70 ms
		Fh	75 ms

5.6.1.4 AVDD (03h)

The AVDD register can be written to and read from.

Figure 5-27. AVDD Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented			AVDD				
			R/W-*0*	R/W-*1*	R/W-*1*	R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-7. AVDD Register Field Descriptions

Bit	Field	Value	Description
1	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
0	AVDD		These bits determine the output voltage of boost converter 1 (AV_{DD}).
		00h	6.5 V
		01h	6.6 V
		02h	6.7 V
		03h	6.8 V
		04h	6.9 V
		05h	7.0 V
		06h	7.1 V
		07h	7.2 V
		08h	7.3 V
		09h	7.4 V
		0Ah	7.5 V
		0Bh	7.6 V
		0Ch	7.7 V
		0Dh	7.8 V
		0Eh	7.9 V
		0Fh	8.0 V
		10h	8.1 V
		11h	8.2 V
		12h	8.3 V
		13h	8.4 V
		14h	8.5 V
		15h	8.6 V
		16h	8.7 V
		17h	8.8 V
		18h	8.9 V
		19h	9.0 V
		1Ah	9.1 V
		1Bh	9.2 V
		1Ch	9.3 V
		1Dh	9.4 V
		1Eh	9.5 V
		1Fh	9.6 V

5.6.1.5 FSW1 (04h)

The FSW1 register can be written to and read from.

Figure 5-28. FSW1 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						FSW1	
						R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-8. FSW1 Register Field Descriptions

Bit	Field	Value	Description
7-2	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
1-0	FSW1		These bits determine the switching frequency of boost converter 1 (AV_{DD}).
		0h	400 kHz
		1h	600 kHz
		2h	800 kHz
		3h	1 MHz

5.6.1.6 SS2 (05h)

The SS2 register can be written to and read from.

Figure 5-29. SS2 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				SS2			
				R/W-*0*	R/W-*1*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-9. SS2 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	SS2		These bits determine the soft-start time of boost converter 1 (AV_{DD}).
		0h	0.5 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms
		8h	40 ms
		9h	45 ms
		Ah	50 ms
		Bh	55 ms
		Ch	60 ms
		Dh	65 ms
		Eh	70 ms
		Fh	75 ms

5.6.1.7 DLY2 (06h)

The DLY2 register can be written to and read from.

Figure 5-30. DLY2 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				DLY2			
				R/W-*0*	R/W-*0*	R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-10. DLY2 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	DLY2		These bits determine how soon after $\overline{RST}$ goes high boost converter 1 (AV_{DD}) starts.
		0h	0 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms
		8h	40 ms
		9h	45 ms
		Ah	50 ms
		Bh	55 ms
		Ch	60 ms
		Dh	65 ms
		Eh	70 ms
		Fh	75 ms

5.6.1.8 VGL (07h)

The VGL register can be written to and read from.

Figure 5-31. VGL Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VGL			
				R/W-*1*	R/W-*0*	R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-11. VGL Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	VGL		These bits determine the output voltage of the negative charge pump (V_{GL}).
		0h	–5.0 V
		1h	–5.2 V
		2h	–5.4 V
		3h	–5.6 V
		4h	–5.8 V
		5h	–6.0 V
		6h	–6.2 V
		7h	–6.4 V
		8h	–6.6 V
		9h	–6.8 V
		Ah	–7.0 V
		Bh	–7.2 V
		Ch	–7.4 V
		Dh	–7.6 V
		Eh	–7.8 V
		Fh	–8.0 V

5.6.1.9 SS3 (08h)

The SS3 register can be written to and read from.

Figure 5-32. SS3 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					SS3		
					R/W-*0*	R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-12. SS3 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	SS3		These bits determine the soft-start time of the negative charge pump (V_{GL}).
		0h	0.256 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms

5.6.1.10 DLY3 (09h)

The DLY3 register can be written to and read from.

Figure 5-33. DLY3 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					DLY3		
					R/W-*0*	R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-13. DLY3 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	DLY3		These bits determine how soon after boost converter 1 (AV_{DD}) starts the negative charge pump (V_{GL}) starts.
		0h	0 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms

5.6.1.11 VGH (0Ah)

The VGH register can be written to and read from.

Figure 5-34. VGH Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VGH			
				R/W-*0*	R/W-*1*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-14. VGH Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	VGH		These bits determine the output voltage of boost converter 2 (V_{GH}).
		0h	18.0 V
		1h	18.5 V
		2h	19.0 V
		3h	19.5 V
		4h	20.0 V
		5h	20.5 V
		6h	21.0 V
		7h	21.5 V
		8h	22 0 V
		9h	22.5 V
		Ah	23.0 V
		Bh	23.5 V
		Ch	24.0 V
		Dh	24.5 V
		Eh	25.0 V
		Fh	25.5 V

5.6.1.12 SS4 (0Bh)

The SS4 register can be written to and read from.

Figure 5-35. SS4 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					SS4		
					R/W-*0*	R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-15. SS4 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	SS4		These bits determine the soft-start time of boost converter 2 (V_{GH}).
		0h	0.256 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms

5.6.1.13 FSW3 (0Ch)

The FSW3 register can be written to and read from.

Figure 5-36. FSW3 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						FSW3	
						R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-16. FSW3 Register Field Descriptions

Bit	Field	Value	Description
7-2	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
1-0	FSW3		These bits determine the switching frequency of boost converter 3 (WLED).
		0h	400 kHz
		1h	600 kHz
		2h	800 kHz
		3h	1 MHz

5.6.1.14 DLY4 (0Dh)

The DLY4 register can be written to and read from.

Figure 5-37. DLY4 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					DLY4		
					R/W-*0*	R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-17. DLY4 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	DLY4		These bits determine the start-up delay of the gate voltage shaping function.
		0h	0 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms

5.6.1.15 OVP (0Eh)

The OVP register can be written to and read from.

Figure 5-38. OVP Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						OVP	
						R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-18. OVP Register Field Descriptions

Bit	Field	Value	Description
7-2	Not implemented	N/A	These bits are not implemented. During write operations, data for these bits is ignored, and during read operations 0 is returned.
1-0	OVP		These bits determine the overvoltage threshold of boost converter 3 (WLED).
		0h	30 V
		1h	33 V
		2h	36 V
		3h	39 V

5.6.1.16 FDIM (OFh)

The FDIM register can be written to and read from.

Figure 5-39. FDIM Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					FDIM		
					R/W-*1*	R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-19. FDIM Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	FDIM		These bits determine the WLED driver's output dimming frequency in phase-shift dimming mode.
		0h	15 kHz
		1h	16 kHz
		2h	17 kHz
		3h	18 kHz
		4h	19 kHz
		5h	20 kHz
		6h	21 kHz
		7h	22 kHz

5.6.1.17 RESET (10h)

The RESET register can be written to and read from.

Figure 5-40. RESET Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				RESET			
				R/W-*0*	R/W-*1*	R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-20. RESET Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	RESET		These bits determine the duration of the reset pulse ($\overline{RST}$).
		0h	0 ms
		1h	1 ms
		2h	2 ms
		3h	3 ms
		4h	4 ms
		5h	5 ms
		6h	6 ms
		7h	7 ms
		8h	8 ms
		9h	9 ms
		Ah	10 ms
		Bh	11 ms
		Ch	12 ms
		Dh	13 ms
		Eh	14 ms
		Fh	15 ms

5.6.1.18 VDET (11h)

The VDET register can be written to and read from.

Figure 5-41. VDET Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VDET			
				R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-21. VDET Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	VDET		These bits determine the threshold voltage of the $\overline{XAO}$ signal.
		0h	V_{UVLO}
		1h	2.0 V
		2h	2.1 V
		3h	2.2 V
		4h	2.3 V
		5h	2.4 V
		6h	2.5 V
		7h	2.6 V
		8h	2.7 V
		9h	2.8 V
		Ah	2.9 V
		Bh	3.0 V
		Ch	3.0 V
		Dh	3.0 V
		Eh	3.0 V
		Fh	3.0 V

5.6.1.19 DLY6 (12h)

The DLY6 register can be written to and read from.

Figure 5-42. DLY6 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					DLY6		
					R/W-*0*	R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-22. DLY6 Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	DLY6		These bits determine the start-up delay time of the $\overline{\text{XAO}}$ signal.
		0h	0 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	20 ms
		5h	25 ms
		6h	30 ms
		7h	35 ms

5.6.1.20 VMAX (13h)

The VMAX register can be written to and read from.

Figure 5-43. VMAX Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VMAX			
				R/W-*0*	R/W-*1*	R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-23. VMAX Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	VMAX		These bits determine the maximum V_{COM} voltage.
		0h	2.5/8 × AV_{DD}
		1h	2.6/8 × AV_{DD}
		2h	2.7/8 × AV_{DD}
		3h	2.8/8 × AV_{DD}
		4h	2.9/8 × AV_{DD}
		5h	3.0/8 × AV_{DD}
		6h	3.1/8 × AV_{DD}
		7h	3.2/8 × AV_{DD}
		8h	3.3/8 × AV_{DD}
		9h	3.4/8 × AV_{DD}
		Ah	3.5/8 × AV_{DD}
		Bh	3.6/8 × AV_{DD}
		Ch	3.7/8 × AV_{DD}
		Dh	3.8/8 × AV_{DD}
		Eh	3.9/8 × AV_{DD}
		Fh	4.0/8 × AV_{DD}

5.6.1.21 VMIN (14h)

The VMIN register can be written to and read from.

Figure 5-44. VMIN Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VMIN			
				R/W-*0*	R/W-*1*	R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-24. VMIN Register Field Descriptions

Bit	Field	Value	Description
7-4	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
3-0	VMIN		These bits determine the minimum V_{COM} voltage.
		0h	2.0/8 × AV_{DD}
		1h	2.1/8 × AV_{DD}
		2h	2.2/8 × AV_{DD}
		3h	2.3/8 × AV_{DD}
		4h	2.4/8 × AV_{DD}
		5h	2.5/8 × AV_{DD}
		6h	2.6/8 × AV_{DD}
		7h	2.7/8 × AV_{DD}
		8h	2.8/8 × AV_{DD}
		9h	2.9/8 × AV_{DD}
		Ah	3.0/8 × AV_{DD}
		Bh	3.1/8 × AV_{DD}
		Ch	3.2/8 × AV_{DD}
		Dh	3.3/8 × AV_{DD}
		Eh	3.4/8 × AV_{DD}
		Fh	3.5/8 × AV_{DD}

5.6.1.22 USER (15h)

The USER register can be written to and read from.

Figure 5-45. USER Register Bit Allocation

7	6	5	4	3	2	1	0
USER							
R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-25. USER Register Field Descriptions

Bit	Field	Value	Description
7-0	USER	N/A	These bits are free for customer use. Their contents have no effect on device operation.

5.6.1.23 CONTROL (FFh)

Figure 5-46. CONTROL Register Bit Allocation

7	6	5	4	3	2	1	0
WED	Not Implemented						RED
R/W-*0*							R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-26. CONTROL Register Field Descriptions

Bit	Field	Value	Description
7	WED		This bit determines whether write operations affect the contents of the volatile or non-volatile registers.
		0h	Not applicable (see below).
		1h	Data is copied from the RAM registers to the EEPROM registers. This bit is automatically reset upon completion of this task.
6-1	Not Implemented	N/A	These bits are not implemented. During write operations data for these bits is ignored, and during read operations 0 is returned.
0	RED		This bit determines whether read operations return the contents of the volatile or non-volatile registers.
		0h	Volatile register data is returned.
		1h	Non-volatile register data is returned.

5.6.2 VCOM Registers

5.6.2.1 VCOM DATA (Slave Address 28h, Register Address 00h)

The VCOM DATA register can be written to and read from.

Figure 5-47. VCOM DATA Register Bit Allocation

7	6	5	4	3	2	1	0
NI	VCOM						
R-*0*	R/W-*1*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-27. VCOM DATA Register Bit Description

Bit	Field	Value	Description
7	Not implemented	N/A	This bit is reserved for future use and should be programmed to 0 for proper operation.
6-0	VCOM		Bits 6 through 0 set the value of the V_{COM} voltage.
		N/A	V_{COM}=(VCOM/127) × (V_{MAX}–V_{MIN}) + V_{MIN}

5.6.2.2 VCOM CONTROL (Slave Address 28h, Register Address 02h)

The VCOM CONTROL register is write-only.

Figure 5-48. VCOM CONTROL Register Bit Allocation

7	6	5	4	3	2	1	0
SEL	Not Implemented						
R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -n = factory default

Table 5-28. VCOM CONTROL Register Bit Description

Bit	Field	Value	Description
7	SEL		The SEL bit determines whether read/write operations to the VCOM DATA register access the IVR, the WR, or both.
		0	Write operations store data in the IVR *and* WR. Read operations return the contents of the IVR.
		1	Write operations store data in the WR only. Read operations return the contents of the WR.
6-0	Not implemented	N/A	Bits 6 through 0 are reserved for future use. They should be programmed to 0 for proper operation.

6 Application and Implementation

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The TPS65154 devices is intended primarily for use in notebook PC and tablet applications. It needs these two supply voltages

- A regulated 3.3-V or 5-V supply for the LCD bias functions
- A direct connection to the battery for the WLED driver functions

The device configuration parameters are set by I^2C interface and stored in the on-chip nonvolatile memory.

6.2 Typical Application

Figure 6-1 shows the recommended application circuit for typical applications. The I^2C interface is used to optimize the circuit's operating parameters for a specific application. If different component values are used, make sure that the values are within the recommended operating conditions (see *Recommended Operating Conditions*). If different component values are used, the compensation components may also need to be optimized for stability and best performance.

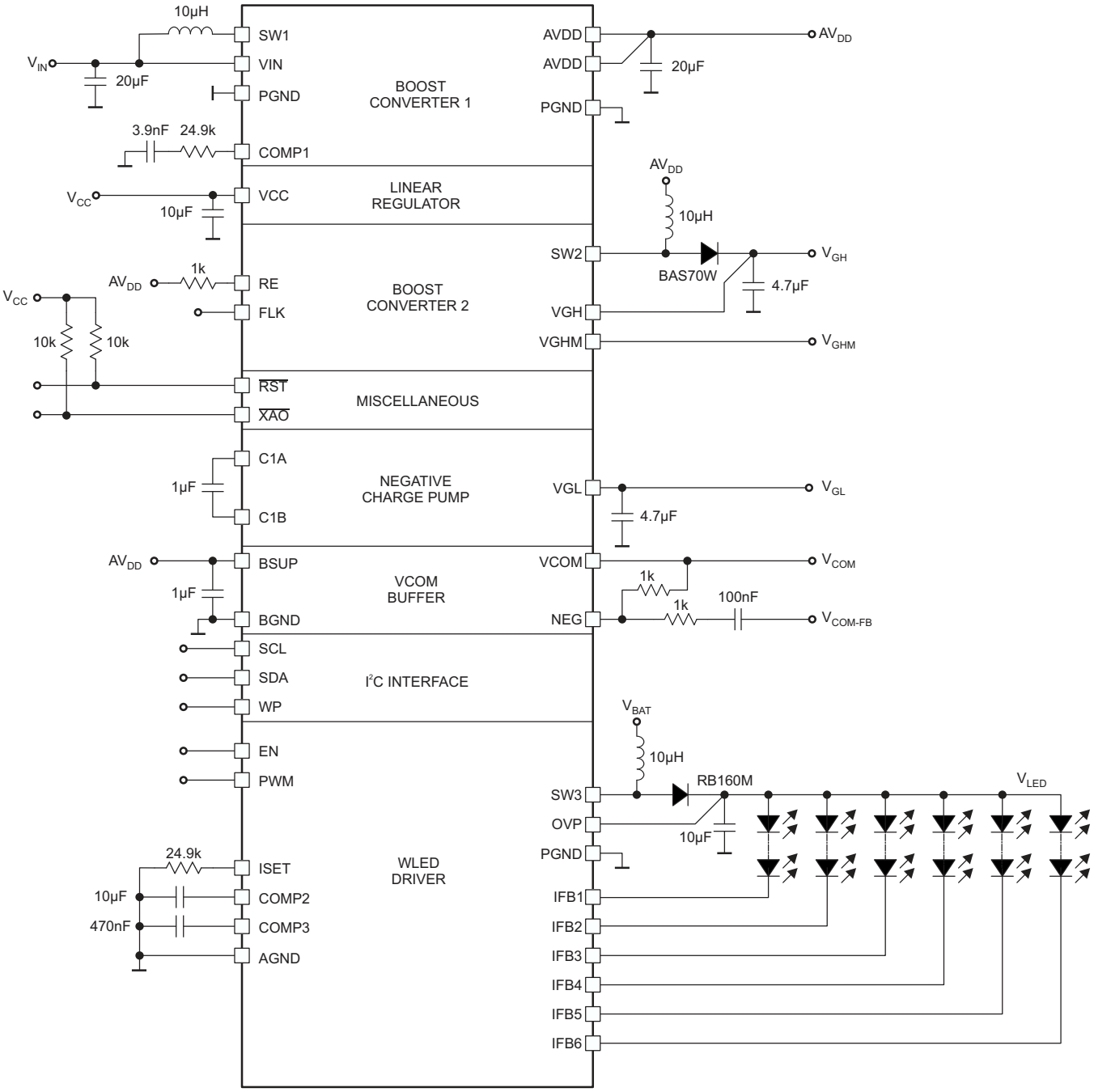


Figure 6-1. Typical Application Circuit

6.2.1 Design Requirements

This design example uses the parameters listed in Table 6-1 as the input parameters.

Table 6-1. Input Parameters

PARAMETER	SYMBOL	VALUE
Input supply voltage – LCD bias functions	V_{IN}	3.3 V
Input supply voltage – WLED driver	V_{BAT}	9 V to 21 V

Table 6-1. Input Parameters (continued)

PARAMETER	SYMBOL	VALUE
Boost converter 1 output voltage	AV_{DD}	8 V
Inverting charge pump output voltage	V_{GL}	–6.8 V
Boost converter 2 output voltage	V_{GH}	20 V
Linear regulator output voltage	V_{CC}	2.5 V
WLED driver output current (per string)	I_{SET}	50 mA

6.2.2 Detailed Design Procedure

6.2.2.1 External Component Selection

Care should be applied to the choice of external components since they greatly affect overall performance. The TPS65154 was developed with the twin goals of high performance and small/low-profile solution size. Since these two goals are often in direct opposition to one another (for example, larger inductors tend to achieve higher efficiencies), some trade-off is always necessary.

Inductors must have adequate current capability so that they do not saturate under worst-case conditions. For high efficiency, they should also have low dc resistance (DCR).

Capacitors must have adequate *effective* capacitance under the applicable dc bias conditions they experience in the application. MLCC capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions and this must be taken into consideration when selecting them. This problem is especially acute in low profile capacitors, in which the dielectric field strength is higher than in taller components. In general, the capacitance values shown in circuit diagrams in this data sheet refer to the *effective* capacitance after dc bias effects have been taken into consideration. Reputable capacitor manufacturers provide capacitance versus dc bias curves that greatly simplify component selection.

The following tables list some components suitable for use with the TPS65154. The list is not exhaustive – other components may exist that are equally suitable (or better), however, these components have been proven to work well and were used extensively during the development of the TPS65154.

Table 6-2. Linear Regulator External Component Recommendations

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	MAX. THICKNESS
C_{OUT}	10 µF, 6.3 V, ±20%, X5R, 0603	GRM188R60J106ME84	Murata	0.95 mm

Table 6-3. Boost Converter 1 External Components

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	MAX. THICKNESS
L	10 µH, 1.5 A, 0.205 Ω	NRS6012T100MMGG	Taiyo Yuden	1.2 mm
C_{OUT}	10 µF, 16 V, ±10%, X5R, 1206	GRM319R61C106KE15D	Murata	0.85 ±0.1 mm

Table 6-4. Boost Converter 2 External Components

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	MAX. THICKNESS
L	10 µH, 0.6 A	NRH3010T100MN	Taiyo Yuden	1 mm
C_{OUT}	4.7 µF, 50 V, ±10%, X5R, 1206	GRM319R61H475KA12	Murata	0.95 mm

Table 6-5. Boost Converter 3 External Components

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	MAX. THICKNESS
L	10 µH, 1.5 A, 0.205 Ω	NRS6012T100MMGGJ	Taiyo Yuden	1.2 mm
C_{OUT}	4.7 µF, 50 V, ±10%, X5R, 1206	GRM319R61H475KA12	Murata	0.95 mm

6.2.3 Application Curves

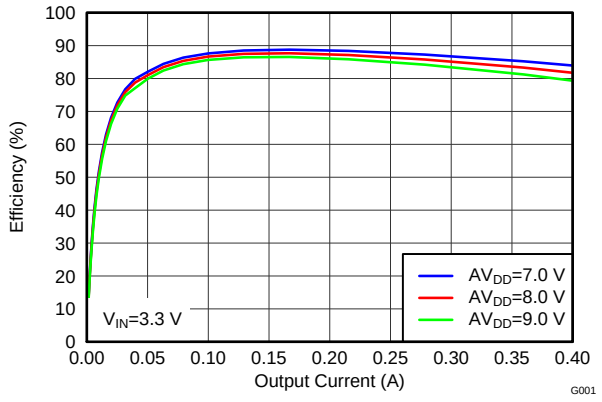


Figure 6-2. Boost Converter 1 (AV_{DD}) Efficiency

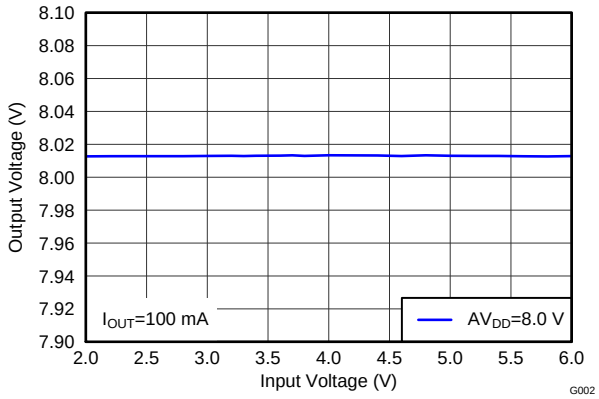


Figure 6-3. Boost Converter 1 (AV_{DD}) Line Regulation

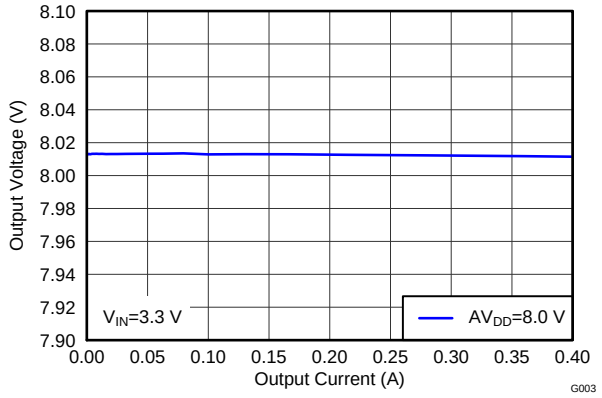


Figure 6-4. Boost Converter 1 (AV_{DD}) Load Regulation

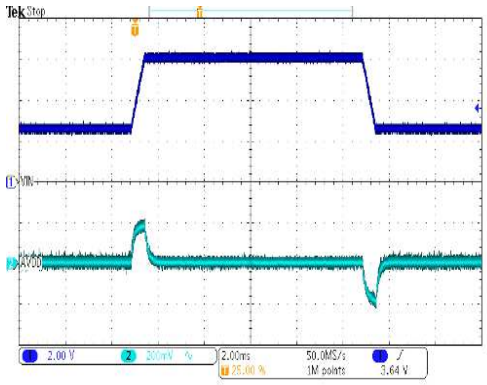


Figure 6-5. Boost Converter 1 (AV_{DD}) Line Transient Response

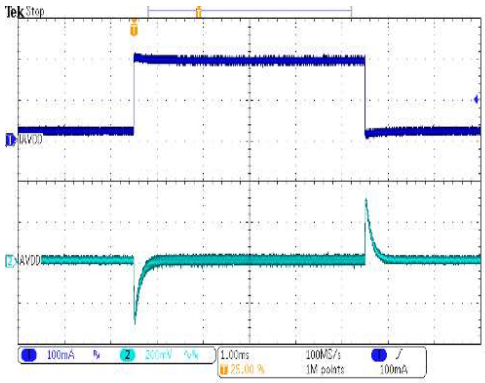


Figure 6-6. Boost Converter 1 (AV_{DD}) Load Transient Response

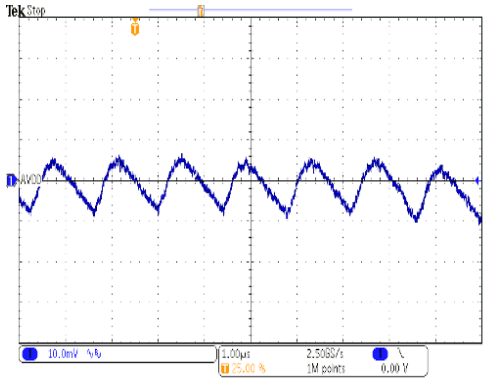


Figure 6-7. Boost Converter 1 (AV_{DD}) Output Voltage Ripple

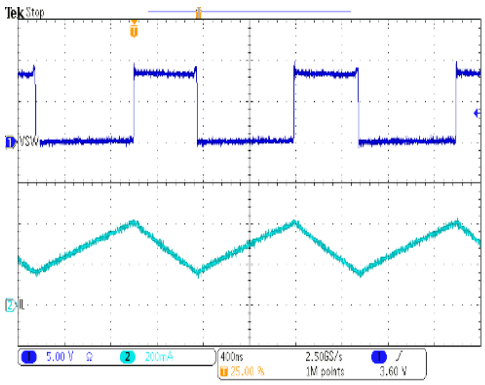


Figure 6-8. Boost Converter 1 (AV_{DD}) Switching Waveforms

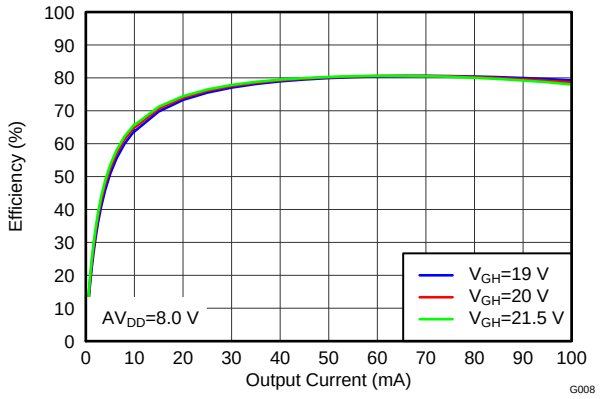


Figure 6-9. Boost Converter 2 (V_{GH}) Efficiency

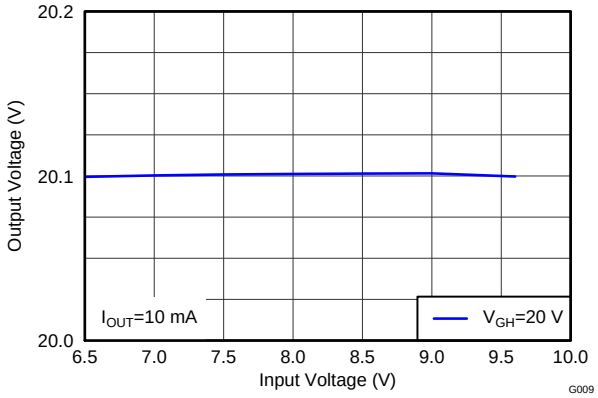


Figure 6-10. Boost Converter 2 (V_{GH}) Line Regulation

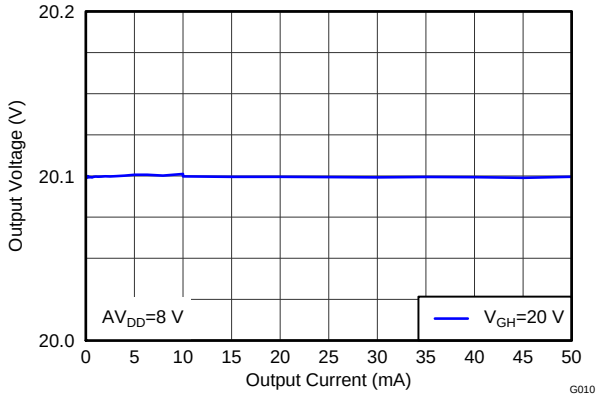


Figure 6-11. Boost Converter 2 (V_{GH}) Load Transient Response

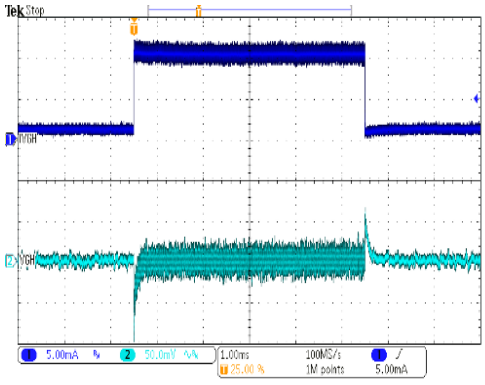


Figure 6-12. Boost Converter 2 (V_{GH}) Load Transient Response

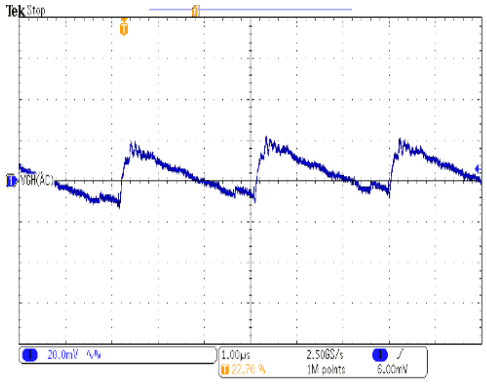


Figure 6-13. Boost Converter 2 (V_{GH}) Output Voltage Ripple

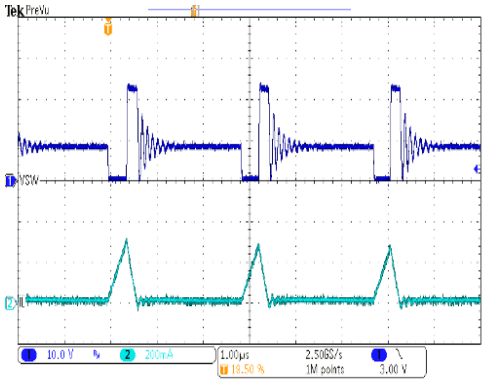


Figure 6-14. Boost Converter 2 (V_{GH}) Switching Waveforms

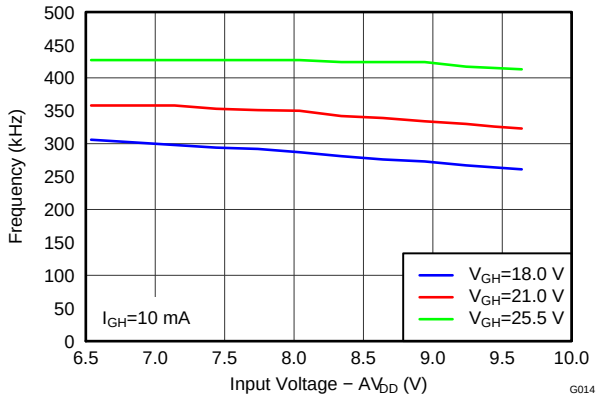


Figure 6-15. Boost Converter 2 (V_{GH}) Switching Frequency

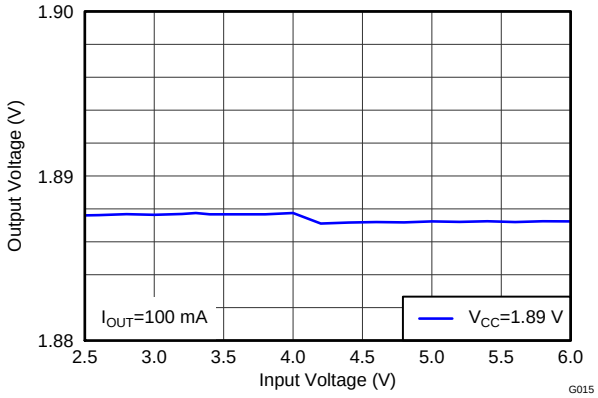


Figure 6-16. Linear Regulator (V_{CC}) Line Regulation

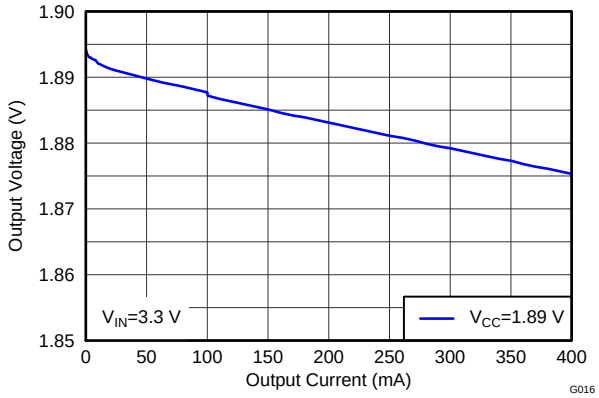


Figure 6-17. Linear Regulator (V_{CC}) Load Regulation

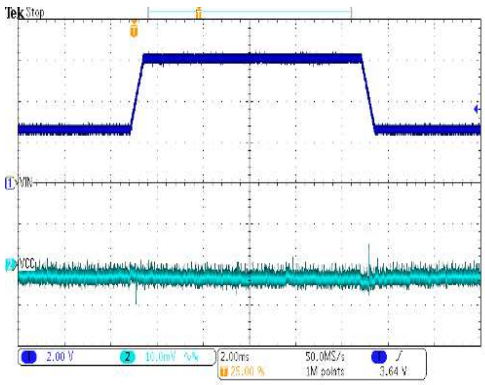


Figure 6-18. Linear Regulator (V_{CC}) Line Transient Response

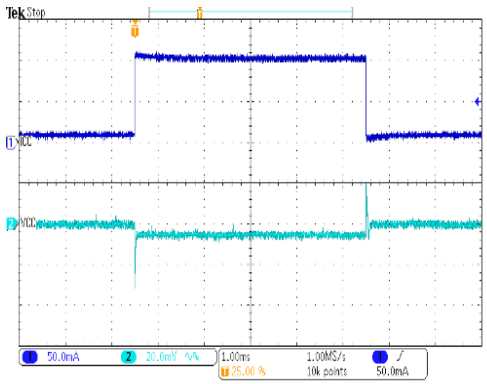


Figure 6-19. Linear Regulator (V_{CC}) Load Transient Response

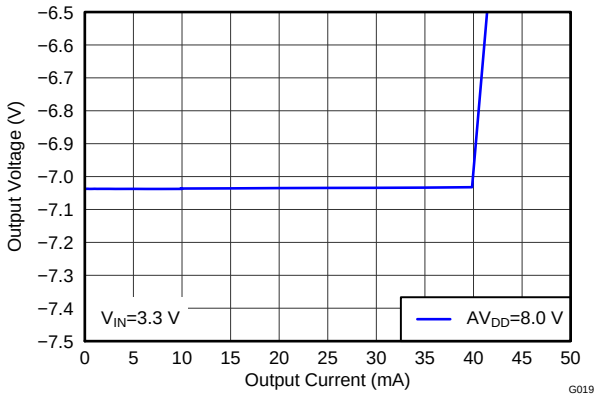


Figure 6-20. Negative Charge Pump (V_{GL}) Load Regulation

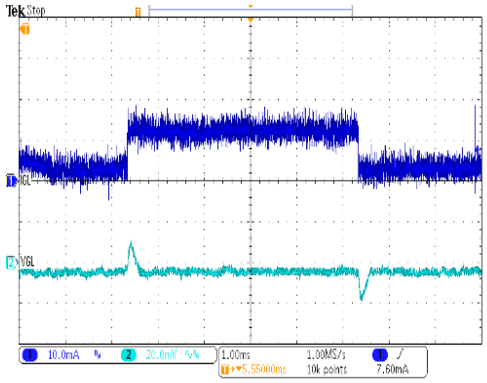


Figure 6-21. Negative Charge Pump (V_{GL}) Load Transient Response

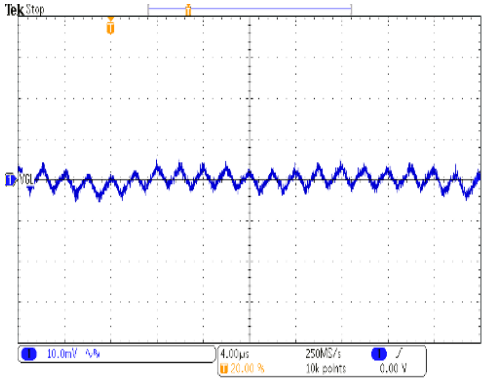


Figure 6-22. Negative Charge Pump (V_{GL}) Output Voltage Ripple

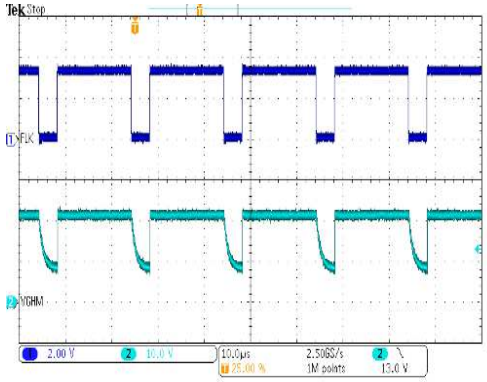


Figure 6-23. Gate Voltage Shaping (V_{GHM}) Switching Waveforms

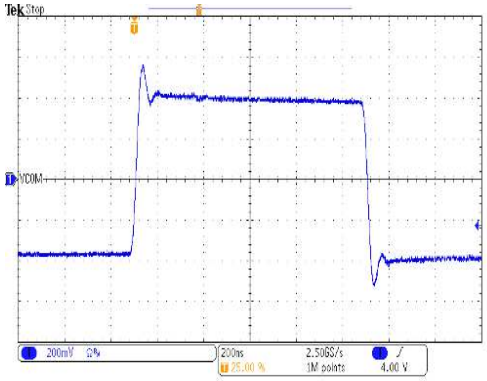


Figure 6-24. VCOM Buffer Large-Signal Response

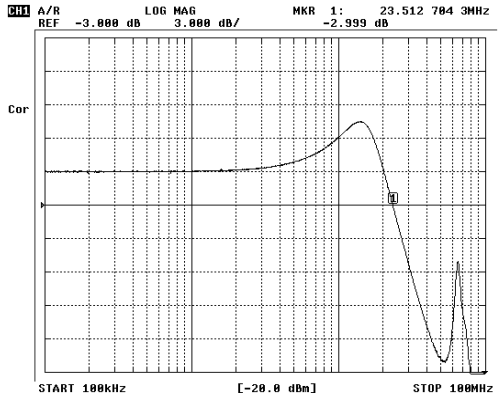


Figure 6-25. VCOM Buffer Small-Signal Bandwidth

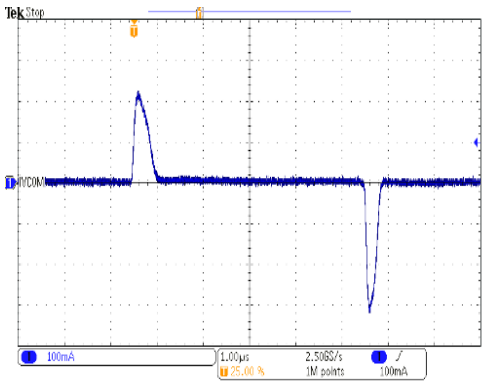


Figure 6-26. VCOM Buffer Peak Output Current

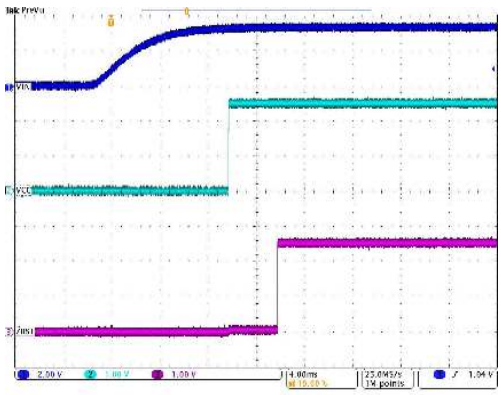


Figure 6-27. LCD Bias Power-Up Sequencing

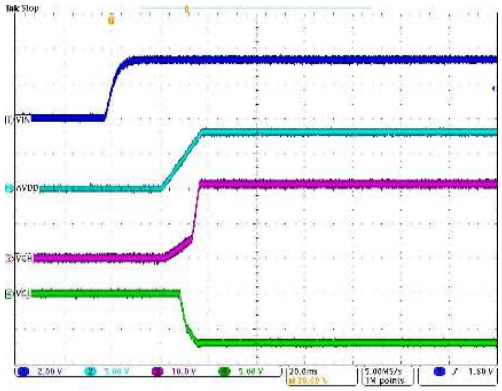


Figure 6-28. LCD Bias Power-Up Sequencing

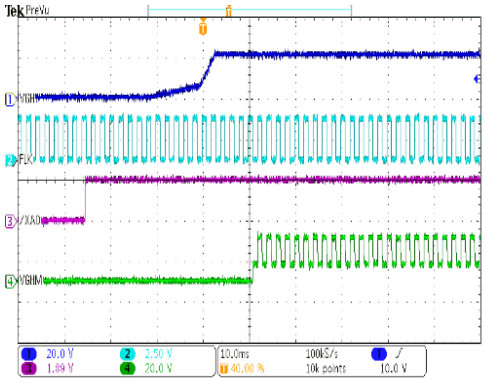


Figure 6-29. LCD Bias Power-Up Sequencing

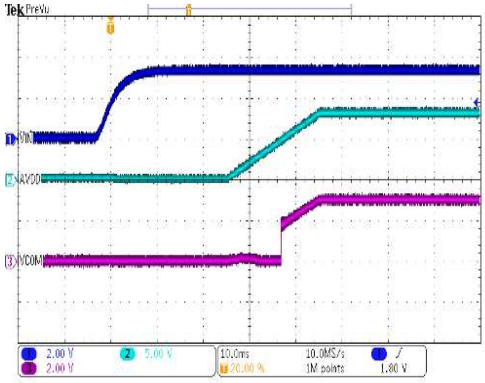


Figure 6-30. LCD Bias Power-Up Sequencing

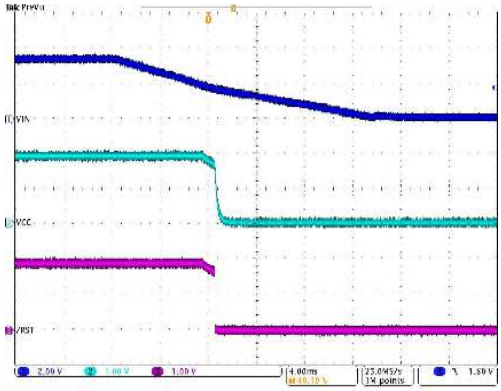


Figure 6-31. LCD Bias Power-Down Sequencing

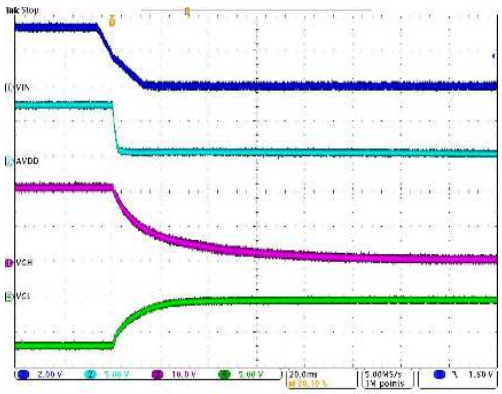


Figure 6-32. LCD Bias Power-Down Sequencing

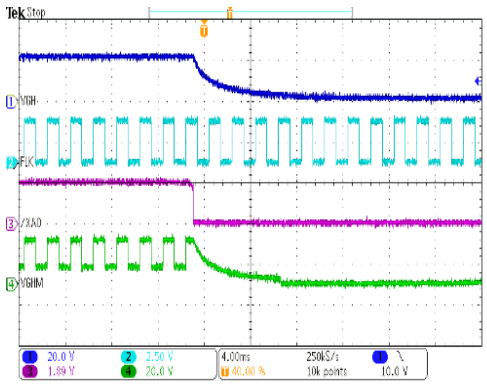


Figure 6-33. LCD Bias Power-Down Sequencing

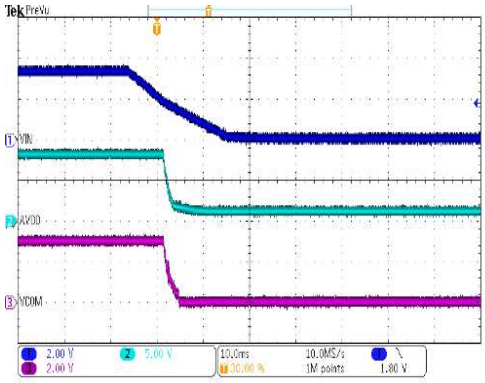


Figure 6-34. LCD Bias Power-Down Sequencing

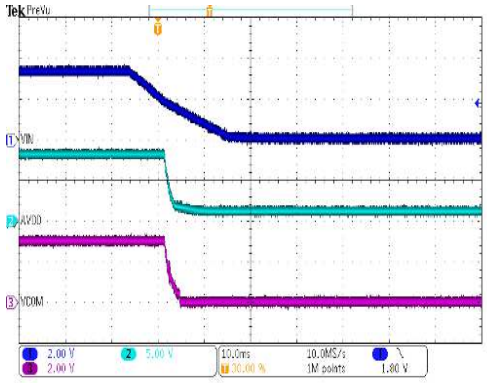


Figure 6-35. Boost Converter 3 (V_{LED}) Efficiency

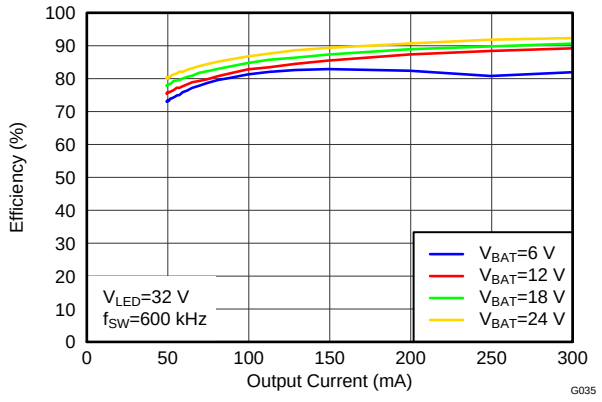


Figure 6-36. Boost Converter 3 (V_{LED}) Efficiency

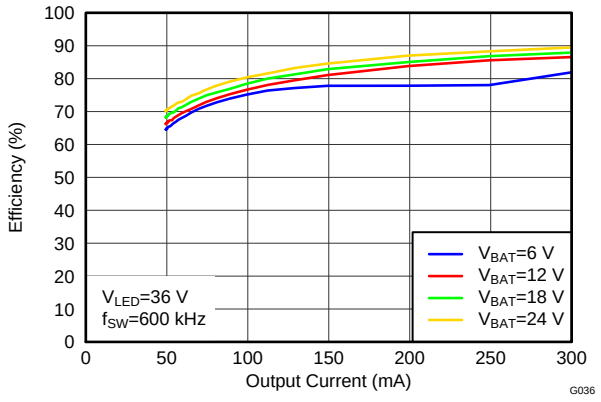


Figure 6-37. Boost Converter 3 (V_{LED}) Efficiency

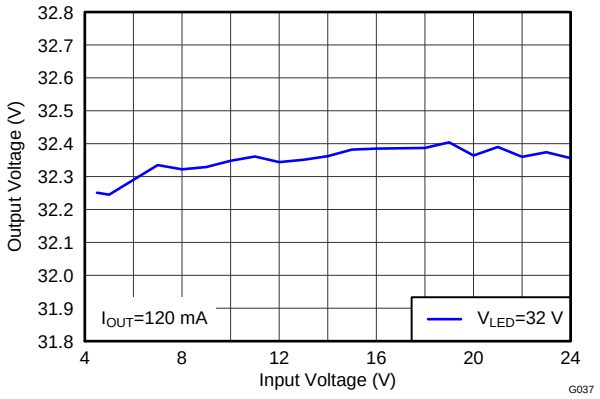


Figure 6-38. Boost Converter 3 (V_{LED}) Line Regulation

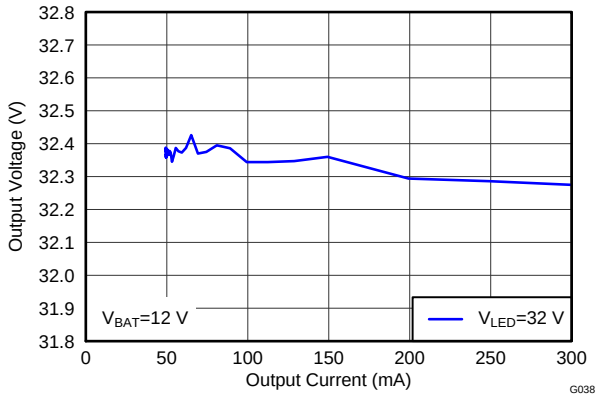


Figure 6-39. Boost Converter 3 (V_{LED}) Load Regulation

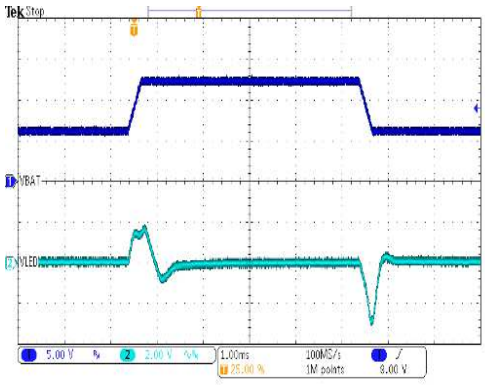


Figure 6-40. Boost Converter 3 (V_{LED}) Line Transient Response

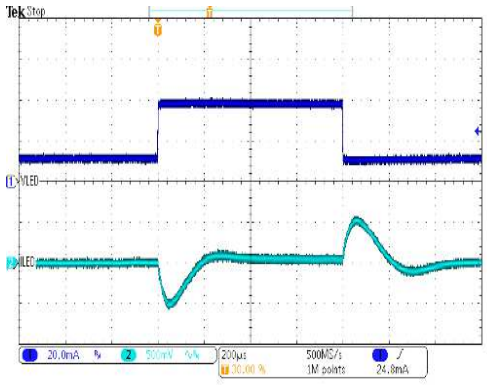


Figure 6-41. Boost Converter 3 (V_{LED}) Load Transient Response

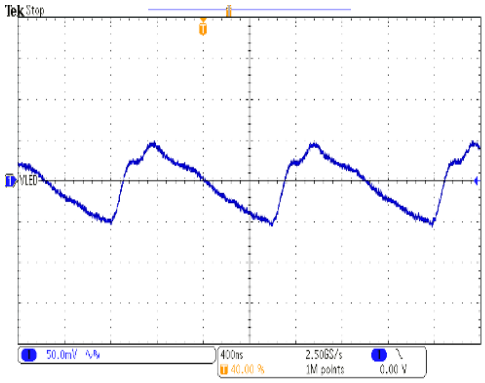


Figure 6-42. Boost Converter 3 (V_{LED}) Output Voltage Ripple

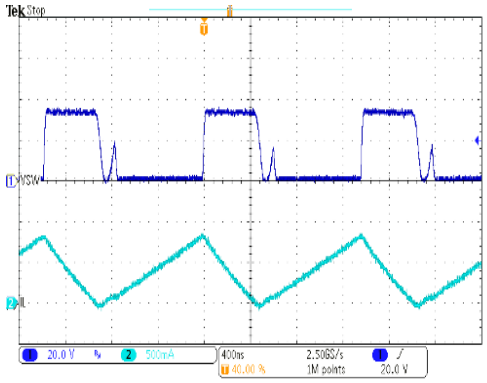


Figure 6-43. Boost Converter 3 (V_{LED}) Switching Waveforms

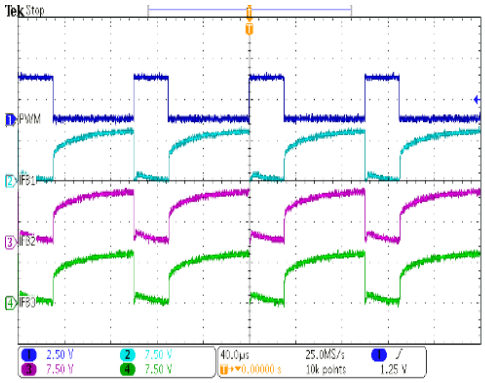


Figure 6-44. PWM Direct Dimming Waveforms

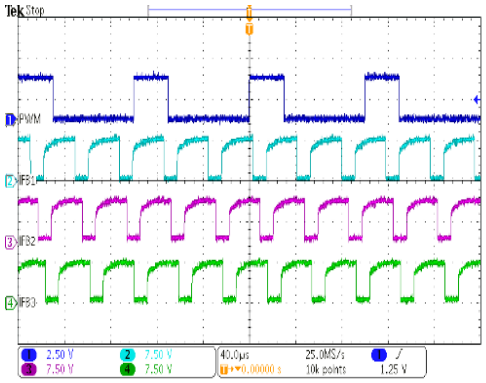


Figure 6-45. PWM Phase-Shifted Dimming

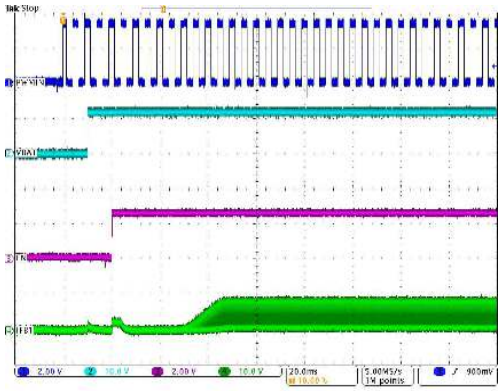


Figure 6-46. WLED Driver Power-Up Sequence

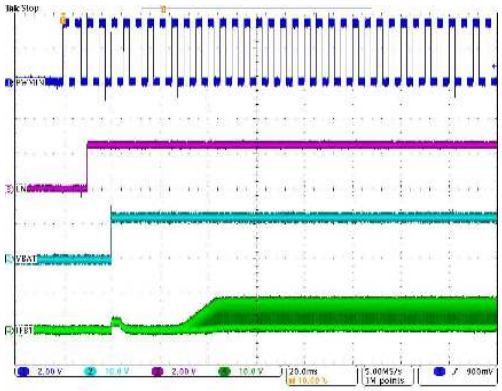


Figure 6-47. WLED Driver Power-Up Sequence

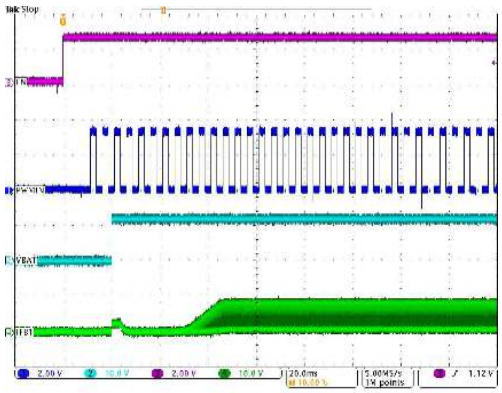


Figure 6-48. WLED Driver Power-Up Sequence

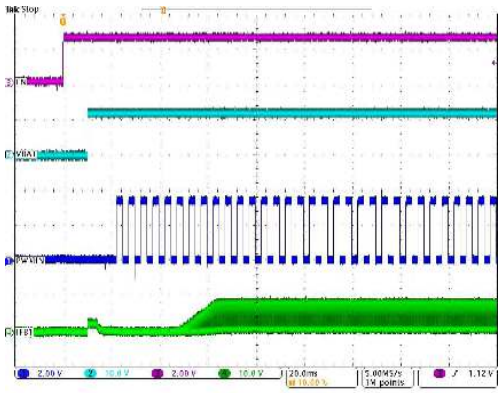


Figure 6-49. WLED Driver Power-Up Sequence

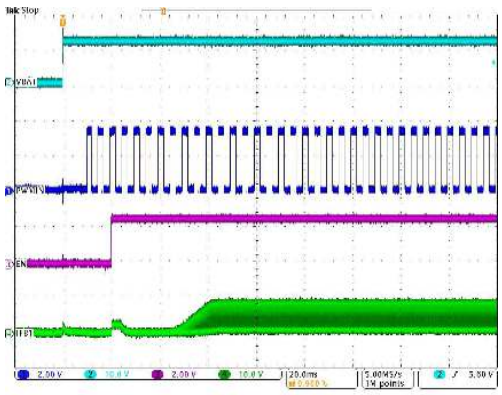


Figure 6-50. WLED Driver Power-Up Sequence

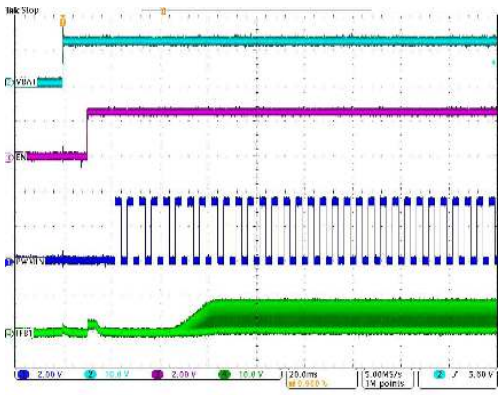


Figure 6-51. WLED Driver Power-Up Sequence

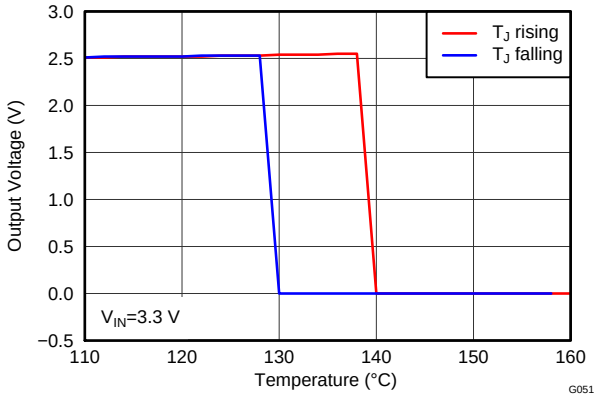


Figure 6-52. Thermal Shutdown

7 Power Supply Recommendations

The TPS65154 device is designed to operate with two input supplies:

- One supply in the range 2 V to 5.5 V powers the LCD bias functions. Typically, this is a regulated 3.3-V or 5-V supply generated by a dc-dc converter somewhere else in the system. Note that this supply must be higher than 2.5 V if the user wants to program the EEPROM.
- One supply in the range 4.5 V to 24 V powers the WLED driver boost converter. Typically, this is an unregulated supply taken from the battery system in a notebook PC or tablet.

The input supplies must be stable and free of noise to achieve the full performance of the device. If the input supplies are located more than a few centimeters away from the TPS65154 device, additional bulk capacitance may be required. The input capacitance shown in Figure 6-1 is sufficient for typical applications.

8 Layout

8.1 Layout Guidelines

The PCB layout is an important step in a power supply design. An incorrect layout can cause converter instability, load regulation problems, noise, and EMI issues. The list of recommendations below highlights the most important points to consider when doing the layout for the TPS65154 device. However, all PCB layout is a trade-off between theory and practice, and some compromise is always necessary.

- If possible, use a 4-layer PCB. Route high di/dt signals on layer 1 and use the second layer to form a solid ground plane. If a 2-layer PCB is used, route high di/dt signals on layer 1 and add a copper pour connected to ground on the bottom layer.
- Place a decoupling capacitor close to the VIN pin. Use short, wide traces on layer 1 to connect to it.
- Place at least one of the boost converter 1 output capacitors close to the device. Use short, wide traces on layer 1 to connect it between pins 3 and 4, and pin 6.
- Place the boost converter 3 rectifier diode and output capacitor close to the device. Use short, wide traces on layer 1 to connect them to pins 9 and 10.
- Place the boost converter 2 rectifier diode and output capacitor close to the device. Use short, wide traces on layer 1 to connect them to pins 33 and 34.
- Place the flying capacitor connected to pins 19 and 20 and the output capacitor connected to pin 18 close to the device. Use short, wide traces on layer 1 to connect to them.
- Place the VCOM buffer decoupling capacitor connected between pin 2 and pin 47 close to the device. Use short, wide traces on layer 1 to connect to it.
- Route the signals to the compensation components connected to pin 7, pin 40 and pin 46 away from noisy signals.
- Use thermal vias to connect the thermal pad to a large, unbroken copper ground plane (typically, on layer 2).

8.2 Layout Example

Figure 8-1 shows the main features of the TPS65154 Evaluation Module PCB layout.

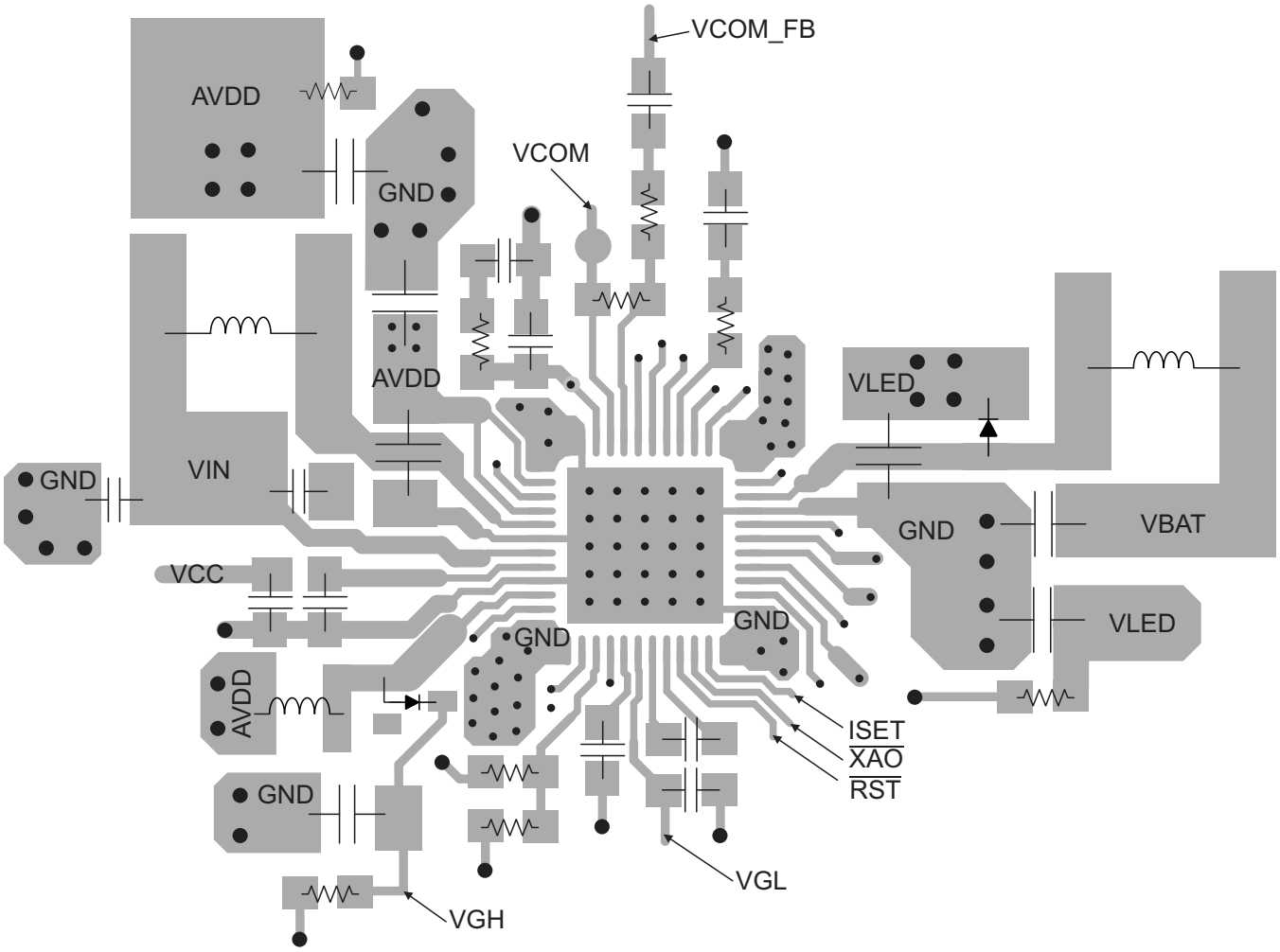


Figure 8-1. Example PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

9.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65154RSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65154	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

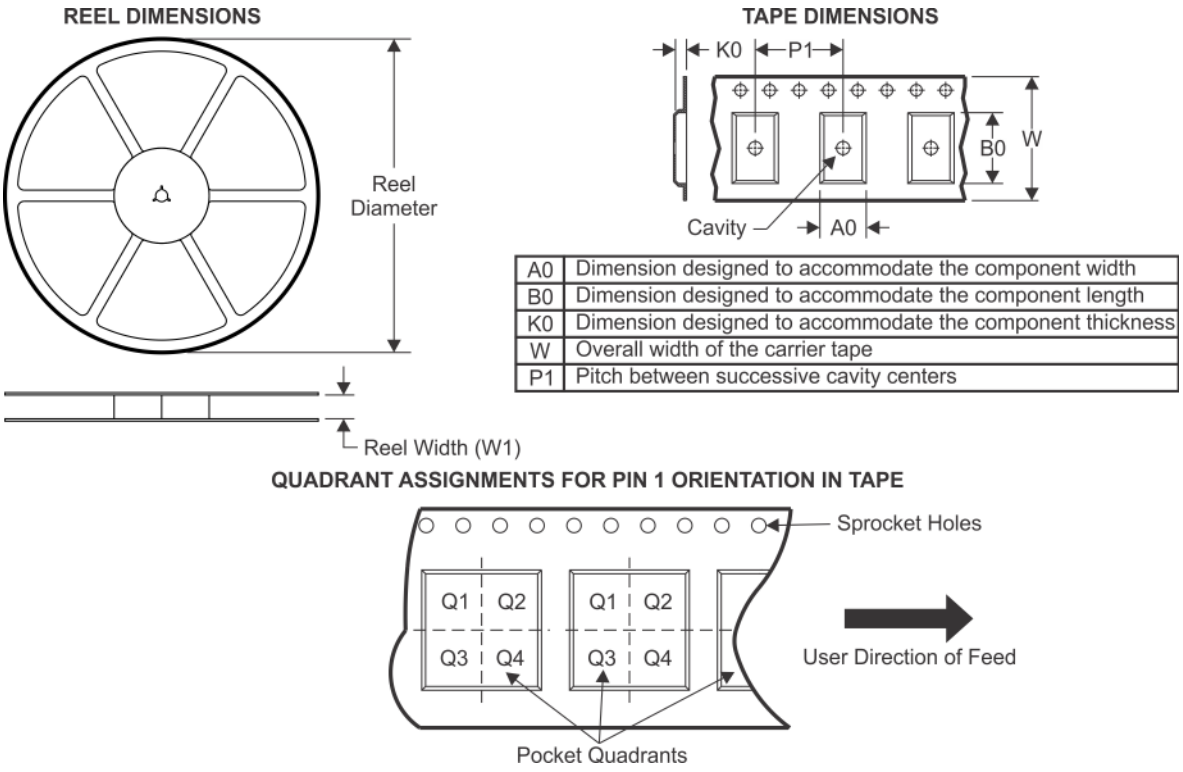
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

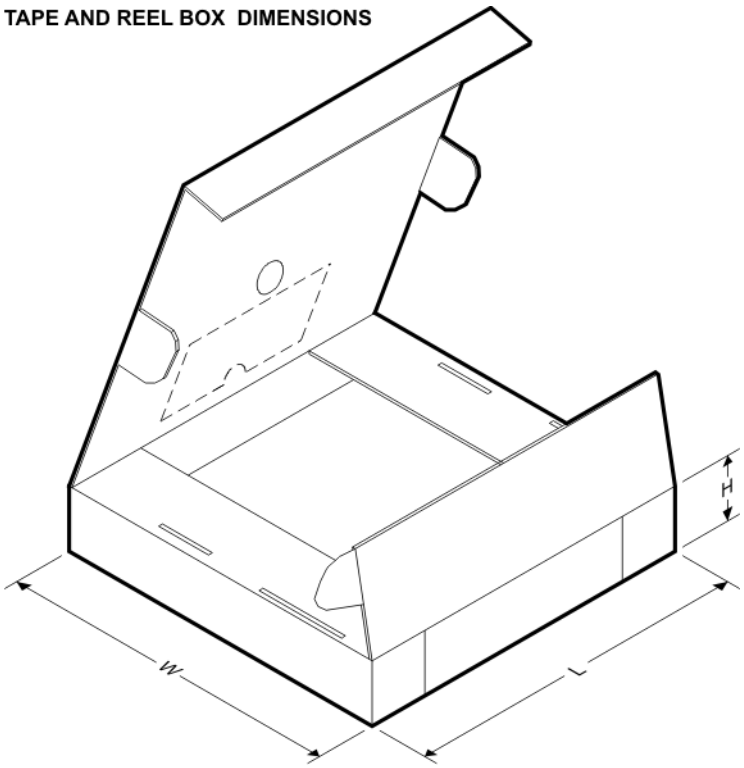


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65154RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

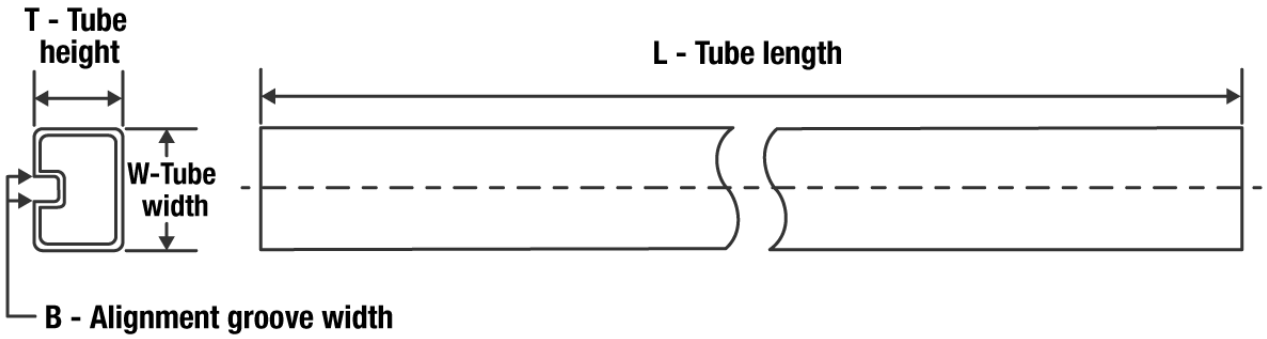
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65154RSLR	VQFN	RSL	48	2500	552.0	367.0	38.0

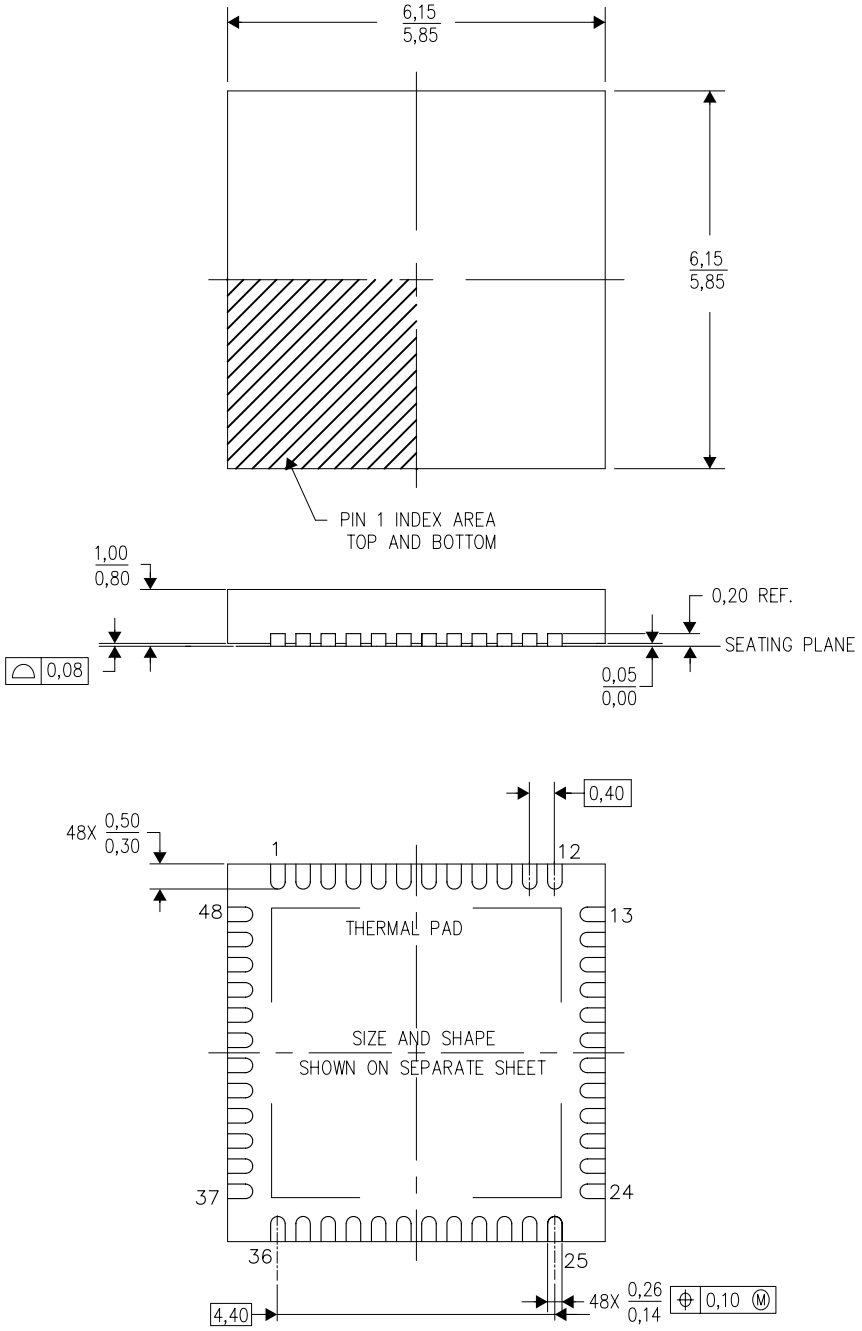
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS65154RSLR	RSL	VQFN	48	2500	381.5	7.92	2286	0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



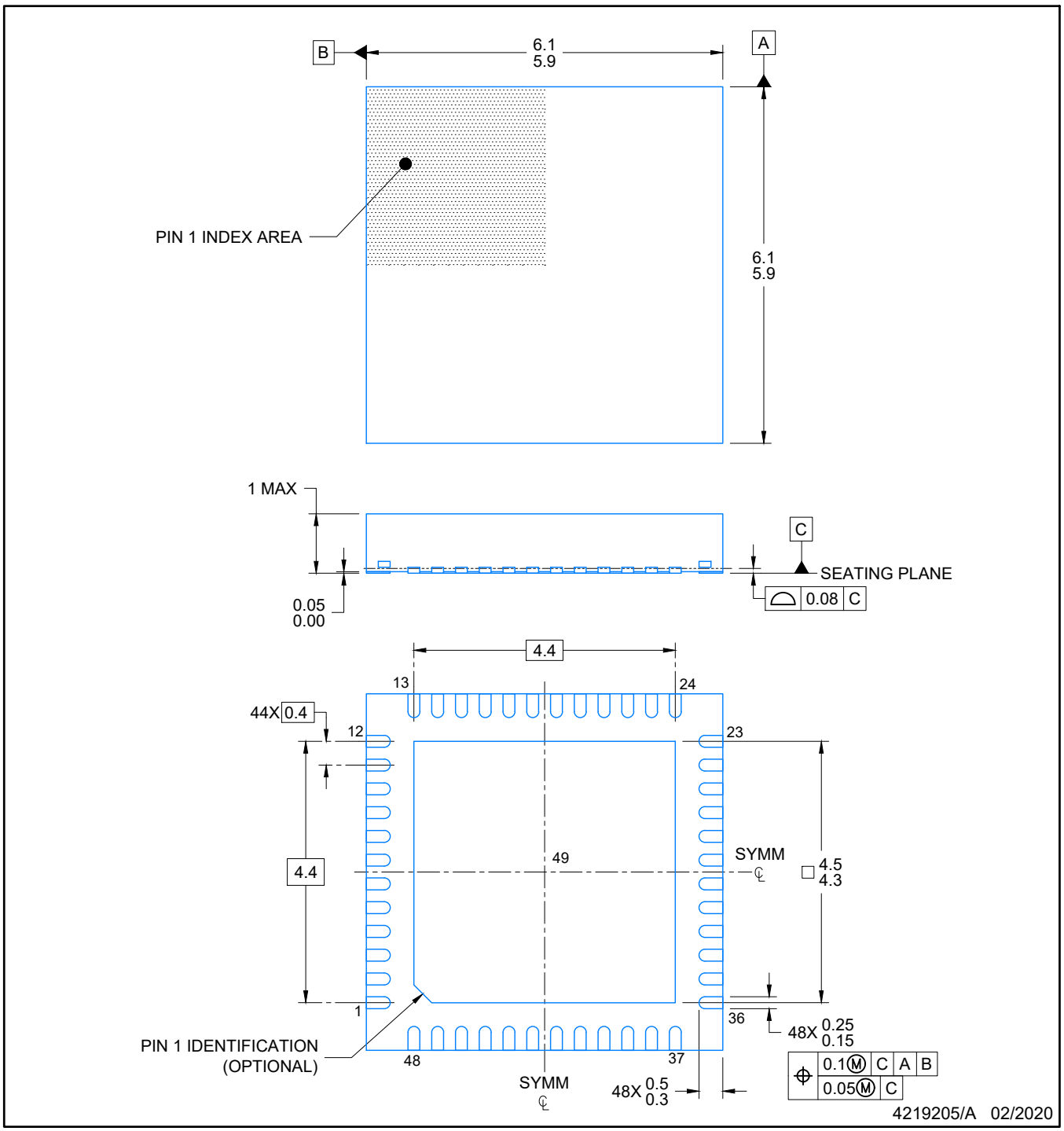
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PACKAGE OUTLINE

RSL0048B

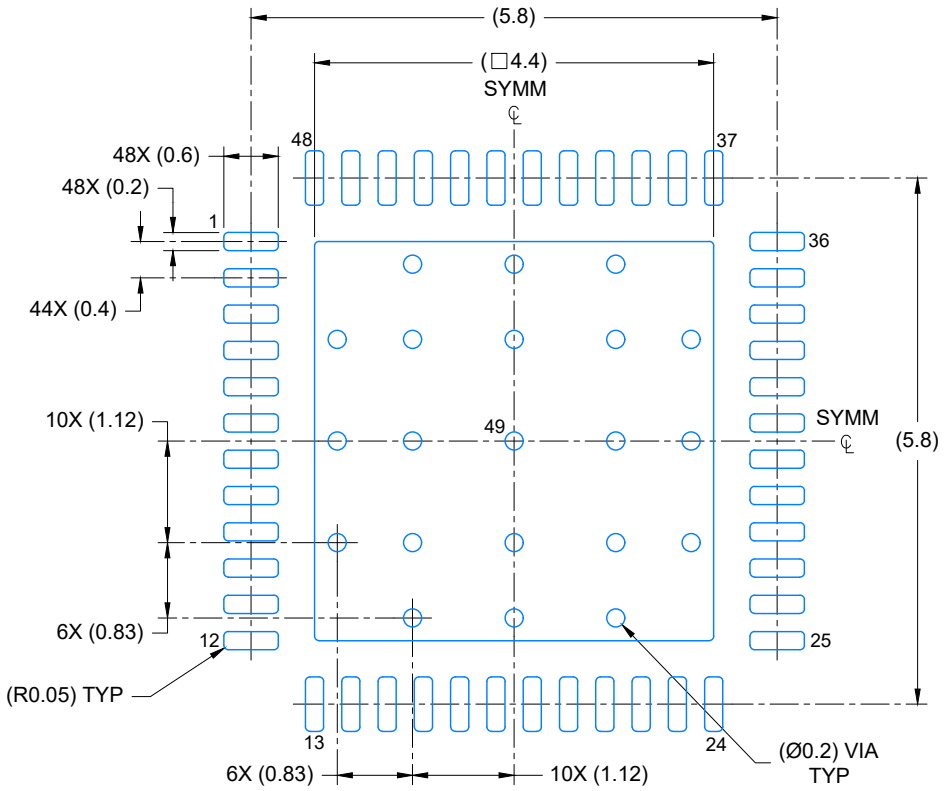
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

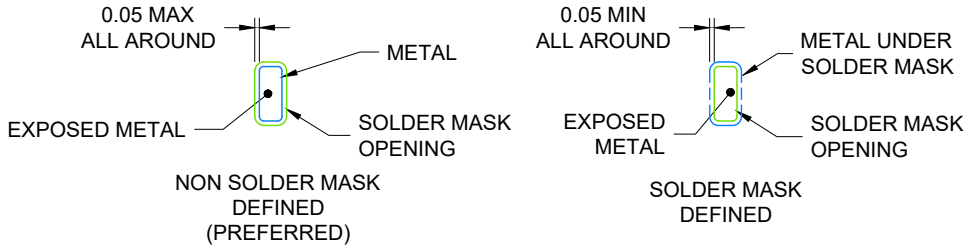


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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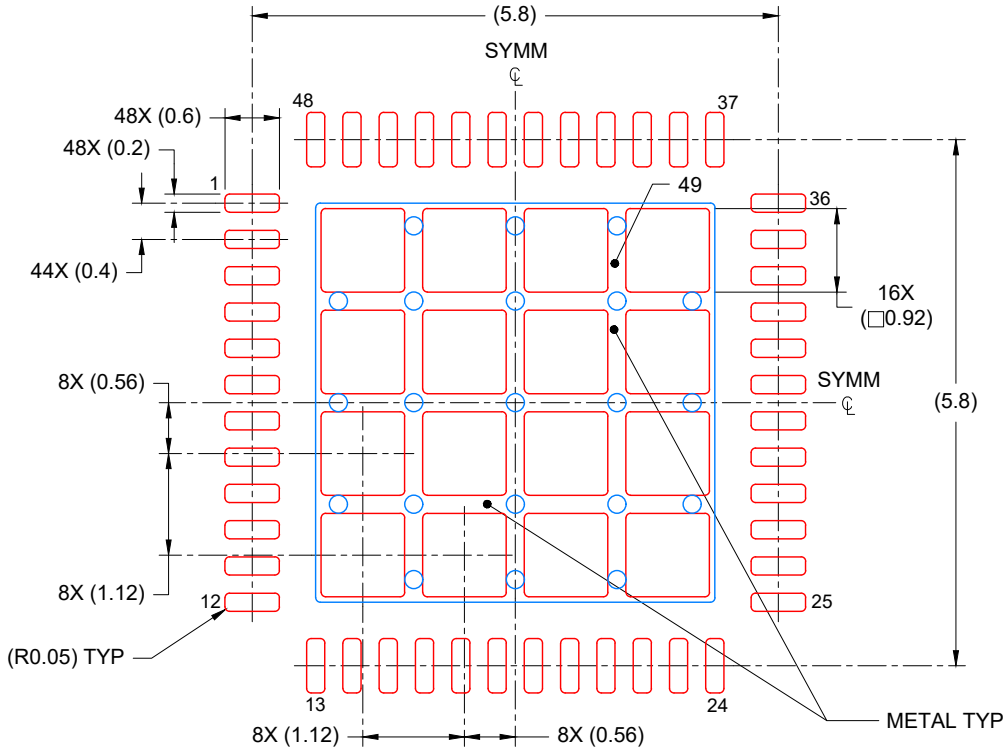
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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