

MOSFET

OptiMOS™ 5 Power-Transistor, 80 V

Features

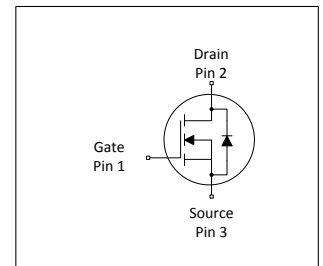
- Ideal for high frequency switching and sync. rec.
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------------|
| V_{DS} | 80 | V |
| $R_{DS(on),max}$ | 5.2 | m Ω |
| I_D | 64 | A |
| Q_{oss} | 51 | nC |
| $Q_G(0V..10V)$ | 42 | nC |



| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-------------------|----------|---------------|
| IPA052N08NM5S | PG-TO 220 FullPAK | 052N085S | - |

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------------|--------|------|----------|------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current | I_D | - | - | 64 46 | A | $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ |
| Pulsed drain current ¹⁾ | $I_{D,pulse}$ | - | - | 256 | A | $T_C=25\text{ °C}$ |
| Avalanche energy, single pulse ²⁾ | E_{AS} | - | - | 84 | mJ | $I_D=64\text{ A}$, $R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 38 | W | $T_C=25\text{ °C}$ |
| Operating and storage temperature | T_j , T_{stg} | -55 | - | 175 | °C | IEC climatic category; DIN IEC 68-1: 55/175/56 |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------------|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 4 | °C/W | - |

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------------|----------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 80 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.2 | 3.0 | 3.8 | V | $V_{DS}=V_{GS}$, $I_D=65\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 1 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 4.6 5.9 | 5.2 - | m Ω | $V_{GS}=10\text{ V}$, $I_D=32\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=16\text{ A}$ |
| Gate resistance ³⁾ | R_G | - | 1.1 | - | Ω | - |
| Transconductance | g_{fs} | - | 69 | - | S | $ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=32\text{ A}$ |

¹⁾ See Diagram 3 for more detailed information

²⁾ See Diagram 13 for more detailed information

³⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance ¹⁾ | C_{iss} | - | 2900 | 3800 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance | C_{oss} | - | 490 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Reverse transfer capacitance | C_{rss} | - | 23 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 17 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=32\text{ A}$, $R_{G,ext}=1.6\ \Omega$ |
| Rise time | t_r | - | 7 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=32\text{ A}$, $R_{G,ext}=1.6\ \Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 27 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=32\text{ A}$, $R_{G,ext}=1.6\ \Omega$ |
| Fall time | t_f | - | 7 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=32\text{ A}$, $R_{G,ext}=1.6\ \Omega$ |

Table 6 Gate charge characteristics²⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 14 | - | nC | $V_{DD}=40\text{ V}$, $I_D=32\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 9 | - | nC | $V_{DD}=40\text{ V}$, $I_D=32\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge | Q_{gd} | - | 9 | - | nC | $V_{DD}=40\text{ V}$, $I_D=32\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Switching charge | Q_{sw} | - | 14 | - | nC | $V_{DD}=40\text{ V}$, $I_D=32\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total ¹⁾ | Q_g | - | 42 | 56 | nC | $V_{DD}=40\text{ V}$, $I_D=32\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 4.6 | - | V | $V_{DD}=40\text{ V}$, $I_D=32\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 36 | - | nC | $V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge | Q_{oss} | - | 51 | - | nC | $V_{DD}=40\text{ V}$, $V_{GS}=0\text{ V}$ |

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 37 | A | $T_C=25\text{ }^\circ\text{C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 256 | A | $T_C=25\text{ }^\circ\text{C}$ |
| Diode forward voltage | V_{SD} | - | 0.88 | 1.2 | V | $V_{GS}=0\text{ V}$, $I_F=32\text{ A}$, $T_j=25\text{ }^\circ\text{C}$ |
| Reverse recovery time ¹⁾ | t_{rr} | - | 56 | - | ns | $V_R=40\text{ V}$, $I_F=32\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁾ | Q_{rr} | - | 92 | - | nC | $V_R=40\text{ V}$, $I_F=32\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ |

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

4 Electrical characteristics diagrams

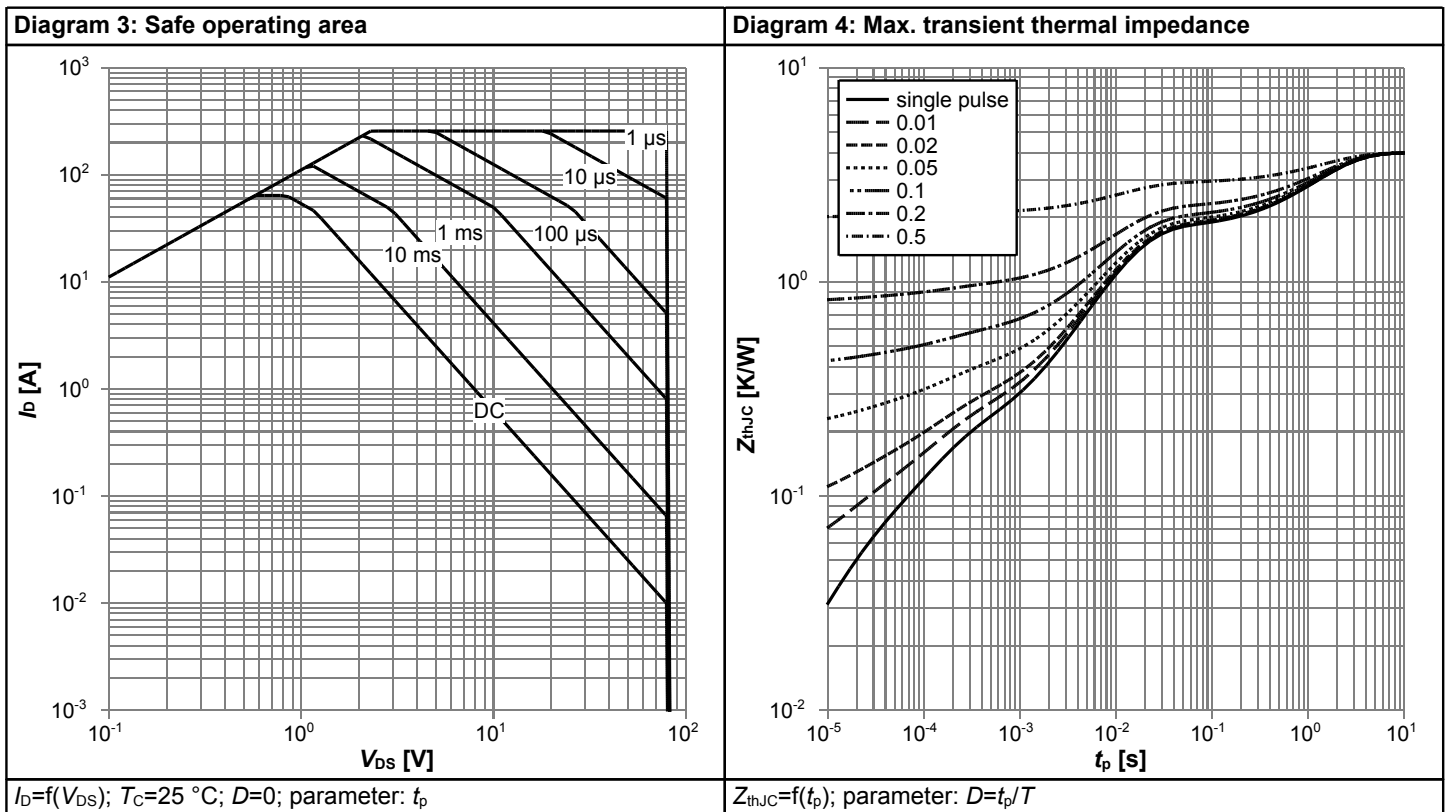
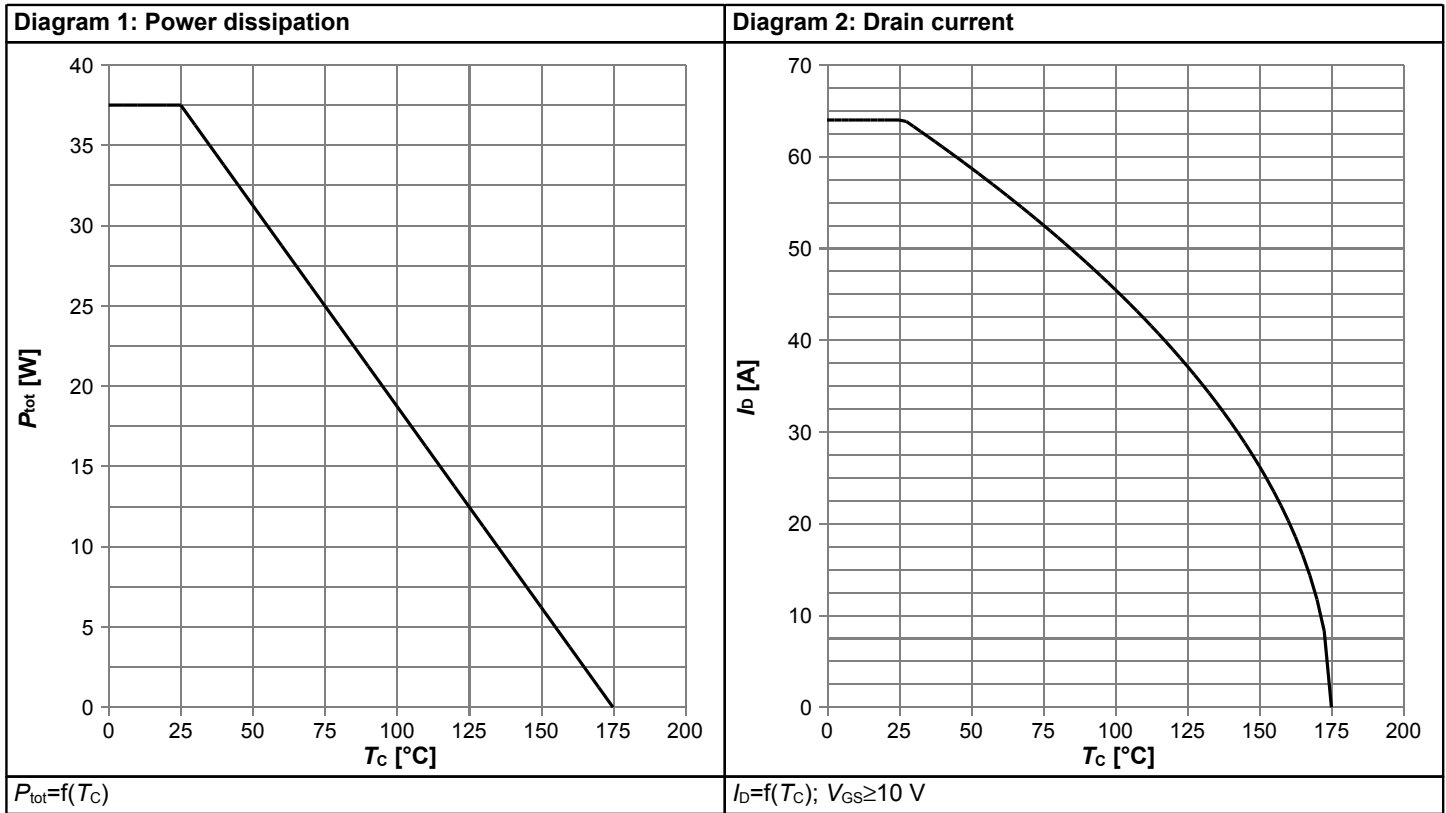
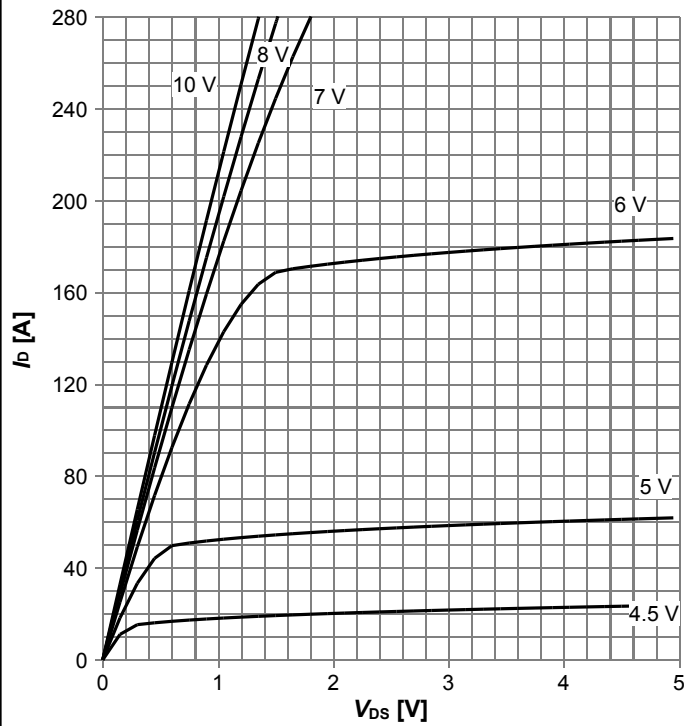
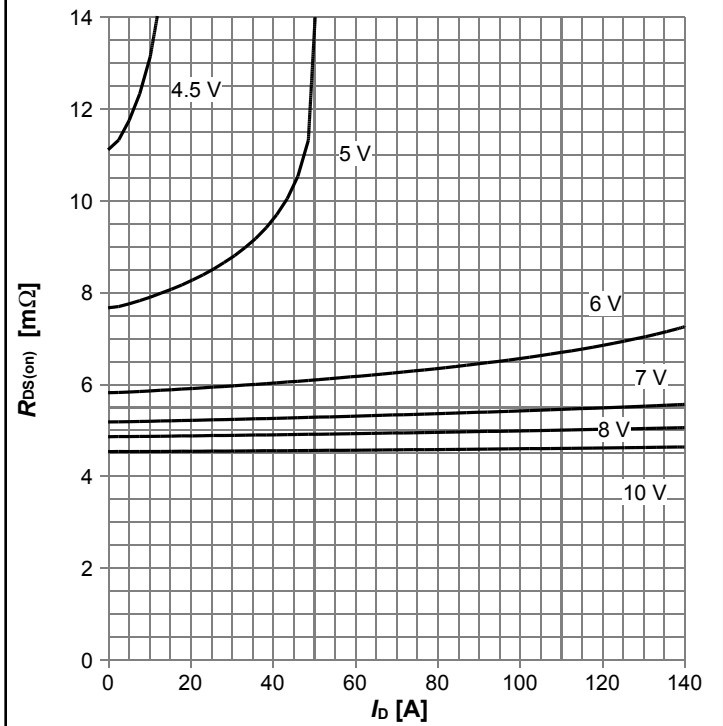


Diagram 5: Typ. output characteristics



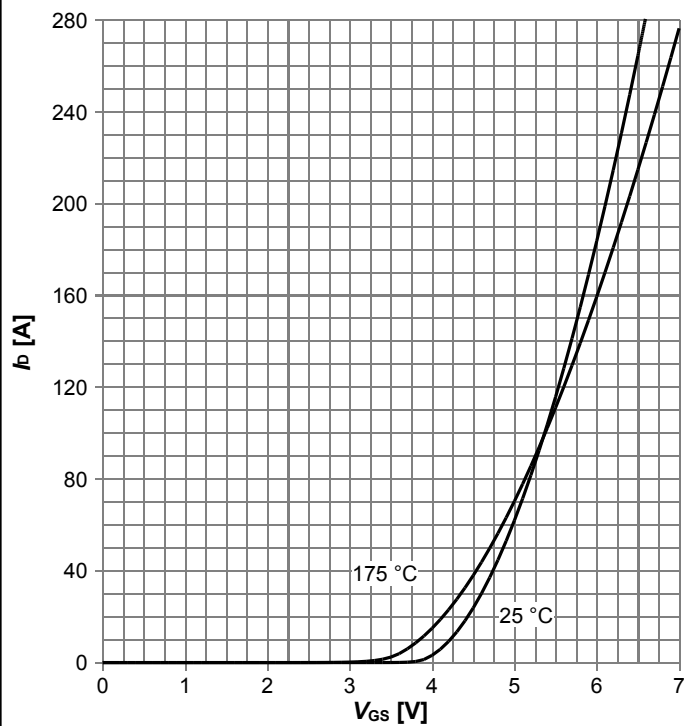
$I_D = f(V_{DS}), T_j = 25^\circ\text{C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



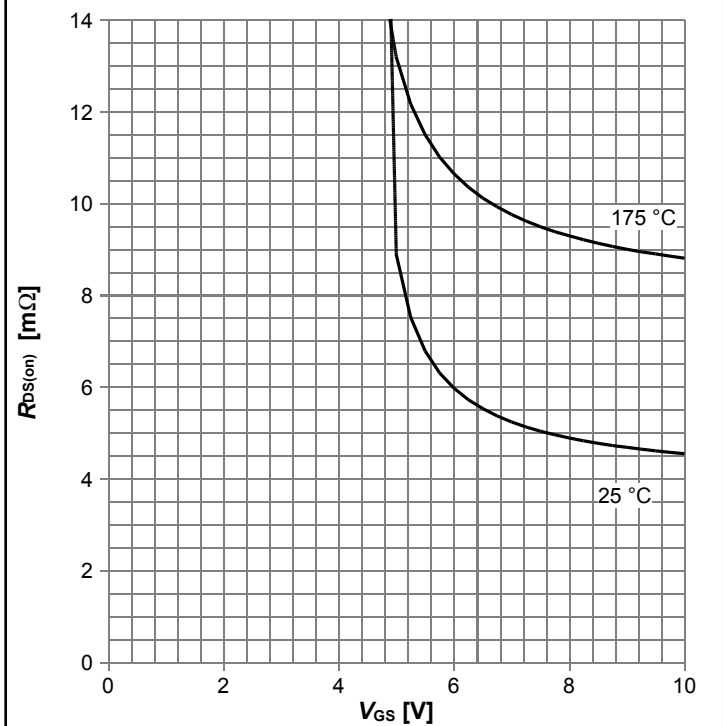
$R_{DS(on)} = f(I_D), T_j = 25^\circ\text{C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



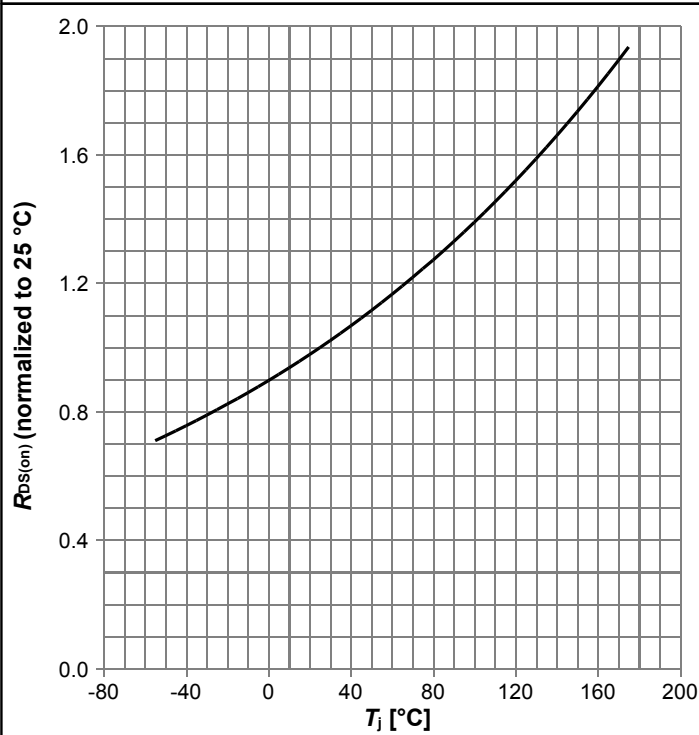
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. drain-source on resistance



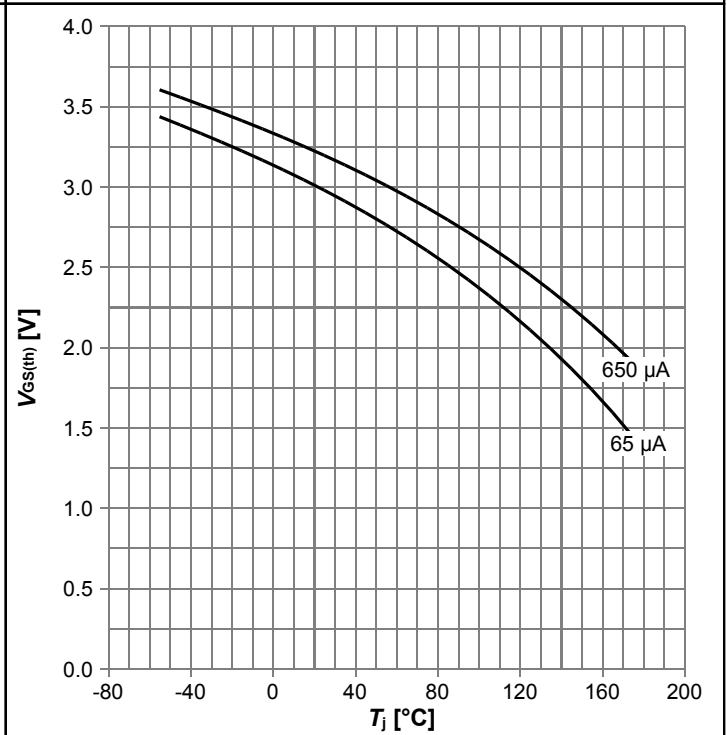
$R_{DS(on)} = f(V_{GS}), I_D = 32\text{ A};$ parameter: T_j

Diagram 9: Normalized drain-source on resistance



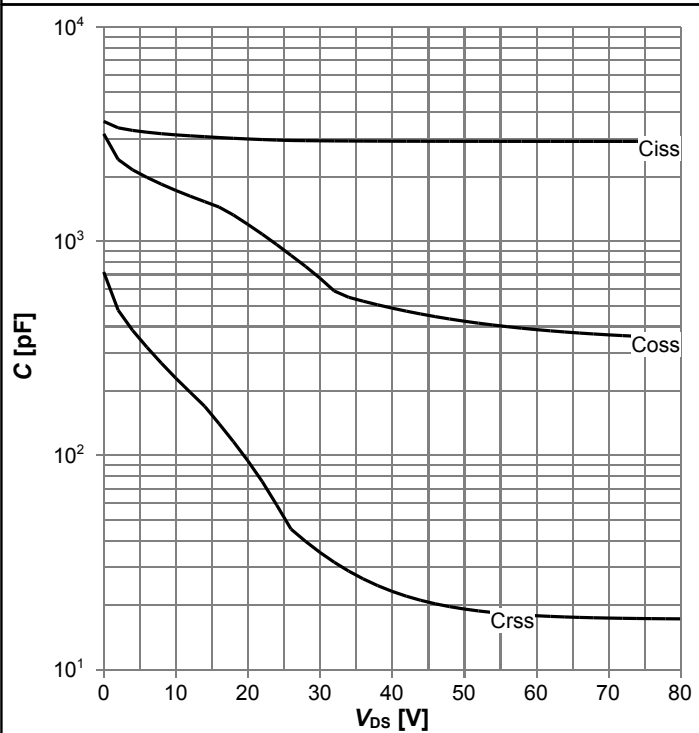
$R_{DS(on)}=f(T_j)$, $I_D=32$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



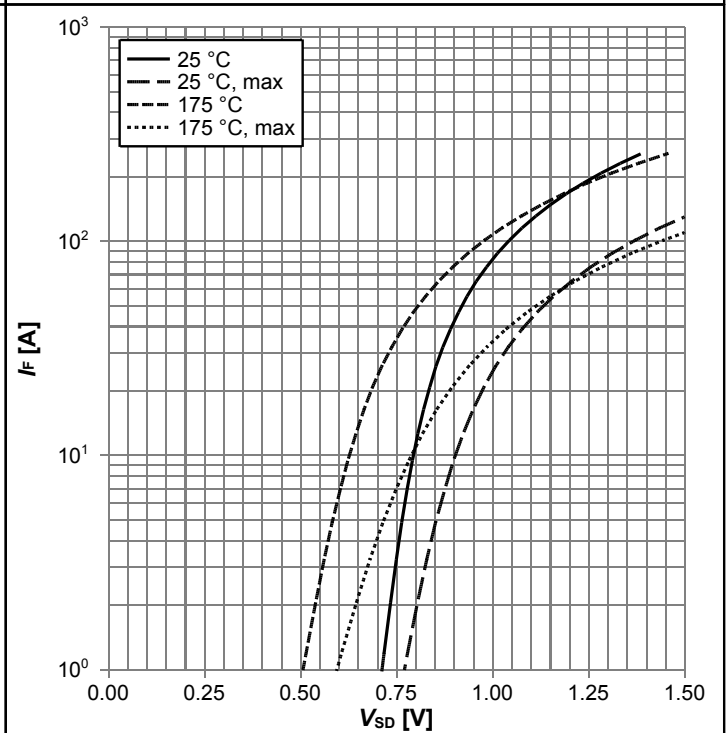
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



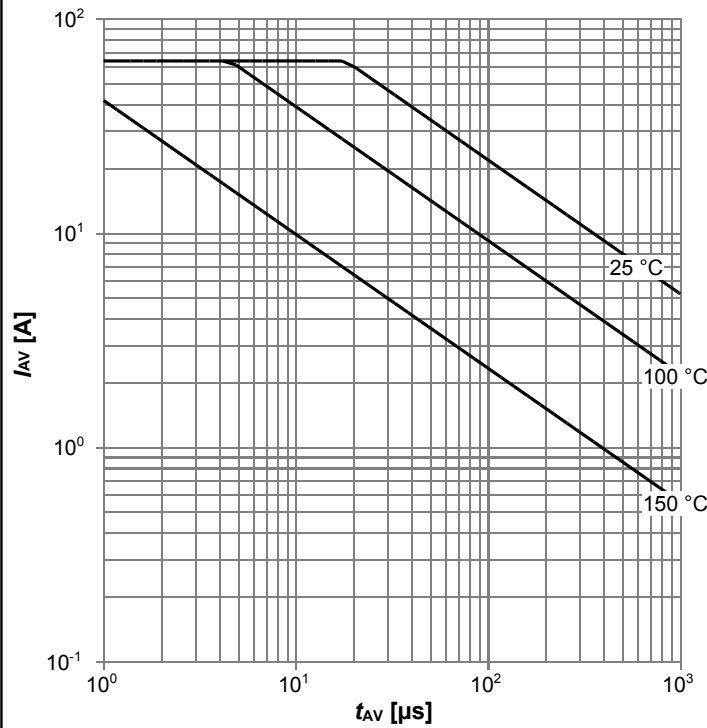
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



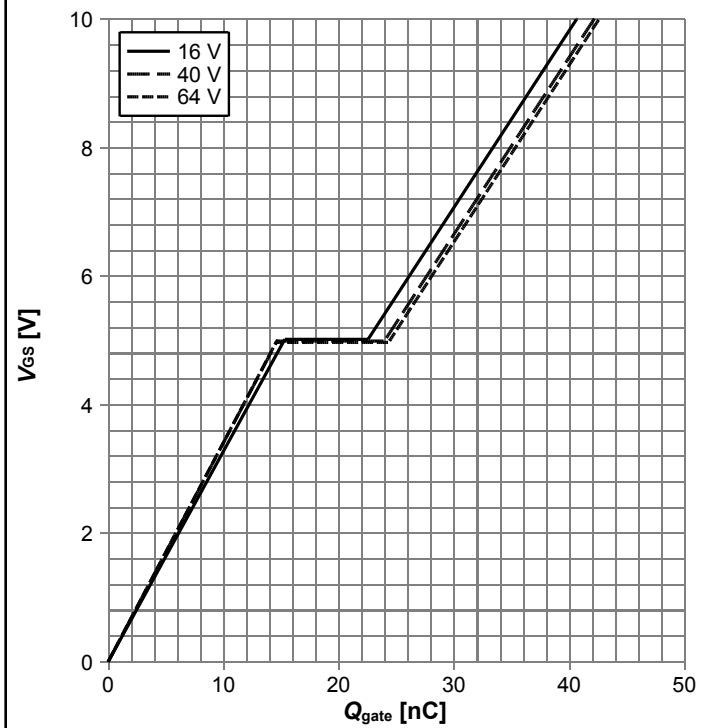
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



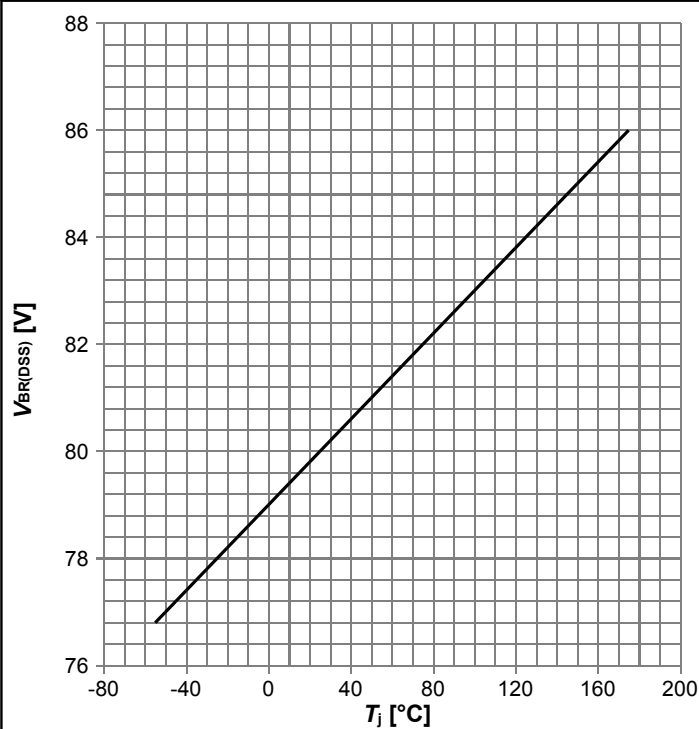
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega; \text{parameter: } T_{j,start}$

Diagram 14: Typ. gate charge



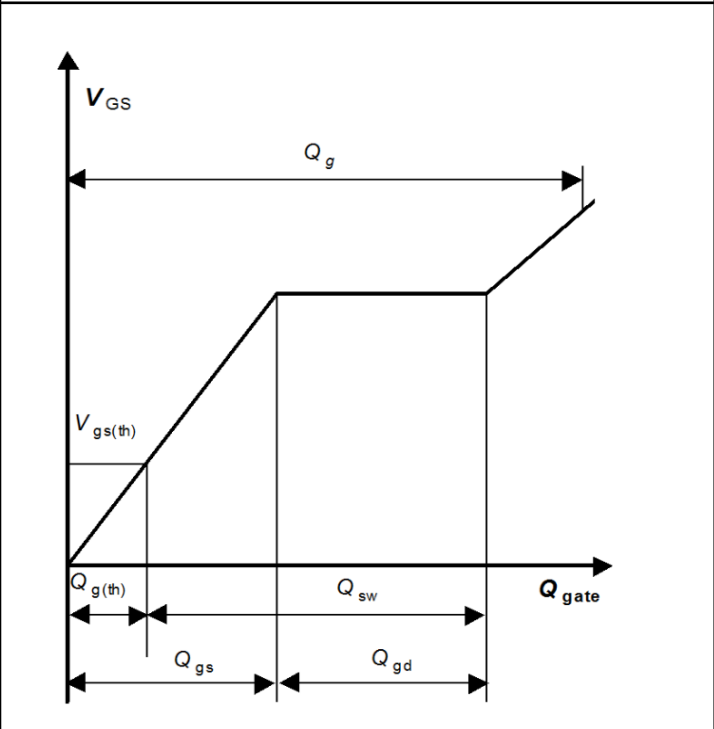
$V_{GS}=f(Q_{gate}), I_D=64 \text{ A pulsed}, T_j=25 \text{ °C}; \text{parameter: } V_{DD}$

Diagram 15: Drain-source breakdown voltage

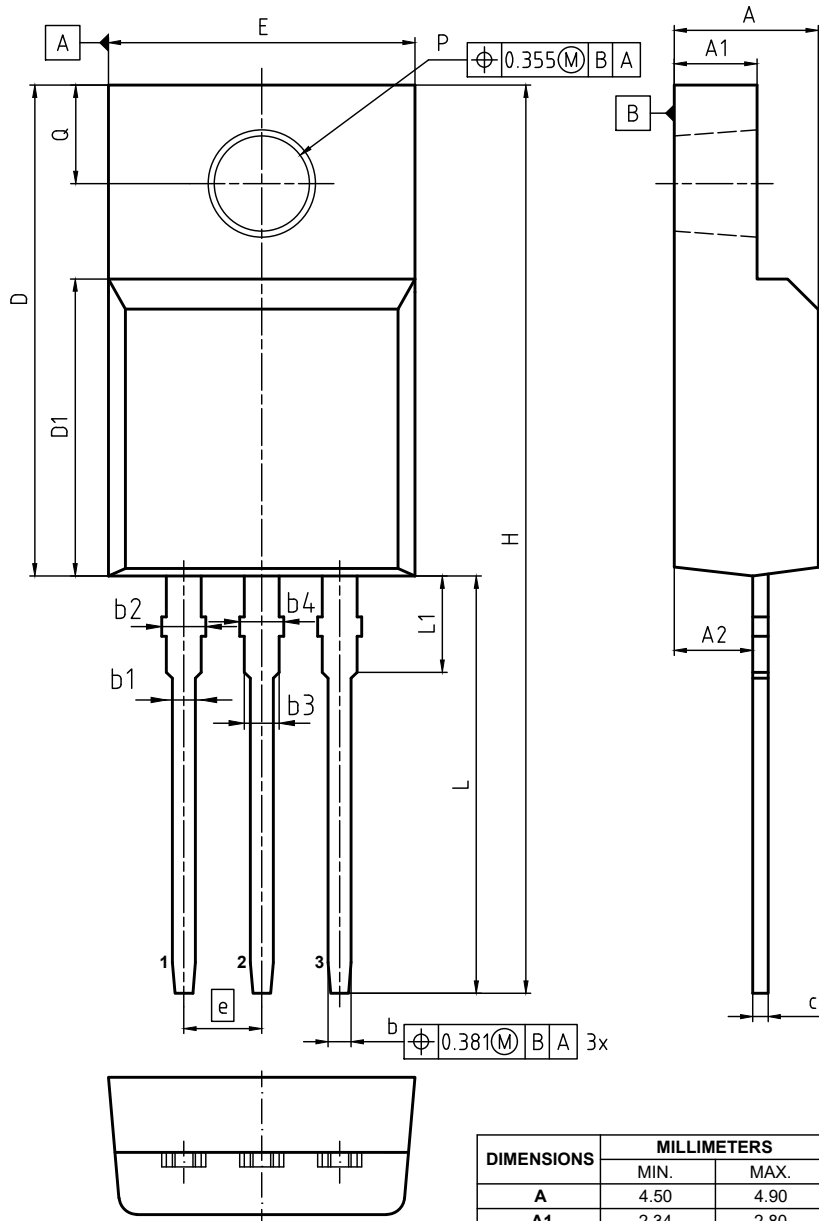


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



NOTES:
 STANDARD QUALITY GRADE
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PRO-
 TRUSIONS OR GATE BURRS

| DIMENSIONS | MILLIMETERS | |
|------------|-------------|-------|
| | MIN. | MAX. |
| A | 4.50 | 4.90 |
| A1 | 2.34 | 2.80 |
| A2 | 2.42 | 2.86 |
| b | 0.65 | 0.90 |
| b1 | 0.95 | 1.38 |
| b2 | 1.20 | 1.50 |
| b3 | 0.65 | 1.38 |
| b4 | 1.20 | 1.50 |
| c | 0.40 | 0.63 |
| D | 15.67 | 16.15 |
| D1 | 8.97 | 9.83 |
| E | 10.00 | 10.65 |
| e | 2.54 | |
| H | 28.70 | 29.75 |
| L | 12.78 | 13.75 |
| L1 | 2.83 | 3.45 |
| øP | 3.00 | 3.38 |
| Q | 3.15 | 3.50 |

| |
|------------------------------------|
| DOCUMENT NO. Z8B00181328 |
| REVISION 03 |
| ISSUE DATE 23.07.2018 |
| SCALE 5:1 0 1 2 3 4 5mm |
| EUROPEAN PROJECTION |

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

Revision History

IPA052N08NM5S

Revision: 2019-09-02, Rev. 2.1

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2019-07-16 | Release of final version |
| 2.1 | 2019-09-02 | Update package outline |

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