SM840021

125MHz Ultra-Low Jitter Clock Synthesizer

General Description

The SM840021 synthesizer was designed for Ethernet applications. This clock synthesizer is optimized for 125MHz using a standard 25MHz fundamental parallel resonant crystal, with unparalleled stability and accuracy over the full operating range. The SM840021 design includes a unique power reduction methodology, along with a patented RotaryWave™ architecture that provides a very stable clock with very low noise for optimized performance yielding an overall improved Bit Error Rate (BER) and improved waveform integrity.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Generates an optimized 125MHz LVCMOS Output
- Integrated loop filter components
- RMS Phase Jitter: 250 fs (typ)
- Operates with either a 3.3V or 2.5V supply
- Power consumption is <77mA @ 3.3V
- Input frequency: 25MHz parallel resonant crystal
- Output frequency: 125MHz
- Temperature range: –40°C to +75°C
- Green, RoHS-compliant and PFOS-compliant
- Available in 8-pin TSSOP package

Applications

- Gigabit Ethernet
- Datacom/Telecom
- Ethernet Switch

Block Diagram
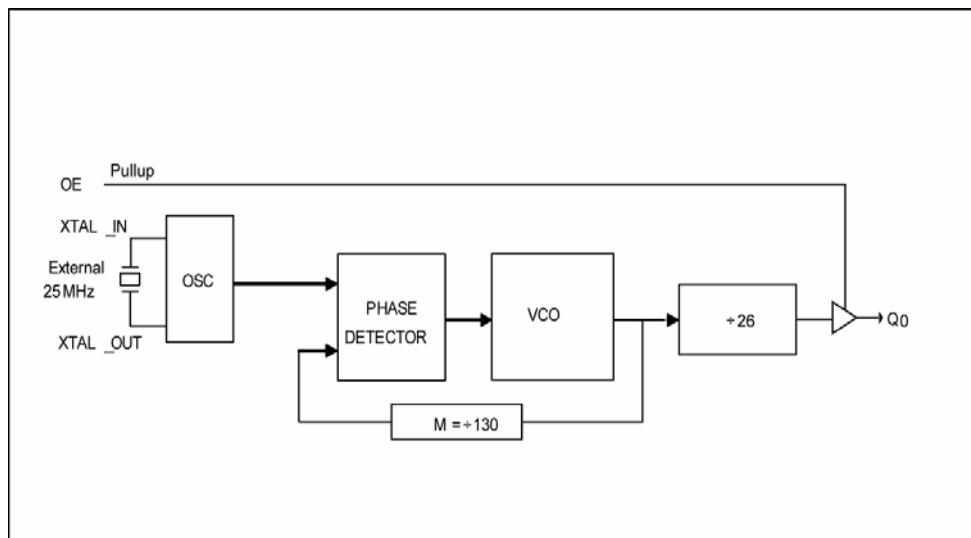
RotaryWave is a registered trademark of Multigig, Inc.

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SM840021KA	K-8	-40°C to +75°C	840021	NiPdAu
SM840021KA TR[2]	K-8	-40°C to +75°C	840021	NiPdAu

Note:

1. Devices are Green, RoHS-compliant and PFOS-compliant.

2. Tape and Reel

Pin Configuration
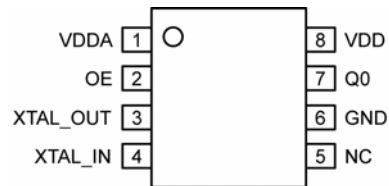
8-Pin TSSOP (K-8)

Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	V_{DDA}	P		Analog Power.
2	OE	I	Pull-up	Output Enable: 1 = Enable, 0 = Disable.
3	XTAL OUT	O		Crystal Output.
4	XTAL IN	I		Crystal Input.
5	NC			No Connect.
6	GND	P		Ground.
7	Q0	O		Single Ended LVCMOS Clock Out.
8	V_{DD}	P		Core Power.

Output Enable

OE	Output
0	Disable
1	Enable

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD})..+4.6V
Input Voltage (V_{IN})................................ –0.50V to V_{DD}+0.5V
Output Voltage (V_{OUT}) ....–0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20sec.).......................260°C
Storage Temperature (T_s) ....–65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN})............................. +2.375V to +3.465V
Ambient Temperature (T_A) ....–40°C to +75°C
Junction Thermal Resistance
    TSSOP (θ_{JA})...150°C/W

DC Electrical Characteristics

V_{DD} = 2.5V ±5%; T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		2.375	2.50	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.50	2.625	V
I_{DD}	Core Supply Current	No load		12	20	mA
I_{DDA}	Analog Supply Current			48	55	mA

DC Electrical Characteristics

V_{DD} = 3.3V ±5%; T_A = -40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.30	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.30	3.465	V
I_{DD}	Core Supply Current	No load		15	22	mA
I_{DDA}	Analog Supply Current			49	55	mA

LVCMOS DC Characteristics

V_{DD} = 2.5V ±5% and 3.3V ±5%; T_A = -40°C to +75°C, unless noted.

| Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	3.3V Operation	2		V_{DD} +0.3	V
		2.5V Operation	1.7		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V Operation	-0.3		0.8	V
		2.5V Operation	-0.3		0.7	V
I_{IH}	Input HIGH Current	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input LOW Current	V_{DD} = 3.465V; V_{IN} = 0V	-150			µA
V_{OH}	Output HIGH Voltage[3]	V_{DD} = 3.3V ±5%	2.6			V
		V_{DD} = 2.5V ±5%	1.8			V
V_{OL}	Output LOW Voltage[3]	V_{DD} = 3.3V ±5% or V_{DD} = 2.5V ±5%			0.5	V

Notes:

1. Exceeding the absolute maximum rating may damage the device.

2. The device is not guaranteed to function outside its operating rating.

3. Outputs terminated with 50Ω to V_{DD}/2. See Parameters measurements 3.3V load test circuit.

AC Electrical Characteristics

V_{DD} = 2.5V ±5% and 3.3V ±5%; T_A = -40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output Frequency	25MHz Crystal		125		MHz
t_{JITTER}	RMS phase jitter @ 125MHz	Integration Range: 1.875MHz to 20MHz		250		fs
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		350	ps
ODC	Output Duty Cycle		48	50	52	%

Test Circuit

(Output Load AC Test Circuit, 3.3V)
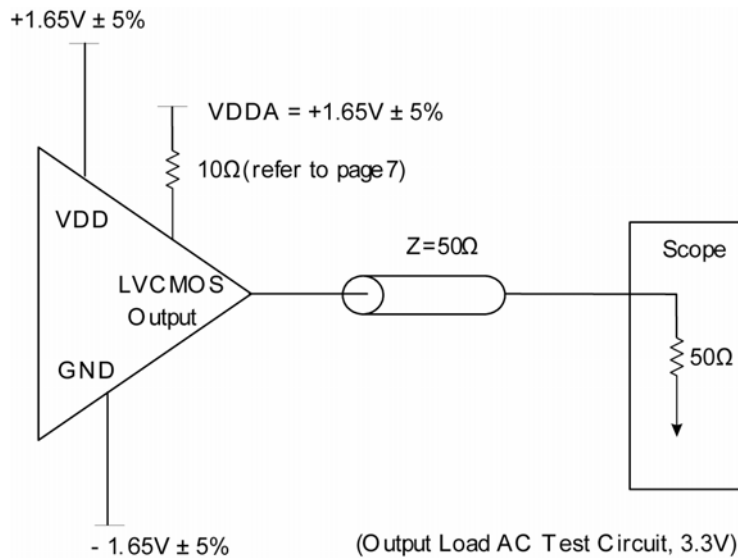
3.3V Carrier Frequency, 125MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-103	dBc/Hz
1kHz	-126	dBc/Hz
10kHz	-134	dBc/Hz
100kHz	-130	dBc/Hz
1MHz	-143	dBc/Hz
1.875MHz	-152	dBc/Hz
10MHz	-166	dBc/Hz
20MHz	-167	dBc/Hz

Functional Description

The SM840021 provides a high performance and high accuracy solution for a precision clock source at 125MHz derived, from a low cost 25MHz Xtal.
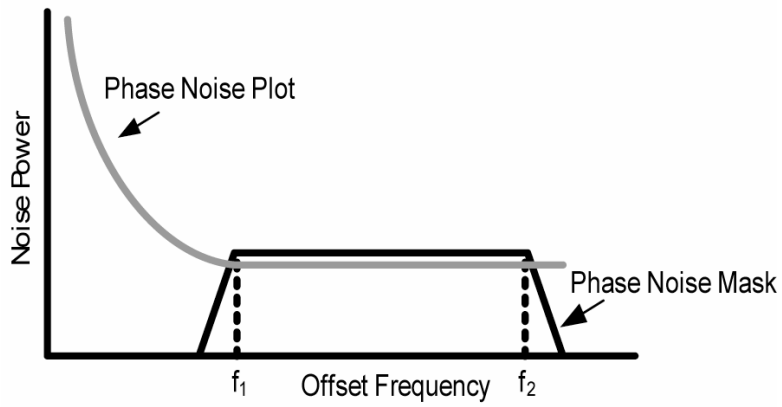
The design of the SM840021 consumes very low power in the PLL due to a proprietary technology in the VCO and the associated dividers. The output divider is fixed at $\div 26$, and the feedback divider is also fixed at $\div 130$

providing a precision clock at 125MHz. Duty Cycle is inherently improved to provide a tight control and stability on this critical specification.
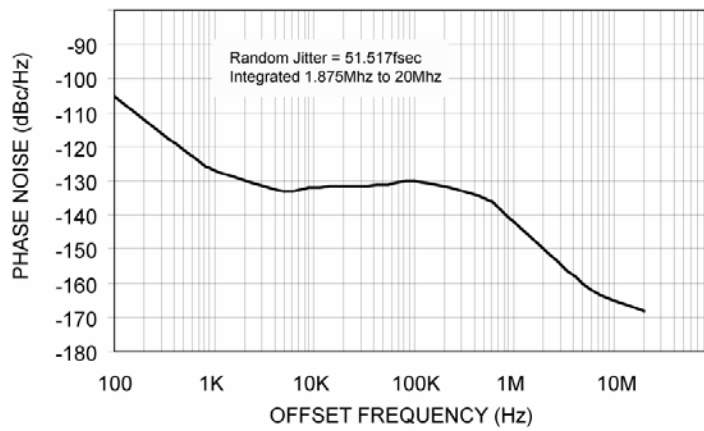
The device provides improved specifications for Duty Cycle, Jitter, Phase Noise, Power Consumption, and noise sensitivity. Additionally, the SM840021 will operate at either 3.3V or 2.5V supplies.
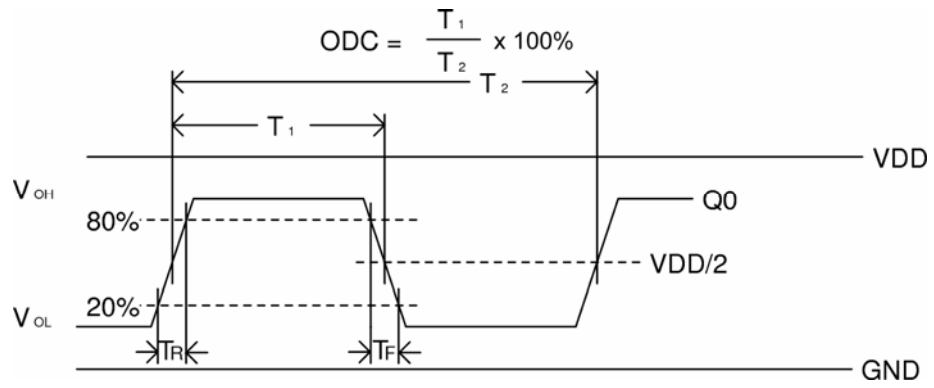
RMS Phase Noise/Jitter

RMS Phase Noise/Jitter

Phase Noise Plot

Noise Power

Phase Noise Mask

f_1 Offset Frequency f_2

RMS Jitter = $\sqrt{\text{Area Under The Masked Phase Noise Plot}}$

Random Jitter = 51.517fsec
Integrated 1.875Mhz to 20Mhz

PHASE NOISE (dBc/Hz)

-90
-100
-110
-120
-130
-140
-150
-160
-170
-180

100   1K   10K   100K   1M   10M

OFFSET FREQUENCY (Hz)

Phase Noise Plot: 125MHz @ 3.3V

Switching Waveforms

The figure shows the definition:
$$ODC = \frac{T_1}{T_2} \times 100\%$$

with waveform Q0, voltage levels V_{OH}, V_{OL}, 80%, 20%, VDD, VDD/2, GND, and timing intervals T_1, T_2, T_R, T_F.

Power Supply Filtering

The SM840021 provides separate power supply pins to isolate any high switching noise from outputs to internal core blocks. VDD and VDDA should be individually connected to the power plane through vias. Bypass capacitors should be used for each pin. Figure 2 illustrates how the power supply filter for 3.3 V and 2.5 V is configured.
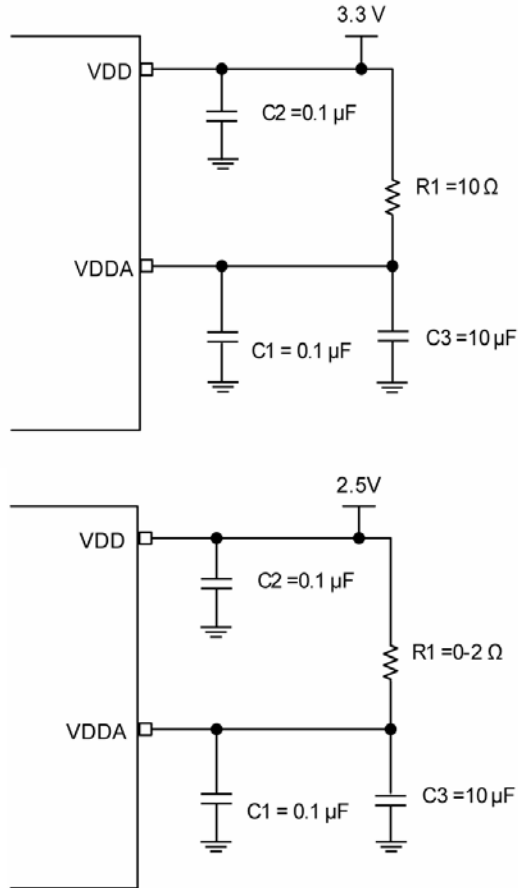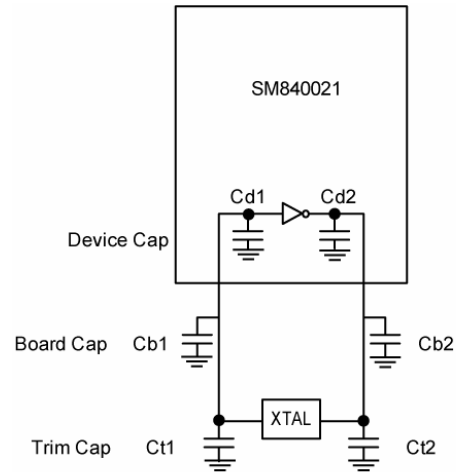

Figure 2.

Crystal Loading

Crystal Recommendations

This device requires a parallel resonance crystal. Substituting a series resonance crystal will cause this device to operate at the wrong frequency and violate the ppm specifications.

To achieve low ppm error, the total capacitance of the crystal must be considered in order to calculate appropriate capacitive loading (CL).

Load Capacitance at each side: Trim Capacitance = Ct = (2*CL-(Cb + Cd))

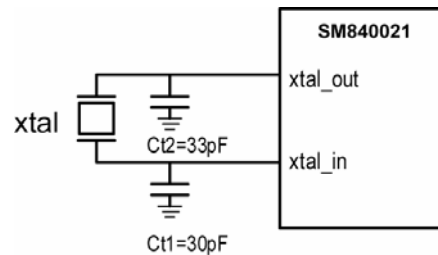CL: Crystal load capacitance. Defined by manufacturer

Ct: External trim capacitors. (Trimmed CL Load capacitance to get the right ppm)

Cb: Board capacitance (vias, traces, etc.)

Cd: Internal capacitance of the device (lead frame, bond wires, pin, etc.)

Equivalent Series Resistance (ESR) Max.	Cut	Load Cap.	Shunt Cap. Max.	Drive Max.
70Ω	AT		7pF	0.1mW

Crystal Input Interface

Total capacitance seen by crystal = CL =

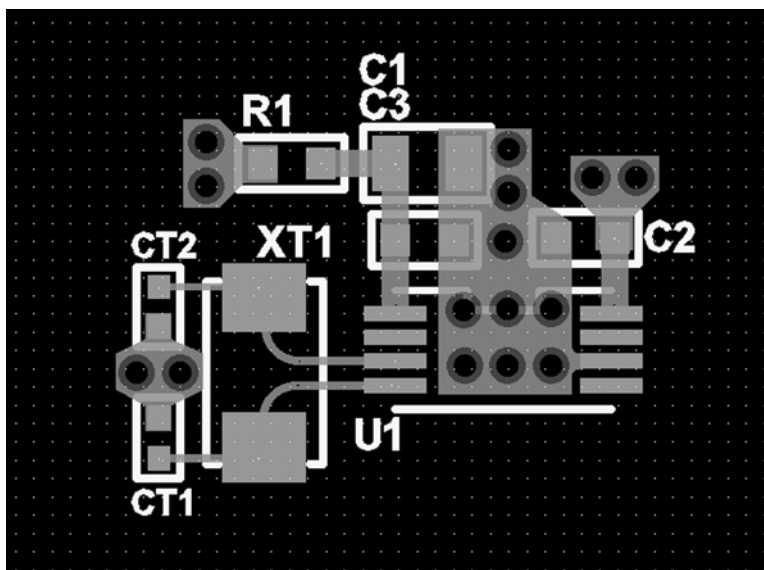$$CL = \cfrac{1}{\cfrac{1}{(Ct1 + Cb1 + Cd1)} + \cfrac{1}{(Ct2 + Cb2 + Cd2)}}$$

Example:

CL = 18pF, Cb = 2pF, Cd = 4pF

Trim Cap = Ct = 2 (18pF) - (2pF +4pF) = 30pF
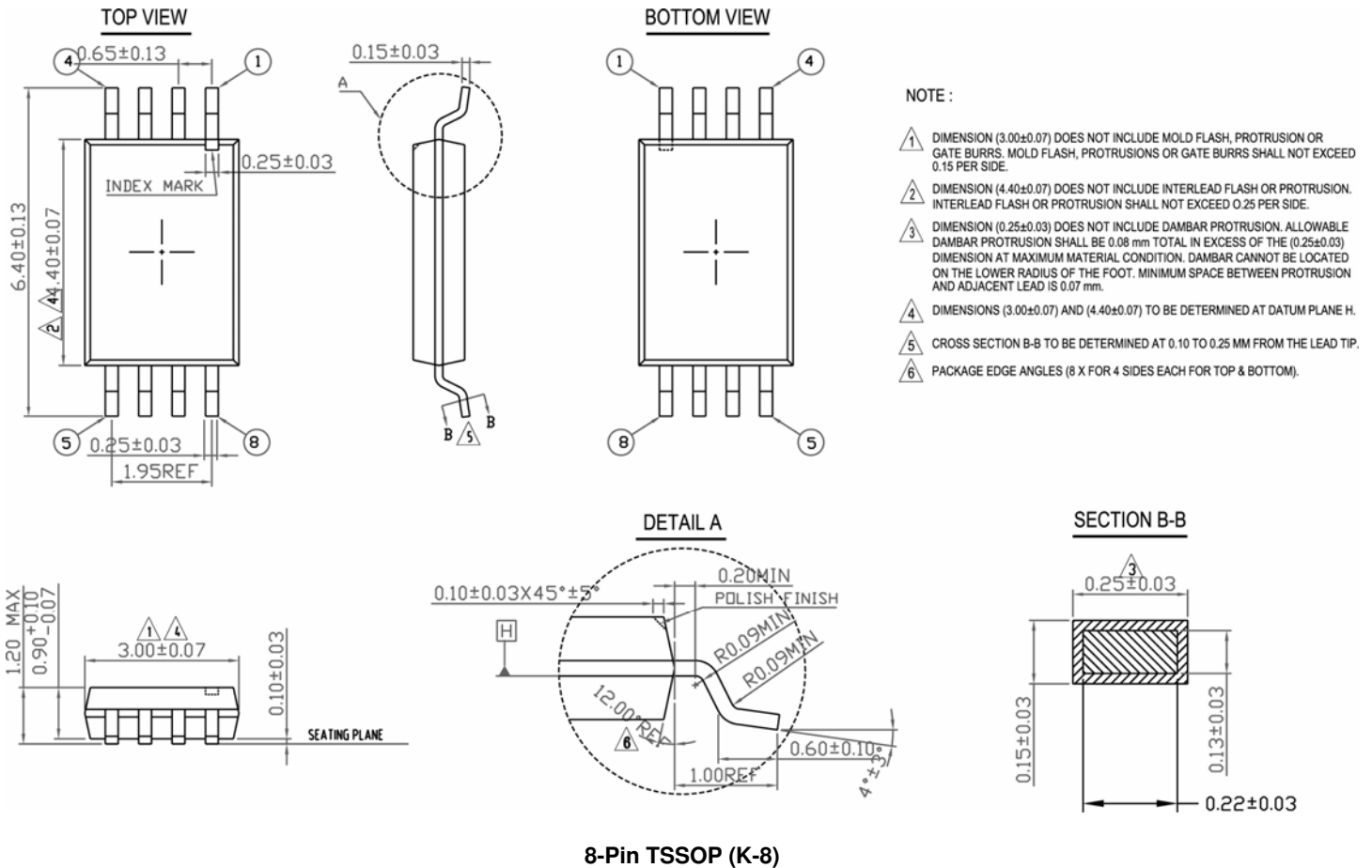
The SM840021 has been characterized with 25MHz, 18pF parallel resonant crystal. The trim capacitors Ct1 and Ct2 were optimized to minimize the ppm error.

To minimize the board capacitance, a short trace from pin to crystal footprint without vias is desirable. It is preferable to have ground shielding or distance between the crystal traces and noisy signals on the board.

Board Layout

Package Information

NOTE :

1. DIMENSION (3.00±0.07) DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

2. DIMENSION (4.40±0.07) DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED O.25 PER SIDE.

3. DIMENSION (0.25±0.03) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF THE (0.25±0.03) DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 mm.

4. DIMENSIONS (3.00±0.07) AND (4.40±0.07) TO BE DETERMINED AT DATUM PLANE H.

5. CROSS SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.

6. PACKAGE EDGE ANGLES (8 X FOR 4 SIDES EACH FOR TOP & BOTTOM).

8-Pin TSSOP (K-8)

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