



# FXP1500/1800 AC-DC Power Supply FXR-3-48G Power Shelf

The FXP1500/1800 front-ends are power-factor-corrected (PFC) and provide a 48 VDC (1500 or 1800 watt) output, and can be used in hot-swap redundant systems. Their very small dimensions allow configuration of up to three units in a 1U rack. The FXP front-ends have a rear-mounted AC connector. The highly efficient thermal design with internal-fan cooling permits their use over wide temperature ranges and provides very high reliability.



Status information is provided with front panel LEDs, logic signals, and via an I<sup>2</sup>C management interface. In addition, the I<sup>2</sup>C bus can enable the power supply, set high fan speed, adjust the output voltage, and set the output current limit. The FXP1500/1800's meet international safety standards and display the CE-Mark for the European Low Voltage FXR-3-48G power-shelf solutions provide rectification, system management, and power distribution, while maintaining high reliability and offering flexibility for future expansion. The power shelves can be configured with up to three hot-swappable 1500 or 1800-watt AC-DC front-ends.



## Key Features & Benefits

- RoHS compliant for all six substances
- High density front-ends 15.2 to 18.3 W/in<sup>3</sup>
- Wide input voltage range 85 to 264 VAC
- 12 V standby voltage, 1 A per front-end
- Highly efficient topology reduces operating costs
- I<sup>2</sup>C interface status and control
- I<sup>2</sup>C voltage and current limit setting
- Analog output voltage setting
- Overtemperature, output overvoltage, and output overcurrent protection
- ORing circuits for true redundant operation:  
V<sub>o1</sub>: ORing FETs; V<sub>o2</sub>: ORing Diodes
- Status LEDs: AC OK, DC OK, and Fan Fail/Overtemperature Fail



## Applications

- Telecommunications
- Data Communications
- Servers
- Distributed Power

## 1. MODEL SELECTION

| MODEL       | INPUT VOLTAGE<br>VAC<br>AUTO SELECTED <sup>1</sup> | OUTPUT 1                    |                             | OUTPUT 2                    |                             | RATED POWER<br>W | COMPATIBLE<br>SHELF <sup>2</sup> |
|-------------|--|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------------------|----------------------------------|
|             |  | $V_{o1 \text{ nom}}$<br>VDC | $I_{o1 \text{ max}}$<br>ADC | $V_{o2 \text{ nom}}$<br>VDC | $I_{o2 \text{ max}}$<br>ADC |                  |                                  |
| FXP1500-48G | 105 – 264  | 48                          | 32.2                        | 12                          | 1                           | 1512             | FXR-3-48G                        |
|             | 85 – 105   | 48                          | 25.4                        | 12                          | 1                           | 1212             |                                  |
| FXP1800-48G | 180 – 264  | 48                          | 39.2                        | 12                          | 1                           | 1812             | FXR-3-48G                        |
|             | 105 – 180<br>85 – 105                              | 48                          | 32.2<br>25.4                | 12                          | 1                           | 1512<br>1212     |                                  |

<sup>1</sup> The available output power is automatically adjusted depending on the input voltage.

<sup>2</sup> 1U standard racks are available from Bel Power Solutions. See the Rack (Power Shelf) section of this data sheet for configurations and details.

## 2. ABSOLUTE MAXIMUM RATINGS

Stress in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, or cause permanent damage to the converter.

| PARAMETER                     | CONDITIONS / DESCRIPTION   | MIN          | MAX | UNIT |    |
|-------------------------------|--|--------------|-----|------|----|
| Input Voltage                 | Continuous   |              | 264 | VAC  |    |
|                               | Transient, 60 ms max.  |              | 300 |      |    |
| Operating Ambient Temperature | $V_{\text{min}} - V_{\text{max}}$ , $I_{\text{o nom}}$ , cooling by internal fan | @ 100 % load | 0   | 50   | °C |
|                               |  | @ 50 % load  | 0   | 70   |    |
| Storage Temperature           | Non-Operating  | -40          | 85  | °C   |    |

## 3. INPUT SPECIFICATIONS

Specification is valid for input voltage, load, and temperature ranges, unless otherwise stated.

| PARAMETER                 | CONDITIONS / DESCRIPTION  | MIN  | NOM   | MAX | UNIT             |
|---------------------------|---|------|-------|-----|------------------|
| Input Voltage             |   | 85   | 230   | 264 | VAC              |
| Input Frequency           |   | 47   | 50/60 | 63  | Hz               |
| Turn-On Input Voltage     | Ramping up  | 79   |       | 85  | VAC              |
| Turn-Off Input Voltage    | Ramping down  | 70   |       | 78  | VAC              |
| Inrush Current Limitation | 115/230 VAC acc. ETS 300 132-1<br>< 100 ms                            |      |       | 50  | A <sub>pk</sub>  |
| Hold-Up Time              | After last AC line peak, $V_i = 230 \text{ VAC}$ , $P_{\text{o nom}}$ | 20   |       |     | ms               |
| Power Factor              | $V_{\text{nom}}$ , $I_{\text{o nom}}$                                 | 0.95 |       |     | W/VA             |
| Efficiency                | $V_i = 230 \text{ VAC}$ , $I_{\text{o nom}}$ , $T_c = 25 \text{ °C}$  | 89   | 90    |     | %                |
| Max Input Current         |   |      |       | 20  | A <sub>rms</sub> |
| Input Connector           | 16 A – 20 A / 250 VAC; according to IEC320 C19                        |      |       |     |                  |

## 4. OUTPUT SPECIFICATIONS - 48 VOUT MODELS

Specification is valid for input voltage, load, and temperature ranges, unless otherwise stated.

| PARAMETER   | CONDITIONS / DESCRIPTION   | MIN   | NOM  | MAX   | UNITS                  |
|---|--|---|------|-------|------------------------|
| Nominal Output Voltage Vo1  | $I_o = 16.1 \text{ A}$   |   | 48   |       | VDC                    |
| Nominal Output Voltage Vo2  | $I_o = 0.5 \text{ A}$  |   | 12   |       | VDC                    |
| Output Voltage Set Point Accuracy   | $V_i = 230 \text{ VAC}$ , $I_{o1} = 16.1 \text{ A}$ , $T_c = 25 \text{ }^\circ\text{C}$<br>(47.8 - 48.2 VDC)   | -0.5  |      | +0.5  | % $V_{o1 \text{ nom}}$ |
| Output Voltage Trimming<br>(via I <sup>2</sup> C or with external resistor) | Adjustable (44.16 to 51.84 VDC)  | -8  |      | +8    | % $V_{o1 \text{ nom}}$ |
| Nominal Current Output 1  | FXP1500-48G<br>$I_{o1 \text{ nom}}$ @ $V_i = 105 \text{ VAC} - 264 \text{ VAC}$ , $P_o 1.5 \text{ kW}$   |   | 32.2 |       | ADC                    |
|   | $I_{o1 \text{ nom}}$ @ $V_i = 85 \text{ VAC} - 105 \text{ VAC}$ , $P_o 1.2 \text{ kW}$   |   | 25.4 |       | ADC                    |
|   | FXP1800-48G<br>$I_{o1 \text{ nom}}$ @ $V_i = 180 \text{ VAC} - 264 \text{ VAC}$ , $P_o 1.8 \text{ kW}$   |   | 39.2 | 39.2  | ADC                    |
|   | $I_{o1 \text{ nom}}$ @ $V_i = 105 \text{ VAC} - 180 \text{ VAC}$ , $P_o 1.5 \text{ kW}$  |   | 32.2 |       | ADC                    |
| Current Limit Output 1  | FXP1500-48G<br>$I_{o1 \text{ max}}$ @ $V_i = 105 \text{ VAC} - 264 \text{ VAC}$ droop hiccup   |   | 36.8 |       | ADC                    |
|   | $I_{o1 \text{ max}}$ @ $V_i = 85 \text{ VAC} - 105 \text{ VAC}$ droop hiccup   |   | 30   |       | ADC                    |
|   | FXP1800-48G<br>$I_{o1 \text{ max}}$ @ $V_i = 180 \text{ VAC} - 264 \text{ VAC}$ droop hiccup   |   | 43.8 |       | ADC                    |
|   | $I_{o1 \text{ max}}$ @ $V_i = 105 \text{ VAC} - 180 \text{ VAC}$ droop hiccup  |   | 36.8 |       | ADC                    |
| Nominal Current Output 2  | $I_{o2 \text{ nom}}$ @ $V_i = 85 \text{ VAC} - 264 \text{ VAC}$ , $P_o 12 \text{ W}$   |   | 1.0  | 1.0   | ADC                    |
|   | Current Limit Output 2   | $I_{o2 \text{ max}}$ @ $V_i = 85 \text{ VAC} - 264 \text{ VAC}$ |      | 1.5   | ADC                    |
| Static Line Regulation Output 1   | $V_{i \text{ min}} - V_{i \text{ max}}$ , 50 % $I_{o \text{ nom}}$   | -0.5  |      | 0.5   | % $V_{o \text{ nom}}$  |
| Static Load Regulation Output 1<br>(Droop Characteristic)                   | FXP1500-48G<br>$V_i = 230 \text{ V}$ , 5-100 % $I_{o \text{ nom}}$<br>$V_o$ : full load (32.2 ADC) to no load  | 46.65   | 83.5 | 49.34 | mV/A<br>VDC            |
|   | FXP1800-48G<br>$V_i = 230 \text{ V}$ , 5-100 % $I_{o \text{ nom}}$<br>$V_o$ : full load (32.2 ADC) to no load  | 46.07   | 83.5 | 49.34 | mV/A<br>VDC            |
| Static Load Regulation Output 2<br>(Droop Characteristic)                   | $V_i = 230 \text{ V}$ , 5-100 % $I_{o \text{ nom}}$<br>$V_o$ : full load (32.2 ADC) to no load   |   | 0.4  |       | VDC                    |
| Dynamic Load Regulation   | FXP1500-48G<br>Load change 50% <-> 100% $I_{o \text{ nom}}$ , $dI_o/dt = 1 \text{ A}/\mu\text{s}$<br>Voltage deviation (droop + over- or undershoot) | -5  |      | 5     | % $V_{o \text{ nom}}$  |
|   | FXP1800-48G  | -5.7  |      | 5.7   | % $V_{o \text{ nom}}$  |
|   | All models   | Max. recovery time to within 1 % of $V_{o1 \text{ nom}}$        |      | 400   | $\mu\text{s}$          |
| Current Share   | Difference in current between two units for $V_{o1}$ above 10 % load.  |   |      | 3.2   | ADC                    |
|   | FXP1800-48G  |   |      | 3.9   | ADC                    |
| Start-Up Time   | Time required for output within regulation after initial application of AC-input ( $V_{i \text{ nom}}$ , $I_{o \text{ nom}}$ )                       |   |      | 1.5   | s                      |
|   | after removal of inhibit ( $V_{i \text{ nom}}$ , $I_{o \text{ nom}}$ )   |   | 100  |       | ms                     |
| Output Voltage Ripple and Noise<br>(Filter 10 nF/10 $\mu\text{F}$ )         | $V_{i \text{ nom}}$ , $I_{o \text{ nom}}$ , 20 MHz bandwidth   |   |      | 480   | mV <sub>pp</sub>       |
|   | $V_{o1}$   |   |      | 120   | mV <sub>pp</sub>       |
| Remote Sense  | Total compensation for cable losses  |   |      | 500   | mV                     |

## 5. PROTECTION

| PARAMETER                                    | CONDITIONS/DESCRIPTION            | MIN   | NOM             | MAX         | UNIT                       |
|--|-----------------------------------|---|-----------------|-------------|----------------------------|
| Input Fuse                                   | Not user accessible               |   | 25 A, fast blow |             |                            |
| Inrush Current Limitation                    |                                   |   | With NTCs       |             |                            |
| Output                                       |                                   | No-load -, short circuit - and overload proof |                 |             |                            |
| Overvoltage Protection Latching <sup>3</sup> | Tracking<br>Absolute              | 115   |                 | 122<br>59.5 | % $V_{o \text{ nom}}$<br>V |
| Overtemperature Protection                   | Automatic power shutdown at $T_c$ |   | 95              |             | $^\circ\text{C}$           |

<sup>3</sup> Remove input voltage to reset.



## 6. CONTROLS AND INDICATORS

Specification is valid for input voltage, load, and temperature ranges, unless otherwise stated.

| PARAMETER                                     | TYPE <sup>4</sup>          | CONDITIONS / DESCRIPTION   |
|---|----------------------------|--|
| Visual Status Indication                      | FP                         | LED indicators <sup>5</sup> : <ul style="list-style-type: none"> <li>• DC OK (green)</li> <li>• AC OK (green)</li> <li>• Fan fail &amp; Over-temperature (amber)</li> </ul>  |
| I <sup>2</sup> C Communication Bus            | OC[S1, S2]                 | <ul style="list-style-type: none"> <li>• Monitors alarm functions and allows control of specific parameters.</li> <li>• Uses standard Philips two wire bus (SCL and SDA signal lines)</li> </ul>   |
| I <sup>2</sup> C Communication Bus Addressing | OC[T1-T5]                  | Five lines provide up to 32 separate PSU I <sup>2</sup> C addresses  |
| PS Present Pin                                | OC[U3]                     | <ul style="list-style-type: none"> <li>• Used by system to indicate a PSU is installed in a system shelf</li> <li>• Contact closure to logic ground ( internal pull-down resistor of 1 k<math>\Omega</math>)</li> </ul>  |
| PS Main Output Remote Shutdown                | OC[R1]<br>FP               | <ul style="list-style-type: none"> <li>• TTL compatible signal, inhibited when open contact, high or at TTL logic "1"</li> <li>• Signal referenced to logic return (LRTN)</li> </ul> Two position switch in series with OC signal (logical AND) allows local enable/disable; "0" Position => PS disabled; "1" Position => PS Enabled   |
| Power Supply OK                               | I <sup>2</sup> C           | AC OK & DC OK & no overcurrent & no over-temperature & fans working  |
| DC Current Fail                               | I <sup>2</sup> C           | Reports over-current condition on main output, I <sub>O1</sub>   |
| AC Fail / Power Down Warning                  | OC[U2] & I <sup>2</sup> C  | Provides a warning that the input power has failed at least 5 ms before the output falls out of regulation (<90% V <sub>O1</sub> set). <ul style="list-style-type: none"> <li>• Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN).</li> <li>• AC fail will go high or open during power fail condition and will go low when input is within the operating range.</li> <li>• A Power Fail warning will turn off the front panel green AC OK LED.</li> </ul> Internal under-voltage and overvoltage supervision of V <sub>O1</sub> . <ul style="list-style-type: none"> <li>• Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN).</li> <li>• DC fail will go high or open if V<sub>O1</sub> &lt; 90% or V<sub>O1</sub> &gt; 110% of V<sub>O1</sub> set, measured in front of the ORing FETs.</li> <li>• Green LED on the front panel indicates normal operation; LED will flash if in parallel operation V<sub>O1</sub> is OK, but the unit is disabled.</li> </ul> |
| DC Fail / Output Voltage Fault                | OC[U4] & I <sup>2</sup> C  | Internal under-voltage and overvoltage supervision of V <sub>O1</sub> . <ul style="list-style-type: none"> <li>• Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN).</li> <li>• DC fail will go high or open if V<sub>O1</sub> &lt; 90% or V<sub>O1</sub> &gt; 110% of V<sub>O1</sub> set, measured in front of the ORing FETs.</li> <li>• Green LED on the front panel indicates normal operation; LED will flash if in parallel operation V<sub>O1</sub> is OK, but the unit is disabled.</li> </ul>   |
| Critical Temperature Warning/Fan Fail         | OC[U1] & I <sup>2</sup> C  | Indicates the PSU operating temperature has reached [T <sub>shut-down</sub> - 10K] Indicates if the unit is in over-temperature shutdown. <ul style="list-style-type: none"> <li>• Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN).</li> <li>• The OC-output will go low 100 ms before an over-temperature condition shuts down the unit.</li> <li>• An amber LED on the front panel indicates over-temperature or fan fail.</li> </ul>   |
| DC Voltage Monitoring                         | I <sup>2</sup> C           | Monitors the main output voltage, V <sub>O1</sub> , seen at the output connector. Accuracy is $\pm 0.45V$ over setting range and temperature.  |
| DC Current Monitoring                         | I <sup>2</sup> C           | Monitors the output current I <sub>O1</sub> : Accuracy $\pm 0.4A$ over the load range.   |
| DC Voltage Trimming (Margining)               | OC[R4]<br>I <sup>2</sup> C | Output voltage trimming V <sub>O1</sub> : $\pm 8\%$ of V <sub>O</sub> set using external resistor<br>Setting accuracy over I <sup>2</sup> C: $\pm 50mV$ at V <sub>O1nom</sub> , $\pm 150mV$ over setting range   |
| Fan Speed Control                             | I <sup>2</sup> C           | Two fan speed levels automatically set depending on the internal temperature. The fan speed can be set to full speed or automatic control via I <sup>2</sup> C command.  |
| Fan OK/FAIL                                   | OC[U1] & I <sup>2</sup> C  | Indicates if the cooling fans are operating or have failed.  |
| Synchronized Startup Pin                      | OC[R5]                     | Overcurrent signal which can be used for synchronous startup of units in parallel or to recover from an overload condition.  |

<sup>4</sup> Abbreviations used:

- **OC[#]** => Hardwired signal accessible at PSU output connector, with pin number reference
- **FP** => Provided by devices located on PSU Front panel
- **I<sup>2</sup>C** => Signal provided over I<sup>2</sup>C communication system; detailed I<sup>2</sup>C information is available from the specific model's I<sup>2</sup>C Manual found on the Bel Power Solutions web site.

<sup>5</sup> See LED Function table for further details

## 7. ENVIRONMENTAL, MECHANICAL, & RELIABILITY SPECIFICATIONS

| PARAMETER                         | CONDITIONS / DESCRIPTION                   | MIN | NOM  | MAX  | UNIT             |
|-----------------------------------|--|-----|------|------|------------------|
| Altitude                          | Operating                                  |     |      | 10 k | ASL Ft.          |
|                                   | Non-Operating                              |     |      | 40 k |                  |
| Relative Humidity, Non-Condensing | Operating                                  | 10  |      | 90   | % RH             |
|                                   | Storage                                    | 5   |      | 95   | % RH             |
| Temperature Coefficient           | 0 °C to 70 °C (after 15 min warm-up)       |     |      | 0.02 | %/K              |
| Shock                             | IEC/EN 60068-2-27, 11 ms                   |     |      | 40   | g <sub>pk</sub>  |
| Sinusoidal Vibration              | IEC/EN 60068-2-6                           |     |      |      |                  |
|                                   | 2-8 Hz                                     |     | 7.5  |      | mil              |
|                                   | 8-200 Hz                                   |     | 2    |      | g <sub>pk</sub>  |
| Random Vibration                  | 200-500 Hz                                 |     | 4    |      | g <sub>pk</sub>  |
|                                   | 10-2000 Hz                                 |     | 6.15 |      | g <sub>rms</sub> |
| MTBF                              | Calculated per Bellcore (SR-332, Issue 1): |     |      |      |                  |
|                                   | GB 25 °C                                   | 230 |      |      | kh               |
|                                   | GB 25 °C (FNP1500-12G)                     | TBD |      |      |                  |
|                                   | Demonstrated                               | 250 |      |      |                  |

## 8. SAFETY SPECIFICATIONS

Maximum electric strength testing is performed in the factory according to EN50514, IEC/EN60950-1 2<sup>nd</sup> ed. and UL/CSA60950-1 2<sup>nd</sup> ed. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

| PARAMETER                      | CONDITIONS / DESCRIPTION  | MIN              | NOM        | MAX | UNIT |
|--------------------------------|---|------------------|------------|-----|------|
| Agency Approvals               | Approved to latest edition of the following standards:<br>UL/CSA60950-1, IEC60950-1 and EN60950-1.<br>CE Mark for LVD |                  |            |     |      |
| Insulation Safety Rating       | Input to case   |                  | Basic      |     |      |
|                                | Input to output   |                  | Reinforced |     |      |
|                                | Output to case  |                  | Functional |     |      |
| Electric Strength Test Voltage | Input to case   | 2.12             |            |     | kVDC |
|                                | Input to output   | 4.2 <sup>6</sup> |            |     | kVDC |
|                                | Output to case  | 0.5              |            |     | kVDC |
|                                | Output 1 to output 2  | 0.1              |            |     | kVDC |

<sup>6</sup> Subassemblies are pre-tested with 4.2 kVDC in accordance with EN50514 and IEC/EN60950-1 2<sup>nd</sup> ed.

## 9. EMC SPECIFICATIONS

| PARAMETER                        | DESCRIPTION                     | CRITERION   |
|----------------------------------|---------------------------------|---|
| Electrostatic Discharge          | IEC/EN 61000-4-2, level 4       | Performance criterion B                           |
| Electromagnetic Field            | IEC/EN 61000-4-3, level 3       | Performance criterion A                           |
| Electrical Fast Transients/Burst | IEC/EN 61000-4-4, level 3       | Performance criterion B                           |
| Surge                            | IEC/EN 61000-4-5, level 3       | Performance criterion B                           |
| Voltage Dips and Interruptions   | IEC/EN 61000-4-11               | Performance criterion B or better                 |
| RF Conducted Immunity            | IEC/EN 61000-4-6                | 10 VAC, AM 80 %, 1 kHz<br>Performance criterion A |
| Emissions Conducted              | CISPR 22/EN 55022/EN 61204      | Class B   |
| Emissions Radiated               | CISPR 22/EN 55022/EN 61204      | Class A   |
| Harmonics                        | IEC/EN 61000-3-2                | Class B   |
| Voltage Fluctuation and Flicker  | IEC/EN 61000-3-3                | Pass  |
| Voltage Sag                      | SEMI F47-0200 (High Line 230 V) | Pass  |



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## 10. OUTPUT CONNECTOR PINNING AND SIGNAL SPECIFICATION (48V MODELS)

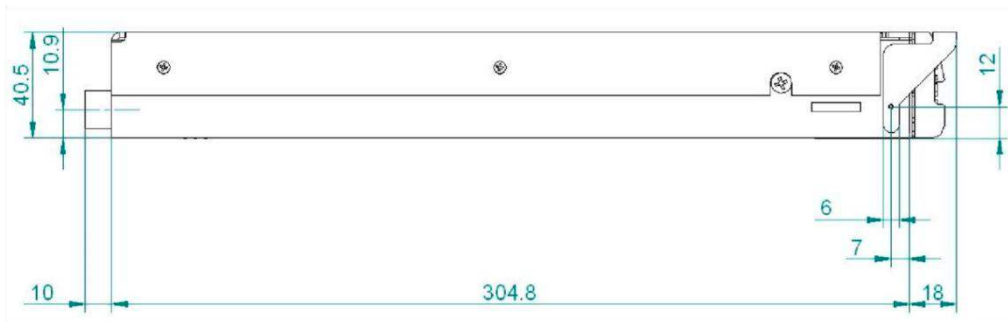
| OUTPUT CONNECTOR DESCRIPTION                | OC PIN #   | TYPE   | SIGNAL REFERENCE   | LOW LEVEL HIGH LEVEL      | V MAX I MAX                   |
|---|------------|--|--|---------------------------|-------------------------------|
| Over-temperature / Fan Fail                 | U1         | OC-output, protected by 16 V Zener diode and a 10Ω resistor in series  | LGND   | <0.4 V @ 20 mA<br>Pull up | 15 V<br>20 mA                 |
| AC Fail / Power down warning                | U2         |  |  | <0.4 V @ 20 mA<br>Pull up | 15 V<br>20 mA                 |
| Power Supply Present                        | U3         | 1KΩ Resistor connected to logic GND  | LGND   | Open<br>Pull up           | 10 V<br>10 mA                 |
| DC Fail / Output voltage fault              | U4         | OC-output, protected by 16 V Zener diode and a 10Ω resistor in series  | LGND   | <0.4V @ 20 mA<br>Pull up  | 15 V<br>20 mA                 |
| Internal ground (INT GND)                   | U5         | Used only for ADDR <sub>x</sub> and V <sub>O1</sub> set. Do not connect the internal grounds in systems with several units.  | Connected to V <sub>O1</sub> - line before the output filter | -                         | -                             |
| ADDR0 I <sup>2</sup> C address bus          | T1         | High = internal 10 KΩ PU to 5V=> Logic 1<br>Low = connect to INT GND => Logic 0  | INT GND  | Logic 1<br>Logic 0        | 5V<br>0V                      |
| ADDR1 I <sup>2</sup> C address bus          | T2         |  |  |                           |                               |
| ADDR2 I <sup>2</sup> C address bus          | T3         |  |  |                           |                               |
| ADDR3 I <sup>2</sup> C address bus          | T4         |  |  |                           |                               |
| ADDR4 I <sup>2</sup> C address bus          | T5         |  |  |                           |                               |
| SDA, I <sup>2</sup> C serial data line      | S1         | I <sup>2</sup> C compatible signal referenced to logic GND 5 V or 3.3 V logic  | LGND   | Logic 1<br>Logic 0        | 3.3V to 5V<br>0V              |
| SCL, I <sup>2</sup> C serial clock line     | S2         |  |  |                           |                               |
| Auxiliary power +12 V                       | S3         | V <sub>O2+</sub> output, isolated from main output   | Aux output is floating                                       | -                         | -                             |
| Auxiliary power +12VRTN                     | S4         | Aux output return; ground isolated from main output  |  |                           |                               |
| Logic ground (LGND)                         | S5         | Internally connected to Aux GND through 10Ω resistor. Wire LGND separately from Aux RTN and main output GND to minimize noise on signals and I <sup>2</sup> C bus. Leave open if not used. | -  | -                         | -                             |
| Output inhibit R1                           | R1         | PS active when pulled low (DC-DC stage off when left open)   | LGND   | <0.8 V<br>>2.0 V          | 10 V<br>3.5 mA                |
| V sense +                                   | R2         | Open or connected to V <sub>O1+</sub> at the load<br>Internally connected to V <sub>O1+</sub> via 100 Ω.   | -  | -                         | dV<3 V <sub>pp</sub><br>30 mA |
| V sense -                                   | R3         | Open or connected to V <sub>O1-</sub> at the load<br>Internally connected to V <sub>O1-</sub> via 100 Ω.   | -  | -                         |                               |
| Output margin                               | R4         | Open or connected to INT GND (+8% V <sub>O1</sub> ) or V <sub>sense+</sub> (-8% V <sub>O1</sub> ), Do not interconnect margin pins in systems with paralleled PSUs.                        | -  | -                         | 60 V                          |
| Synchronized Startup (for paralleled units) | R5         | Open or connected to synch startup circuit   | V <sub>O1</sub> - at the OC                                  | -                         | 12 V<br>2 mA                  |
| V <sub>O1-</sub>                            | P1, P3, P5 | Main output - pins   | -  | -                         | -                             |
| V <sub>O1+</sub>                            | P2, P4, P6 | Main output + pins   | -  | -                         | -                             |
| INPUT CONNECTOR DESCRIPTION                 | OC PIN #   | TYPE   |  |                           |                               |
| Protection Earth                            | P1         | PE   |  |                           |                               |
| Phase                                       | P2         | L  |  |                           |                               |
| Neutral                                     | P3         | N  |  |                           |                               |

## 11.LED INDICATOR FUNCTIONALITY

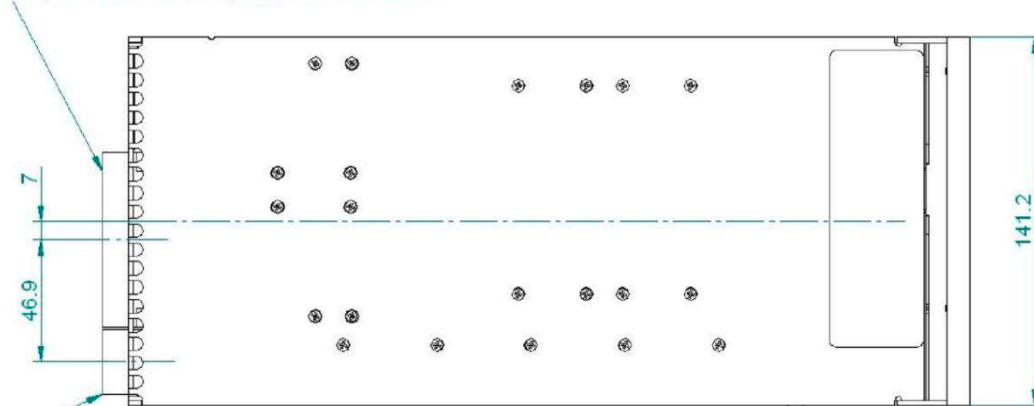
| CONDITION                                 | POWER FAIL (AC OK) | OUTPUT GOOD (DC OK) | FAN FAIL AND OVER - TEMPERATURE |
|---|--------------------|---------------------|---------------------------------|
| Normal Operation                          | Green              | Green               | OFF                             |
| Power Supply is Inhibited                 | Green              | OFF                 | Amber                           |
| Input AC is Low                           | OFF                | OFF                 | Amber                           |
| Input AC is Low Or Missing                | OFF                | OFF                 | Amber/OFF                       |
| Over-Temperature                          | Green              | OFF                 | Amber                           |
| Output Overload (In Regulation)           | Green              | Green               | OFF                             |
| Output Overloaded (Out Of Regulation)     | Green              | OFF                 | OFF                             |
| Fan Fault (No Overtemperature Shutdown)   | Green              | Green               | Amber                           |
| Fan Fault (With Overtemperature Shutdown) | Green              | OFF                 | Amber                           |
| Power Supply Failed                       | OFF                | OFF                 | OFF/ Amber                      |

## 12.MECHANICAL DATA

Mechanical Dimensions (W x H x D): 5.6" (141.2 mm) x 1.6" (40.5 mm) x 12" (304.8 mm)



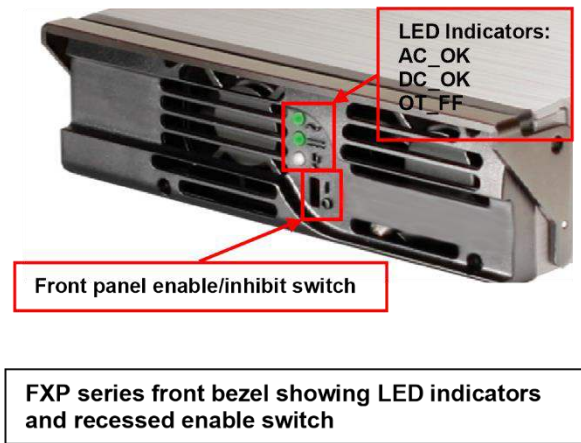
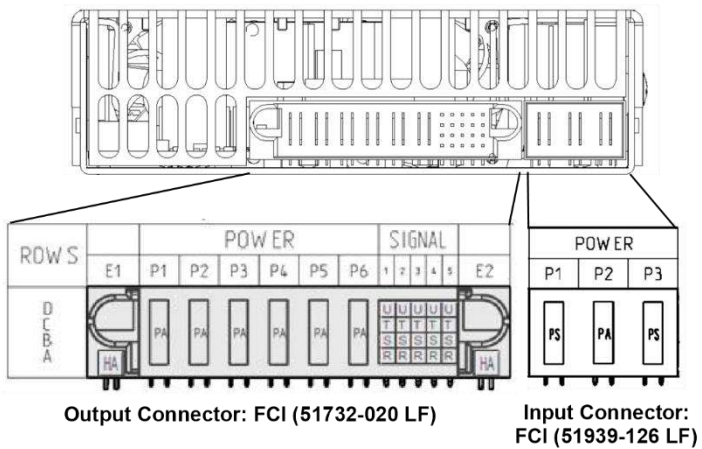
Output Connector FCI part no. 51732-020LF



Input Connector FCI part no. 51939-126LF



### 13.INPUT & OUTPUT CONNECTOR DESCRIPTION



Female ledge connector: Manufacturer: FCI

Output connector Part No.: 51762-106020000AA LF (Horizontal)

Output connector Part No.: 51742-106020000AA LF (Vertical)

Input connector Part No.: 51915-056LF (Horizontal)

Input connector Part No.: 51940-099LF (Vertical)

Information on availability under <http://www.stkcheck.com/evs/fcielectronics/fcisearch.asp>

### 14.PARALLELING FRONT-ENDS

For parallel use in minimal configuration systems, only the inhibit pins must be shorted to logic GND. All other pins can be left open. The power supplies will share the output current automatically (droop current share).

For parallel applications without I2C bus, but the use of all other features, it is recommended to connect all logic GND's on a backplane together, to connect all Vo2 -, all V o2 + and to leave the internal GND's open.

The sense wires can be left open or connected to a common load point, the synch-start pin can be left open or connected to a synch-start circuit, the inhibit pins can be connected together or used individually. All I2C signals (T1-T5, S1, and S2) can be left open.

Use of a small foil capacitor > 3 $\mu$ F directly at the power outputs of each unit is recommended in order to prevent voltage drops at the hot plug. For additional information on paralleling see the following Rack (Power Shelf) section.

### 15.COOLING

To achieve best cooling results sufficient airflow through the unit must be ensured. Do not block or obstruct the airflow at the rear of the unit by placing large components directly at the output connector.





## 16.FXR-3-48G POWER SHELF

Each rack (power shelf) is 1U high with backplane and designed for up to three front-end models in parallel or in n+1 operation. Each power shelf has:

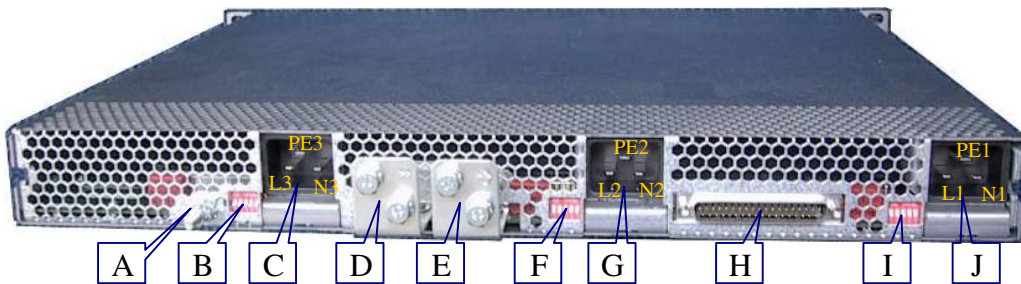
- Massive copper bus bars for low-loss current distribution.
- Output terminals with two M4-screws on each power tab.
- Two fast-on contacts for system earthing.
- Address coding over five pole DIP switch on each unit, 37-pin D-Sub connector with I<sup>2</sup>C-lines, monitoring signals and support functions.
- Provides a start-up synchronization circuit and EMV filters.

Overall Mechanical Dimensions (W x H x D): 17.7" (449.6 mm) x 1.7" (43.1 mm) x 14" (355.6 mm)



FXR-3-48G Power Shelf Front View

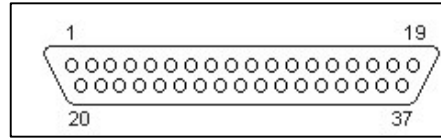
### Output Connector Descriptions (FXR-3-48G)



| LOCATION | DESCRIPTION  |  |
|----------|--|--|
| A        | Earth connection   |  |
| B        | 5-bit DIP switch for I <sup>2</sup> C addressing of PSU #3                   |  |
| C        | Mains connector of PSU #3  |  |
| D        | Output 1 Minus   |  |
| E        | Output 1 Plus  |  |
| F        | 5-bit DIP switch for I <sup>2</sup> C addressing of PSU #2                   |  |
| G        | Mains connector of PSU #2  |  |
| H        | 37-pin SUB-D connector, control, sense, check and Auxiliary power (Output 2) |  |
| I        | 5-bit DIP switch for I <sup>2</sup> C addressing of PSU #1                   |  |
| J        | Mains connector of PSU #1  |  |

## SUB-D Output Connector Pinout and Signal Specification

| OUTPUT CONNECTOR DESCRIPTION         | OC PIN | TYPE   | SIGNAL REFERENCE | LOW LEVEL HIGH LEVEL                                      | V MAX I MAX                     |
|--------------------------------------|--------|--|------------------|---|---------------------------------|
| Overtemperature / Fan Fail PSU1      | 1      | OC-output, protected by 16 V Zener diode and a 10 $\Omega$ resistor in series.   | LGND             | <0.4 V @ 20 mA<br>Pull up                                 | 15 V<br>20 mA                   |
| Power Supply Present PSU 1           | 2      | Resistor (1 k $\Omega$ ) connected to logic GND  | LGND             | Open<br>Pull up   | 10 V<br>10 mA                   |
| Power Supply Present PSU 2           | 3      |  |                  |   |                                 |
| Spare                                | 4      |  |                  |   |                                 |
| Overtemperature / Fan Fail PSU 3     | 5      | OC-output, protected by 16 V Zener diode and a 10 $\Omega$ resistor in series.   | LGND             | <0.4 V @ 20 mA<br>Pull up                                 | 15 V<br>20 mA                   |
| AC Fail /Power down warning PSU 3    | 6      |  |                  |   |                                 |
| Power Supply Present PSU 3           | 7      | Resistor (1 k $\Omega$ ) connected to logic GND  | LGND             | Open<br>Pull up   | 10 V<br>10 mA                   |
| DC Fail / Output voltage fault PSU 3 | 8      | OC-output, protected by 16 V Zener diode and a 10 $\Omega$ resistor in series  | LGND             | <0.4 V @ 20 mA<br>Pull up                                 | 15 V<br>20 mA                   |
| Overtemperature / Fan Fail PSU 2     | 9      |  |                  |   |                                 |
| Synch._Start_A                       | 10     | Sync_start_A , Active high<br>The signals of several racks can be connected together in such a way that all supplies will be inhibited until the last supply has recovered from its overcurrent condition. | LGND             | <7V off<br>< 9V   | 15V<br>10mA                     |
| Spare                                | 11     |  |                  |   |                                 |
| Output inhibit PSU 1-3               | 12     | DC-DC stage ON when pin is open or connected to LGND<br>DC-DC stage OFF when pin is connected on high potential  | LGND             | <0.8 V<br>>2.0 V  | 10 V<br>3.5 mA                  |
| V sense +                            | 13     | Open or connected to $V_{o1+}$ at the load Internally (PSU) connected to $V_{o1+}$ over 100 $\Omega$   | $V_{o1+}$        |   | dV < 3 V <sub>pp</sub><br>30 mA |
| V sense -                            | 14     | Open or connected to $V_{o1-}$ at the load Internally (PSU) connected to $V_{o1-}$ over 100 $\Omega$   | $V_{o1-}$        |   | dV < 3 V <sub>pp</sub><br>30 mA |
| Spare                                | 15     |  |                  |   |                                 |
| NC                                   | 16     |  |                  |   |                                 |
| NC                                   | 17     |  |                  |   |                                 |
| NC                                   | 18     |  |                  |   |                                 |
| NC                                   | 19     |  |                  |   |                                 |
| AC Fail/Power-down warning PSU 1     | 20     |  |                  |   |                                 |
| DC Fail/Output voltage fault PSU 1   | 21     | OC-output, protected by 16 V Zener diode and a 10 $\Omega$ resistor in series  | LGND             | <0.4 V @ 20 mA<br>Pull up                                 | 15 V<br>20 mA                   |
| AC Fail/Power-down warning PSU 2     | 22     |  |                  |   |                                 |
| DC Fail/Output voltage fault PSU 2   | 23     |  |                  |   |                                 |
| SDA, I <sup>2</sup> C data line      | 24     |  |                  |   |                                 |
| SCL, I <sup>2</sup> C clock line     | 25     | I <sup>2</sup> C compatible signal   | LGND             | 5 V or 3.3 V logic  |                                 |
| Vo2+ = +12 V (Auxiliary power)       | 26     | Vo2+ Aux output, insulated from main output  |                  | Aux output is isolated supply                             |                                 |
| Vo2- = +12 VRTN (Auxiliary power)    | 27     | Vo2- Aux output, insulated from main output  |                  |   |                                 |
| Logic Gnd (LGND)                     | 28     | Wire separately from auxiliary and main output GND to minimize noise and avoid voltage drops on signal- and I2C return. Leave open if not used.  |                  | Internally connected to Vo2 Auxiliary GND via 10 $\Omega$ |                                 |
| Output margin PSU 1                  | 29     | Open or connected to V sense:<br>V sense- (+8 % Vo1) or V sense+ (-8 % Vo1)  |                  |   | 60 V                            |
| Output margin PSU 2                  | 30     |  |                  |   |                                 |
| Output margin PSU 3                  | 31     |  |                  |   |                                 |
| NC                                   | 32     |  |                  |   |                                 |
| NC                                   | 33     |  |                  |   |                                 |
| NC                                   | 34     |  |                  |   |                                 |
| NC                                   | 35     |  |                  |   |                                 |
| NC                                   | 36     |  |                  |   |                                 |
| NC                                   | 37     |  |                  |   |                                 |

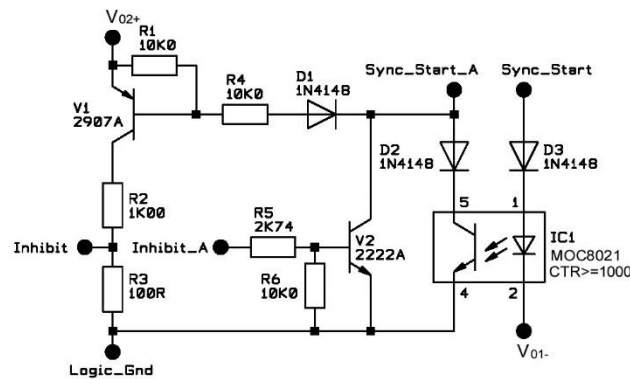


SUB-D Output Connector

## Synchronized Start-Up Circuit for Paralleling Operation

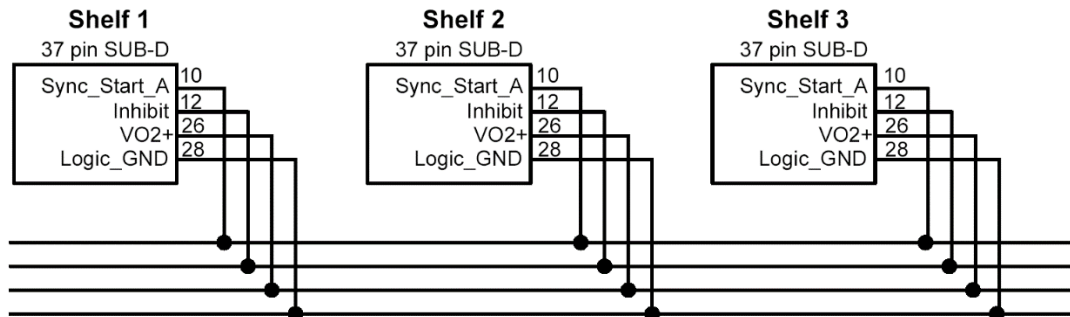
The FXP1500-48G and FXP1800-48G power supplies exhibit an overcurrent hiccup behaviour. This means if either of these supplies reaches an overcurrent limit, the output voltage will immediately turn OFF and after a delay turn ON again. In parallel use, all power supplies have to start synchronized because of the internal hiccup behaviour. Otherwise, the supply which has reached overcurrent first will go to hiccup; this will overload the other supplies, which then will also go to hiccup. When the first supply has recovered from hiccup (hiccup dead time), the others remain in hiccup. This will immediately drive the first one into hiccup once again. This means that without a start-up circuit, a system with several power supplies can never recover from an overload condition or start-up into full load.

The following additional circuit, required to reach synchronized startup, is already implemented inside the FXR-3-48G shelf.



## Synch Start-up Connection between Shelves

The following connection between the shelves is required to achieve a parallel operation. The synch-start circuits inside the shelves inhibit all power supplies until the last one has recovered from its overcurrent condition and then synchronize the restart of the outputs.

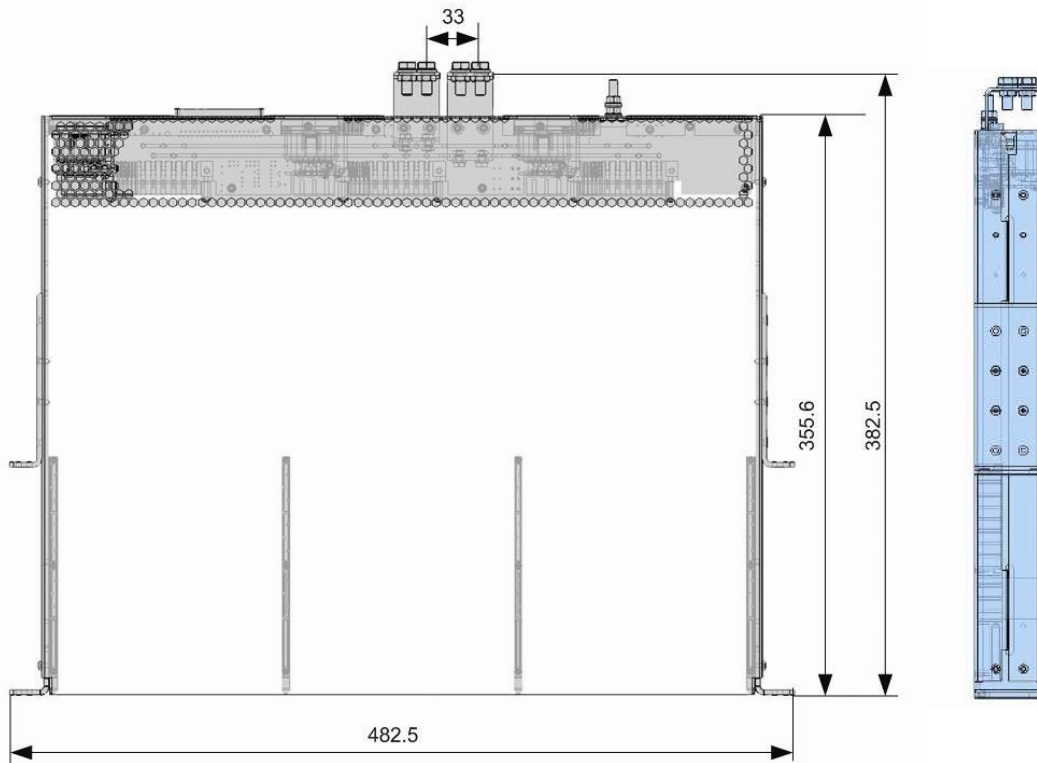


### Synch Start-up Circuit Description

| DESCRIPTION   | PIN LOCATION, DEFINITION | TYPE   | SIGNAL REFERENCE                                   | LOW LEVEL<br>HIGH LEVEL | V MAX<br>I MAX |
|---|--------------------------|--|--|-------------------------|----------------|
| Auxiliary Power +12 V (Output 2)  | 26                       | $V_{o2+}$ , Aux output, insulated from main output   |  |                         |                |
| Logic Ground  | 28                       | Logic_GND ,Internally connected over 10 $\Omega$ to $V_{o2-}$ , ( Auxiliary power ground (Output 2))   | Internally connected over 10 $\Omega$ to $V_{o2-}$ |                         |                |
| Output Inhibit_A PSU 1-3  | 12                       | Inhibit_A,<br>DC-DC stage ON when pin is open or connected to LGND<br>DC-DC stage OFF when pin is connected on high potential  | LGND   | <0.8 V<br>>2.0 V        | 10 V<br>3.5 mA |
| Synch. Startup 1 PSU 1-3  | R5 (at PSU)              | The synch_start pin is connected to the over-current signal of the PSU1-3. In the case of an overcurrent shutdown, this signal goes high.  | $V_{o1-}$  | <7V off<br>> 9V         | 15V<br>10mA    |
| Synch. Startup_A Rack FXR-3-48G 1-N Pin on the D-Sub connector on the backplane | 10                       | Sync_start_A, Active high The signals of several racks can be connected together in such a way that all supplies will be inhibited until the last supply has recovered from its overcurrent condition. | LGND   |                         |                |

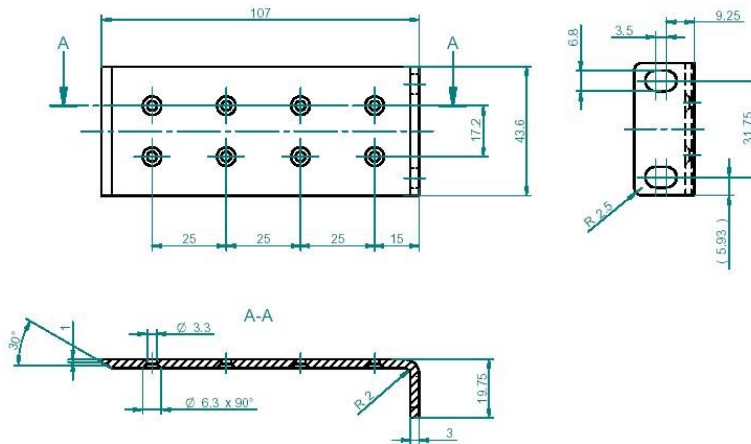
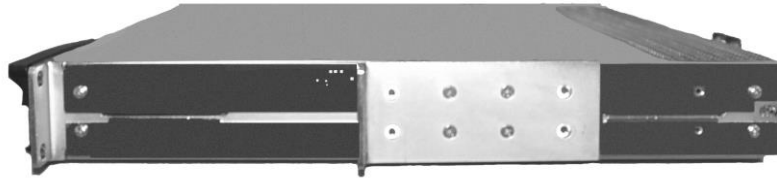
NOTE: The Sync-Start pins can be wired together only if the power supplies are connected with a minimal voltage drop on power ground as achieved on a backplane with massive copper bus bars. If there is a less ideal connection, it is recommended to use an opto-coupler for each unit (IC1, D3, D2).

### Mechanical Data (FXR-3-48G Power Shelf)

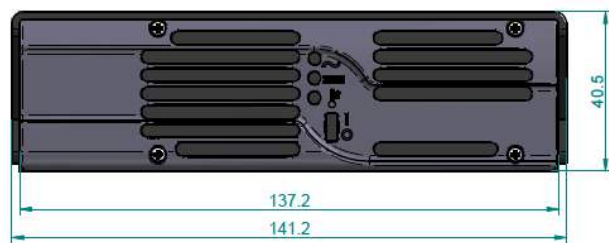
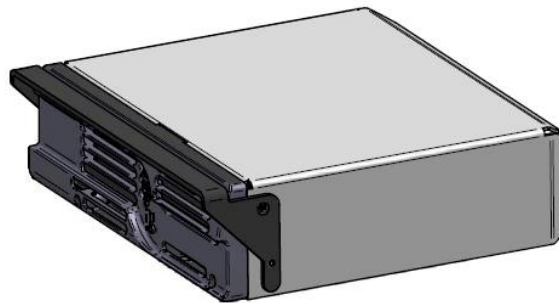


## 17.ACCESSORIES

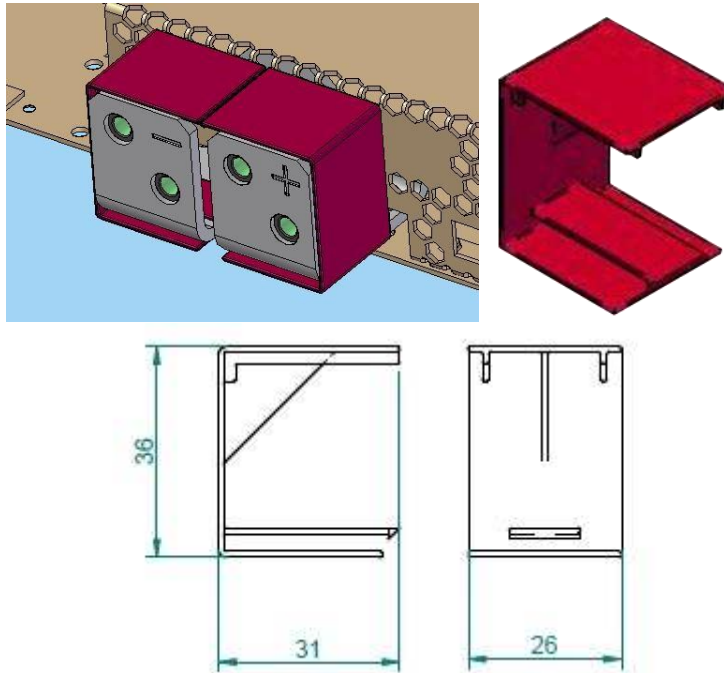
Center Angular Brackets are set in the middle for shelf mounting:



Center Angular Bracket sets can be ordered: Bel Power Solutions part no.: HZZ01222 Note: Each Center Angular Bracket set contains 2 brackets and 8 screws. Filler for covering of the empty shelf slots



Filler can be ordered: Bel Power Solutions part no.: XAK.00043.0  
 Plastic cover set for the bus bars:



Plastic cover set can be ordered: Bel Power Solutions part no.: XEB.00031.0

Note1: Available upon special request.

Note2: Each plastic cover set contains 2pcs.

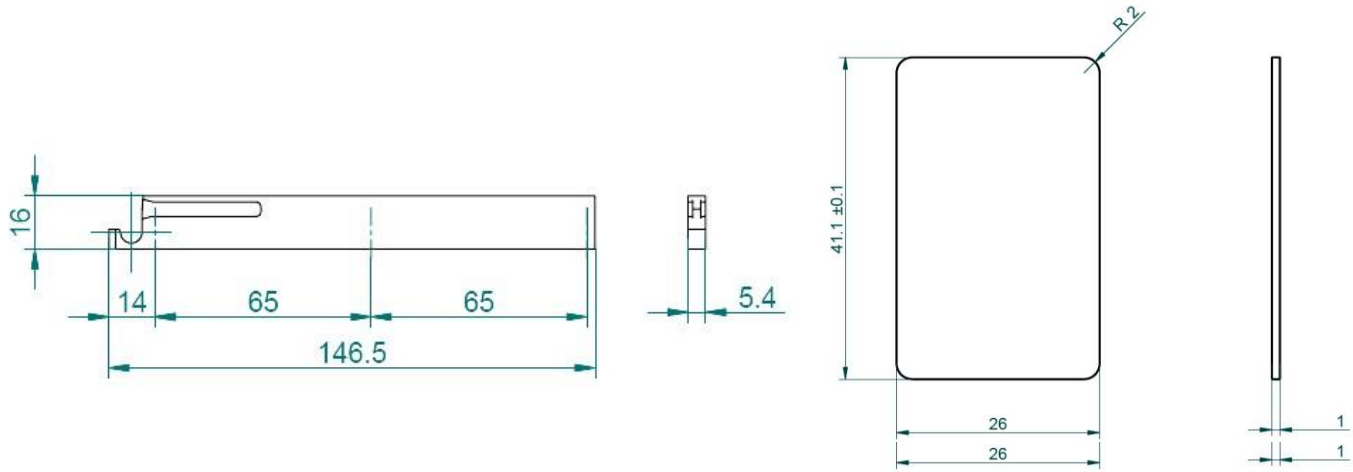
### Fulcrum

The handle has been designed to allow easy plug-in and -out in a rack system. The handle (lever) fits into a counter piece (fulcrum) which is fixed to the bottom of the rack. During the plug, the fulcrum holds the unit down and guides it towards the output connector. The Bel Power Solutions part number of the fulcrum and its associated mounting accessories is: HZZ01223.

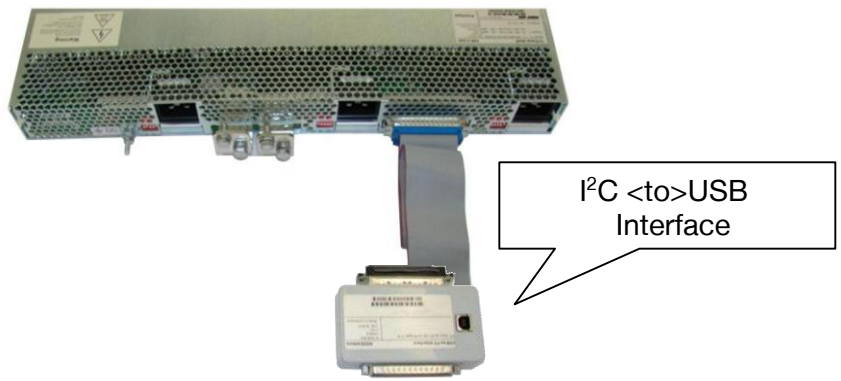
Individual fulcrum sets can be also ordered: Bel Power Solutions part no.: HZZ01223.

Note: Each HZZ01223 set contain 2 fulcrums, 2 supports, and mounting accessories.





I<sup>2</sup>C to USB Interface HZZ02002G



**I<sup>2</sup>C Management Software:** All FNP and FXP front-ends can be controlled via Bel Power Solutions GUI-driven I<sup>2</sup>C Management software and an I<sup>2</sup>C-to-USB interface (P/N HZZ02002G). An I<sup>2</sup>C Programming Manual describes the complete range of parameters that can be programmed to the FXP1500/1800 front-ends. This manual is available by searching on "FXP1500" at [www.belpowersolutions.com](http://www.belpowersolutions.com).

**For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)**

**NUCLEAR AND MEDICAL APPLICATIONS** - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

**TECHNICAL REVISIONS** - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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