

## Quad Complementary CMOS Analog Switch

### DESCRIPTION

The versatile DG213 analog switch has two NC and two NO switches. It can be used in various configurations, including four single-pole single-throw (SPST), two single-pole double-throw (SPDT), one "T" switch, one DPDT, etc. This device is fabricated in a Vishay Siliconix' proprietary high-voltage silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

This analog switch was designed for a wide variety of general purpose applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. These switches can handle up to  $\pm 22$  V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All switches feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

For additional information, please refer to Application Note AN208 (FaxBack document #70606).

### FEATURES

- $\pm 22$  V supply voltage rating
- TTL and CMOS compatible logic
- Low on-resistance -  $r_{DS(on)}$ : 45  $\Omega$
- Low leakage -  $I_{D(on)}$ : 20 pA
- Single supply operation possible
- Extended temperature range
- Fast switching -  $t_{ON}$ : 85 ns

### BENEFITS

- Low charge injection - Q: 1 pC
- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Low cost

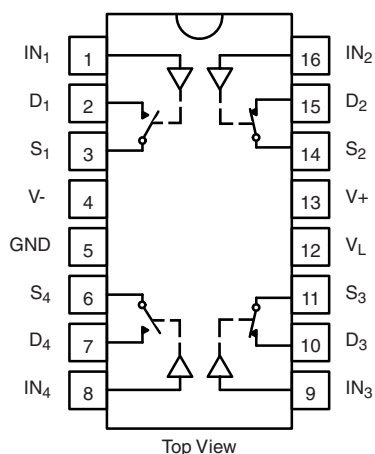
### APPLICATIONS

- Industrial instrumentation
- Test equipment
- Communications systems
- Computer peripherals
- Portable instruments
- Sample-and-hold circuits



Available  
**RoHS\***  
COMPLIANT

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	SW <sub>1</sub> , SW <sub>4</sub>	SW <sub>2</sub> , SW <sub>3</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

\* Pb containing terminations are not RoHS compliant, exemptions may apply.



ORDERING INFORMATION			
Temp. Range	Package	Standard Part Number	Lead (Pb)-free Part Number
- 40 °C to 85 °C	16-Pin Plastic DIP	DG213DJ	DG213DJ-E3
	16-Pin Narrow SOIC	DG213DY DG213DY-T1	DG213DY-E3 DG213DY-T1-E3
	16-Pin TSSOP	DG213DQ DG213DQ-T1	DG213DQ-E3 DG213DQ-T1-E3

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted			
Parameter	Limit	Unit	
Voltages Referenced $V_+$ to $V_-$	44	V	
GND	25		
Digital Inputs <sup>a</sup> $V_S, V_D$	$(V_-) - 2$ to $(V_+) + 2$ or 30 mA, whichever occurs first		
Current, Any Terminal	30	mA	
Peak Current (Pulsed at 1 ms, 10 % duty cycle max.)	100		
Storage Temperature	- 65 to 125	°C	
Power Dissipation <sup>b</sup>	16-Pin Plastic DIP <sup>c</sup>	470	mW
	16-Pin Narrow SOIC <sup>d</sup>	640	
	16-Pin TSSOP <sup>d</sup>	500	

Notes:

- a. Signals on  $S_X, D_X,$  or  $IN_X$  exceeding  $V_+$  or  $V_-$  will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.5 mW/°C above 75 °C.
- d. Derate 7.6 mW/°C above 75 °C.



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ , $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp. <sup>a</sup>	D Suffix - 40 °C to 85 °C			Unit
				Min. <sup>c</sup>	Typ. <sup>b</sup>	Max. <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	V-		V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = 1\text{ mA}$	Room		45	60	$\Omega$
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Full			85	
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}$ , $V_D = \pm 14\text{ V}$	Room	- 0.5	$\pm 0.01$	0.5	nA
Drain Off Leakage Current	$I_{D(off)}$		Full	- 5		5	
Drain On Leakage Current <sup>f</sup>	$I_{D(on)}$	$V_S = V_D = 14\text{ V}$	Room	- 0.5	$\pm 0.02$	0.5	
Full			Full	- 10		10	
<b>Digital Control</b>							
Input Voltage High	$V_{INH}$		Full	2.4			V
Input Voltage Low	$V_{INL}$		Full			0.8	
Input Current	$I_{INL}$ or $I_{INH}$	$V_{INH}$ or $V_{INL}$	Full	- 1		1	$\mu\text{A}$
Input Capacitance	$C_{IN}$		Room		5		pF
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$V_S = 10\text{ V}$ See Figure 2	Room		85	130	ns
Turn-Off Time	$t_{OFF}$		Room			55	
Break-Before-Make Time Delay	$t_D$	$V_S = 10\text{ V}$ , See Figure 3	Room	15	25		
Charge Injection	Q	$C_L = 1000\text{ pF}$ , $V_g = 0\text{ V}$ , $R_g = 0\ \Omega$	Room		1		pC
Source-Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$		Room			5	
Channel On Capacitance	$C_{D(on)}$	$V_D = V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room		16		
Off-Isolation	OIRR	$C_L = 15\text{ pF}$ , $R_L = 50\ \Omega$ $V_S = 1\text{ V}_{RMS}$ , $f = 100\text{ kHz}$	Room		90		dB
Channel-to-Channel Crosstalk	$X_{TALK}$		Room			95	
<b>Power Supply</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0$ or $5\text{ V}$	Room			1	$\mu\text{A}$
Negative Supply Current	$I_-$		Full	- 1		5	
Logic Supply Current	$I_L$		Full	- 5			
Power Supply Range for Continuous Operation	$V_{OP}$		Full	$\pm 3$		$\pm 22$	V



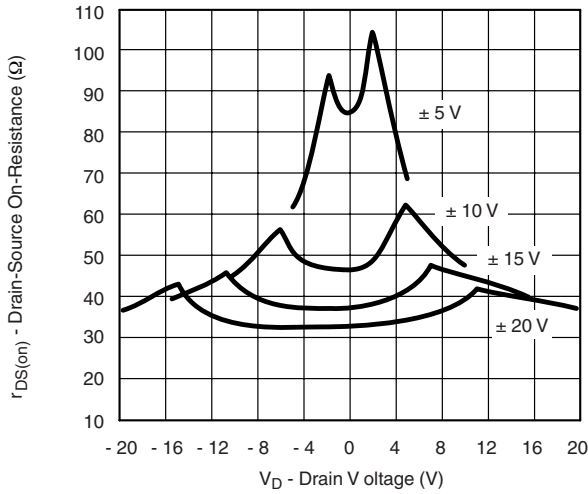
SPECIFICATIONS for Unipolar Supply							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$ , $V_- = 0\text{ V}$ , $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp. <sup>a</sup>	D Suffix - 40 °C to 85 °C			Unit
				Min. <sup>c</sup>	Typ. <sup>b</sup>	Max. <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	V-		V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = 3\text{ V}$ , $I_S = 1\text{ mA}$	Room Full		90	110 140	$\Omega$
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	See Figure 2	Room		125	200	ns
Turn-Off Time	$t_{OFF}$		Room		45	100	
Break-Before-Make Time Delay	$t_D$	$V_S = 8\text{ V}$ , See Figure 3	Room	50	80		
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_{gen} = 6\text{ V}$ , $R_{gen} = 0\ \Omega$	Room		4		pC
<b>Power Supply</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	- 1 - 5			
Logic Supply Current	$I_L$		Room Full			1 5	
Power Supply Range for Continuous Operation	$V_{OP}$		Full	+ 3		+ 40	V

Notes:

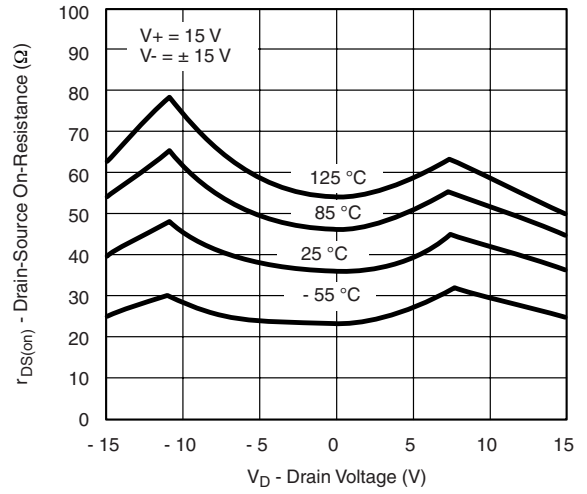
- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

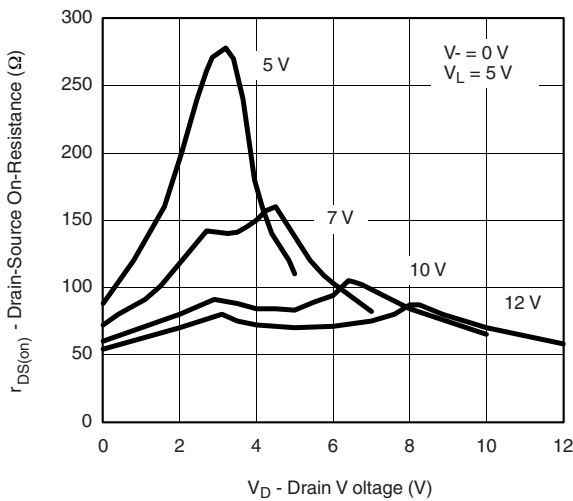
**TYPICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted



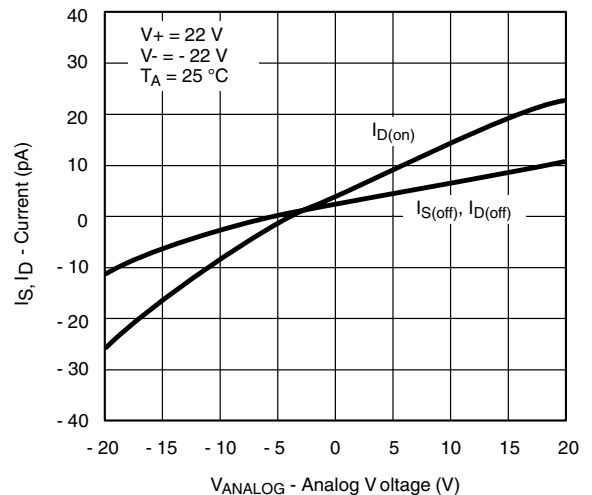
**$r_{DS(on)}$  vs.  $V_D$  and Power Supply Voltages**



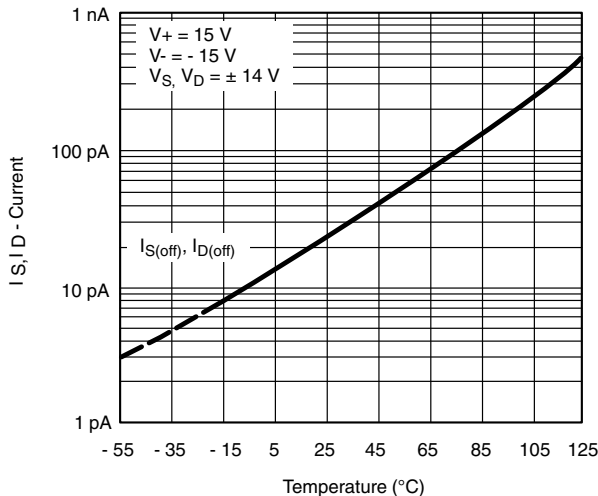
**$r_{DS(on)}$  vs.  $V_D$  and Temperature**



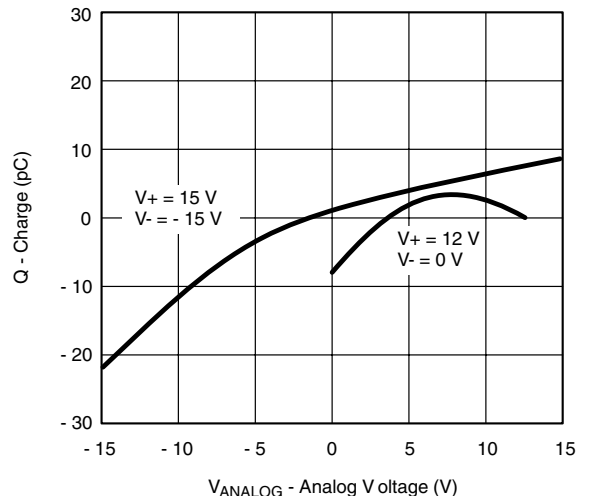
**$r_{DS(on)}$  vs.  $V_D$  and Single Power Supply Voltages**



**Leakage Currents vs. Analog Voltage**

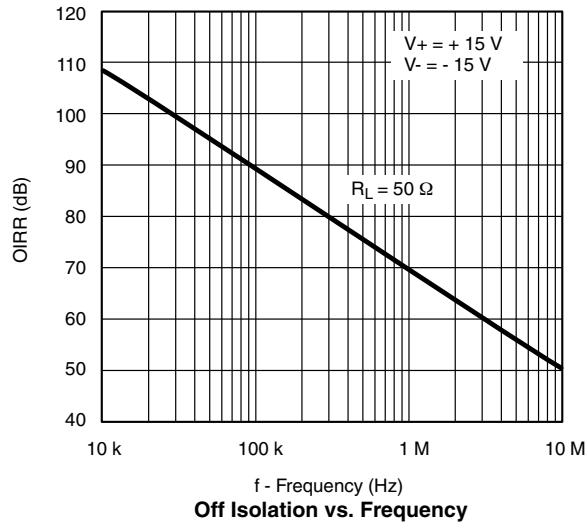


**Leakage Current vs. Temperature**



**$Q_S, Q_D$  - Charge Injection vs. Analog Voltage**

**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



**SCHEMATIC DIAGRAM** Typical Channel

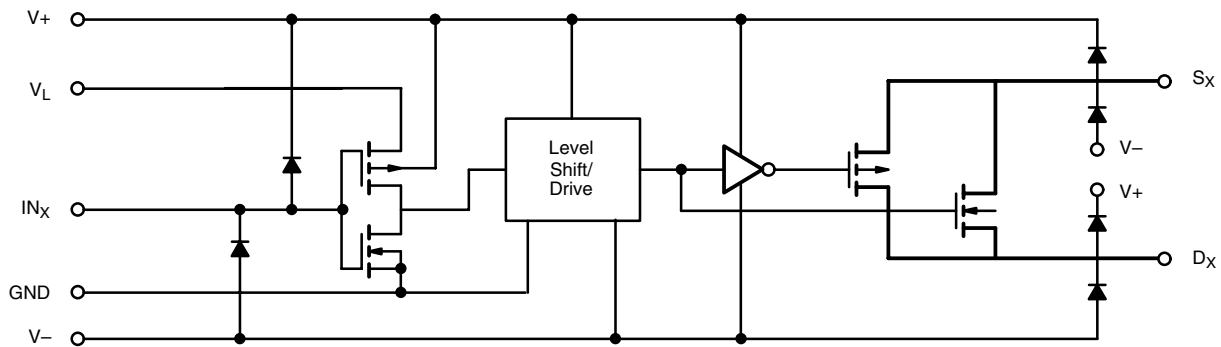


Figure 1.

**TEST CIRCUITS**

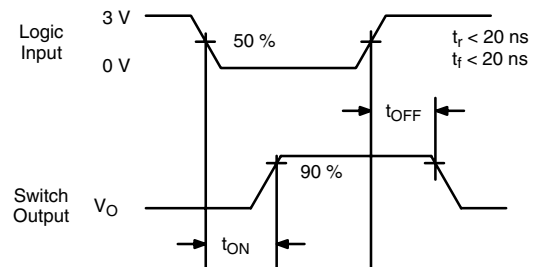
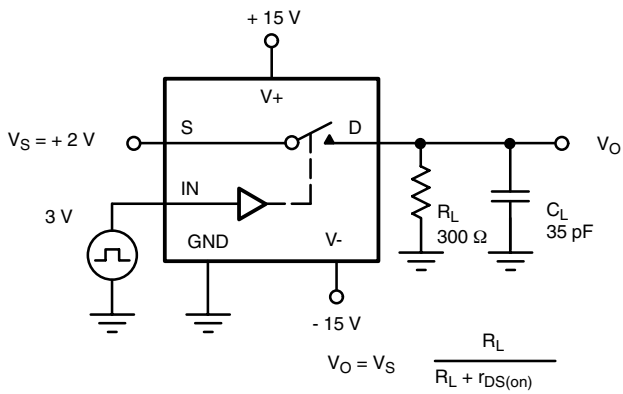
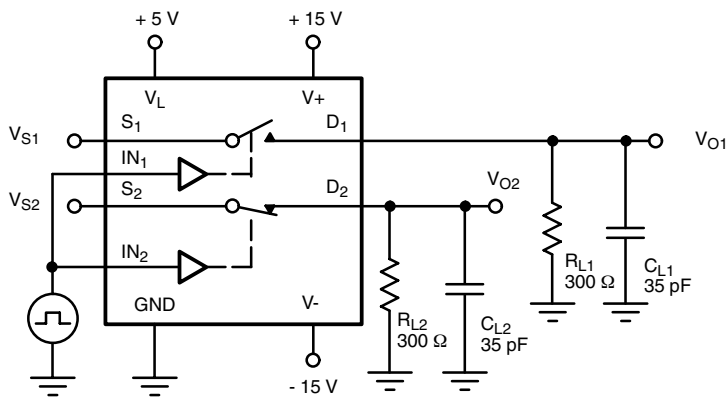


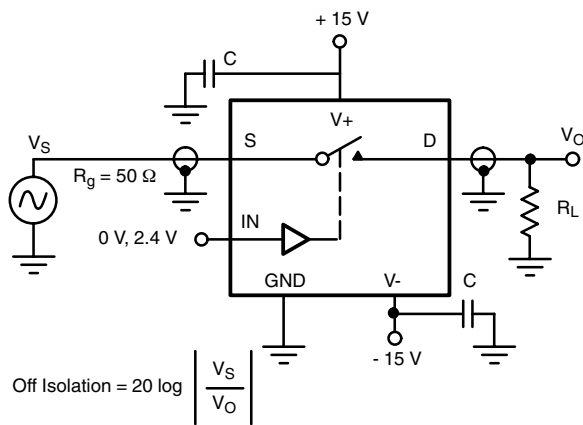
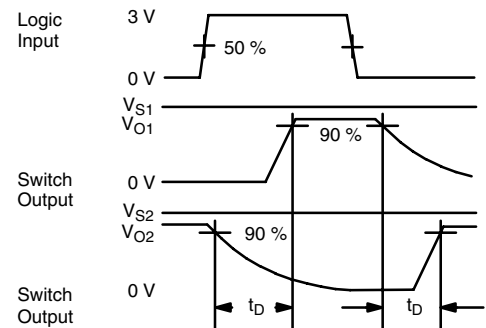
Figure 2. Switching Time

TEST CIRCUITS



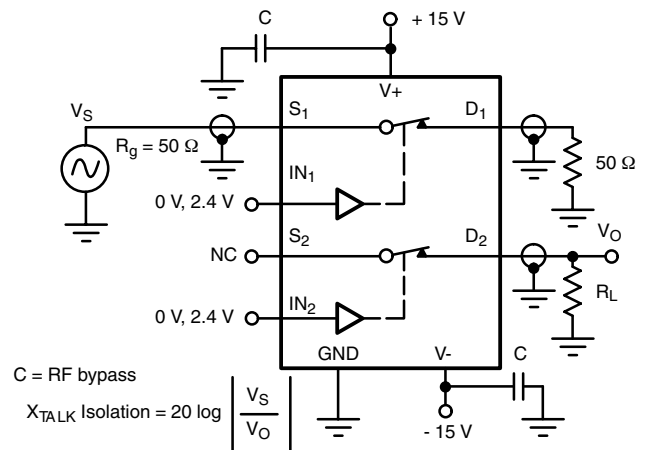
$C_L$  (includes fixture and stray capacitance)

Figure 3. Break-Before-Make



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

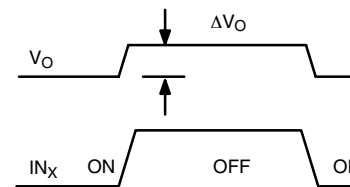
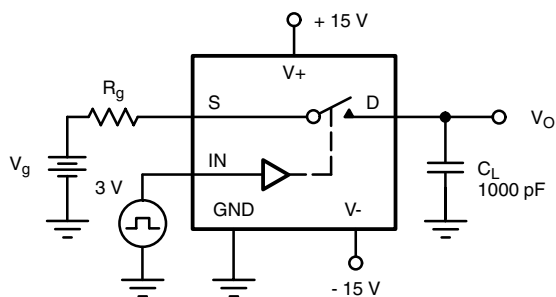
Figure 4. Off Isolation



C = RF bypass

$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

Figure 5. Channel-to-Channel Crosstalk



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

Figure 6. Charge Injection

**APPLICATIONS**

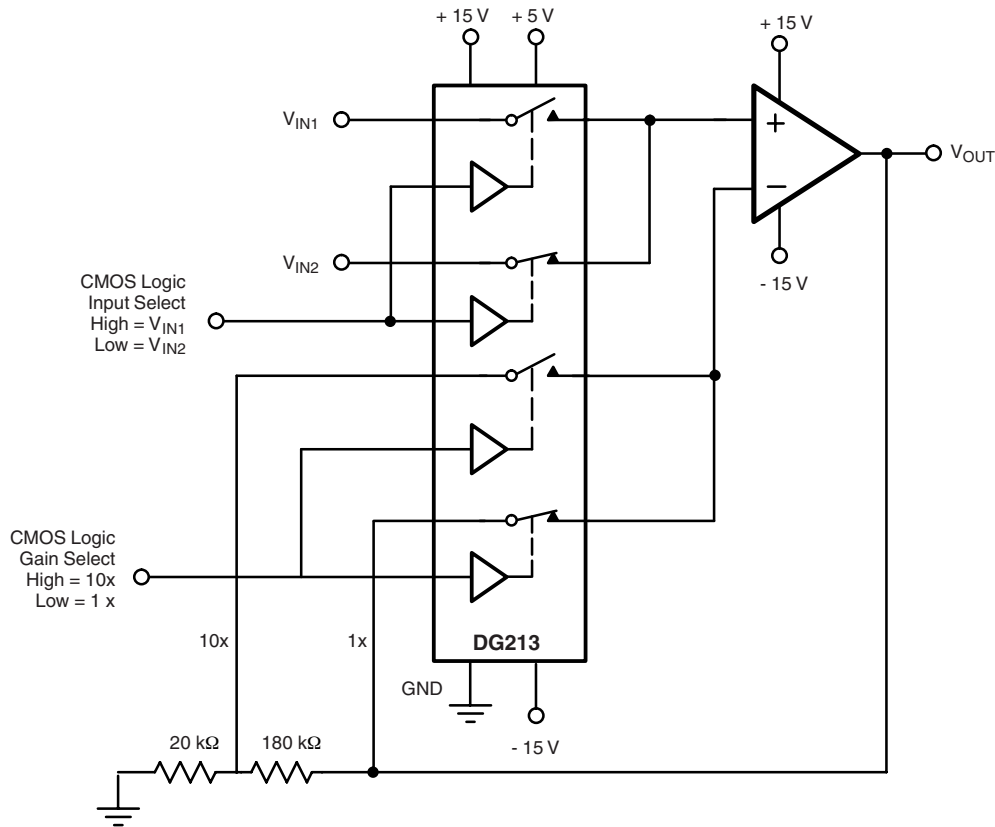


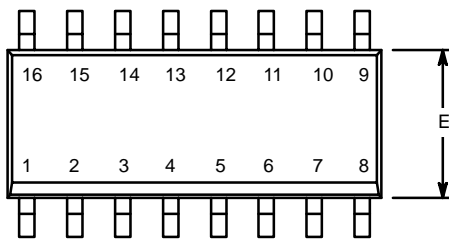
Figure 7. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70662>.



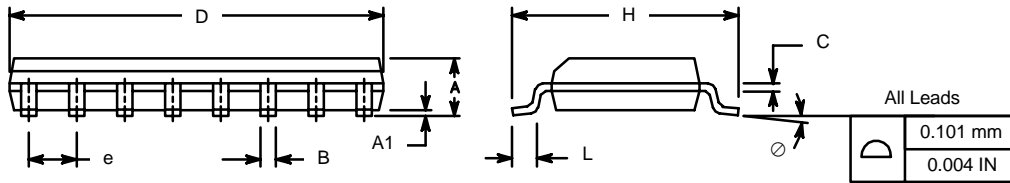


**SOIC (NARROW): 16-LEAD**  
JEDEC Part Number: MS-012



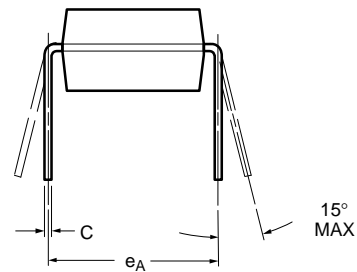
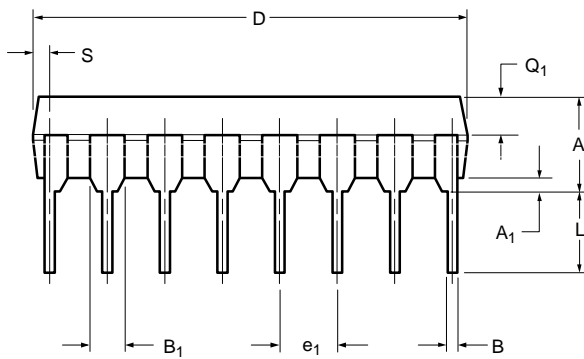
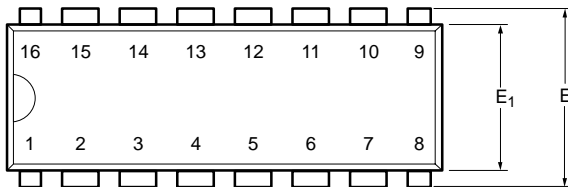
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5300





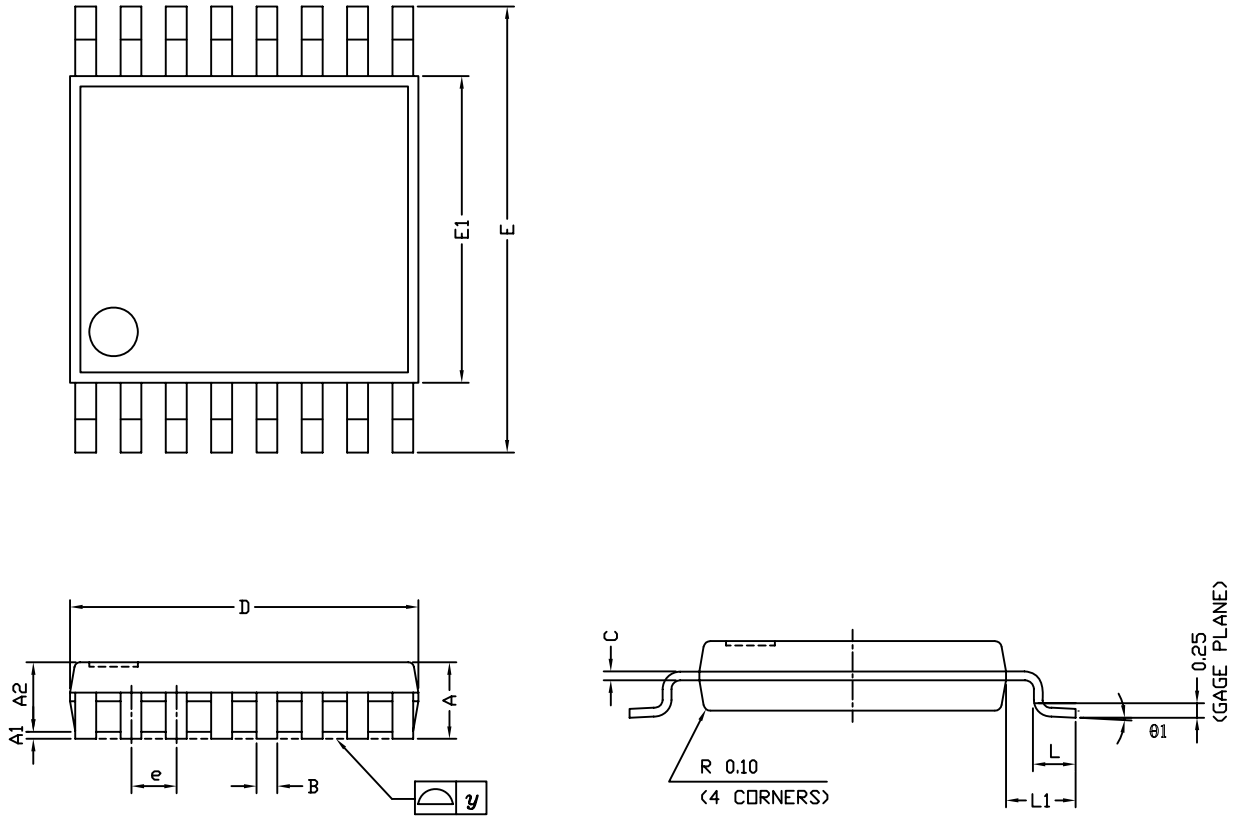
**PDIP: 16-LEAD**



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	18.93	21.33	0.745	0.840
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01  
DWG: 5482

## TSSOP: 16-LEAD

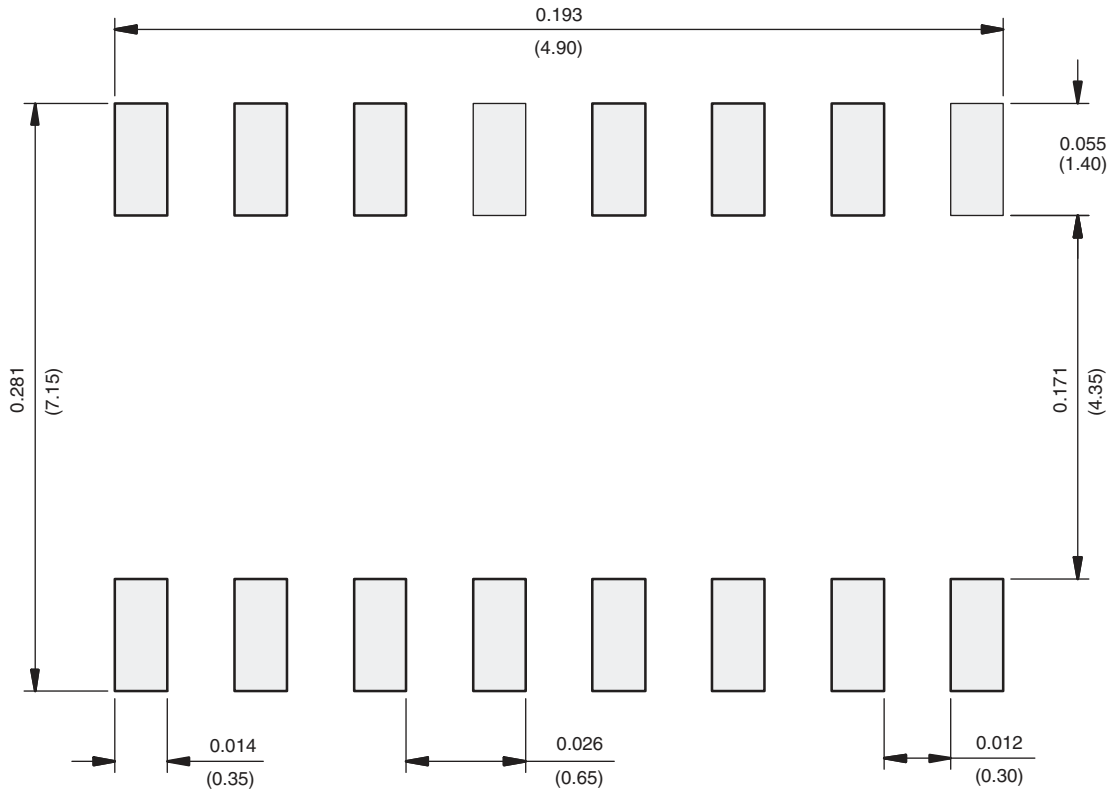


Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°

ECN: S-61920-Rev. D, 23-Oct-06  
 DWG: 5624

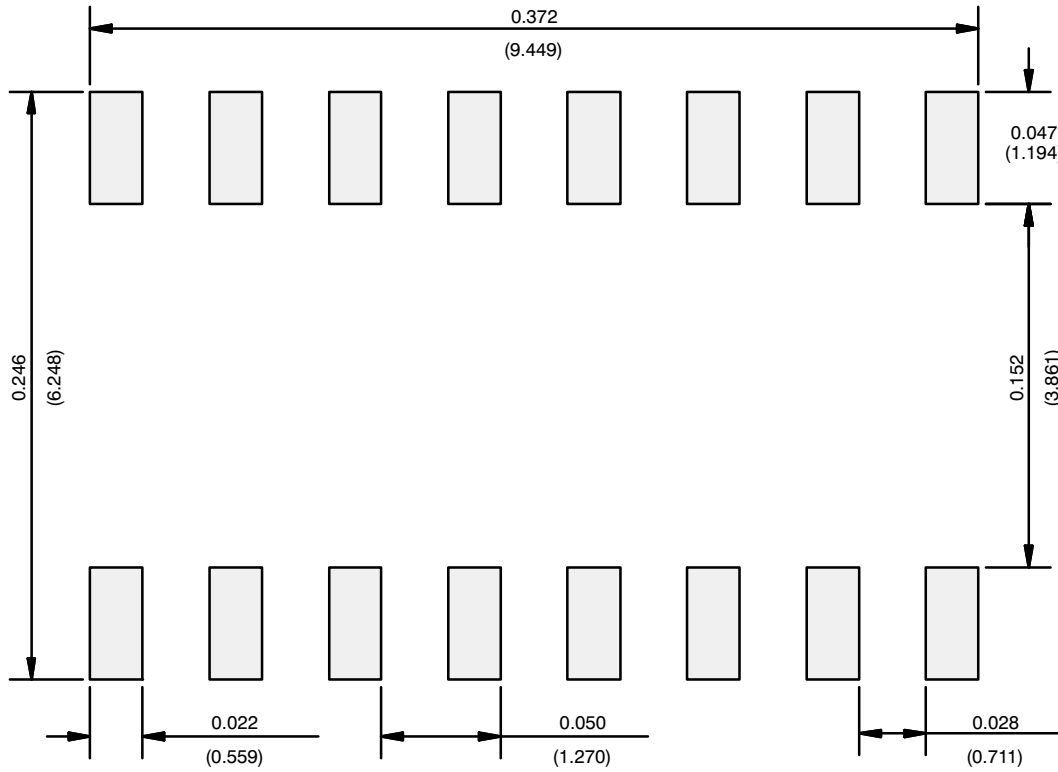


**RECOMMENDED MINIMUM PAD FOR TSSOP-16**



Recommended Minimum Pads  
Dimensions in inches (mm)

## RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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