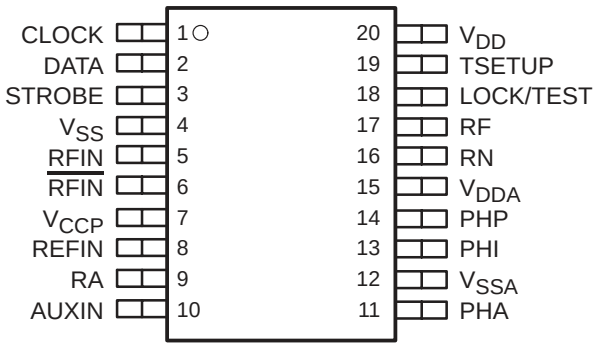
- **1.2-GHz Operation**
- **Two Operating Modes:**
  - **Philips SA7025 Emulation Mode Terminal-for-Terminal and Programming Compatible**
  - **Extended Performance Mode (EPM)**
- **Dual RF-IF Phase-Locked Loops**
- **Fractional-N or Integer-N Operation**
- **Programmable EPM Fractional Modulus of 1–16**
- **Normal, Speed-Up, and Fractional Compensation Charge Pumps**
- **Low-Power Consumption**

PW PACKAGE
(TOP VIEW)



description

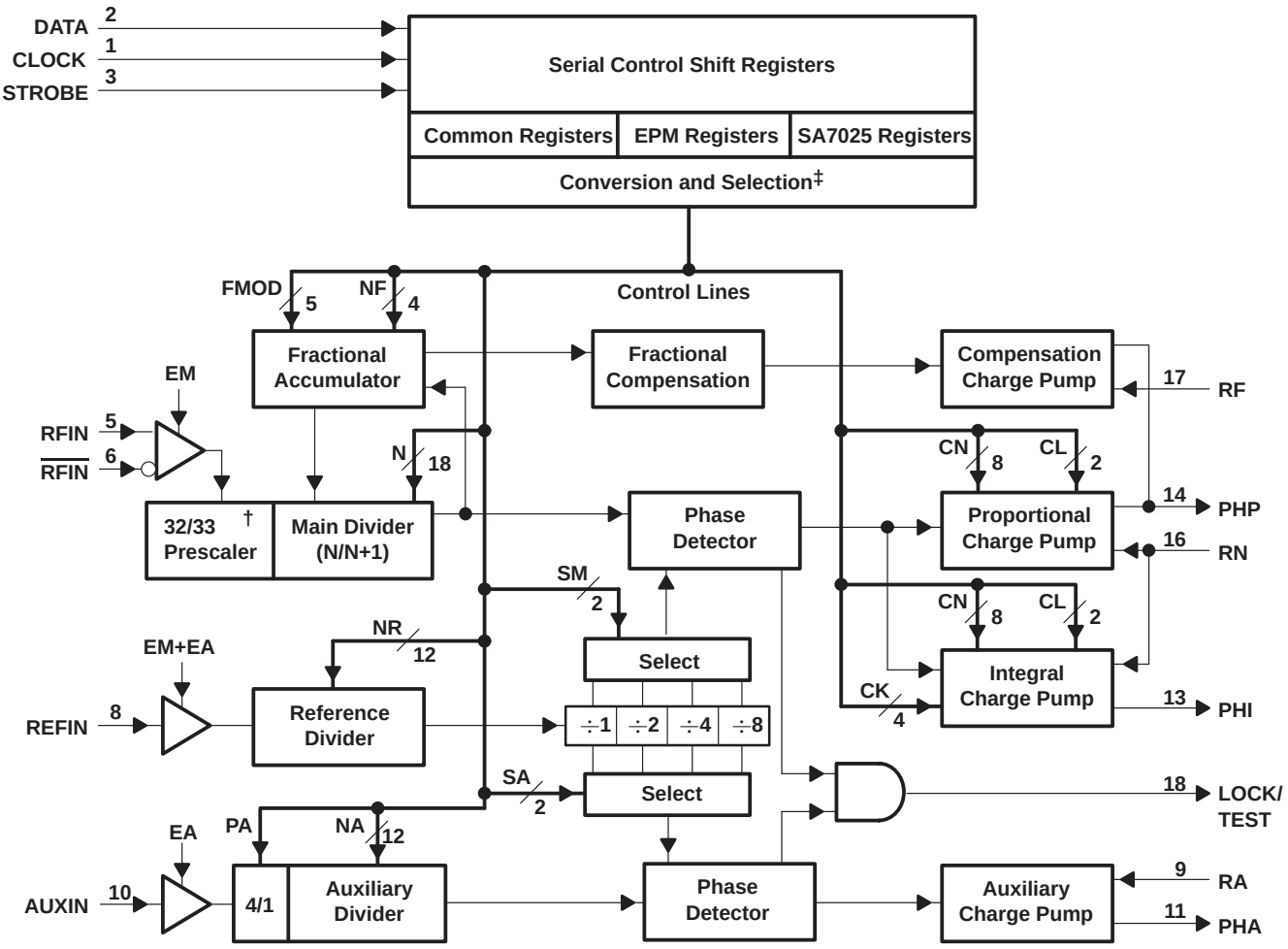
The TRF2056 device is a low-voltage, low-power consumption 1.2-GHz fractional-N/integer-N frequency synthesizer component for wireless applications. Fractional-N division and an integral speed-up charge pump achieve rapid channel switching. Two operating modes are available: 1) SA7025 emulation mode in which the device emulates the Philips SA7025 fractional-N synthesizer and 2) extended performance mode (EPM), which provides additional features, including fractional accumulator modulos from 1 to 16 (compared to only 5 or 8 for the SA7025 synthesizer).

The TRF2056 device provides external loop filters and all functions necessary for voltage-controlled oscillator (VCO) control in a dual phase-locked loop (PLL) frequency synthesizer system. A main channel is provided for radio frequency (RF) channels and an auxiliary channel for intermediate frequency (IF) channels. The current-output charge pumps directly drive passive resistance-capacitance (RC) filter networks to generate VCO control voltages. Rapid main-channel frequency switching is achieved with a charge pump arrangement that increases the current drive and alters the loop-filter frequency response during the speed-up mode portion of the switching interval.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram†



† Terminals 4, 7, 12, 15, and 20 are for supply voltage. Terminal 19 is for testing. These terminals are not shown.
‡ Conversion and selection block provides emulation of SA7025 64/65/72 triple-modulus prescaler operation using the TRF2056 32/33 dual-modulus prescaler.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AUXIN	10	I	Auxiliary channel RF input
CLOCK	1	I	Serial interface clock signal
DATA	2	I	Serial interface data signal
LOCK/ TEST	18	O	Lock detector/test mode output
PHA	11	O	Auxiliary charge pump output
PHI	13	O	Integral charge pump output
PHP	14	O	Proportional charge pump output
RA	9	I	Resistor to V_{SSA} sets auxiliary charge pump reference current
REFIN	8	I	Reference frequency input signal
RF	17	I	Resistor to V_{SSA} sets compensation charge pump reference current
RFIN	5	I	Prescaler positive RF input
$\overline{\text{RFIN}}$	6	I	Prescaler negative RF input
RN	16	I	Resistor to V_{SSA} sets proportional and integral charge pump reference current
STROBE	3	I	Serial interface strobe signal
TSETUP	19	I	Test setup for terminal 18. For lock detect output, terminal 19 connects to V_{CC} through a pullup resistor; for test mode output, terminal 19 terminates to ground.
V_{CCP}	7		Prescaler positive supply voltage
V_{DD}	20		Digital supply voltage
V_{DDA}	15		Analog supply voltage
V_{SS}	4		Digital ground
V_{SSA}	12		Analog ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCP}, V_{DD}, V_{DDA} (see Note 1) . . . . . –0.6 V to 5.6 V
Input voltage range, logic signals . . . . . –0.6 V to 5.6 V
Operating ambient temperature range, T_A . . . . . –55°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to V_{SSA}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DDA}	3.3		3.9	V
Supply voltage, V_{CCP}, V_{DD}	2.9	3.3	3.9	V
Operating free-air temperature, T_A	–40	25	85	°C

dc electrical characteristics $V_{DD} = V_{DDA} = V_{CCP} = 3.3$ V, T_A=25°C internal registers: CN = 128, CL = 1, CK = 3, PA = 1 external components: RN = 18 kΩ, RF = 20 kΩ, RA = 100 kΩ (unless otherwise noted)

supply current: $I = I_{DD} + I_{CCP} + I_{DDA}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0 (see Note 2)			200	µA
I_{MAIN}	Operational supply currents	EM = 1, EA = 0		7.0		mA
I_{AUX}	Operational supply currents	EM = 0, EA = 1		1.5		mA
I_{TOTAL}	Operational supply currents	EM = EA = 1		7.5		mA

NOTE 2: $V_{RN} = V_{RA} = V_{RF} = V_{DDA}$

digital interface

PARAMETER			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	DATA, CLOCK, STROBE	0.7 V_{DD}		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 V_{DD}	V
I_{IH}	High-level input current	DATA, CLOCK, STROBE			10	µA
I_{IL}	Low-level input current				10	µA

charge pump currents (see Figure 1)

auxiliary charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHA} \rvert$	Output current PHA	$V_{PHA} = 0.5\ V_{DDA}$	200	250	300	µA
$\frac{\Delta I_{PHA}}{\lvert I_{PHA} \rvert}$	Relative output current variation PHA (see Figure 1)			2%	10%	
ΔI_{PHA}	Output current matching PHA (see Figure 1)	$V_{PHA} = 0.5\ V_{DDA}$			±50	µA

proportional charge pump, normal mode, $V_{RF} = V_{DDA}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHP-NM} \rvert$	Output current PHP	$V_{PHP} = 0.5\ V_{DDA}$	400	500	600	µA
$\frac{\Delta I_{PHP-NM}}{\lvert I_{PHP-NM} \rvert}$	Relative output current variation PHP (see Figure 1)			2%	10%	
ΔI_{PHP-NM}	Output current matching PHP (see Figure 1)	$V_{PHP} = 0.5\ V_{DDA}$			±50	µA

charge pump currents (see Figure 1) (continued)

proportional charge pump, speed-up mode, $V_{RF} = V_{DDA}$ (see *speed-up mode* operation)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHP-SM} \rvert$	Output current PHP	$V_{PHP} = 0.5\ V_{DDA}$	2	2.5	3	mA
$\frac{\Delta I_{PHP-SM}}{\lvert I_{PHP-SM} \rvert}$	Relative output current variation PHP (see Figure 1)			2%	10%	
ΔI_{PHP-SM}	Output current matching PHP (see Figure 1)	$V_{PHP} = 0.5\ V_{DDA}$			±300	µA

integral charge pump, speed-up mode, $V_{RF} = V_{DDA}$ (see *speed-up mode* operation)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHI-SM} \rvert$	Output current PHI	$V_{PHI} = 0.5\ V_{DDA}$	4.8	6	7.2	mA
$\frac{\Delta I_{PHI-SM}}{\lvert I_{PHI-SM} \rvert}$	Relative output current variation PHI (see Figure 1)			2%	8%	
ΔI_{PHI-SM}	Output current matching PHI (see Figure 1)	$V_{PHI} = 0.5\ V_{DDA}$			±600	µA

fractional compensation proportional charge pump, normal mode, $V_{RN} = V_{DDA}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHP-F-NM} \rvert$	Output current PHP vs fractional numerator (see Note 3)	$V_{PHP} = 0.5\ V_{DDA}$, FNUM = 1		1.25		µA

NOTE: 3. Fractional compensation current is proportional to the numerator content of the fractional accumulator (FNUM).

charge pump leakage currents, $V_{RN} = V_{RA} = V_{RF} = V_{DDA}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHP}	Output current PHP	$V_{PHP} = 0.5\ V_{DDA}$		±10		nA
I_{PHI}	Output current PHI	$V_{PHI} = 0.5\ V_{DDA}$		±10		
I_{PHA}	Output current PHA	$V_{PHA} = 0.5\ V_{DDA}$		±10		

ac electrical characteristics, $V_{DD} = V_{CCP} = 2.9$ V, $V_{DDA} = 3.9$ V, $T_A = 25°C$ (unless otherwise noted)

main divider

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{RFIN}	RF input frequency				1.2	GHz
V_{ID_RFIN}	Differential RF input power	50-Ω single-ended characteristic impedance; ac-coupled	–20		0	dBm

ac electrical characteristics, V_{DD} = V_{CCP} = 2.9 V, V_{DDA} = 3.9 V, T_A = 25°C (unless otherwise noted) (continued)

auxiliary divider

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{AUXIN}	Auxiliary input frequency (ac-coupled)	PA = 1: V_{I_AUXIN} = 350 mVpp			50	MHz
Z_{AUXIN}	Auxiliary input impedance		5	100		kΩ
				3		pF

reference divider

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{REFIN}	Reference input frequency			16.8		MHz
V_{I_REFIN}	Reference input voltage	ac-coupled, 16.8 MHz	0.350	1		V_{PP}
Z_{REFIN}	Reference input impedance			100		kΩ
				3		pF

timing requirements, serial data interface (see Figure 2)

		MIN	MAX	UNIT
f_{CLOCK}	Clock frequency		10	MHz
t_{w_CLKHI}	Clock high time pulse width, CLOCK high	30		ns
t_{w_CLKLO}	Clock low time pulse width, CLOCK low	30		ns
t_{su_Data}	Setup time, data valid before CLOCK↑	30		ns
t_{h_Data}	Hold time, data valid after CLOCK↑	30		ns
t_{h_Strobe}	Hold time, STROBE high before CLOCK↑	30		ns
t_{su_Strobe}	Setup time, STROBE low after CLOCK↑	30		ns
t_{w_STRBHI}	STROBE high time pulse width, STROBE high	50		ns

PARAMETER MEASUREMENT INFORMATION

charge-pump current output definitions

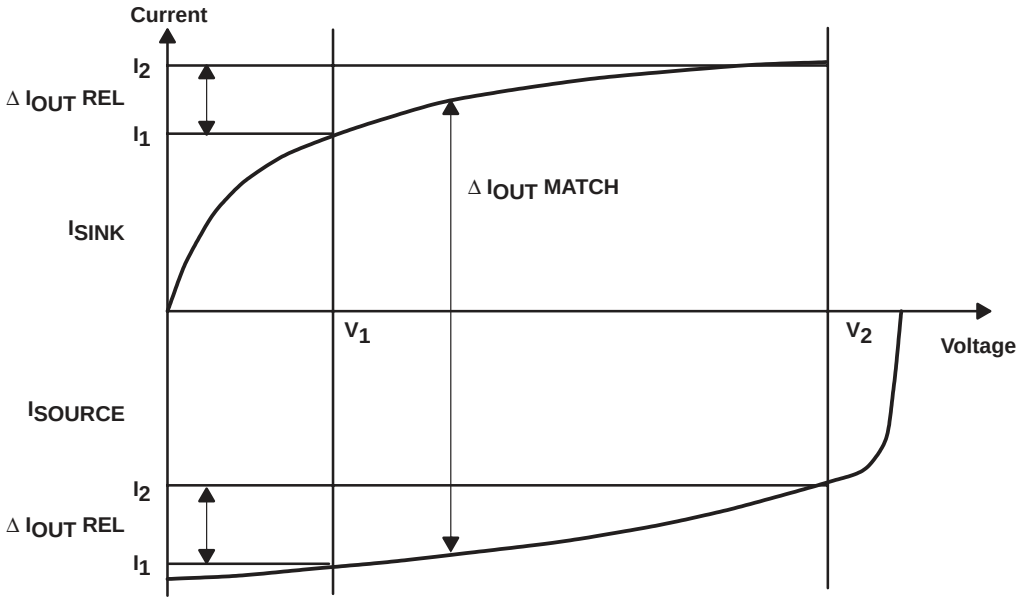


Figure 1. Charge-Pump Output Current Definitions

The relative output current variation is defined as the percent difference between charge-pump current output at two charge-pump output voltages and the mean charge-pump current output (see Figure 1):

$$\frac{\Delta I_{OUT\ REL}}{\left|I_{OUT\ MEAN}\right|} = 2 \times \frac{\left(I_2 - I_1\right)}{\left|\left(I_2 + I_1\right)\right|} \times 100\%$$

where

$V_1 = 0.7\ V,\ V_2 = V_{DDA} - 0.8\ V.$

Output current matching is defined as the difference between charge-pump sinking current output and charge-pump sourcing current output at a given charge-pump output (see Figure 1).

$$\Delta I_{OUT\ MATCH} = I_{SINK} - I_{SOURCE}$$

where

$V_1 \le \text{Voltage} \le V_2.$

serial-data interface timing

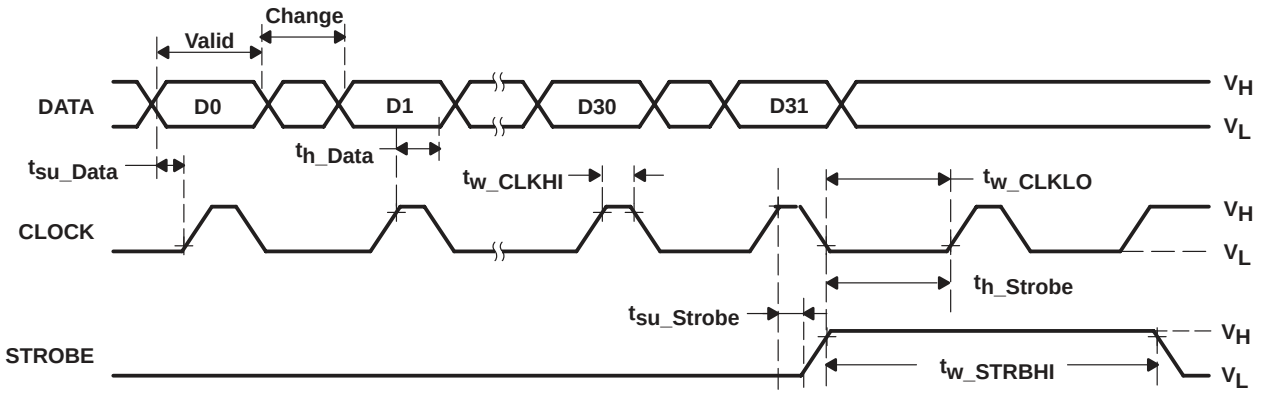


Figure 2. Serial-Data Interface Timing

PRINCIPLES OF OPERATION

serial programming input

The TRF2056 internal registers are programmed using a three-wire (CLOCK, DATA, STROBE) serial interface. The serial data is structured into 24-bit standard-length or 32-bit long-length words where one or four bits are dedicated address bits. The flag LONG in the D-Word determines whether the A0 (LONG = 0) or A1 (LONG = 1) format is applicable. Figure 3 and Figure 4 show the format of the serial data for two modes of TRF2056 operation: SA7025 emulation and EPM, respectively. The least significant bits (LSB) of the C-Word determines the operational mode of the TRF2056 device: 00 = SA7025 emulation, 01 = EPM.

In the SA7025 emulation mode, the TRF2056 device emulates the Philips SA7025 synthesizer with respect to serial programming. Microcontroller software written for the SA7025 synthesizer works transparently when the TRF2056 device is operated in the SA7025 emulation mode.

Figure 2 shows the timing diagram of the serial input. When STROBE is low, the signal on DATA is clocked into a shift register on the positive edges of CLOCK. When STROBE is high, depending on 1 or 4 address bit(s), the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, four words must be sent: D, C, B, and A. The E-Word is for testing purposes only.

The A-Word contains new data for the main divider. The A-Word is loaded only when a main divider synchronization signal is also active. This is done to avoid phase jumps while reprogramming the main divider. The synchronization signal is generated by the main divider.

When the TRF2056 device is operated in any mode, programming the A-Word sets the main charge pumps, which are located on outputs PHP and PHI, to speed-up mode, as long as STROBE is high.

NOTE:
The C-Word must be sent during the first programming cycle after powerup in order to set the mode of operation (SA7025 or EPM).

PRINCIPLES OF OPERATION

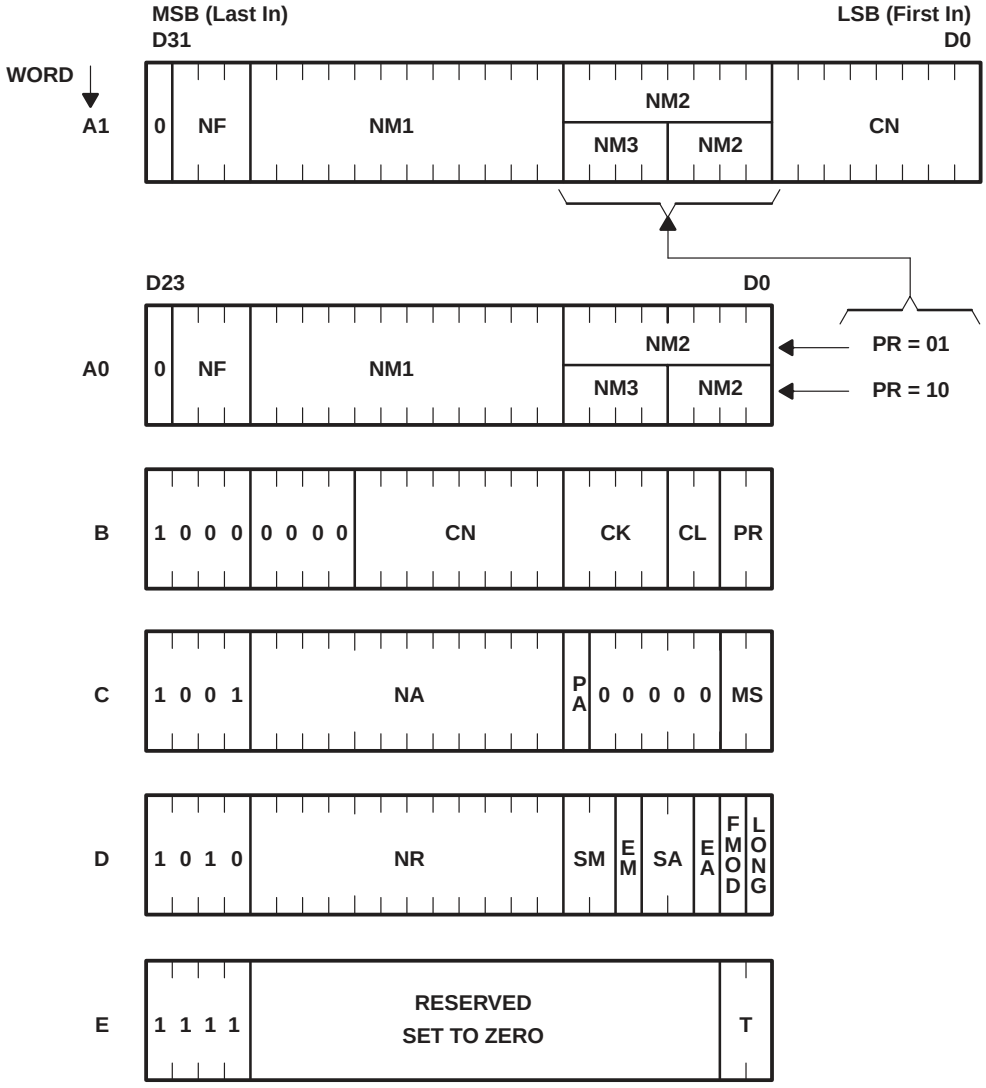


Figure 3. Serial Word Format for SA7025 Emulation Mode

PRINCIPLES OF OPERATION

Table 1. SA7025 Emulation Serial-Word-Format Function Listing

SYMBOL	BITS	FUNCTION
CK	4	Binary acceleration factor for integral charge pump current
CL	2	Binary acceleration factor for proportional charge pump current
CN	8	Binary current-setting factor for main charge pumps
EA	1	Auxiliary divider enable flag: 0 = Disabled 1 = Enabled
EM	1	Main divider enable flag: 0 = Disabled 1 = Enabled
FMOD	1	Fractional-N modulus selection: 0 = Modulo 5 1 = Modulo 8
LONG	1	A word format selection: 0 = 24-bit A0 format 1 = 32-bit A1 format
MS	2	Mode select 00 = SA7025 emulation mode
NA	12	Auxiliary divider ratio
NF	3	Fractional-N increment
NM1	12	Number of main divider cycles when prescaler modulus = 64
NM2	8 if PR = 01 4 if PR = 10	Number of main divider cycles when prescaler modulus = 65
NM3	4 if PR = 10	Number of main divider cycles when prescaler modulus = 72
NR	12	Reference divider ratio
PA	1	Auxiliary prescaler select: 0 = Divide by 4 1 = Divide by 1
PR	2	Prescaler type: 01 = Modulo 2 prescaler (64/65) 10 = Modulo 3 prescaler (64/65/72)
SA	2	Reference select for auxiliary phase detector
SM	2	Reference select for main phase detector
T	2	Test mode connection of internal signals to the LOCK terminal: 00 = ACCU overflow 01 = Auxiliary divider 10 = Main divider 11 = Reference divider

PRINCIPLES OF OPERATION

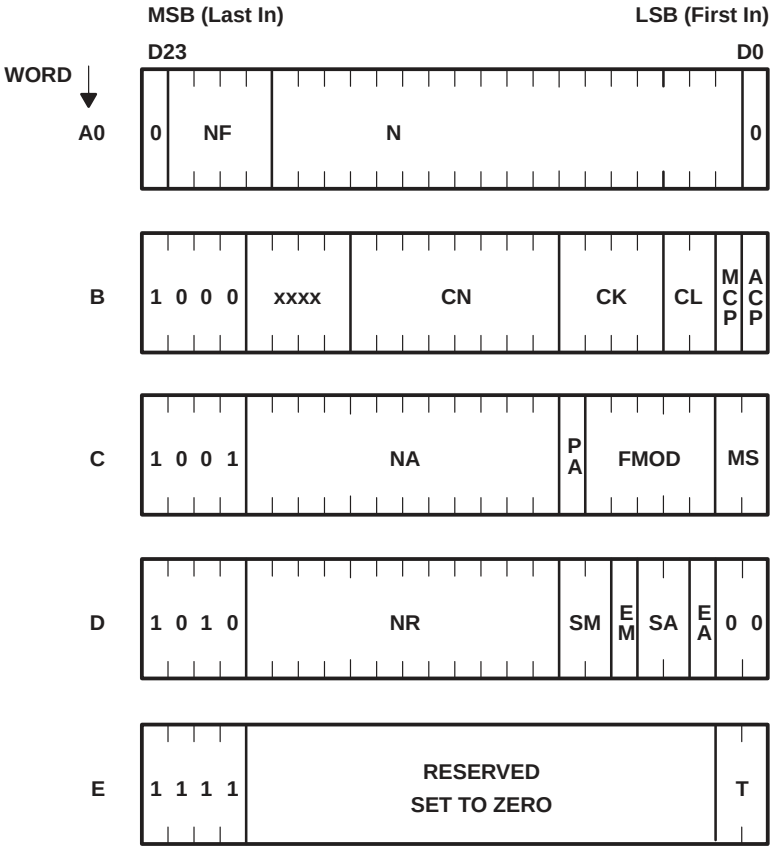


Figure 4. Serial Word Format for Extended Performance Mode

PRINCIPLES OF OPERATION

Table 2. Extended Performance Mode Function

SYMBOL	BITS	SAME AS SA7025 MODE	FUNCTION
ACP	1	No	Auxiliary charge polarity: 0 = Positive 1 = Negative
CK	4	Yes	Binary acceleration factor for integral charge pump current
CL	2	Yes	Binary acceleration factor for proportional charge pump current
CN	8	Yes	Binary current setting factor for main charge pumps
EA	1		Auxiliary divider enable flag: 0 = Disabled 1 = Enabled
EM	1	Yes	Main divider enable flag: 0 = Disabled 1 = Enabled
FMOD	5	No	Fraction accumulator modulus
MCP	1	No	Main charge pump polarity: 0 = Positive 1 = Negative
MS	2	No	Mode select 01 = Extended performance mode
N	18	No	Overall main divider integer division ratio (NM)
NA	12	Yes	Auxiliary divider ratio
NF	4	No	Fractional-N increment
NR	12	Yes	Reference divider ratio
PA	1	Yes	Auxiliary prescaler select: 0 = Divide by 4 1 = Divide by 1
SA	2	Yes	Reference select for auxiliary phase detector
SM	2	Yes	Reference select for main phase detector
T	2	Yes	Test mode connection of internal signals to the LOCK terminal: 00 = ACCU overflow 01 = Auxiliary divider 10 = Main divider 11 = Reference divider

PRINCIPLES OF OPERATION

main divider-general (see Figure 5)

The differential RFIN inputs are amplified to internal ECL logic levels and provide excellent sensitivity (better than –20 dBm at 1 GHz), making the prescaler ideally suited for direct interface with a VCO. The internal dual-modulus (32/33) prescaler and counter sections divide the VCO frequency down to the reference phase detector frequency. The prescaler division ratio (÷32 or ÷33) is controlled by a feedback signal that is a function of the 18-bit N-field counters. The N-field counter section has 2 separate counters: a 5-bit A-Counter and a 13-bit B-Counter. The prescaler divides by 33 until the A-Counter reaches terminal count and then divides by 32 until the B-Counter reaches terminal count, whereupon both counters reset and the cycle repeats. The following equation relates the total N division as a function of the 32/33 prescaler:

$N_{Total} = 32 (B – A) + 33 (A)$

where $0 \le A \le 31$, and $31 \le B \le 8191$.

It is not necessary to determine the values of A and B in the equation above; simply program the N field with the total division ratio desired (fractional effects are ignored).

The N-division ratio has a range of $992 \le N_{Total} \le 262143$.

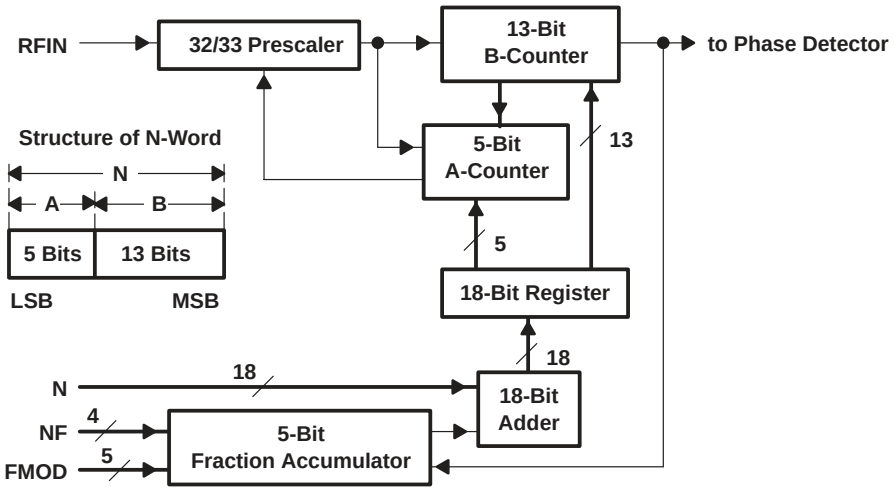


Figure 5. Main Divider Organization

main divider – SA7025 emulation

The internal triple modulus prescaler configuration of the SA7025 synthesizer provides for prescaler division ratios of 64/65/72. The TRF2056 device has internal conversion logic that allows the TRF2056 device to emulate the SA7025 main divider operation. When operated in the SA7025 emulation mode, the TRF2056 device is programmed using the SA7025 serial interface format shown in Figure 3. The TRF2056 internal conversion is transparent and need not be considered under normal use, thereby allowing use of existing SA7025 programming codes without change.

The following equations relate the total N-division as a function of the emulated 64/65 dual-modulus and 64/65/72 triple-modulus prescalers:

$N_{Total} = 64 (NM1 + 2) + 65 (NM2)$

where PR = 01 and

$N_{Total} = 64 (NM1 + 2) + 65 (NM2) + 72 (NM3 + 1)$

where PR = 10.

PRINCIPLES OF OPERATION

For contiguous channels, the following rules must be observed:

For PR = 01: 61 ≤ NM1 ≤ 4095 and 0 ≤ NM2 ≤ 63, which yields minimum and maximum divide ratios of 4032 and 266303, respectively.

For PR = 10: 14 ≤ NM1 ≤ 4095 and 0 ≤ NM2 ≤ 15, and 0 ≤ NM3 ≤ 15, which yields minimum and maximum divide ratios of 1096 and 264335, respectively.

main divider – synchronization

The A-Word is loaded only when a main divider synchronization signal is active. This prevents phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider, and it is active while the main divider is counting down from the programmed value. When the main divider reaches its terminal count, a main divider output pulse is sent to the main phase detector. Also at this time, the loading of the A-Word is disabled. Therefore, to correctly load the new A-Word, STROBE must be active high for at least a minimum number of VCO input cycles at RFIN.

main divider – fractional accumulator

The TRF2056 main synthesizer loop can operate as a traditional integer-N feedback PLL or as a fractional-N feedback PLL. The integer-N feedback loop divides the VCO frequency by integer values of N, which results in phase detector reference comparisons at the desired channel spacing. A fractional-N feedback loop divides the VCO frequency by an integer term plus a fractional term, which results in phase detector reference comparisons at integer multiples of the desired system channel spacing.

Integer-N division: VCO frequency $\div$ N = phase detector reference frequency
= channel spacing

Fractional-N division: VCO frequency $\div$ (N + NF/FMOD) = phase detector reference frequency
= FMOD $\times$ channel spacing

where 0 ≤ NF < FMOD and 1 ≤ FMOD ≤ 16.

Because the main counter and prescaler sections cannot divide by a fraction of an integer, the fractional-N division is accomplished by averaging main divider cycles by N and N+1. A fractional accumulator is programmed with values of NF and FMOD to control the main counter and prescaler sections to divide by N or N+1.

The fractional accumulator operates modulo FMOD and is incremented by NF at the completion of each main divider cycle. When the fractional accumulator overflows, division by N+1 occurs. Otherwise, the main counters and prescaler divide by N; division by N+1 is transparent to the user. Table 3 shows the contents of the fractional accumulator and the resulting N or N+1 division for two fractional division ratios.

PRINCIPLES OF OPERATION

Table 3. Fractional Accumulator Operation

NF = 3, FMOD = 8	
ACCUMULATOR NUMERATOR	STATE
3	÷ N
6	÷ N
1	÷ N + 1, overflow
4	÷ N
7	÷ N
2	÷ N + 1, overflow
5	÷ N
0	÷ N + 1, overflow

NF = 6, FMOD = 8	
ACCUMULATOR NUMERATOR	STATE
6	÷ N
4	÷ N + 1, overflow
2	÷ N + 1, overflow
0	÷ N + 1, overflow
6	÷ N
4	÷ N + 1, overflow
2	÷ N + 1, overflow
0	÷ N + 1, overflow

For example, suppose that a typical AMPS channel of 953.25 MHz is desired. Because AMPS channel spacing is 30 kHz, for fractional-N operation the main phase detector reference frequency must be a multiple of 30 kHz; 240 kHz is typical. A value of FMOD = 8 is selected because 240 kHz / 30 kHz = 8. Dividing the channel frequency by the reference frequency results in 953.13 MHz ÷ 240 kHz = 3971.375 = 3971 3/8. This example is shown in Table 3 where NF = 3 and FMOD = 8. The table shows that over the period of a complete fractional accumulator cycle, the fractional accumulator overflows 3 times for every 8 main divider cycles. Figure 6 illustrates the division by N or N+1 for this 3/8 fractional channel example.

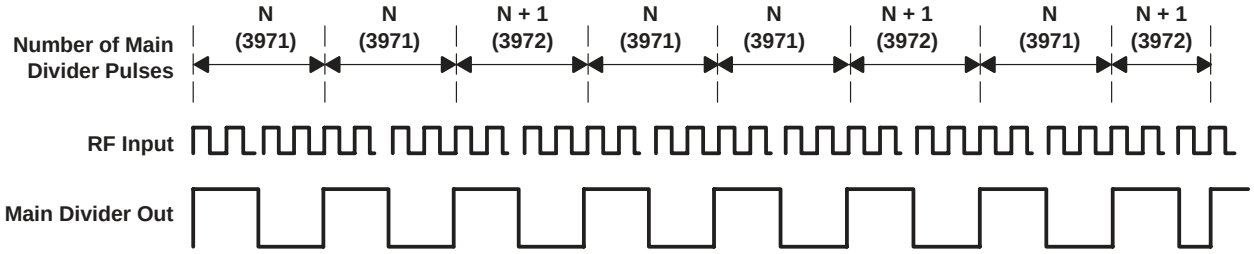


Figure 6. 3/8 Fractional Channel Main Divider Operation

The mean division over the complete fractional accumulator cycle as shown in Figure 6 is:

$$N_{MEAN} = \frac{3971 + 3971 + 3972 + 3971 + 3971 + 3972 + 3971 + 3972}{8} = 3971.375$$
$$= 3971 + 3/8$$

Therefore, fractional channels are available every 30 kHz or 240 kHz $\frac{1}{FMOD} = \frac{240\ kHz}{8}$.

main divider – integer channels

In the case where NF = 0, only division by N occurs, and the fractional accumulator is essentially in a steady state with a numerator of 0. It never increments or overflows. A channel that requires NF = 0 is a pure integer channel because the fractional term of $\frac{NF}{FMOD}$ is zero.

PRINCIPLES OF OPERATION

main divider – fractional-N sidebands and compensation

Programming a fractional-N channel means the main divider and prescaler divide by N or N + 1 as dictated by the operation of the fractional accumulator. Because the main divider operation is integer in nature and the desired VCO frequency is not, the output of the main phase detector is modulated with a resultant fractional-N phase ripple that produces sideband energy if left uncompensated. This phase ripple is proportional and synchronized to the contents of the fractional accumulator that is used to control fractional-N sideband compensation. Only channels that require a nonzero value of NF have the fractional-N sideband energy. The fractional-N sidebands, which appear at offset frequencies from the VCO fundamental tone, are multiples of NF/FMOD. Figure 7 shows the fractional-N phase detector ripple for a 3/8 fractional channel.

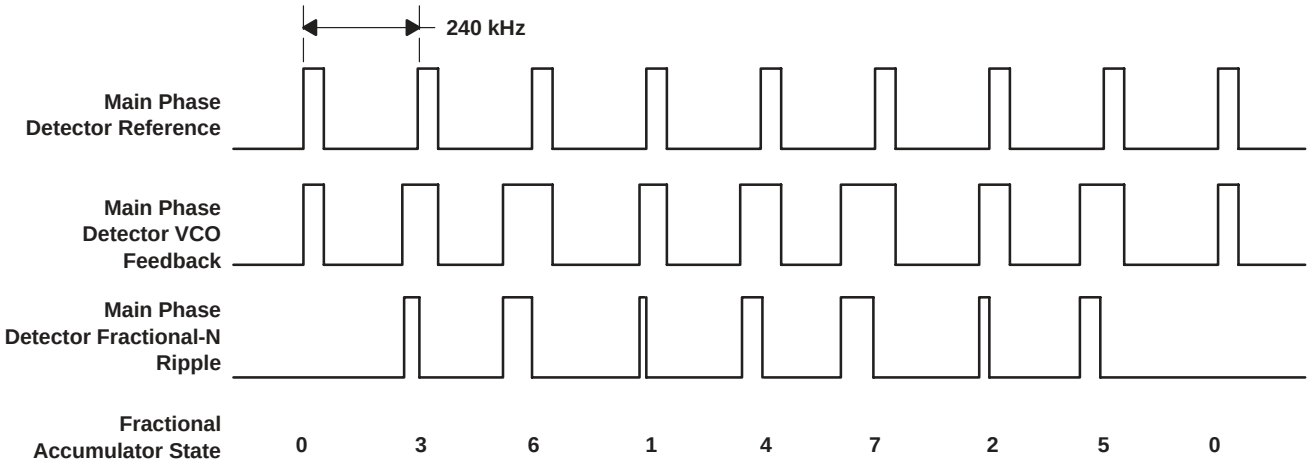


Figure 7. Fractional-N Phase Detector Ripple for 3/8 Channel

The TRF2056 device has internal circuitry that provides a means to compensate for the phase detector fractional-N phase ripple, thereby significantly reducing the magnitude of the fractional-N sidebands. Because the current waveform output of the main PLL proportional charge pumps is modulated with the phase detector fractional-N phase ripple, a fractional-N compensation charge-pump output is summed with the main PLL proportional charge pump.

Figure 8 shows the fractional-N ripple magnitude on the main PHP charge-pump output. The magnitude is essentially constant, and the pulse width is modulated with the contents of the fractional accumulator. The area under the main PHP charge-pump curve represents the amount of charge delivered to the loop filter network. In order to minimize fractional-N sidebands in the VCO spectrum, the compensation current waveform is generated to have equal and opposite sign magnitude area to the main PHP charge pump.

PRINCIPLES OF OPERATION

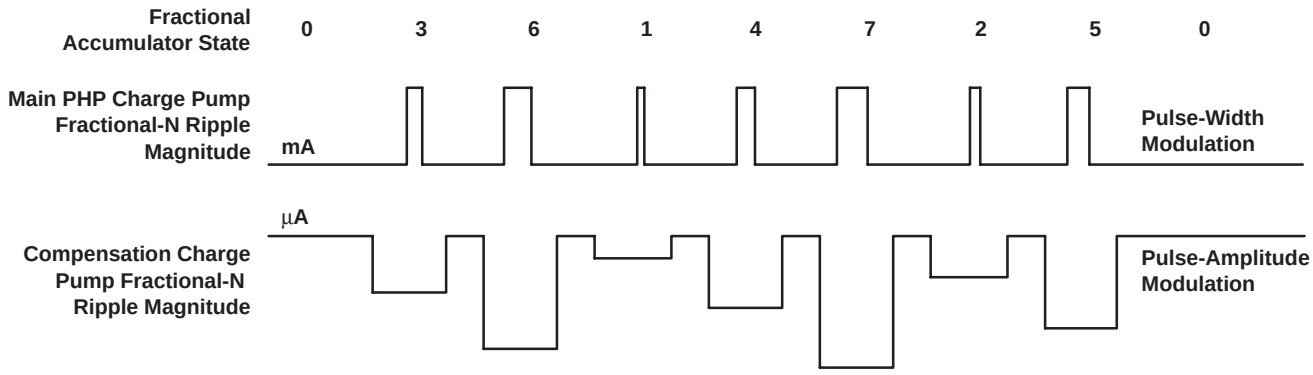


Figure 8. Main PHP and Compensation Charge Pump Fractional-N Waveforms for 3/8 Channel

The compensation waveform is pulse-amplitude modulated with the contents of the fractional accumulator. The main PHP pulse magnitude is much larger than the compensation pulse magnitude but the compensation pulse has a much longer duration than that of the main PHP pulse. The compensation pulse is optimally centered around the main PHP charge pump pulse in order to avoid additional sideband energy due to the phase offset between the main and compensation pulses.

The following example illustrates a method for determining correct values for RN, RF, and CN for minimal fractional-N sidebands based on VCO frequency and reference frequency.

Assumptions:
The main VCO is locked on channel.
953 MHz ± 10 MHz main VCO operation (942.99 MHz to 962.91 MHz)
19.44 MHz reference frequency
240 kHz phase detector reference frequency
500 µA peak main PHP current

1. Determine the fundamental fractional-N pulse width portion of the main PHP charge-pump output waveform for the lower, upper, and mean frequencies.

$$\text{Frac}_{PW-LWR} = \frac{1}{f_{PD}} - \frac{N}{f_{VCO}} = \frac{1}{240\text{ kHz}} - \frac{3929}{942.99\text{ MHz}} = 132.557\text{ ps},$$

$$\text{Frac}_{PW-UPR} = \frac{1}{f_{PD}} - \frac{N}{f_{VCO}} = \frac{1}{240\text{ kHz}} - \frac{4012}{962.91\text{ MHz}} = 129.815\text{ ps},$$

$$\text{Frac}_{PW-MEAN} = \frac{\text{Frac}_{PW-LWR} + \text{Frac}_{PW-UPR}}{2} = \frac{132.557\text{ ps} + 129.815\text{ ps}}{2} = 131.186\text{ ps}.$$

The mean-unit pulse width of the fractional-N portion of the main PHP charge-pump output waveform over the VCO frequencies of interest is 131.186 picoseconds (ps). This fundamental pulse width is modulated by the contents of the fractional accumulator. For the 3/8 fractional-N channel example, the pulse width varies as shown in Table 4.

PRINCIPLES OF OPERATION

Table 4. Main PHP Fractional-N Pulse-Widths and Areas for 3/8 Channel

NF = 3, FMOD = 8		
ACCUMULATOR STATE	**MAIN PHP FRACTIONAL PULSE WIDTH (ps)**	**MAIN PHP FRACTIONAL AREA (ps X AMPS)**
3	3 x *PW–Mean* = 393.558	393.558 ps x 500 μA = 0.196779
6	6 x *PW–Mean* = 787.116	787.116 ps x 500 μA = 0.393558
1	1 x *PW–Mean* = 131.186	131.186 ps x 500 μA = 0.065593
4	4 x *PW–Mean* = 524.744	524.744 ps x 500 μA = 0.262372
7	7 x *PW–Mean* = 918.302	918.302 ps x 500 μA = 0.459151
2	2 x *PW–Mean* = 262.372	262.372 ps x 500 μA = 0.131186
5	5 x *PW–Mean* = 655.930	655.930 ps x 500 μA = 0.327965
0	0 x *PW–Mean* = 0	0 ps x 500 μA = 0

Table 4 also shows the area of the fractional-N portion of the main PHP charge-pump waveform.

2. Determine the pulse width of the compensation charge-pump output waveform.

$$Comp_{PW} = \frac{1}{f_{Ref}} = \frac{1}{19.44\ MHz} = 51.440\ ns$$

3. Determine the fundamental compensation charge-pump current magnitude using the fundamental main PHP fractional area.

$$Comp_{Mag} = \frac{Frac_{Area}}{Comp_{PW}} = \frac{0.065593\ psA}{51.440\ ns} = 1.275\ \mu A$$

Table 5 shows the magnitude of the compensation pulse as a function of the fractional accumulator.

Table 5. Compensation Pulse Magnitudes for 3/8 Channel

NF = 3, FMOD = 8	
Accumulator Numerator	**Compensation Pulse Magnitude (μA)**
3	3 x 1.275 = 3.825
6	6 x 1.275 = 7.651
1	1 x 1.275 = 1.275
4	4 x 1.275 = 5.101
7	7 x 1.275 = 8.926
2	2 x 1.275 = 2.550
5	5 x 1.275 = 6.376
0	0 x 1.275 = 0

4. Using the result of step 3, determine the value of RF to give the fundamental compensation pulse magnitude.

$$RF\ (k\Omega) = \frac{25}{Comp_{Mag}(\mu A)} = \frac{25}{1.275} = 19.6\ k\Omega$$

PRINCIPLES OF OPERATION

5. Determine the values of CN and RN for the main PHP charge-pump peak current of 500 μA. Assume that a midrange value of CN equals 128.

$$RN(k\Omega) = \left(18.75 \times \frac{CN}{256} \times \frac{1}{I(mA)}\right) - 0.75 = \left(18.75 \times \frac{128}{256} \times \frac{1}{0.5\ mA}\right) - 0.75 = 18\ k\Omega$$

6. The values of the fundamental compensation pulse magnitude calculated in step 3 and the compensation pulse width calculated in step 2 are fixed. However, because the VCO can tune over a significant range of frequencies, the pulse width of the fractional-N portion of the main PHP charge-pump waveform varies; thus, the area of the same waveform varies. In order to maintain equal areas under the fractional-N portion of the main PHP charge-pump and compensation waveforms, CN must vary with the VCO frequency. As the VCO frequency increases, the fractional-N portion of the main PHP charge-pump waveform pulse width decreases proportionally, thereby decreasing the area under the same waveform. Therefore, CN is adjusted to equalize the main PHP and compensation waveform areas, as follows:

   $Frac_{PW\text{-}LWR}$ = 132.557 ps for f_{VCO} = 942.99 MHz
   $Frac_{PW\text{-}UPR}$ = 129.815 ps for f_{VCO} = 962.91 MHz

   The fundamental area of the fractional-N portion of the main PHP charge-pump waveform (step 1) is calculated as 0.065593 ps-A. If you calculate the fundamental area of the fractional-N portion of the main PHP charge-pump waveform using the actual pulse widths above in place of the average pulse width calculated in step 1, the fractional-N main PHP areas are obtained as follows:

   $Frac_{Area\text{-}LWR}$ = (132.557 ps) (0.500 mA) = 0.066279 (ps-A)
   $Frac_{Area\text{-}UPR}$ = (129.815 ps) (0.500 mA) = 0.064908 (ps-A)

   The actual areas under the fractional-N portion of the main PHP waveform require slight modification in the charge-pump current. The variation of CN required for area equalization is determined using a simple ratio form:

$$CN_{LWR} = \frac{Frac_{Area-AVG}}{Frac_{Area-LPR}} \times CN_{AVG} = \frac{0.065593}{0.066279} \times 128 = 126$$

$$CN_{UPR} = \frac{Frac_{Area-AVG}}{Frac_{Area-UPR}} \times CN_{AVG} = \frac{0.065593}{0.064908} \times 128 = 130$$

   Therefore, for this example, CN can vary from 126 to 130 over the VCO frequency range of 942.99 MHz to 962.91 MHz for optimum fractional-N sideband suppression. Due to component and circuit tolerances, additional deviations in CN may be appropriate.

auxiliary divider

The input signal on AUXIN is amplified by a single-ended, ac-coupled input buffer/amplifier that has sufficient sensitivity (200 mVpp at 100 MHz) for direct connection to a typical VCO. The 12-bit (NA) auxiliary divider incorporates a divide by 1 (PA = 1) or divide by 4 (PA = 0) prescaler. The total division ratio can be expressed as:

N_{Total} = 4 x NA

where PA = 0

N_{Total} = NA,

where PA = 1 and NA = 4 to 4095.

PRINCIPLES OF OPERATION

reference divider

The input signal on REFIN is amplified by a single-ended, ac-coupled input buffer/amplifier that has sufficient sensitivity (300 mVpp at 50 MHz) for direct connection to a typical TCXO. The 12-bit (NR) reference divider total division ratio can be expressed as:

$N_{Total} = NR$

where NR = 4 to 4095.

A four-section postscaler is connected to the output of the reference divider section. The main and auxiliary synthesizer sections can individually select a reference postscaler division of 1, 2, 4, or 8 by programming fields SM and SA, respectively (see Figure 9).

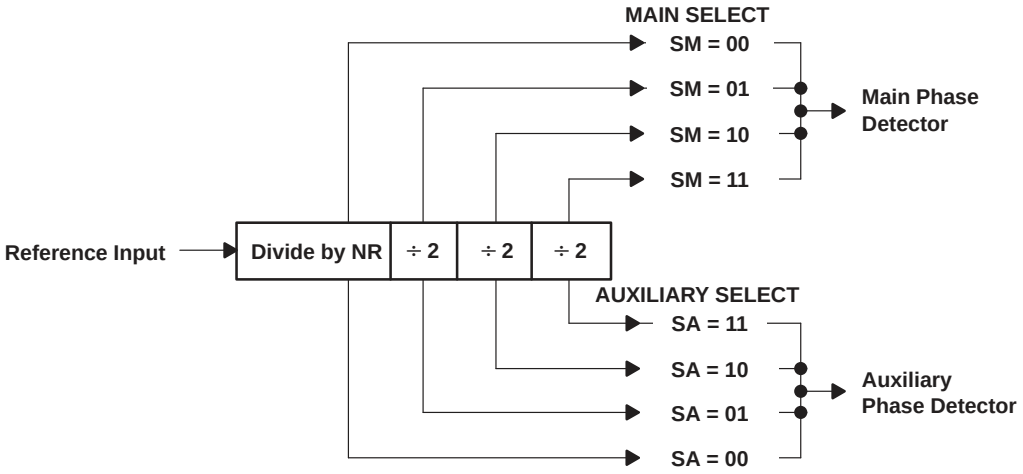


Figure 9. Reference Divider

phase detectors

The main and auxiliary synthesizer sections (see Figure 10) incorporate dual D-type flip-flop phase-frequency detectors (PFD). A PFD has gain with a phase error over a range of $\pm 2\pi$ and exhibits an infinite pull-in range. Dead-band compensation about zero-phase error is provided by forcing the sourcing and sinking charge pumps to have a minimum on-time of $1/f_{Ref}$ when the loop is operating in a locked condition.

The phase detectors can be programmed for polarity sense. Normally, external system VCOs have a positive slope control-voltage frequency characteristic. Some VCOs have a negative slope characteristic. The TRF2056 main and auxiliary phase detectors can be programmed for use with positive or negative slope VCOs using the MCP and ACP fields, respectively, in the B-Word (EPM mode).

For positive slope VCOs: MCP = ACP = 0

For negative slope VCOs: MCP = ACP = 1

PRINCIPLES OF OPERATION

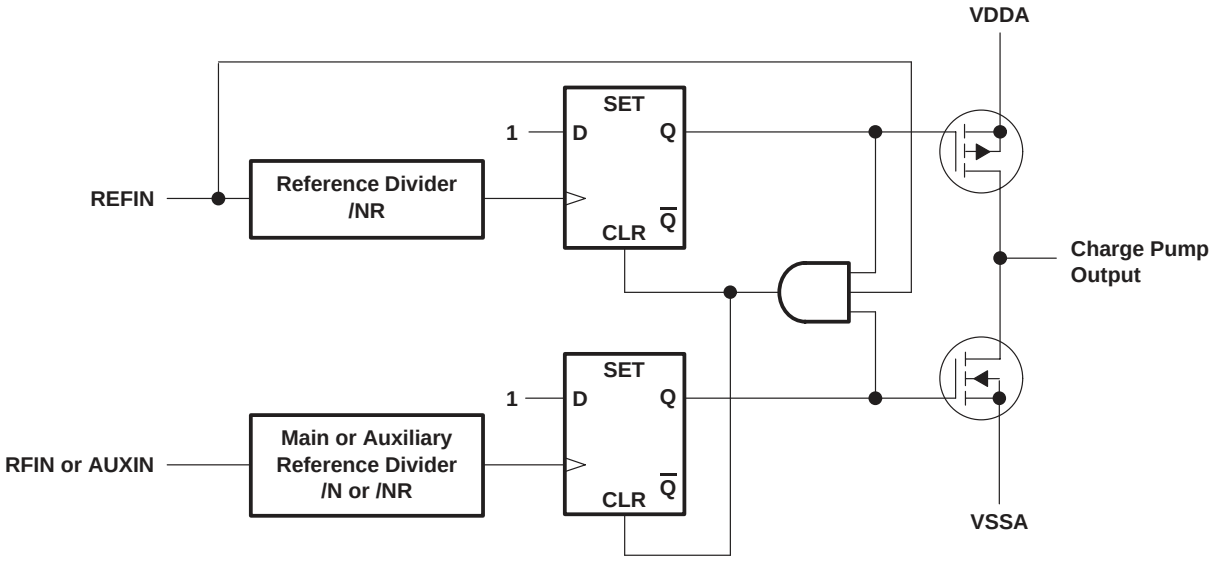


Figure 10. Main and Auxiliary Phase Detector Circuit

charge-pump current plans

The TRF2056 device uses internal band-gap references and external resistors to develop biasing reference currents for the various charge pumps sections. Three terminals are designated for the external resistors: RN, RF, and RA. Internal programmable coefficients CN, CL, and CK are also used. Table 6 shows how the external resistors achieve desired charge-pump peak currents.

Table 6. Charge Pump Current Plans

PARAMETER	MODE	CONDITION	UNIT
Peak proportional, normal mode current $PHP_{PK-NM} = \left(\frac{18.75}{RN + 0.75} \times \frac{CN}{256}\right)$	Normal	RN in kΩ	mA
Peak proportional, speed-up mode current $PHP_{PK-SM} = \left(\frac{18.75}{RN + 0.75} \times \frac{CN}{256}\right) + \left(\frac{18.75}{RN + 0.75} \times \frac{CN}{256} \times 2^{CL+1}\right)$	Speed-up	RN in kΩ	mA
Peak integral, speed-up mode current $PHI_{PK-SM} = \left(\frac{18.75}{RN + 0.75} \times \frac{CN}{256} \times CK \times 2^{CL+1}\right)$	Speed-up	RN in kΩ	mA
†Peak compensation, normal mode current $Comp_{PK} = \frac{30}{RF}$	Normal	RF in kΩ	µA
Peak auxiliary current $PHA_{PK} = \left(\frac{1.25}{RA} \times 20\right)$	Normal	RA in kΩ	mA

† The compensation charge-pump current is a pulse-amplitude modulated with the contents of the fractional accumulator. See *main divider – fractional-N sidebands and compensation*.

The average charge-pump current for the PHP, PHI, and PHA terminals is defined by:

$$I_{AVG} = \frac{\theta_{error}}{2\pi} \times I_{PK}.$$

PRINCIPLES OF OPERATION

loop enable/disable

The main and auxiliary loops can be enabled and disabled by the contents of the enable bits EM and EA, respectively. When disabled, all currents in the RF input stages are switched off; the bias currents for the respective charge-pump circuits are switched off as well. When both loops are disabled (EM = EA = 0), the reference input stage currents are switched off. The reference chain can be turned off because the serial interface operates independent of the reference input for the loading of serial words.

Table 7. Loop Enable/Disable

EM	EA	ENABLED	DISABLED
0	0		Main, Auxiliary, Reference
0	1	Auxiliary, Reference	Main
1	0	Main, Reference	Auxiliary
1	1	Main, Auxiliary, Reference	

speed-up mode

When the main synthesizer frequency is changed, it may be desirable to increase the loop bandwidth for a short time in order to achieve a faster locking speed. The proportional charge-pump current is increased and the integral charge-pump current is switched on for the duration of speed-up mode. The *charge-pump current plans* section illustrates how the charge-pump currents are a function of the external resistor RN and the programmable coefficients CN, CL, and CK.

lock detect

The lock condition of the PLL is defined as a phase difference of less than a ±1 cycle on the reference input REFIN. The LOCK terminal can be polled to determine the synthesizer lock condition of either or both loops. The lock detect function is described by the Boolean expression:

$$\text{LOCK} = \left(\text{LD}_{\text{Main}} + \overline{\text{EM}}\right) \cdot \left(\text{LD}_{\text{Aux}} + \overline{\text{EA}}\right)$$

test modes

The LOCK terminal may be used for test operations by terminating terminal 19 to ground. When test modes are enabled, the LOCK terminal is connected to internal nodes of the TRF2056 device. Test modes are enabled by writing ones to the two LSBs of the E-Word. Test modes are disabled by terminating terminal 19 to V_{CC} through a 10-kΩ pull-up resistor.

Table 8. Test Modes

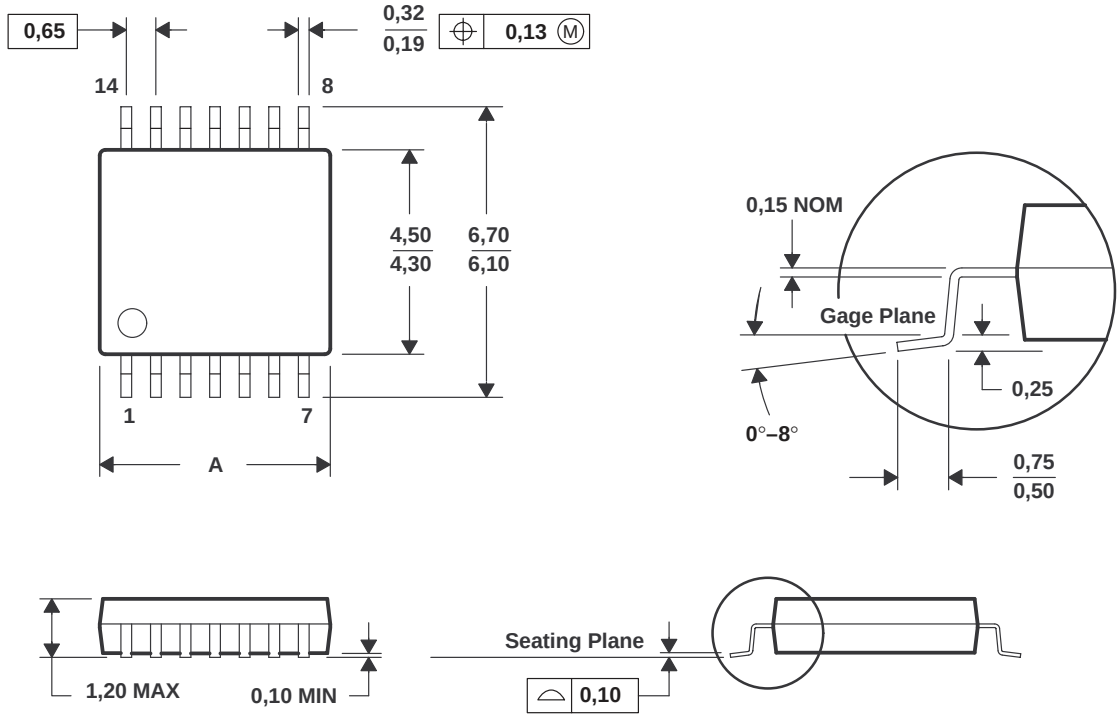
T1	T0	MODE
0	0	Buffered output of the fractional accumulator
0	1	Buffered output of the auxiliary divider
1	0	Buffered output of the main divider
1	1	Buffered output of the reference divider

The test mode can verify the division ratio of the reference divider, the auxiliary divider, and the main divider and prescaler.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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