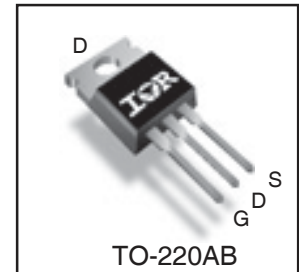
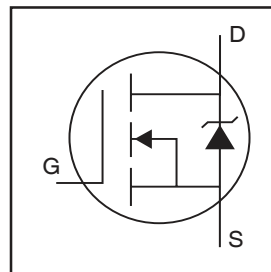


**Features**

- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low  $R_{DS(ON)}$  for Improved Efficiency
- Low  $Q_G$  and  $Q_{SW}$  for Better THD and Improved Efficiency
- Low  $Q_{RR}$  for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Can Deliver up to 300W per Channel into 8Ω Load in Half-Bridge Configuration Amplifier

Key Parameters		
$V_{DS}$	200	V
$R_{DS(ON)}$ typ. @ 10V	60	mΩ
$Q_g$ typ.	25	nC
$Q_{sw}$ typ.	9.8	nC
$R_{G(int)}$ typ.	2.6	Ω
$T_J$ max	175	°C



G	D	S
Gate	Drain	Source

**Description**

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MOSFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for ClassD audio amplifier applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	200	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	25	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	18	
$I_{DM}$	Pulsed Drain Current ①	100	
$P_D @ T_C = 25^\circ C$	Power Dissipation ④	144	W
$P_D @ T_C = 100^\circ C$	Power Dissipation ④	72	
	Linear Derating Factor	0.96	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

**Thermal Resistance**

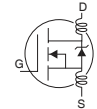
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	1.045	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ④	—	62	

Notes ① through ⑤ are on page 2

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.22	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	60	72.5	m $\Omega$	$V_{GS} = 10V, I_D = 15A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-14	—	mV/ $^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	37	—	—	S	$V_{DS} = 50V, I_D = 15A$
$Q_g$	Total Gate Charge	—	25	38	nC	$V_{DS} = 100V$ $V_{GS} = 10V$ $I_D = 15A$ See Fig. 6 and 19
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	6.3	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	1.9	—		
$Q_{gd}$	Gate-to-Drain Charge	—	7.9	—		
$Q_{godr}$	Gate Charge Overdrive	—	9.3	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	9.8	—		
$R_{G(int)}$	Internal Gate Resistance	—	2.6	5.0	$\Omega$	
$t_{d(on)}$	Turn-On Delay Time	—	8.6	—	ns	$V_{DD} = 100V, V_{GS} = 10V$ ③ $I_D = 15A$ $R_G = 2.4\Omega$
$t_r$	Rise Time	—	14.6	—		
$t_{d(off)}$	Turn-Off Delay Time	—	17.1	—		
$t_f$	Fall Time	—	9.9	—		
$C_{iss}$	Input Capacitance	—	1710	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz,$ See Fig.5 $V_{GS} = 0V, V_{DS} = 0V$ to 160V
$C_{oss}$	Output Capacitance	—	125	—		
$C_{rss}$	Reverse Transfer Capacitance	—	30	—		
$C_{oss}$	Effective Output Capacitance	—	138	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		

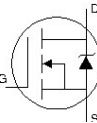


## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	113	mJ
$I_{AR}$	Avalanche Current ⑤	See Fig. 14, 15, 17a, 17b		A
$E_{AR}$	Repetitive Avalanche Energy ⑤			mJ

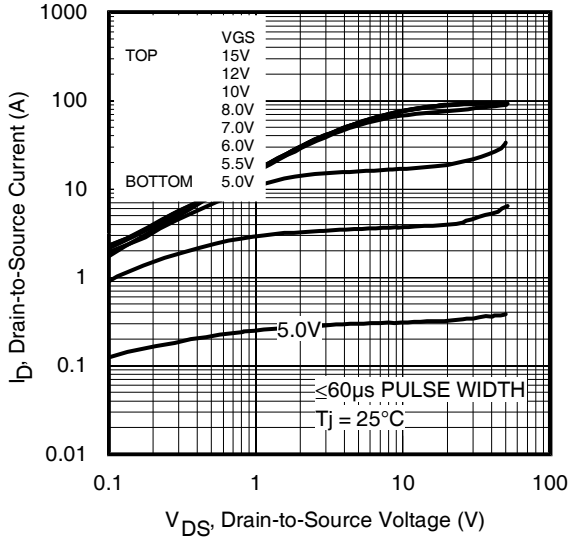
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$ @ $T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	25	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	100		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 15A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	98	147	ns	$T_J = 25^\circ\text{C}, I_F = 15A, V_R = 160V$
$Q_{rr}$	Reverse Recovery Charge	—	491	737	nC	$di/dt = 100A/\mu s$ ③

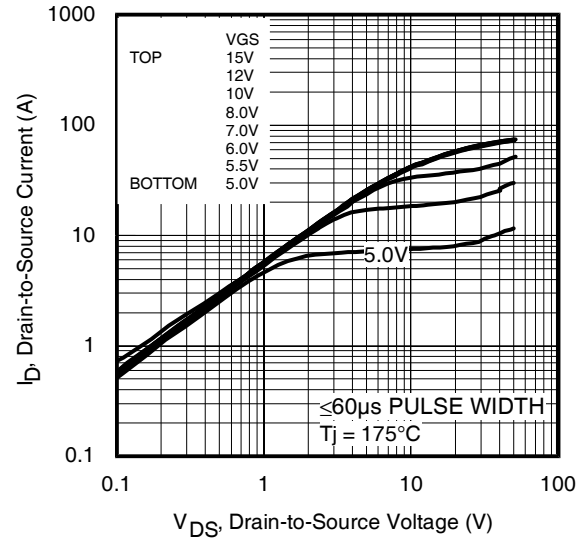


### Notes:

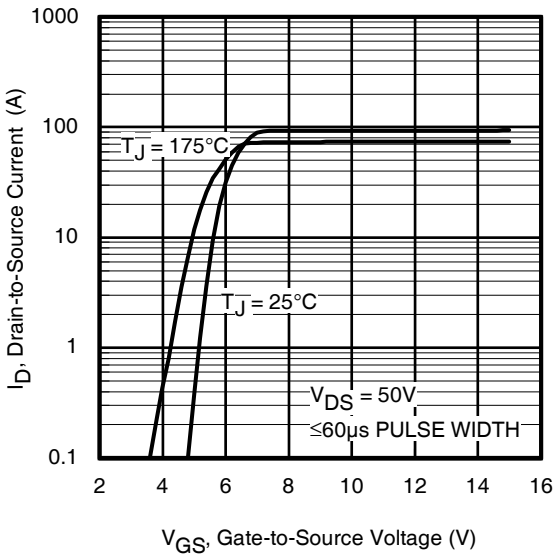
- ① Repetitive rating; pulse width limited by max. junction temperature. ④  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .  
 ② Starting  $T_J = 25^\circ\text{C}, L = 1.00mH, R_G = 25\Omega, I_{AS} = 15A$ . ⑤ Limited by  $T_{jmax}$ . See Figs. 14, 15, 17a, 17b for repetitive avalanche information  
 ③ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .



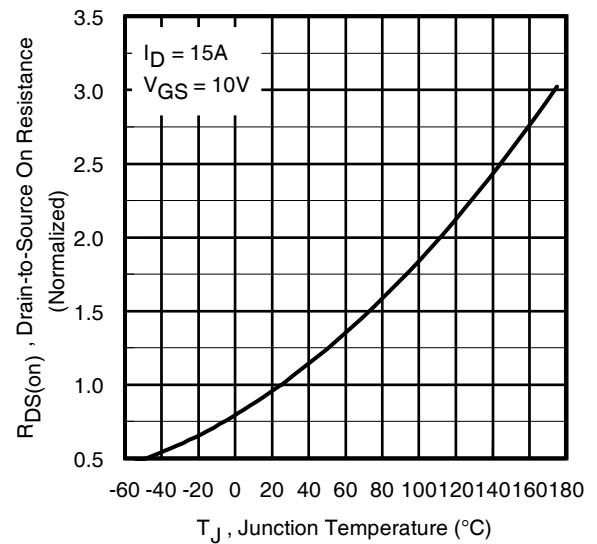
**Fig 1.** Typical Output Characteristics



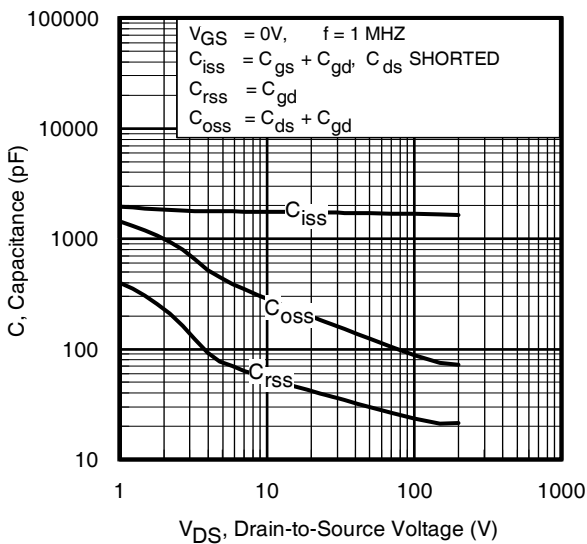
**Fig 2.** Typical Output Characteristics



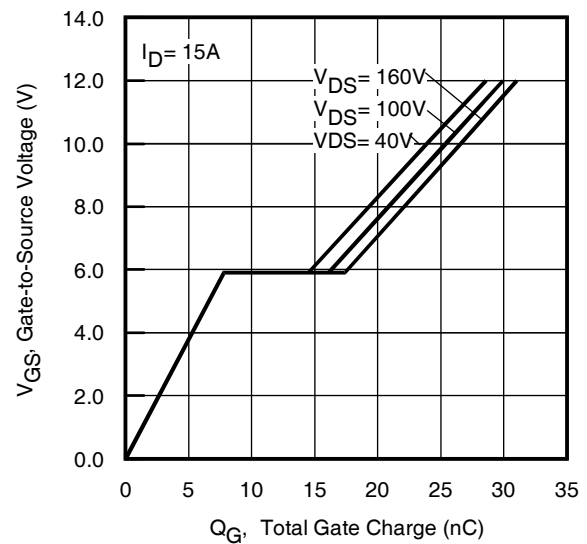
**Fig 3.** Typical Transfer Characteristics



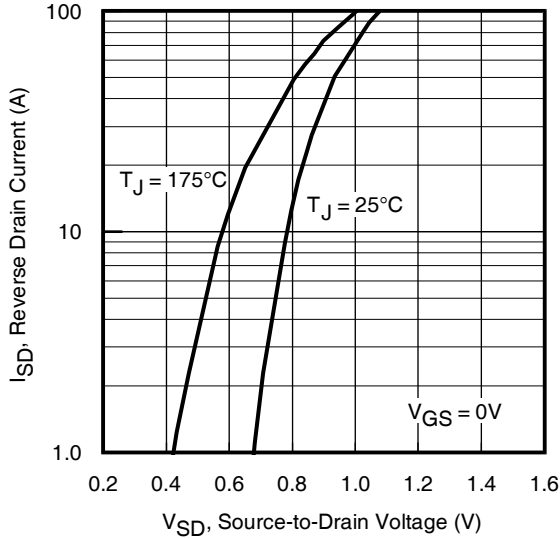
**Fig 4.** Normalized On-Resistance vs. Temperature



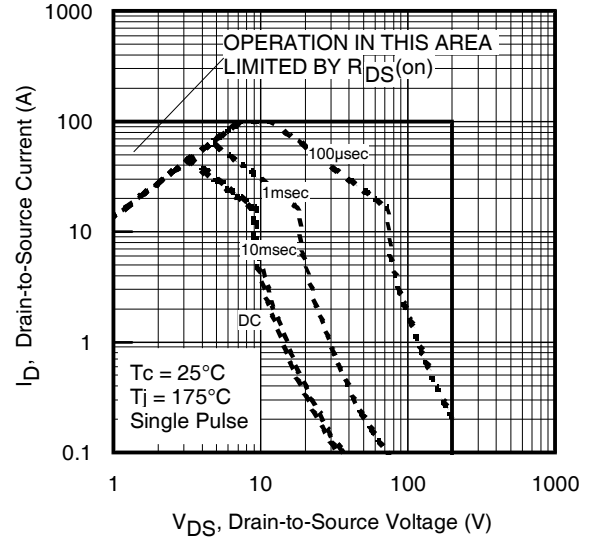
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
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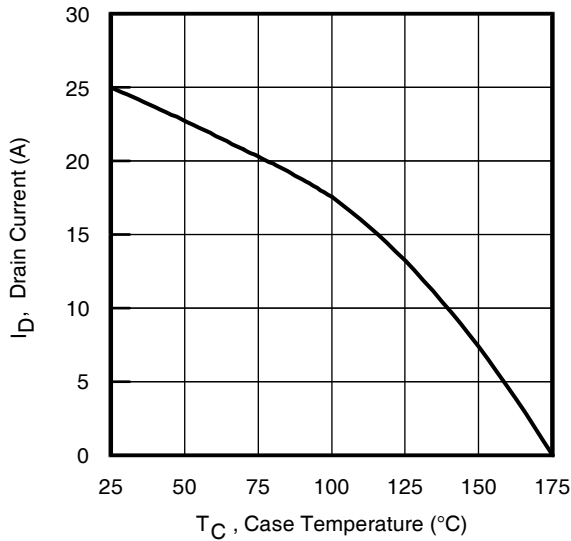
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



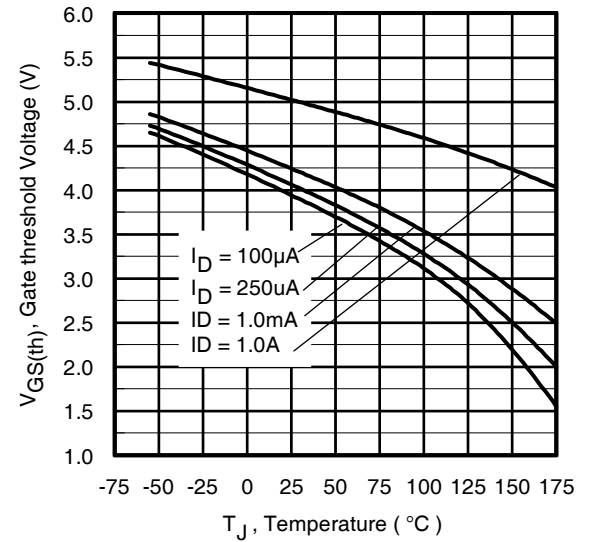
**Fig 7.** Typical Source-Drain Diode Forward Voltage



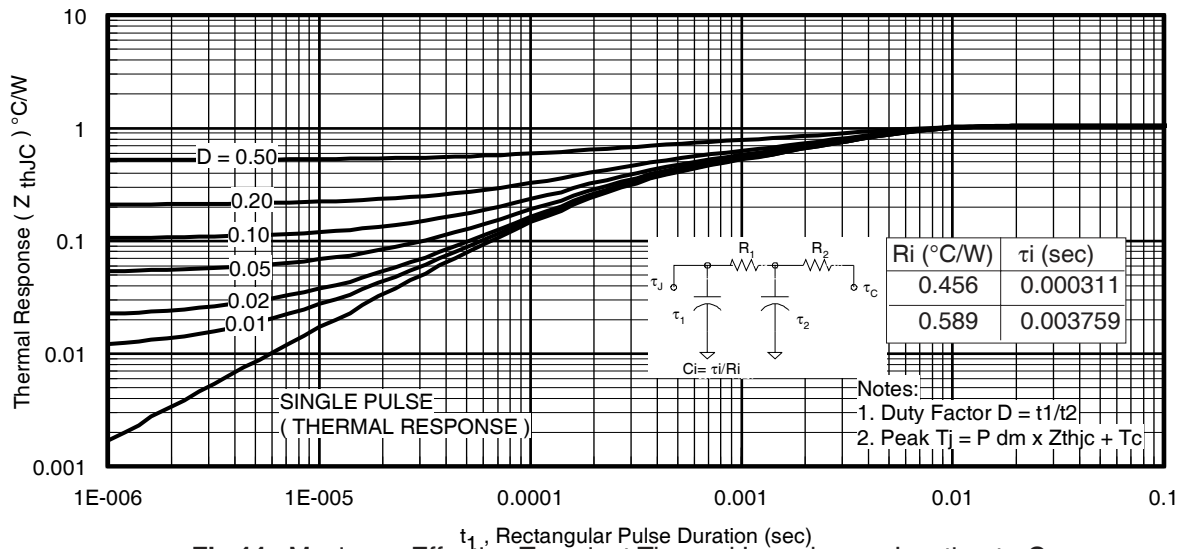
**Fig 8.** Maximum Safe Operating Area



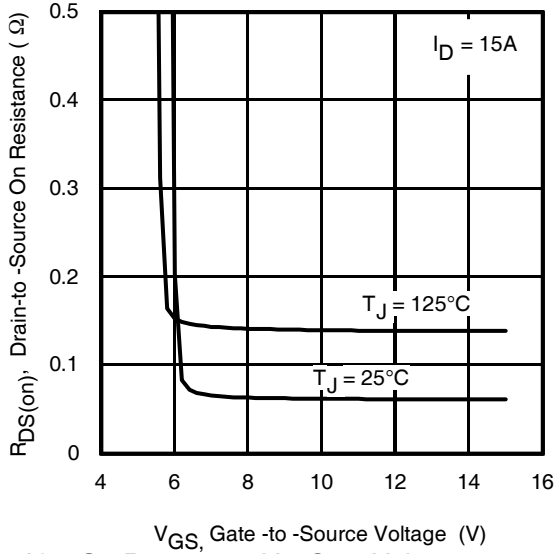
**Fig 9.** Maximum Drain Current vs. Case Temperature



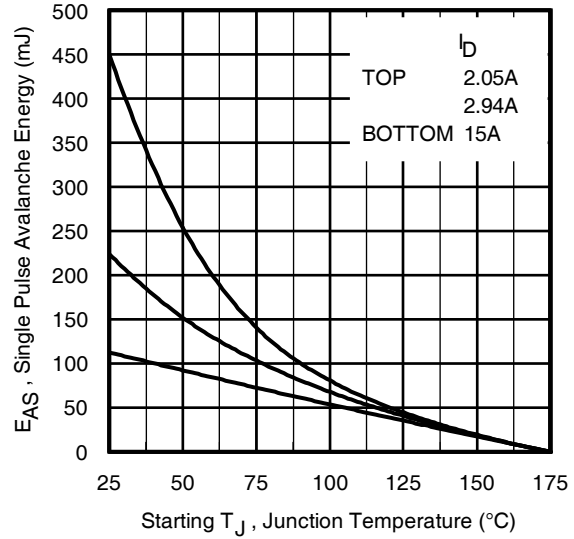
**Fig 10.** Threshold Voltage vs. Temperature



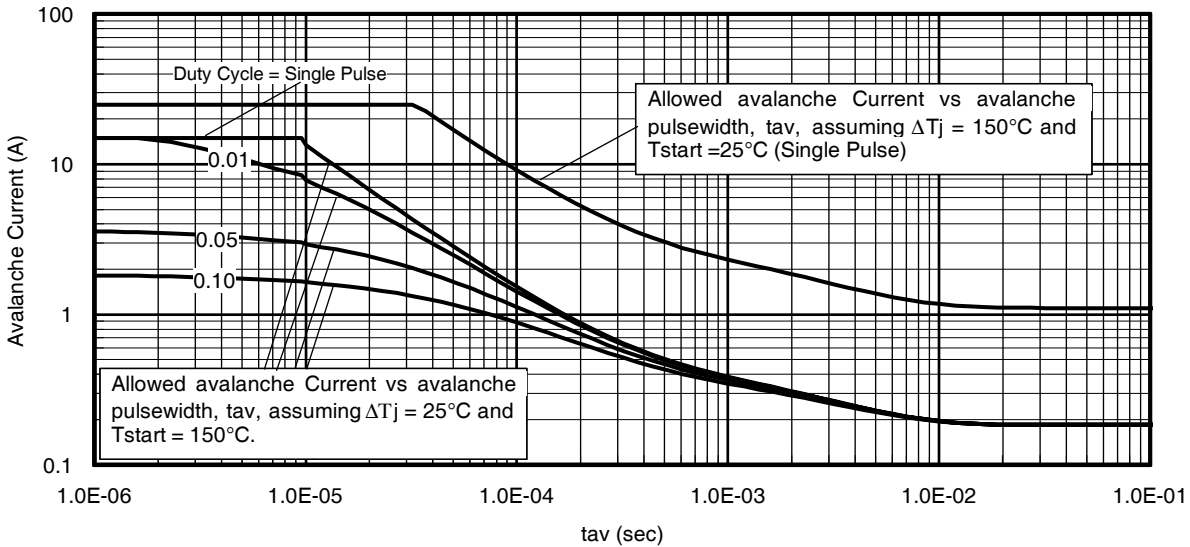
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



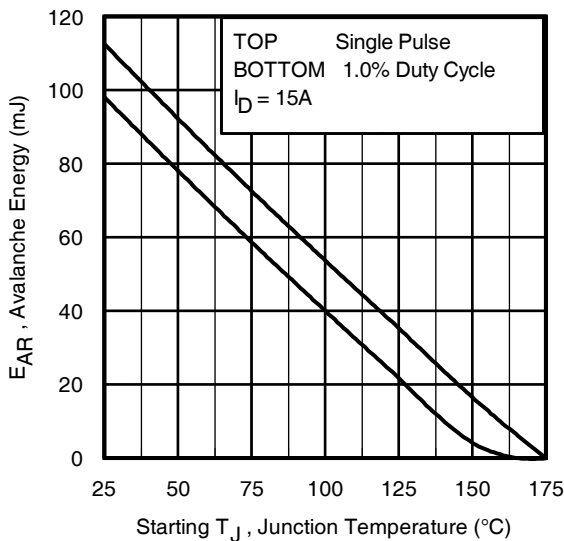
**Fig 12.** On-Resistance Vs. Gate Voltage



**Fig 13.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Typical Avalanche Current Vs. Pulsewidth



**Fig 15.** Maximum Avalanche Energy Vs. Temperature

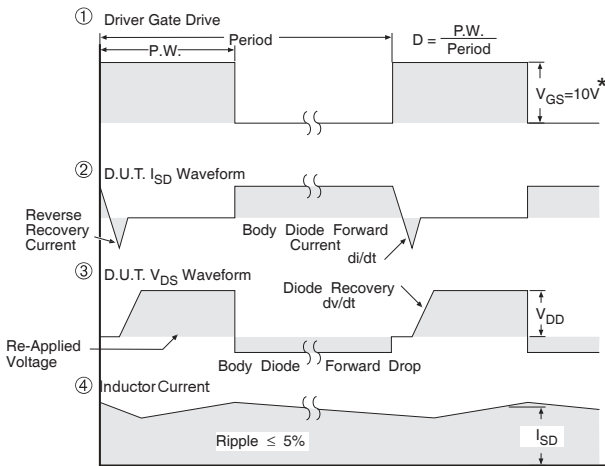
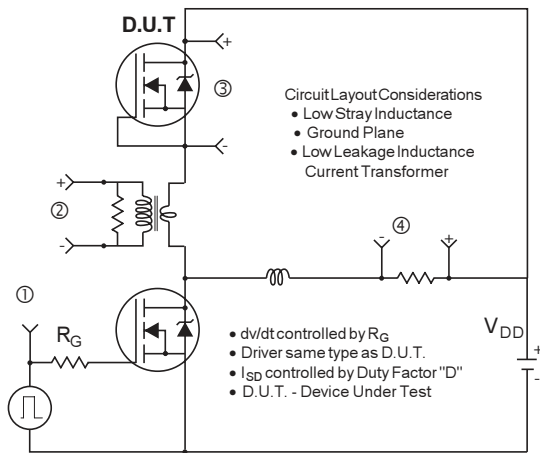
**Notes on Repetitive Avalanche Curves, Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither  $T_{jmax}$  nor  $I_{av}$  (max) is exceeded
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $B_V$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot B_V \cdot I_{av}) = \Delta T / Z_{thJC}$$

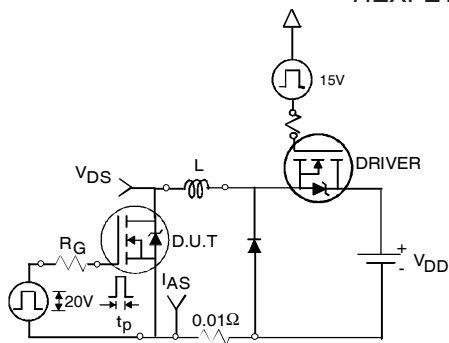
$$I_{av} = 2\Delta T / [1.3 \cdot B_V \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

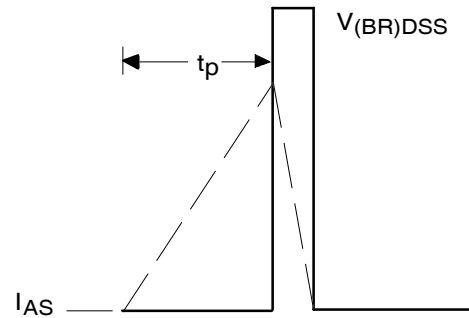


\*  $V_{GS} = 5V$  for Logic Level Devices

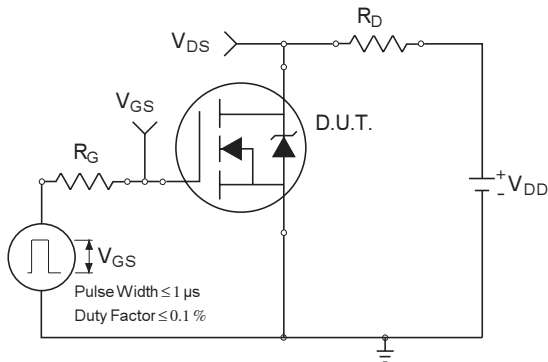
**Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



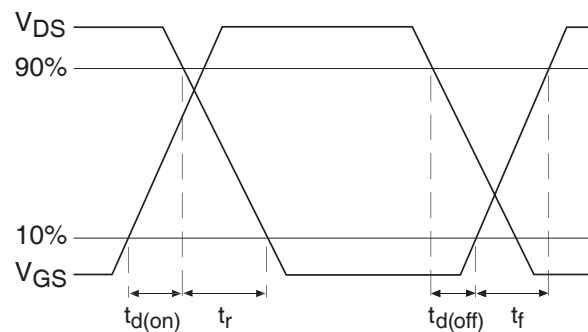
**Fig 17a. Unclamped Inductive Test Circuit**



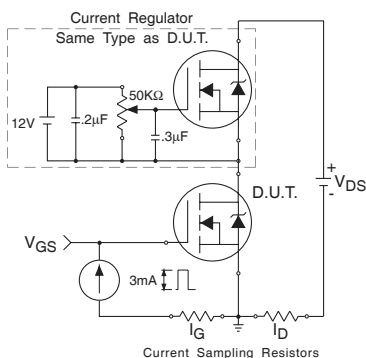
**Fig 17b. Unclamped Inductive Waveforms**



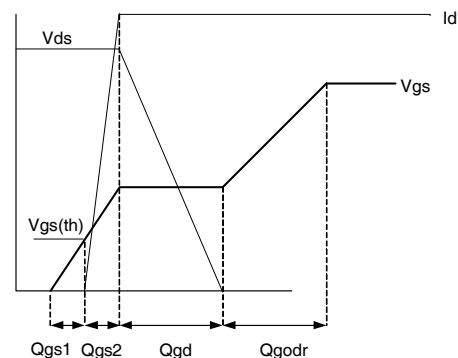
**Fig 18a. Switching Time Test Circuit**



**Fig 18b. Switching Time Waveforms**



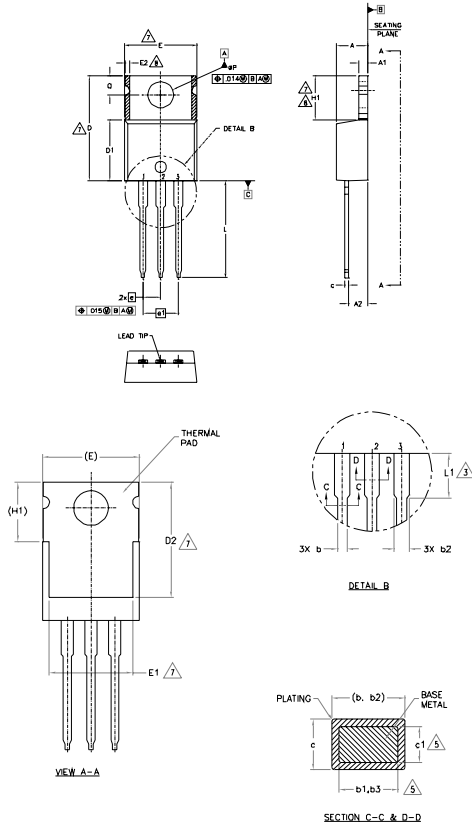
**Fig 19a. Gate Charge Test Circuit**



**Fig 19b. Gate Charge Waveform**

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
  - 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1
  - 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 6.- CONTROLLING DIMENSION - INCHES.
  - 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E.H1,D2 & E1
  - 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
  - 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	5
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	18.51	.560	.750	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.85	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
pP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

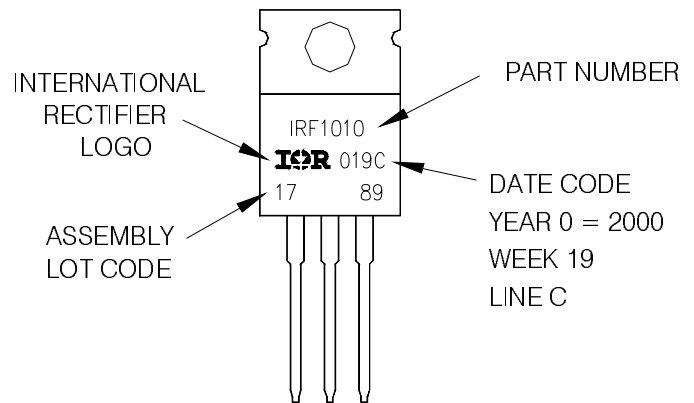
**LEAD ASSIGNMENTS**

- HEFET**  
1- GATE  
2- DRAIN  
3- SOURCE
- IRFL-GpAId**  
1- GATE  
2- COLLECTOR  
3- EMITTER
- DIODES**  
1- ANODE  
2- CATHODE  
3- ANODE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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