260 MHz, 16 × 5 Buffered Video Crosspoint Switches

Data Sheet

AD8106/AD8107

FEATURES

- 16 × 5 high speed, nonblocking switch arrays
  - AD8106: G = 1
  - AD8107: G = 2
- Pin compatible with AD8110/AD8111, 16 × 8 switch arrays
  - For a 16 × 16 array, see AD8114/AD8115
  - For a 16 x 8 array, see AD8110/AD8111
- Complete solution
  - Buffered inputs
  - Five output amplifiers
  - Drives 150 Ω loads
- Excellent video performance
  - 60 MHz 0.1 dB gain flatness
  - 0.02% differential gain error (R_L = 150 Ω)
  - 0.02° differential phase error (R_L = 150 Ω)
- Excellent ac performance
  - −3 dB bandwidth > 260 MHz
  - 500 V/µs slew rate
- Low power of 50 mA
- Low all-hostile crosstalk of −78 dB at 5 MHz
- Output disable allows connection of multiple device outputs
- Reset pin allows disabling of all outputs
- Excellent ESD rating: exceeds 4000 V human body model
- 80-lead LQFP (12 mm × 12 mm)

APPLICATIONS

- Routing of high speed signals including:
  - Composite video (NTSC, PAL, S, SECAM)
  - Component video (YUV, RGB)
  - Compressed video (MPEG, Wavelet)
  - 3-level digital video (HDB3)

FUNCTIONAL BLOCK DIAGRAM

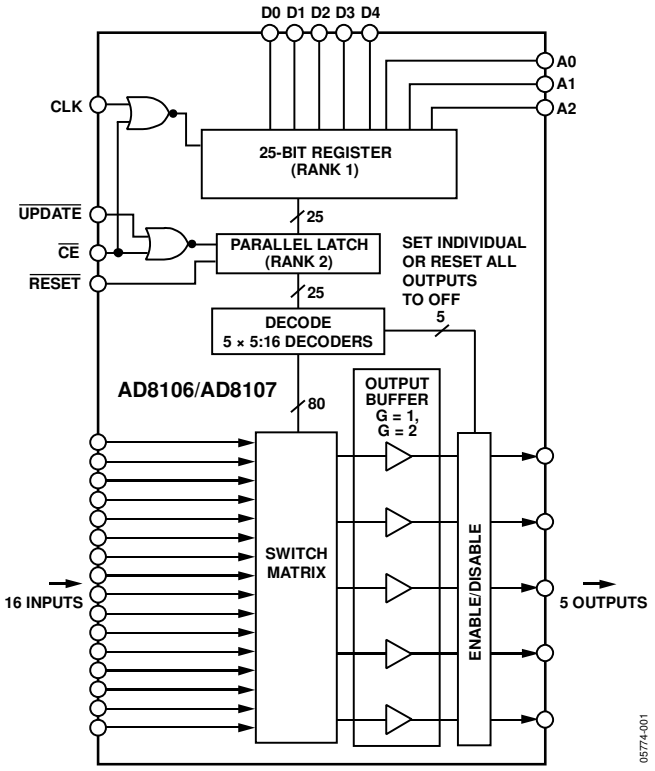

Figure 1.

GENERAL DESCRIPTION

The AD8106 and AD8107 are high speed, 16 × 5 video crosspoint switch matrices. They offer a −3 dB signal bandwidth greater than 260 MHz, and channel switch times of less than 25 ns with 1% settling. With −78 dB of crosstalk and −97 dB isolation (at 5 MHz), the AD8106/AD8107 are useful in many high speed applications. The differential gain and differential phase of greater than 0.02% and 0.02° respectively, along with 0.1 dB flatness out to 60 MHz, make the AD8106/AD8107 ideal for video signal switching.

The AD8106 and AD8107 include five independent output buffers that can be placed into a high impedance state for paralleling crosspoint outputs, preventing off channels from loading the output bus. The AD8106 has a gain of 1, while the AD8107 offers a gain of 2. Both operate on voltage supplies of ±5 V while consuming only 30 mA of idle current. The channel switching is performed via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8106/AD8107 are offered in an 80-lead LQFP and are available over the extended industrial temperature range of −40°C to +85°C.

Rev. A
Document Feedback

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3/06—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	Reference
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	200 mV p-p, R_L = 150 Ω	300/190	390/260		MHz	Figure 10, Figure 16
	2 V p-p, R_L = 150 Ω		150		MHz	Figure 10, Figure 16
Propagation Delay	2 V p-p, R_L = 150 Ω		5		ns	
Slew Rate	2 V step, R_L = 150 Ω		500		V/µs	
Settling Time	0.1%, 2 V step, R_L = 150 Ω		40		ns	Figure 15, Figure 21
Gain Flatness	0.05 dB, 200 mV p-p, R_L = 150 Ω		60/40		MHz	Figure 10, Figure 16
	0.05 dB, 2 V p-p, R_L = 150 Ω		65/40		MHz	Figure 10, Figure 16
	0.1 dB, 200 mV p-p, R_L = 150 Ω		80/57		MHz	Figure 10, Figure 16
	0.1 dB, 2 V p-p, R_L = 150 Ω		70/57		MHz	Figure 10, Figure 16
NOISE/DISTORTION PERFORMANCE						
Differential Gain Error	NTSC or PAL, R_L = 1 kΩ		0.01		%	
	NTSC or PAL, R_L = 150 Ω		0.02		%	
Differential Phase Error	NTSC or PAL, R_L = 1 kΩ		0.01		Degrees	
	NTSC or PAL, R_L = 150 Ω		0.02		Degrees	
Crosstalk, All Hostile	f = 5 MHz		−78/−85		dB	Figure 11, Figure 17
	f = 10 MHz		−70/−80		dB	Figure 11, Figure 17
Off Isolation, Input/Output	f = 5 MHz, R_L = 150 Ω, one channel		−97/−103		dB	Figure 26, Figure 32
Input Voltage Noise	0.01 MHz to 50 MHz		15		nV/√Hz	Figure 23, Figure 29
DC PERFORMANCE						
Gain Error	R_L = 1 kΩ		0.04/0.1	0.07/0.5	%	
	R_L = 150 Ω		0.15/0.25		%	
Gain Matching	No load, channel-to-channel			0.02/1.0	%	
	R_L = 1 kΩ, channel-to-channel			0.09/1.0	%	
Gain Temperature Coefficient			0.5/8		ppm/°C	
OUTPUT CHARACTERISTICS						
Output Impedance	DC, enabled		0.2		Ω	Figure 27, Figure 33
	Disabled		10/0.001		MΩ	Figure 24, Figure 30
Output Disable Capacitance	Disabled		2		pF	
Output Leakage Current	Disabled, AD8106 only		1/NA		µA	
Output Voltage Range	No load	±2.5	±3		V	
Output Current		20	40		mA	
Short-Circuit Current			65		mA	
INPUT CHARACTERISTICS						
Input Offset Voltage	Worst case (all configurations)		5	20	mV	Figure 38, Figure 44
	Temperature coefficient		12		µV/°C	Figure 39, Figure 45
Input Voltage Range		±2.5/±1.25	±3/±1.5		V	
Input Capacitance	Any switch configuration		2.5		pF	
Input Resistance		1	10		MΩ	
Input Bias Current	Per output selected		2	5	µA	
SWITCHING CHARACTERISTICS						
Enable On Time			60		ns	
Switching Time, 2 V Step	50% $\overline{\text{UPDATE}}$ to 1% settling		25		ns	
Switching Transient (Glitch)	Measured at output		20/30		mV p-p	Figure 25, Figure 31

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	Reference
POWER SUPPLIES						
Supply Current	AVCC, outputs enabled, no load		30		mA	
	AVCC, outputs disabled		15		mA	
	AVEE, outputs enabled, no load		30		mA	
	AVEE, outputs disabled		15		mA	
	DVCC		11		mA	
Supply Voltage Range			±4.5 to ±5.5		V	
PSRR	f = 100 kHz		75/78		dB	Figure 22, Figure 28
	f = 1 MHz		−55/−58		dB	
OPERATING TEMPERATURE						
Temperature Range	Operating (still air)		−40 to +85		°C	
θ_{JA}	Operating (still air)		48		°C/W	

TIMING CHARACTERISTICS

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	Data setup time
t_2	100	ns min	CLK pulse width
t_3	20	ns min	Data hold time
t_4	100	ns min	CLK pulse separation
t_5	0	ns min	CLK to $\overline{\text{UPDATE}}$ delay
t_6	50	ns min	$\overline{\text{UPDATE}}$ pulse width
–	8	ns max	Propagation delay, $\overline{\text{UPDATE}}$ to switch on or off
–	100	ns max	CLK, $\overline{\text{UPDATE}}$ rise and fall times
–	200	ns min	$\overline{\text{RESET}}$ time

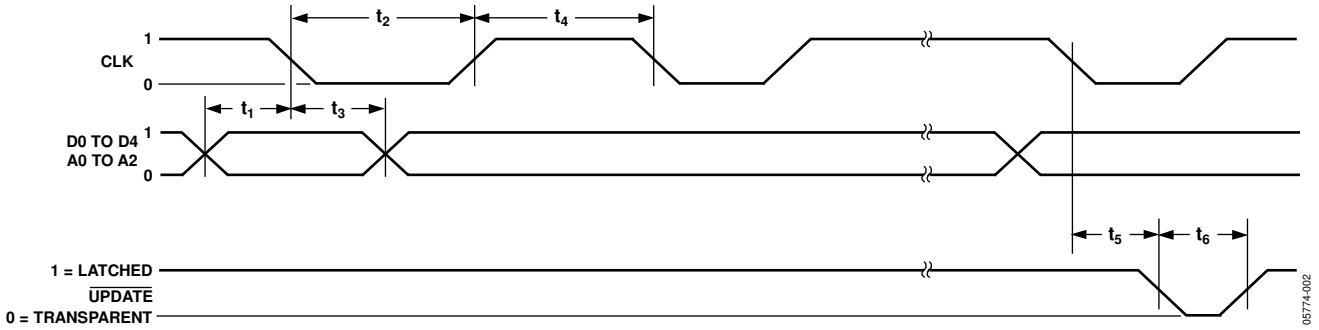

Figure 2. Timing Diagram

Table 3. Logic Levels

V_{IH}	V_{IL}	I_{IH}	I_{IL}
$\overline{\text{RESET}}$, CLK, D0, D1, D2, D3, D4, A0, A1, A2, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, CLK, D0, D1, D2, D3, D4, A0, A1, A2, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, CLK, D0, D1, D2, D3, D4, A0, A1, A2, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, CLK, D0, D1, D2, D3, D4, A0, A1, A2, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$
2.0 V min	0.8 V max	20 μA max	−400 μA min

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.0 V
Internal Power Dissipation	
AD8106/AD8107 80-Lead LQFP (ST-80-1)	2.6 W
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power derating curves
θ_{JA}	48°C/W
Operating Temperature Range	−40°C to 85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8106/AD8107 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8106/AD8107 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

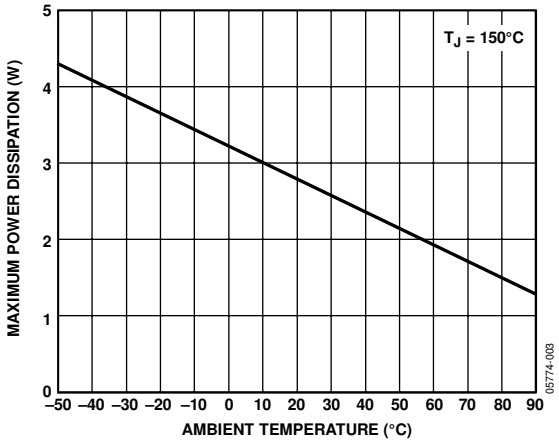

Figure 3. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 5. Operation Truth Table

$\overline{CE}$	$\overline{UPDATE}$	CLK	DATA IN	DATA OUT	$\overline{RESET}$	Operation/Comment
1	X	X	X	X	X	No change in logic.
0	1	*f*	D0 … D4 A0 … A2	NA in parallel mode	1	The data on the parallel data lines, D0 to D4, are loaded into the 40-bit serial shift register location addressed by A0 to A2.
0	0	X	X	X	1	Data in the 40-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

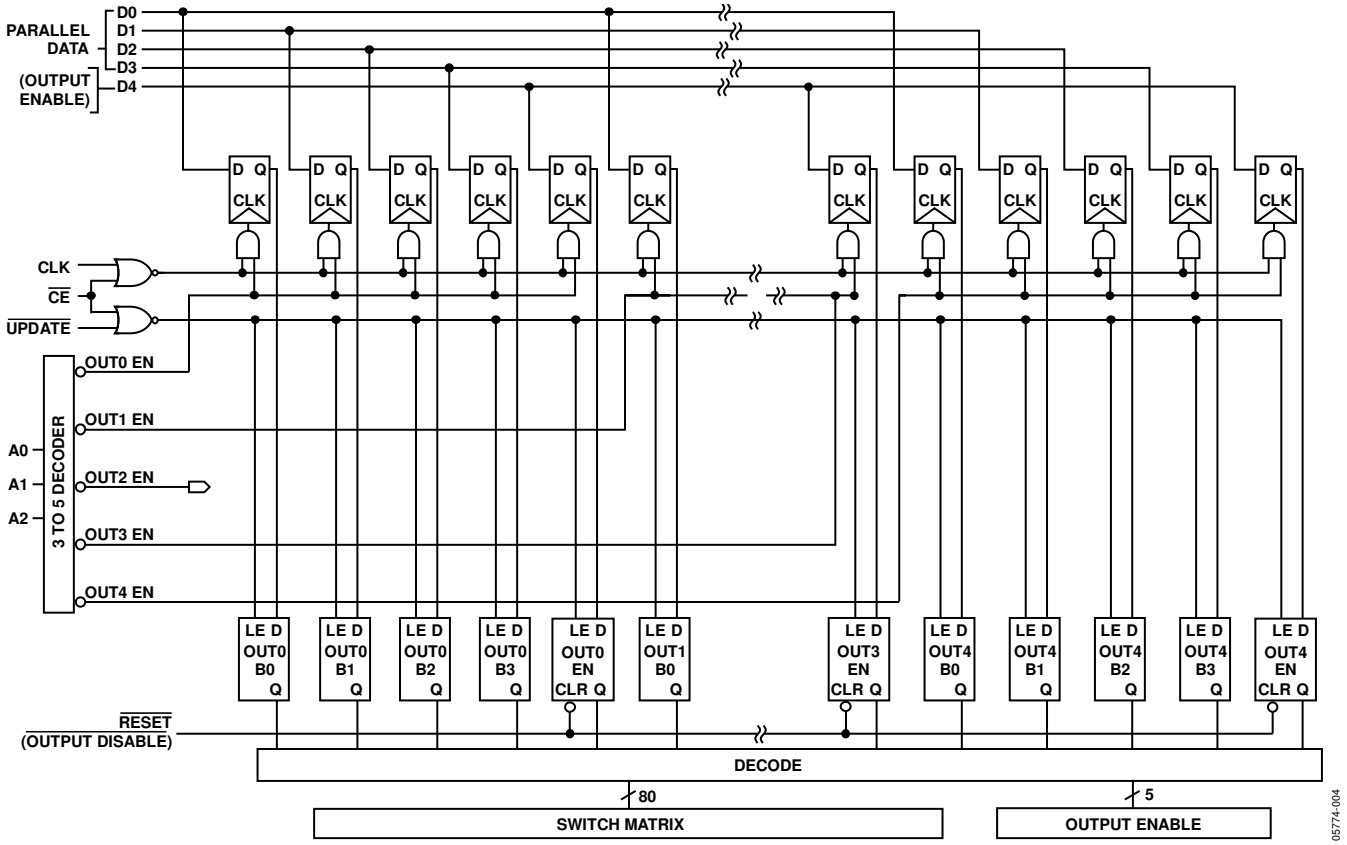

Figure 4. Logic Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

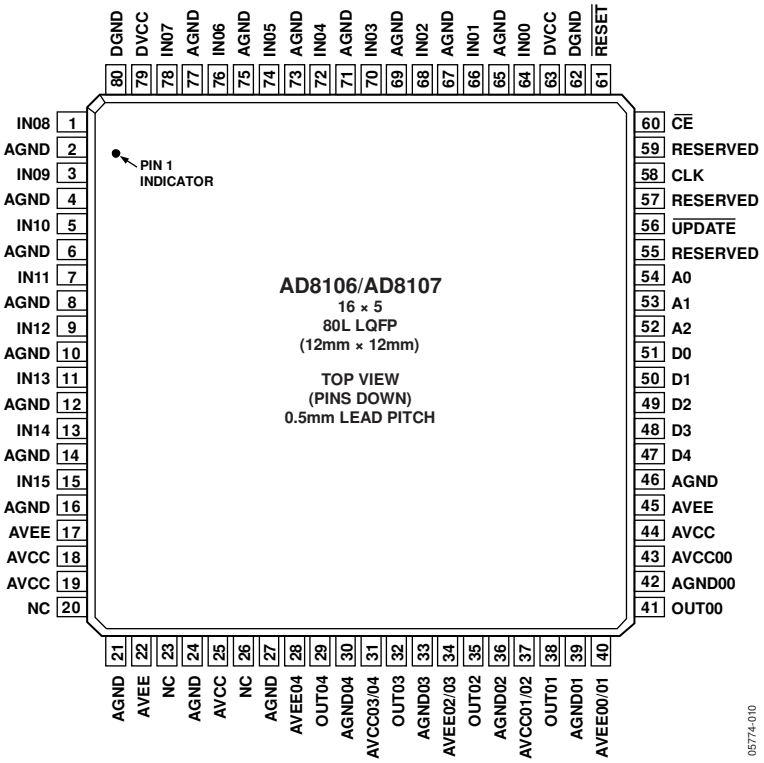

Figure 5. 80-Lead Plastic LQFP

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
64 , 66, 68, 70, 72, 74, 76, 78, 1, 3, 5, 7, 9, 11, 13, 15,	INxx	Analog Inputs; xx = Channel Numbers 00 through 15.
58	CLK	Clock, TTL Compatible. Falling edge triggered.
56	$\overline{\text{UPDATE}}$	Enable (Transparent) Low. Allows serial register to connect directly to switch matrix. Data latched when high.
61	$\overline{\text{RESET}}$	Disable Outputs, Active Low.
60	$\overline{\text{CE}}$	Chip Enable, Enable Low. Must be low to clock in and latch data.
41, 38, 35, 32, 29	OUTyy	Analog Outputs; yy = Channel Numbers 00 Through 04.
2, 4, 6, 8, 10, 12, 14, 16, 21, 24, 27, 46, 65, 67, 69, 71, 73, 75, 77	AGND	Analog Ground for Inputs and Switch Matrix.
63, 79	DVCC	5 V for Digital Circuitry.
62, 80	DGND	Ground for Digital Circuitry.
17, 22, 45	AVEE	−5 V for Inputs and Switch Matrix.
18, 19, 25, 44	AVCC	+5 V for Inputs and Switch Matrix.
42, 39, 36, 33, 30	AGNDxx	Ground for Output Amp; xx = Output Channel Numbers 00 Through 07. Must be connected.
43, 37, 31, 22	AVCCxx/yy	+5 V for Output Amplifier. Shared by channel numbers xx and yy. Must be connected.
40, 34, 28	AVEExx/yy	−5 V for Output Amplifier. Shared by channel numbers xx and yy. Must be connected.
54	A0	Parallel Data Input, TTL Compatible (Output Select LSB).
53	A1	Parallel Data Input, TTL Compatible (Output Select).
52	A2	Parallel Data Input, TTL Compatible (Output Select MSB).
51	D0	Parallel Data Input, TTL Compatible (Input Select LSB).
50	D1	Parallel Data Input, TTL Compatible (Input Select).
49	D2	Parallel Data Input, TTL Compatible (Input Select).
48	D3	Parallel Data Input, TTL Compatible (Input Select MSB).
47	D4	Parallel Data Input, TTL Compatible (Output Enable).

INPUT/OUTPUT SCHEMATICS

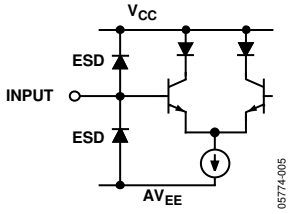

Figure 6. Analog Input

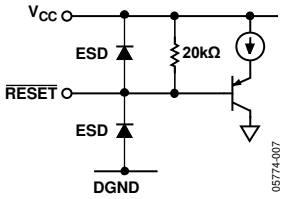

Figure 8. $\overline{RESET}$ Input

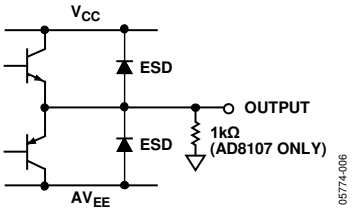

Figure 7. Analog Output

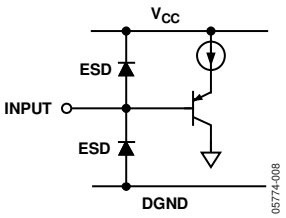

Figure 9. Logic Input

TYPICAL PERFORMANCE CHARACTERISTICS

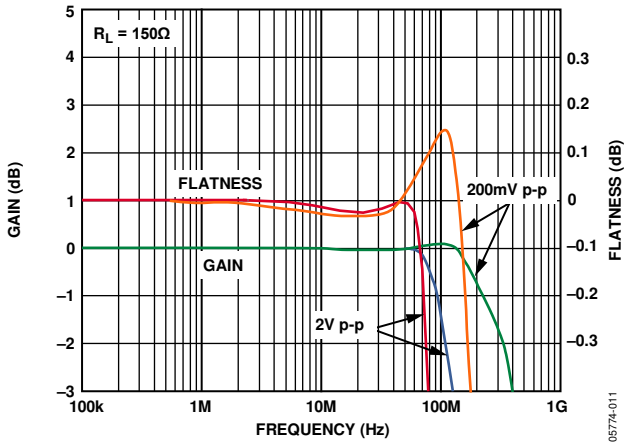

Figure 10. AD8106 Frequency Response

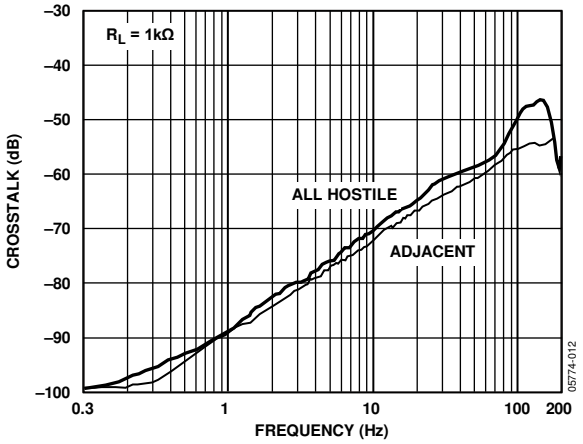

Figure 11. AD8106 Crosstalk vs. Frequency

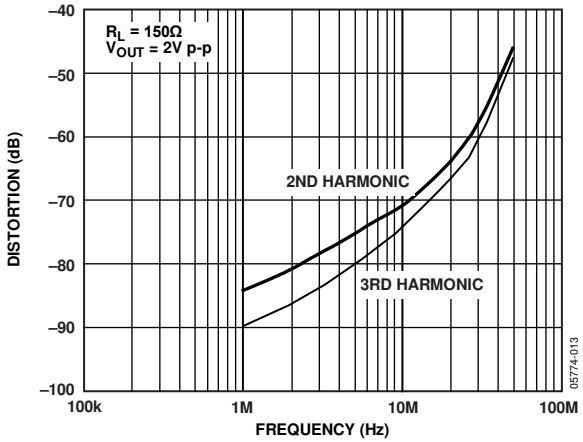

Figure 12. AD8106 Distortion vs. Frequency

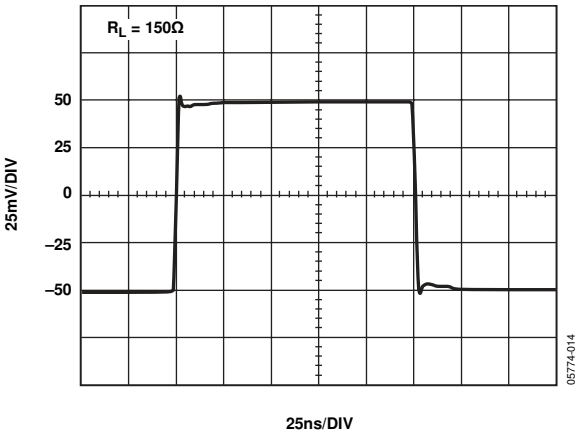

Figure 13. AD8106 Step Response, 100 mV Step

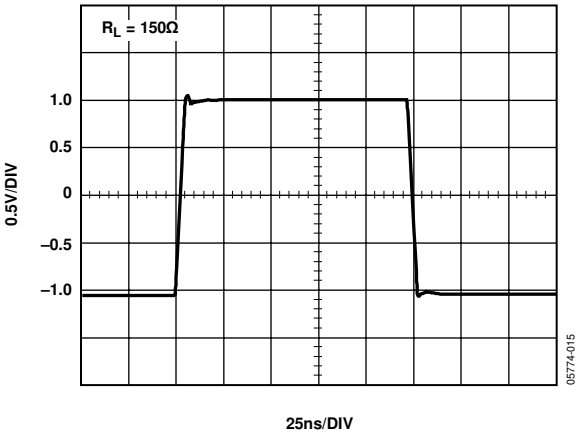

Figure 14. AD8106 Step Response, 2 V Step

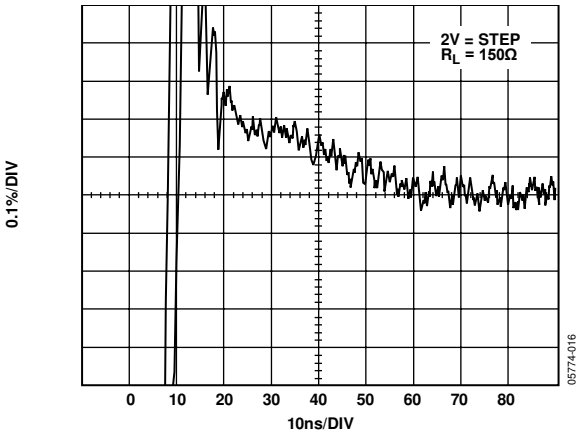

Figure 15. AD8106 Settling Time

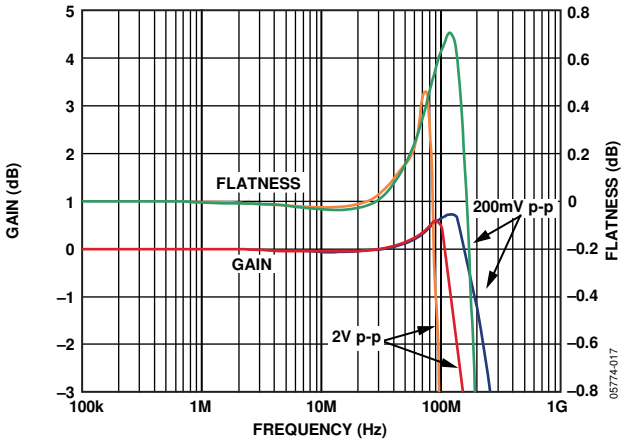

Figure 16. AD8107 Frequency Response

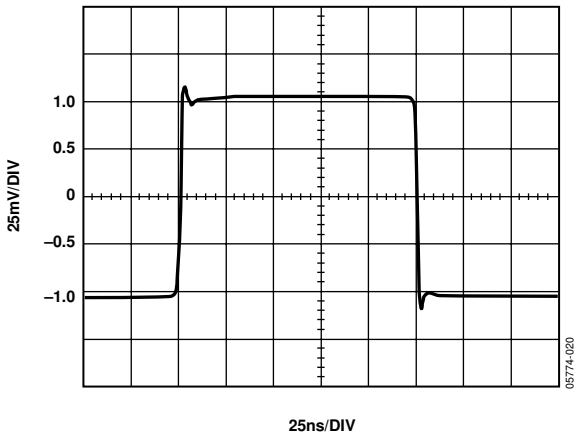

Figure 19. AD8107 Step Response, 100 mV Step

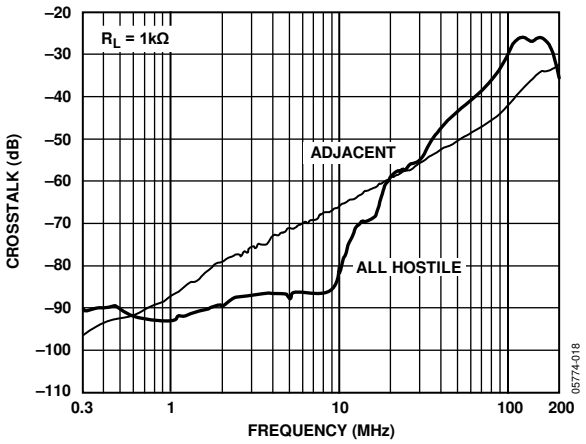

Figure 17. AD8107 Crosstalk vs. Frequency

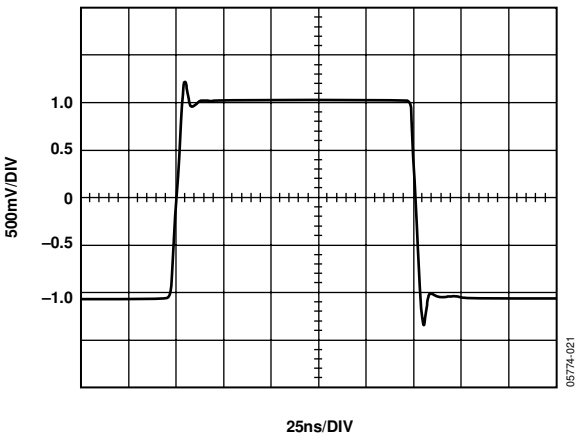

Figure 20. AD8107 Step Response, 2 V Step

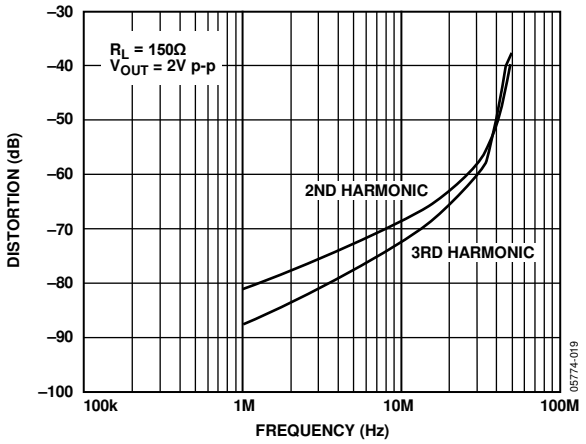

Figure 18. AD8107 Distortion vs. Frequency

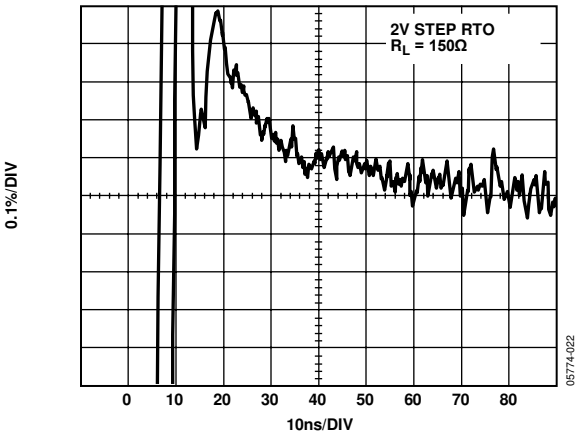

Figure 21. AD8107 Settling Time

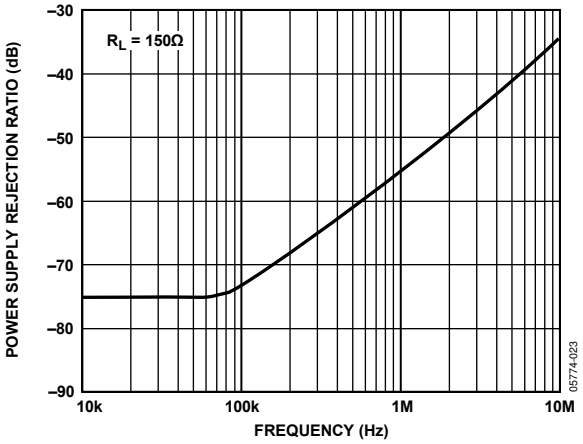

Figure 22. AD8106 PSRR vs. Frequency

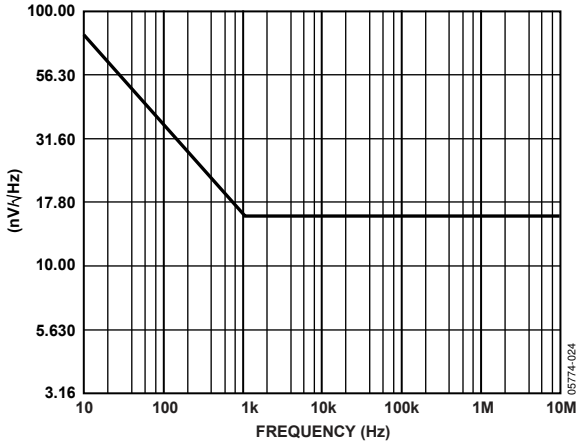

Figure 23. AD8106 Voltage Noise vs. Frequency

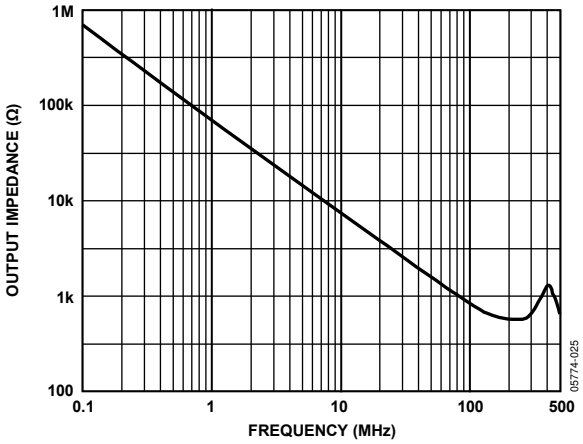

Figure 24. AD8106 Output Impedance, Disabled

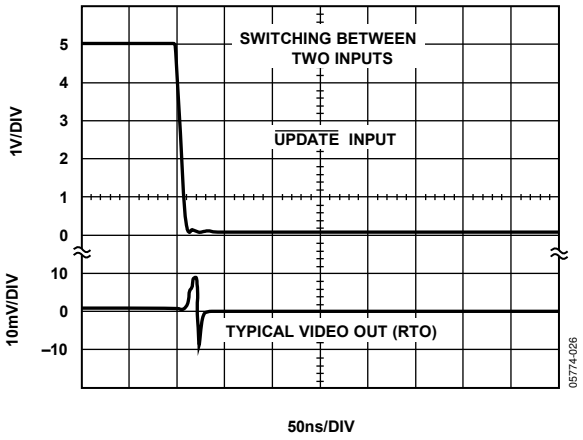

Figure 25. AD8106 Switching Transient (Glitch)

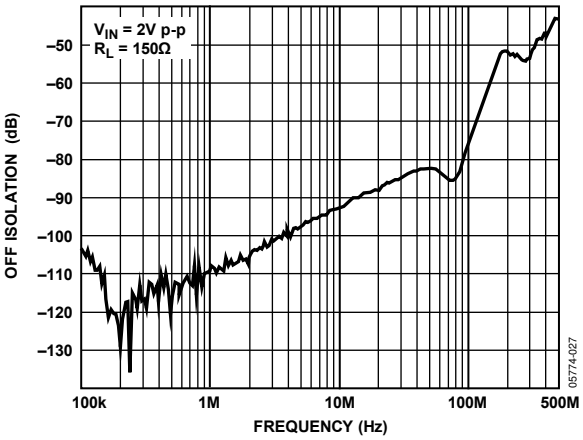

Figure 26. AD8106 Off Isolation, Input/Output

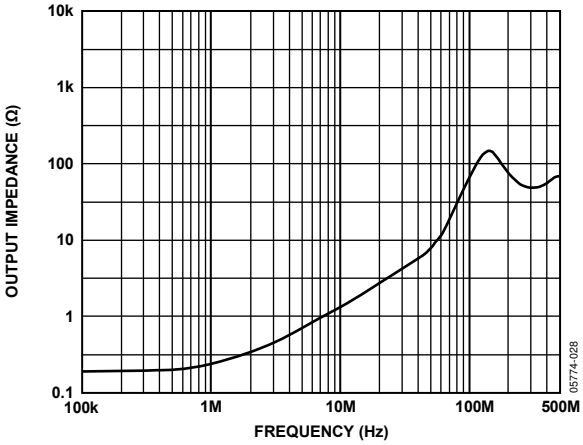

Figure 27. AD8106 Output Impedance, Enabled

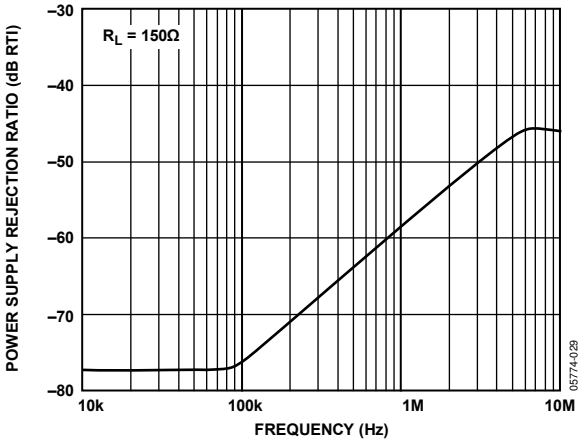

Figure 28. AD8107 PSRR vs. Frequency

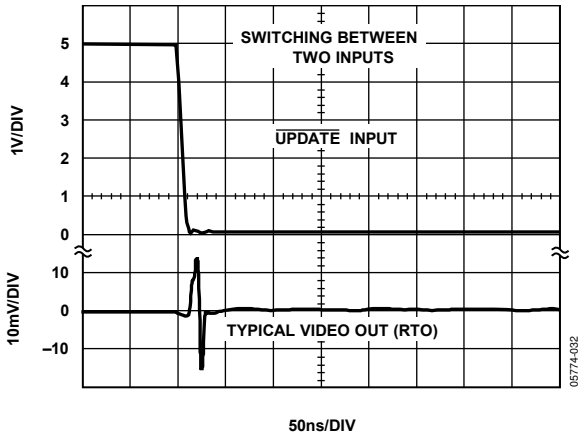

Figure 31. AD8107 Switching Transient (Glitch)

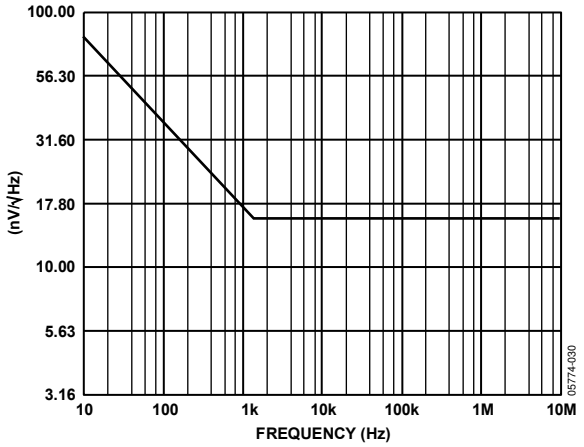

Figure 29. AD8107 Voltage Noise vs. Frequency

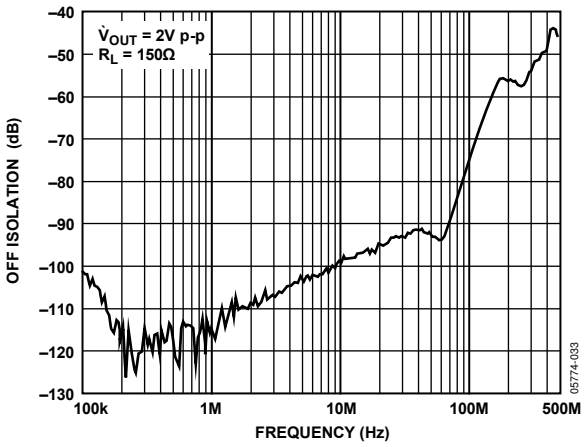

Figure 32. AD8107 Off Isolation, Input/Output

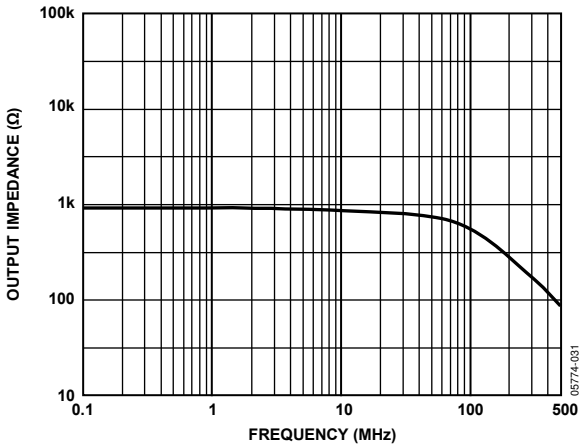

Figure 30. AD8107 Output Impedance, Disabled

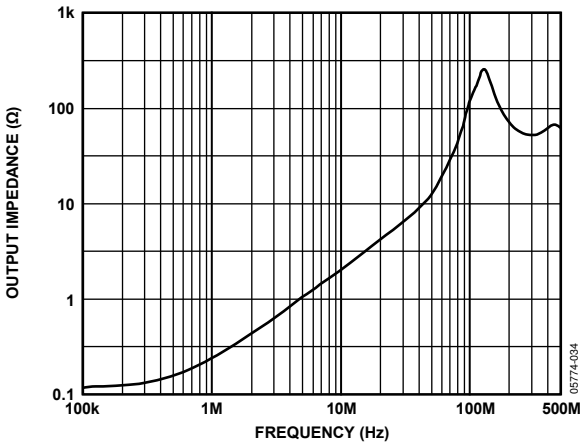

Figure 33. AD8107 Output Impedance, Enabled

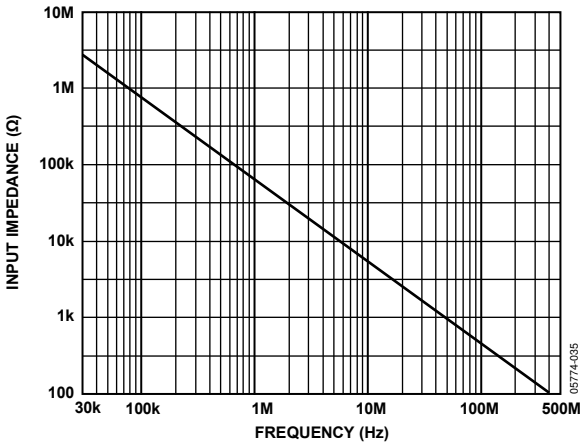

Figure 34. AD8106 Input Impedance vs. Frequency

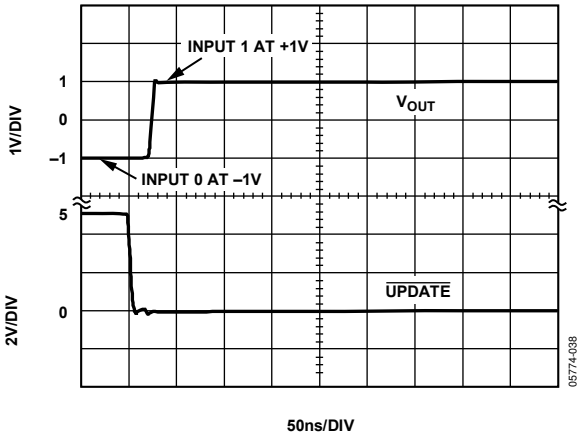

Figure 37. AD8106 Switching Time

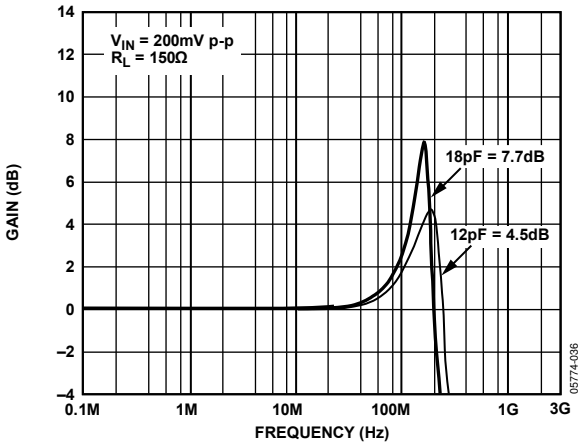

Figure 35. AD8106 Frequency Response vs. Capacitive Load

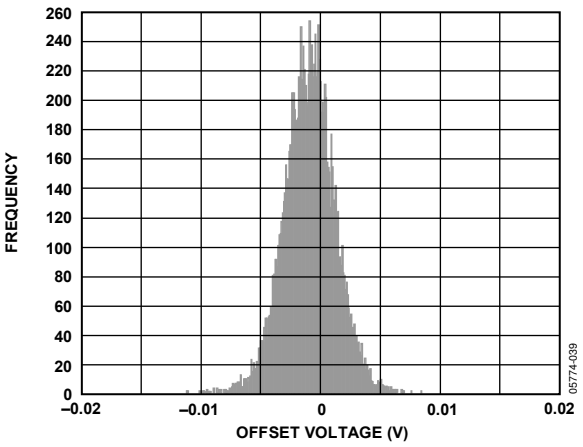

Figure 38. AD8106 Offset Voltage Distribution

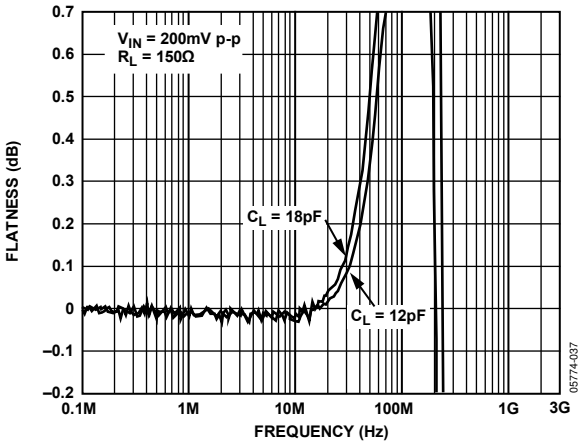

Figure 36. AD8106 Flatness vs. Capacitance Load

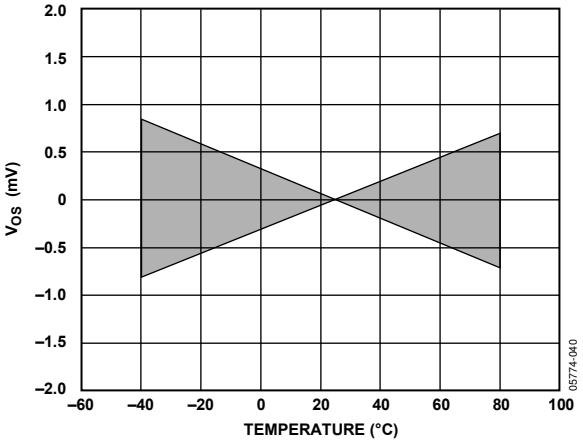

Figure 39. AD8106 Offset Voltage vs. Temperature (Normalized at 25°C)

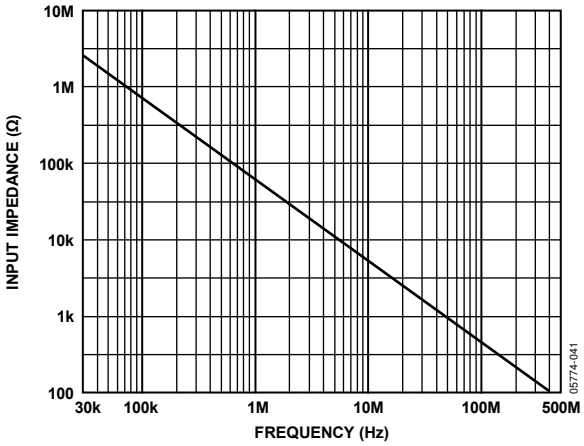

Figure 40. AD8107 Input Impedance vs. Frequency

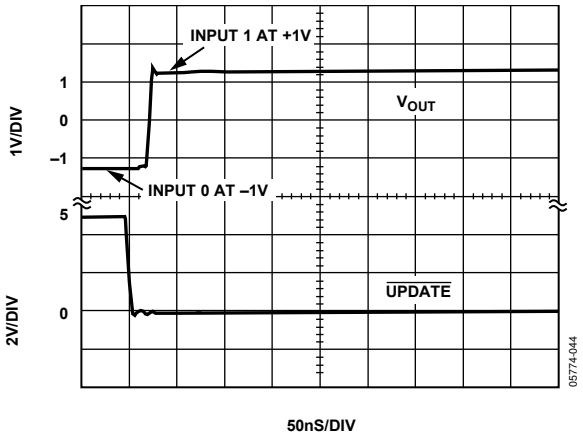

Figure 43. AD8107 Switching Time

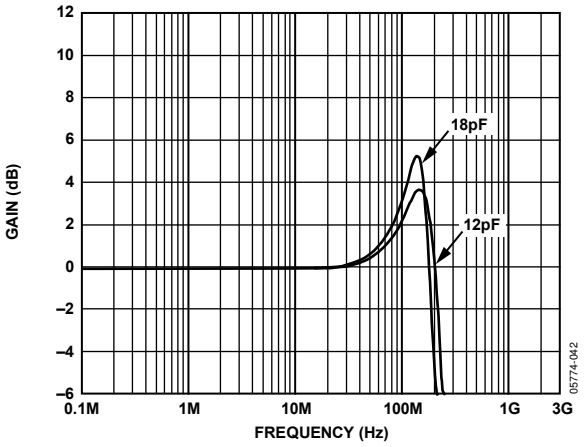

Figure 41. AD8107 Frequency Response vs. Capacitive Load

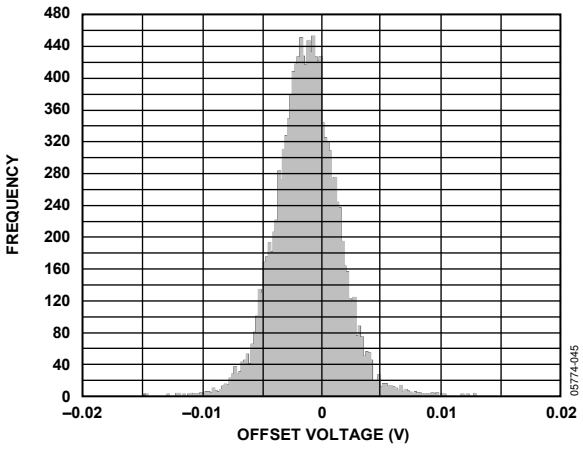

Figure 44. AD8107 Offset Voltage Distribution (RTI)

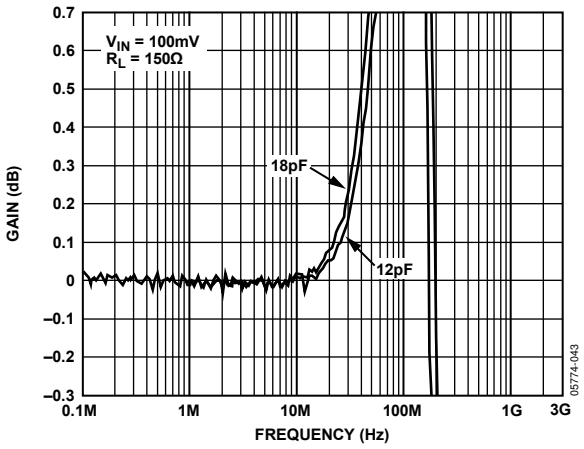

Figure 42. AD8107 Flatness vs. Capacitive Load

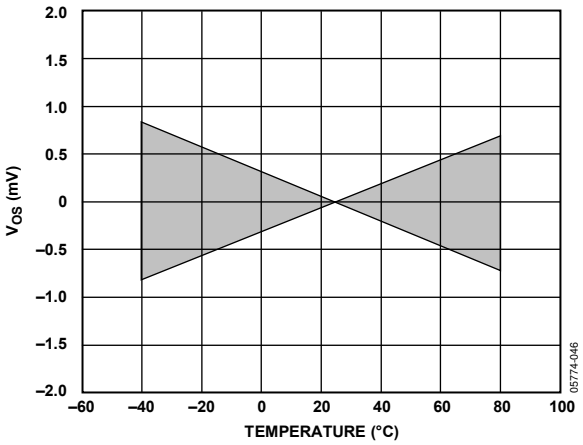

Figure 45. AD8107 Offset Voltage Drift vs. Temperature (Normalized at 25°C)

THEORY OF OPERATION

The AD8106 (G = 1) and AD8107 (G = 2) share a common core architecture consisting of an array of 80 transconductance (gm) input stages that are organized as five 16:1 multiplexers with a common, 16-line analog input bus. Each multiplexer is essentially a folded-cascode high speed voltage, feedback amplifier with 16 input stages. The input stages are NPN differential pairs whose differential current outputs are combined at the output stage, which contains the high impedance node, compensation, and a complementary emitter follower output buffer. In the AD8106, the output of each multiplexer is fed directly back to the inverting inputs of its 16 gm stages. In the AD8107, the feedback network is a voltage divider consisting of two equal-value resistors.

This switched-gm architecture results in a low power crosspoint switch that is able to directly drive a back-terminated video load (150 Ω) with low distortion (differential gain and differential phase errors are better than 0.02% and 0.02°, respectively). This design also achieves high input resistance and low input capacitance without the signal degradation and power dissipation of additional input buffers. However, the small input bias current at any input increases almost linearly with the number of outputs programmed to that input.

The output disable feature of these crosspoints allows larger switch matrices to be built simply by busing together the outputs of multiple 16 × 5 ICs. However, while the disabled output impedance of the AD8106 is very high (10 MΩ), the AD8107 output impedance is limited by the resistive feedback network, which has a nominal total resistance of 1 kΩ and appears in parallel with the disabled output. If the outputs of multiple AD8107 devices are connected through separate back termination resistors, the loading lowers the effective back termination impedance of the overall matrix because of these finite output impedances. This problem is eliminated if the outputs of multiple AD8107 devices are connected directly and share a single back-termination resistor for each output of the overall matrix. This configuration increases the capacitive loading of the disabled AD8107 on the output of the enabled AD8107.

POWER-ON RESET

When powering up the AD8106/AD8107, it is usually necessary to have the outputs be in the disabled state. The $\overline{\text{RESET}}$ pin, when taken low, causes all outputs to be in the disabled state.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to DVDD that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds $\overline{\text{RESET}}$ low for some time while the rest of the device stabilizes. The low condition causes all the outputs to disable. The capacitor then charges through the pull-up resistor to the high state, allowing full programming capability of the device.

INITIALIZATION

The AD8106/AD8107 should be initialized after power up to control the supply and bias currents, and to make sure that no unexpected program states are encountered. Initialization is performed by writing a data word of 00000 into all address locations 00 to 07 (000 to 111 binary).

GAIN SELECTION

The 16 × 5 crosspoints come in two versions depending on the desired gain of the analog circuit paths. The AD8106 device is unity gain and can be used for analog logic switching and other applications where unity gain is desired. The AD8106 can also be used for the input and interior sections of larger crosspoint arrays where termination of output signals is not usually used. The AD8106 outputs have very high impedance when their outputs are disabled.

For devices that drive a terminated cable with its outputs, the AD8107 can be used. This device has a built-in gain of two that eliminates the need for a gain-of-two buffer to drive a video line. Because of the presence of the feedback network in these devices, the disabled output impedance is about 1 kΩ.

CREATING LARGER CROSSPOINT ARRAYS

The AD8106/AD8107 are high density building blocks that create crosspoint arrays for dimensions larger than 16 × 5. Various features such as output disable, chip enable, and gain-of-one and gain-of-two options are useful for creating larger arrays. For very large arrays, they can be used with the AD8114/AD8115, 16 × 16 video crosspoint devices, or the AD8110/AD8111, 16 x 8 video crosspoint devices. When required for customizing a crosspoint array size, the parts can also be used with the AD8108 and AD8109, a pair (unity gain and gain-of-two) of 8 × 8 video crosspoint switches.

The first consideration in constructing a larger crosspoint is to determine the minimum number of required devices. The 16 × 5 architecture of the AD8106/AD8107 contains 80 points. For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other output.

Some nonblocking crosspoint architectures require more than this minimum as calculated above. In addition, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to wire-OR the outputs together in a vertical direction.

Figure 46 illustrates this concept for a 32 × 5 crosspoint array.

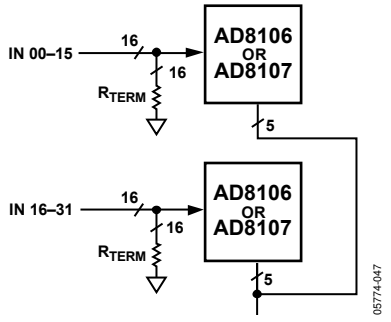

Figure 46. A 32 × 5 Crosspoint Array Using Two AD8106 or AD8107 Devices

The inputs are uniquely assigned to each of the 32 inputs of the two devices and terminated appropriately. The outputs are wire-OR'ed together in pairs. The output from only one of a wire-OR'ed pair should be enabled at any given time. The device programming software must be properly written to cause this to happen.

At some point, the number of outputs that are wire-OR'ed becomes too great to maintain system performance. This varies according to which system specifications are most important. It also depends on whether the matrix consists of AD8106 devices or AD8107 devices. The output disabled impedance of the AD8106 is much higher than that of the AD8107. As a result, its disabled parasitics have a smaller effect on the one output that is enabled. For example, a 128 × 5 crosspoint can be created with eight AD8106 devices or AD8107 devices. This design has 128 separate inputs and the corresponding outputs of each device wire-OR'ed together in groups of eight.

Using additional crosspoint devices in the design can lower the number of outputs that must be wire-OR'ed together. Figure 47 shows a block diagram of a system using eight AD8106 devices and two AD8107 devices to create a nonblocking, gain-of-two, 128 × 5 crosspoint that restricts the wire-OR'ing at the output to only four outputs.

Additionally, by using the lower four outputs from each of the two Rank 2 AD8107 devices, a blocking 128 × 10 crosspoint array can be realized. There are, however, some drawbacks to this technique. The offset voltages of the various cascaded devices accumulate and the bandwidth limitations of the devices compound. The extra devices also consume more current and take up more board space. Once again, the overall system design specifications determine which tradeoffs should be made.

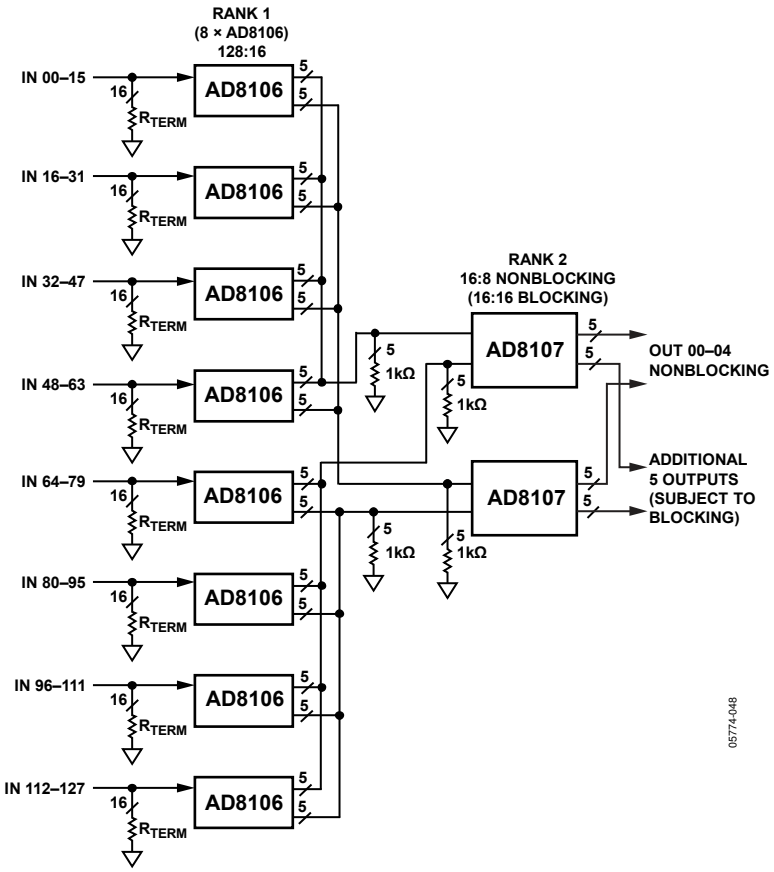

Figure 47. A Gain-of-Two 128 × 5 Nonblocking Crosspoint Array (128 × 10 Blocking)

CROSSTALK

Many systems, such as broadcast video, handle numerous analog signal channels that have strict requirements for keeping the various signals from influencing others in the system. Crosstalk is the term used to describe the undesired coupling between signals of other nearby channels to a given channel.

When many signals are in close proximity in a system, as is undoubtedly the case in a system that uses the AD8106/AD8107, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and its associated terms is required to specify a system that uses one or more AD8106/AD8107 devices.

Types of Crosstalk

Crosstalk can be propagated by means of one of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (free space, for example), couples with the receiver, and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing into conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these channels are crosstalk signals. The channels that crosstalk have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows into one of these paths, a voltage develops across the impedance and becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions when driving additional circuits in parallel in a given configuration can actually reduce the crosstalk.

Areas of Crosstalk

A practical AD8106/AD8107 circuit must be mounted to some sort of circuit board to connect to the power supplies and the measurement equipment. Take great care to create a board that adds minimum crosstalk to the intrinsic device. Note that the crosstalk of a system is a combination of the intrinsic crosstalk of the device and the circuit board to which it is mounted. It is important to try to separate these two areas of crosstalk when attempting to minimize its effect.

In addition, crosstalk can occur among the inputs to a crosspoint as well as among the outputs. It can also occur from input to output. Refer to the Input and Output Crosstalk section for techniques to diagnose which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20 \log_{10} \left(Asel(s) / Atest(s) \right) \quad (1)$$

where:
$s = jw$ is the Laplace transform variable.
Asel(s) is the amplitude of the crosstalk-induced signal in the selected channel.
Atest(s) is the amplitude of the test signal.

It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). The crosstalk signal also has a phase relative to its associated test signal.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 16 x 5 matrix of the AD8106/AD8107, examine the number of crosstalk terms that can be considered for a single channel, such as the IN00 input. IN00 is programmed to connect to one of the AD8106/AD8107 outputs where the measurement can be made.

First, measure the crosstalk terms associated with driving a test signal into each of the other 15 inputs one at a time. Then measure the crosstalk terms associated with driving a parallel test signal into all 15 other inputs taken two at a time in all possible combinations; and then three at a time, and so on, until finally, there is only one way to drive a test signal into all 15 other inputs.

Each of these cases is legitimately different from the others and could yield a unique value depending on the resolution of the measurement system. However, it is impractical to measure all of these terms and then to specify them. In addition, this describes the crosstalk matrix for only one input channel. A similar crosstalk matrix can be proposed for every other input. If the possible combinations and permutations for connecting inputs to the other outputs (not used for measurement) are taken into consideration, the numbers grow rather quickly to astronomical proportions. If a larger crosspoint array of multiple AD8106/AD8107 devices is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk, which means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one of the nearest neighbors or by two of the nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, so they can serve as a worst-case measure for any other one-channel or two-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the AD8106/AD8107 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. For example, a given input channel, such as IN07 in the middle, can be programmed to drive OUT01. The input to IN07 is terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier) with all other outputs disabled, except OUT01. Because grounded IN07 is programmed to drive OUT01, no signal should be present. If any signal is present, it can be attributed to the other 15 hostile input signals because no other outputs are driven; that is, they are all disabled. Thus, this method measures the all-hostile input contribution to crosstalk into IN07. This method can also be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel (IN00, for example) is driven and all outputs other than a given output are programmed to connect to IN00. OUT01 is programmed to connect to IN15, which is far away from IN00, and is terminated to ground. As a result, OUT01 should not have a signal present because it is listening for a quiet input. Any signal measured at the OUT01 can be attributed to the output crosstalk of the other seven hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the printed circuit board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10}((R_S C_M) \times s) \quad (2)$$

where:
R_S is the source resistance.
C_M is the mutual capacitance between the test signal circuit and the selected circuit.
s is the Laplace transform variable.

Equation 2 shows that this crosstalk mechanism has a high-pass nature; it can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8106/AD8107 are specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk is higher than the minimum obtainable because of the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8106/AD8107.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drive a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10} \left(Mxy \times s / R_L \right) \quad (3)$$

where:
Mxy is the mutual inductance of output *x* to output *y*.
R_L is the load resistance on the measured output.

This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

PCB LAYOUT

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the AD8106/AD8107 is designed to help keep the crosstalk to a minimum. Each input is separated from other inputs by an analog ground pin. All of these AGNDs should be connected directly to the ground plane of the circuit board. These ground pins provide shielding, low impedance return paths, and physical separation for the inputs. All of these help to reduce crosstalk.

Each output is separated from its two neighboring outputs by an analog ground pin and an analog supply pin of one polarity or the other. Each of these analog supply pins provides power to the output stages for only the two nearest outputs. These supply pins and analog grounds provide shielding, physical separation, and a low impedance supply for the outputs. Individual bypassing of these supply pins with a 0.01 µF chip capacitor directly to the ground plane minimizes high frequency output crosstalk via the mechanism of sharing common impedances.

Each output also has an on-chip compensation capacitor that is individually tied to the nearby analog ground pins AGND00 through AGND03. This technique reduces crosstalk by preventing the currents that flow in these paths from sharing a common impedance on the IC and in the package pins. These AGNDxx signals should all be connected directly to the ground plane.

The input and output signals have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The only place the input and output signals surface is at the input termination resistors and the output series back termination resistors. These signals should also be separated, to the largest extent possible, as soon as they emerge from the IC package.

OUTLINE DIMENSIONS

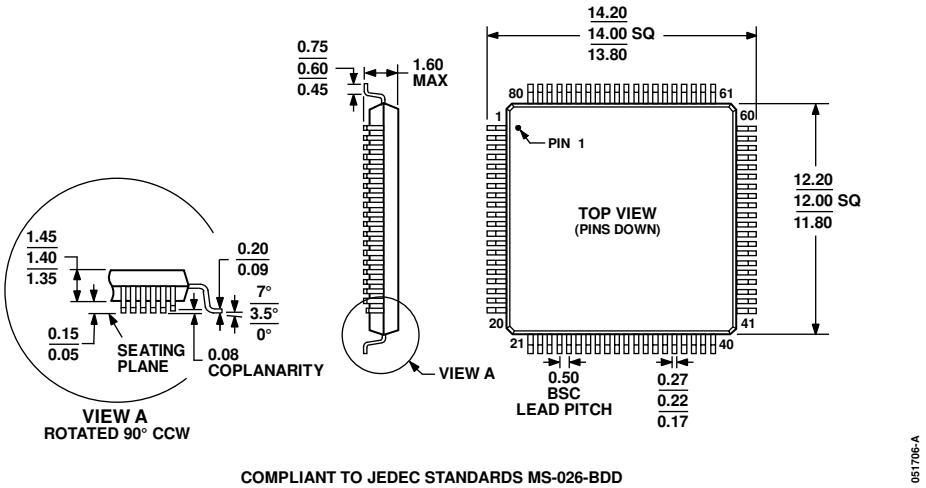

Figure 48. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8106ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1
AD8107ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1

[1] Z = RoHS Compliant Part.

NOTES