Available at Digi-Key www.digikey.com



Aurora, Illinois 60505 Phone: 630-851-4722 Email: sales@conwin.com www.conwin.com

Precision 5.0x 3.2mm TCXO Model D53G

Description:

The Connor-Winfield D53G is a 3.3V Clipped Sinewave, Surface Mount, Temperature Compensated Crystal Oscillator (TCXO) designed for applications requiring tight frequency stability. The RoHS compliant surface mount package is designed for high-density mounting and is optimum for mass production.





Features:

- 3.3 Vdc Operation
- Clipped Sinewave Output
- Frequency Stability: ±0.50 ppm
- Temperature Range: -30 to 85°C
- Low Jitter <1ps RMS
- 5.0x3.2mm SMT Package
- Tape and Reel Packaging

Absolute Maximum Ratings					
Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	85	°C	
Supply Voltage (Vcc)	-0.5	-	Vcc+0.5	Vdc	

Operating Specifications

		5 1			
Parameter	Minimum	Nominal	Maximum	Units	Notes
Center Frequency (Fo)	-	20.0 or 26.0	-	MHz	
Freq. Stability vs. Cal. @ 25℃	-1.0	-	1.0	ppm	1
Freq. Stability vs. Temp.	-0.50	-	0.50	ppm	2
Freq. Stability vs. Voltage	-0.25	-	0.25	ppm	±5%
Freq. Stability vs. Load	-0.25	-	0.25	ppm	±5%
Static Temperature Hysteresis	-	-	0.40	ppm	3
Freq. Shift after Reflow Soldering	-1.0	-	1.0	ppm	4
Aging	-1.0	-	1.0	ppm/year	
Operating Temperature Range:	-30	-	85	°C	
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	±5%
Supply Current (Icc)	-	-	2	mA	
Period Jitter	-	3	5	ps rms	
Integrated Phase Jitter	-	0.5	1.0	ps rms	5
SSB Phase Noise Fo =20 MHz					
10Hz offset	-	-98	-	dBc/Hz	
100Hz offset	-	-122	-	dBc/Hz	
1KHz offset	-	-143	-	dBc/Hz	
10KHz offset	-	-154	-	dBc/Hz	
100KHz offset	-	-156	-	dBc/Hz	
Start-up Time	-	-	5	ms	

Clipped Sinewave Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Output Voltage	1.0	-	-	V pk-pk	6
Load Resistance	-	10K	-	Ohm	
Load Capacitance	-	10	-	рF	7

Package Characteristics coalod co - al ca

Package	Hermetically sealed ceramic package and metal cover	
Environmental Characteristics		
Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A	
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.	
Soldering Process;	RoHS compliant lead free. See soldering profile on page 2.	

Ordering Information

D53G-020.0M, D53G-026.0M

1. Frequency Calibration; frequency measured at Vcc = 3.3 Vdc, 25°C, referenced to Fo.

2. Frequency stability vs. change in temperature. [±(Fmax - Fmin)/2.Fo].

3. Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C.

4. Within two hours after reflow soldering

5. BW=12K Hz to 20 MHz.

6. Output is DC coupled

7. For best performance it is recommended that the circuit connected to this output should have an equivalent input capacitance of 10 pF.



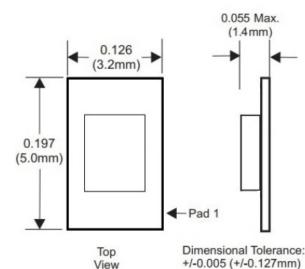
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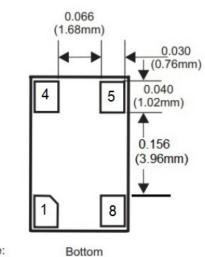
Notes:



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Package Layout





View

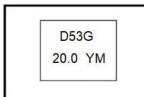
* <u>Keep Out Area</u>: Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.

Suggested Pad Layout

Pad Connections

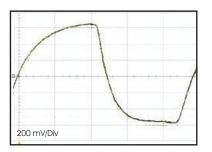
1:	N/C
4:	Ground
5:	Output
8:	Supply Voltage (Vcc)

Marking Information



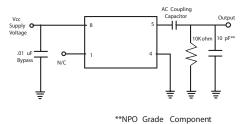
Two Character Date Code M = Month<u>Y = Year</u> 2 = 2022 A = Jan 3 = 2023 B = Feb 4 = 2024 C = March D = April 5 = 2025 6 = 2026 E = May 7 = 2 8 = 2 9 = 20 = 2

Output Waveform

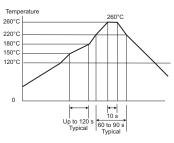


2027	F = June	
2028	G - July	
2029	H = Aug	
2030	J = Sept	
	K = Oct	
	M = Nov	
	N = Dec	

Test Circuit



Solder Profile



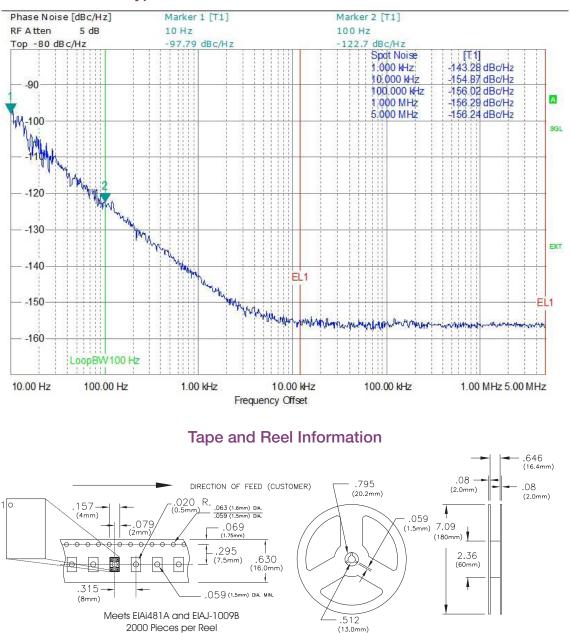
Meets IPC/JEDEC J-STD-020C

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Typical Phase Noise Plot for D53G-020.0M

Revision History

Revision	Revision Date	Note
01	11/14/08	New release GD 11/14/08
02	01/03/11	Updated to new data sheet format
03	11/16/12	Updated Phase noise information.
04	06/24/15	Added Marking Information
05	10/11/22	Updated package drawings and phase noise, removed "-T" part # option

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