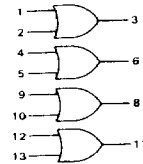
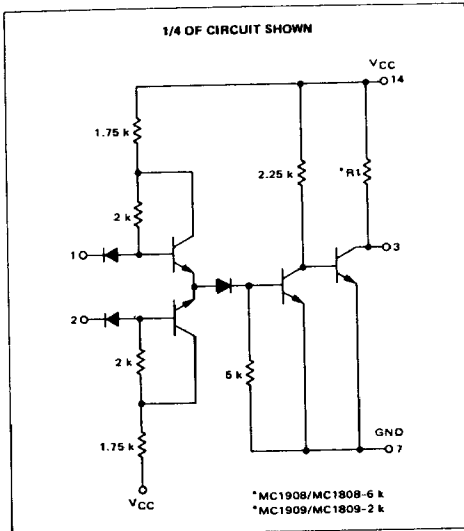


MDTL MC930/830 series

QUAD 2-INPUT "OR" GATE

MC1908F • MC1808F,P  
MC1909F • MC1809F,P

This device consists of four 2-input gates, each performing the logical OR function. Added logic flexibility provided by this device helps to optimize system designs.



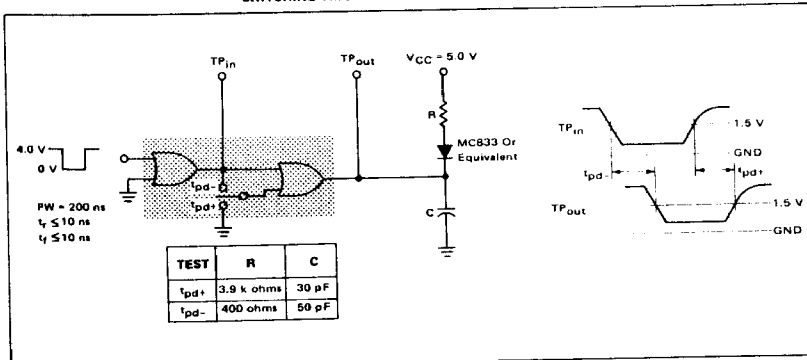
Positive Logic: 3 = 1 + 2  
Negative Logic: 3 = 1 • 2

Input Loading Factor = 1  
Output Loading Factor = 1  
MC1908, MC1808 = 8  
MC1909, MC1809 = 7  
Total Power Dissipation

	MC1908 MC1808	MC1909 MC1809
Inputs Low	95 mW	130 mW
Inputs High	100 mW	100 mW
50% Duty Cycle	97 mW	115 mW

Propagation Delay Time  
MC1908/MC1808 = 35 ns typ  
MC1909/MC1809 = 30 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





## PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

**Table 1** DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D

