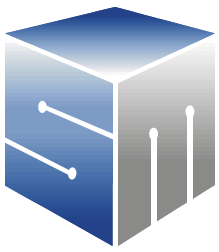

Silicon Motion, Inc.

Mobile Computer Display Controller

Version 1.0

Last Updated 05/24/06

Lynx3DM+ Databook

Silicon Motion®, Inc.

Lynx3DM+ DataBook

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Version Number	Date	Note
0.1	1/23/01	• Changed External Display Memory Interface & Video Port Interface in Figure 4 on page 5-2 • Updated in conformance to the Addendum 0.5. Changed FPR33[6] to be Hitachi 24-bit TFT only
0.2	1/30/01	• General revision based on Engineering inputs and verification results.
0.3	2/8/01	• Changed Power-on Configuration Register bits [27, 25, 24, 2, 1, 0] to reserved • Deleted Flat Panel Interface Pins [FPDATA35-FPDATA24] • Added definition to register CRT36 bit 2. • Changed register MCR62 bit [3:0] to reserved • Changed tables in Electrical Specifications chapter to TBD
0.4	5/1/01	• Added Ordering Information table • Added Appendix H • Revised Pin List • Changed Block Diagram
0.5	5/30/01	• Added DC operating voltages to Electrical Specification chapter
0.6	6/29/01	• Changed pin J9 from MVDD to VSS
0.7	8/15/01	• Changed Electrical Specification chapter
0.8	5/21/02	• Changed Memory Mapped Address Diagram • Changed Table 9 - ZV Port (Input mode) column
1.0	5/24/06	• Removed page 28-2 (Ordering information)

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Chapter 1: Overview

The Lynx3DM+ is a power managed, desktop equivalent display controller for notebook PCs. This device delivers full featured 3D, a unique memory architecture designed to enhance 3D/2D performance, enhanced multi-display capabilities, and Motion Compensation for DVD.

The Lynx3DM+ incorporates an IEEE Floating Point Setup engine as well as a full featured 3D rendering engine. The setup engine is designed to balance with the triangle delivery capabilities of high end notebook processors. The rendering engine supports key features such as Mip Mapping, Alpha Blend, Anti-Aliasing, Specular Highlights and Fog.

The Lynx3DM+ integrates 4MB, 8MB or 16MB of video memory. This allows up to a 64-bit memory interface and over 1.0GB/s of memory bandwidth.

Lynx3DM+ continues to support all the Dual Application/Dual View capabilities of its predecessor, LynxE. In addition, Lynx3DM+ can drive two independent digital displays, as well as simultaneously drive LCD, CRT and TV displays (multiview). Support for all of these features is provided under Windows 95, Windows 98, Windows Me, Windows NT 4.0, and Windows 2000.

A robust 128-bit Drawing Engine provides no compromise 2D performance. The Drawing Engine supports 3 ROPs, BitBLT, transparent BLT, pattern BLT, color expansion, and line draw. The Host Interface Unit allows support for AGP and PCI. Support for all ACPI power states is provided. A high quality TV encoder, VGA Core, LCD Backend Controller and 200 MHz RAMDAC are incorporated as well.

The Lynx3DM+'s Motion Compensation block, Video Processor block, and Video Capture Unit provide superior video quality for real-time video playback and capture. When combined with high end notebook CPUs, the Motion Compensation block allows full frame playback of DVD video content without the need for additional hardware. The Video Processor supports multiple independent full screen, full motion video windows with overlay. Each motion video window uses hardware YUV-to-RGB conversion, scaling, and color interpolation. When combined with multi-view capabilities of the chip, these independent video streams can be output to each of two display devices and bilinear scaled to support applications such as full screen display of local and remote images for video conferencing.

Lynx3DM+ is designed with 0.25m, 2.5V CMOS process technology. A hierarchical layout approach provides enhanced internal timing control. In addition to built-in test modes and a signature analyzer, the Lynx3DM+ incorporates a 20 bit test bus which can be used to simultaneously monitor internal signals through the Zoom Video (ZV) Port Interface. The capability can be used to increase fault coverage, and to reduce silicon validation and debugging time. The Lynx3DM+ is available in a 316 pin BGA packages.

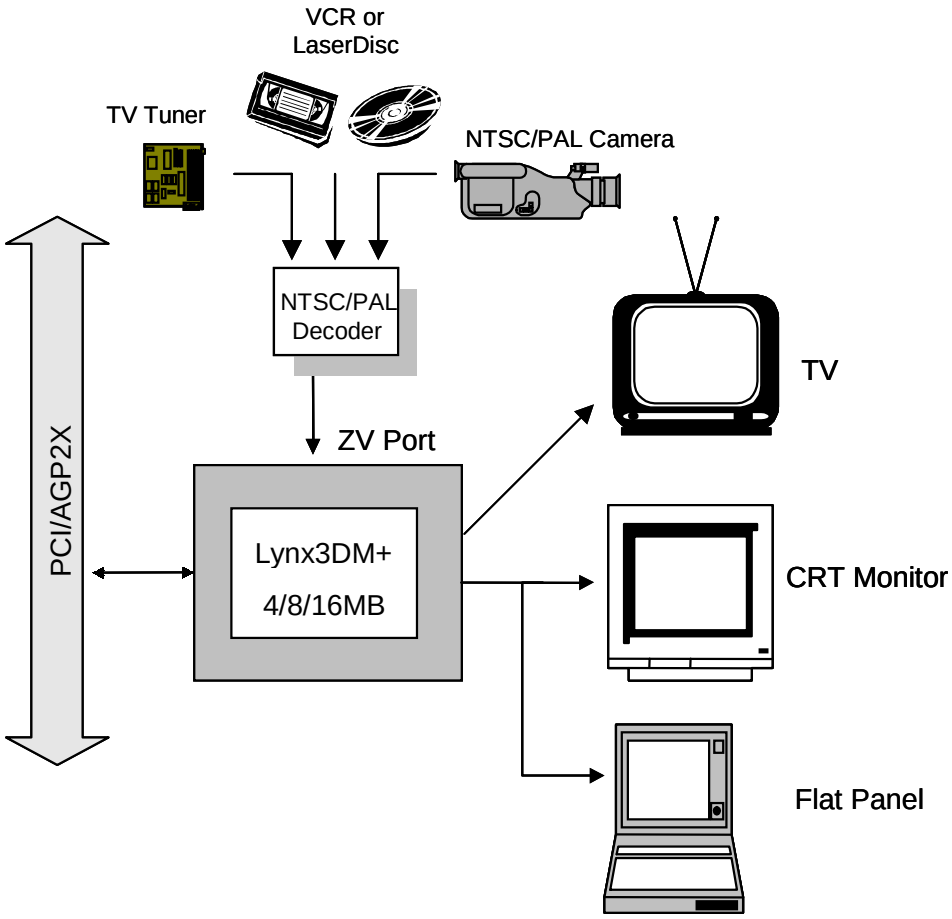


Figure 1: System Block Diagram for Lynx3DM+

Features	Benefits
High performance, power managed 3D	Desktop level 3D performance within the power budget of a notebook system
Motion Compensation	Allows full frame playback of DVD content in software
Multi-Display support under Microsoft Windows 95, Windows NT, Windows 98 and Windows Me with **one** device	• Applications available at the same time across multiple display devices • Single chip implementation ideal for mobile systems
SMI Dual View support under Microsoft Windows 95, Windows NT, Windows 98 and Windows Me	Any rectangular portion of primary display can be zoomed up for display on multiple secondary displays
Dual-Digital support	Independent display support for external digital LCD monitor or LCD projector
Adaptive Power Management • Dynamic functional block shut-down, clock control	• Reduce average power consumption when in operation mode
Multiple independent hardware video windows	• Independent full screen, motion video for separate displays. • Complete dual view support for video
128-bit, single clock cycle Drawing Engine	No compromise 2D graphics performance for mobile systems
High performance memory interface	Delivers over 1.0GB/s bandwidth to support 3D graphics, DVD
AGP 2X sideband and PCI 2.1 support	Provides interface capability for today's most popular PC graphics busses
DSTN and TFT panel support up to 1280x1024	Supports all panel requirements for mobile systems
Integrated TV Encoder with Macrovision	Graphics/video display on TV with no external support logic
Zoom Video Port	Provides support for camera, TV tuner input, or output to VCR
Hardware support for LCD landscape/portrait rotation	Portrait view for desktop publishing, word processing applications
PC2001 Compliant, ACPI Compliant	Meets WHQL certification requirements
SW support for Microsoft Windows 95, Microsoft Windows NT 4.0, Microsoft Windows 98, Windows Me, Windows 2000, and OS/2	Complete OS software support

Overview of Major System Blocks

The Lynx3DM+ consists of a logic block which interfaces to a 4MB, 8MB or 16MB block of integrated memory. The integrated memory supports single clock cycle transfers up to 100MHz. Peak memory bandwidth for the integrated 128-bit memory bus is over 1.6GB/s.

The logic within the Lynx3DM+ consists of 11 functional blocks: PCI Interface, Host Interface (HIF), Memory Controller, Drawing Engine, Power Down Control Unit, Video Processor, Video Capture Module, LCD Backend Controller, VGA Core, PLL Module, and RAMDAC. A summary of each of the functional blocks, along with important features follows:

AGP/PCI Interface and HIF

Lynx3DM+'s PCI Host Interface Unit supports burst read, burst write, and bus master mode with DMA. The Host Interface Unit decodes I/O read, I/O write, memory read, memory write, memory mapped access, 2D/3D Drawing Engine access, VGA access, and others. The unit also supports Little-Endian and Big-Endian format, and 8-bit ROM decode for on board video BIOS ROM. A dual aperture feature is designed to support VGA modes and non-VGA modes. In addition, a special VGA aperture function is added to allow 64-bit memory access in VGA modes.

Lynx3DM+ has an internal HIF (Host Interface) bus which is designed to transfer data between PCI Host Interface Unit and other functional blocks. The PCI Host Interface Unit controls the HIF bus protocol to effectively deliver PCI I/O and memory cycles to each functional block.

Lynx3DM+ supports 2X with sideband Accelerated Graphics Port (AGP). The AGP interface provides a high bandwidth, low latency connection to the system memory; therefore, it can increase the graphics performance for 2D and 3D applications.

Key Feature Summary:

- AGP 2X sideband support
- 33 MHz PCI Master/Slave interface
- PCI 2.1 compliant
- Dual aperture feature for concurrent VGA and video/drawing engine access

Memory Controller

Independent control is provided for the 4/8/16MB block of integrated memory. Page Break Look Ahead support assures a memory cycle is not broken if there is a change of memory bus agent within the same memory page. Programmable memory arbitration allows memory interface usage to be fully optimized - priority and round robin arbitration is supported. The block write function for SGRAM is supported.

Key Feature Summary:

- Independent memory interface control
- Up to 64-bit memory interface
- Over 1.0GB/s memory bandwidth

Drawing Engine

The Lynx3DM+'s 128-bit Drawing Engine is designed to accelerate 2D and 3D through APIs such as Direct Draw and Direct3D. The engine pipeline runs at a single clock per cycle at speeds of 100MHz+. The engine supports key GUI functions such as 3 operand ALU with 256 raster operations, pattern BLT, color expansion, trapezoid fill, and line draw. Direct3D rendering acceleration is provided by support for features such as arithmetic stretching, source transparent BLT, and double buffering.

Key Feature Summary:

- 100MHz single clock/cycle engine
- Designed to accelerate DirectDraw and Direct3D

3D Engine

The Lynx3DM+ incorporates an IEEE Floating Point Setup engine as well as a full featured 3D rendering engine. The diagram below illustrates a top level diagram of the Lynx3DM+ setup and rendering pipeline.

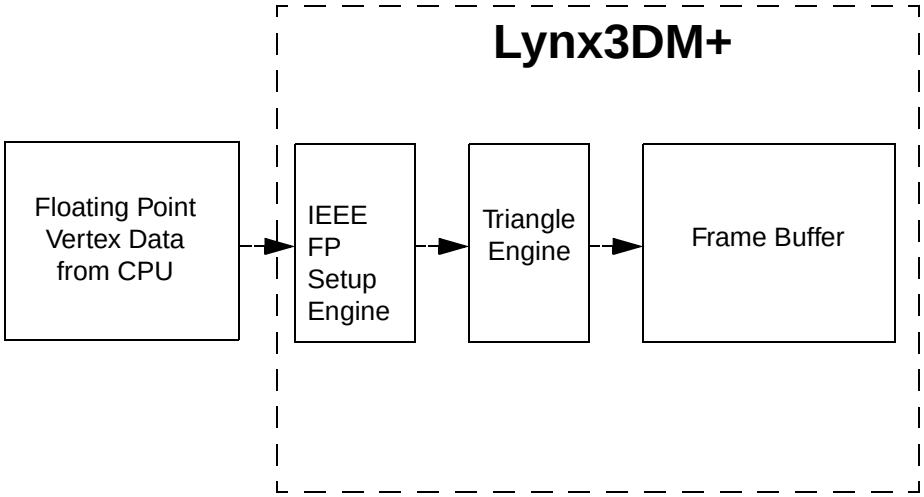


Figure 2: Top Level 3D Flow Diagram

The setup engine is designed to balance with the triangle delivery capabilities of high-end notebook processors. The setup engine performs single precision floating point operations to calculate slope parameters (x, y, z; color - RGB, alpha; texture - s, t, perspective) from the triangle vertex data delivered from the CPU. The slope information is derived with sub-pixel accuracy to eliminate misalignment. The rendering engine utilizes the slope information to render the defined triangle to the screen. The rendering engine supports a full set of 3D rendering features. A representative list of features is provided in the Key Feature Summary below.

Key Feature Summary:

- IEEE Floating Point Setup Engine
- Complete 3D Rendering Engine set:
  - Bi-linear and tri-linear filtering
  - Mip Mapping
  - Vertex and global fog
  - Source and destination alpha blend
  - Specular highlights
  - Edge anti-aliasing
  - Z-buffering
  - Gouraud shading
  - Mirrored textures
  - Texture decompression

Motion Compensation Engine

The Motion Compensation Engine offloads the motion compensation portion of the MPEG-2 decode process. This block can reduce CPU overhead requirements for MPEG-2 decode by 20%-40%, depending on CPU type and MPEG-2 data rate. To insure proper handling of MPEG-2 video data streams, the Lynx3DM+ implements a separate bus master control mechanism for motion compensation command and IDCT data. This approach allows for a dedicated pipeline through

which the motion compensation command and IDCT data can be transferred to the Motion Compensation Engine for processing.

The motion compensation block provides full sub-picture support as well. Both 2-bit/pixel formats and 8-bit/pixel formats (4-bit color data, 4-bit alpha data) are supported.

Key Feature Summary:

- Offloads motion compensation portion of MPEG-2 decode process from CPU
- Separate bus master control for motion compensation command and IDCT data
- Sub-picture support
  - 2-bit/pixel format
  - 8-bit/pixel format

Digital TV-Encoder

The TV Encoder is an NTSC/PAL Composite Video/S-video Encoder. It receives RGB inputs and converts to digital video signals based on CCIR 624 format.

The input video signal of the TV Encoder is RGB 8 bit each. The sampling rate is corresponding to CCIR 601, Square pixel and 4Fsc.

The output video signals of the TV Encoder are Composite Video signal and S-video signals of 10-bit each. These output signals are over-sampled by a double frequency clock called CLKX2. This feature helps for simplify external analog filtering.

The TV Encoder video timing is controlled by vertical sync and the horizontal sync input signals. The blank signal input is optional. If the blank signal input signal is pulled up, internal blanking control will be performed.

Macrovision 7.1.21 and closed captioning functions are included.

Key Feature Summary:

- NTSC/PAL interlace mode digital video encoder
- Composite Video and S-Video digital output
- CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- Interlace mode operation
- 2x over-sampling data output to simplify external analog filtering
- Macrovision function (version 7.1.21)
- Closed captioning function

Power Down Control Unit

The Power Down Control unit provides Dynamic Power Management for all functional blocks within the Lynx3DM+. Dynamic Power Management is made possible by individual clocking control to each of the functional blocks within Lynx3DM+. Each clock to a given functional block is skew matched to maintain synchronization between blocks. The functional blocks can then be turned on/off "on the fly" as needed. Power savings under fully operational conditions is maximized, yet the process completely transparent to the user.

Control for Virtual Refresh is provided through the Power Down Control unit as well. Through Virtual Refresh, LCD panel timing may be driven from a fully independent PLL. VCLK can be significantly reduced, while retaining full graphics performance. The result is significant power savings for LCD only configurations.

Finally, the Power Down Control unit generates power down sequencing for Standby and Suspend modes. Internal auto-standby and system standby implementations are supported.

Under sleep mode, options for memory refresh type and use of internal PLL/external clock for memory refresh clock are provided. Activity detection is supported for resuming from Standby or Suspend modes.

Key Feature Summary:

- Dynamic Power Management
- Virtual Refresh
- Standby and Suspend model support
- ACPI, DPMS, APM compliant

Video Processor

The Video Processor module manages video playback to an LCD, CRT, or TV display. Independent video sources can be scaled up and displayed full screen different display devices - ideal for videoconferencing applications. The Video Processor module supports, bi-linear scaling, YUV to RGB color space conversion, color key, and overlay of graphics over video. The Video Processor module also supports flicker reduction and adjustable overscan/underscan for TV display.

Key Feature Summary:

- Multiple video windows in HW
- Independent video sources on different displays
- Bi-linear scaling
- Flicker filter and underscan for TV display

Video Capture

The Video Capture module processes incoming video data from the Zoom Video Port and sends the data to the local video frame buffer. From there, the data may be displayed, as well as bus mastered out for storage on a hard drive. Incoming data from the Zoom Video port can be interlaced or non-interlace and in YUV or RGB format. The data can be cropped, horizontally filtered (2,3,or 4-tap), and shrunk to ¼ size. Single buffer as well as double buffer capture is supported.

Key Feature Summary:

- Support for Zoom Video Port interface
- Crop, filter, shrink support

LCD Backend Controller

The LCD Backend Controller module manages data flow and generates timing to the selected LCD display. The module provides support for 9, 12, 18, 24 bit TFT and DSTN panels up to SXGA+ resolution. The backend controller contains a color encoder, dithering engines for TFT and DSTN panels, frame accelerator, and a Virtual Refresh timing generation block. Each of the blocks within the LCD Backend controller module can be powered down if not in use.

Key Feature Summary:

- TFT and DSTN support up to SXGA+
- Timing generation for Virtual Refresh

Popup Icon

The Lynx3DM+ support 64x64 popup icon which can be zoomed up by 2 to become 128x128 popup icon. The popup icon can be programmed to anywhere on the screen display. In addition, the popup icon has transparency support.

Key Feature Summary:

- Popup icon location flexible
- Transparency color support

VGA Core

The Lynx3DM+ has a high performance 32-bit VGA core which is 100% IBM VGA compatible. In addition to standard VGA functions, the Lynx3DM+'s VGA core module generates LCD timing, performs LCD screen autocentering and expansion, generates TV timing, and provides Hardware Cursor control.

Key Feature Summary:

- 100% IBM VGA compatible

PLL Module

The PLL module provides three separate PLLs for MCLK, VCLK, and Virtual Refresh clock to drive LCD panel timing. A 14.318MHz base clock is used to drive TV timing. This allows for completely independent timing for LCD/CRT or LCD/TV under dual application or dual view. For instance, the LCD panel can be driven at 60Hz while CRT refresh is 85Hz.

Key Feature Summary:

- Separate PLL for LCD panel timing

RAMDAC

The integrated RAMDAC supports pixel clock frequencies up to 200MHz. Anti-sparkle logic is provided for read/writes to the palette. An internal band gap voltage reference saves need for external RC components.

Key Feature Summary:

- 200MHz speed provides support for popular LCD panels.

Table 1: Lynx3DM+ (4MB): Display Support Modes

CRT Only				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
	75	x	x	x
	85	x	x	x
800x600	60	x	x	x
	75	x	x	x
	85	x	x	x
1024x768	60	x	x	x
	75	x	x	x
	85	x	x	x
1280x1024	60	x	x	x
	75	x	x	-
	85	x	x	-

LCD/Simultaneous Mode				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
800x600	60	x	x	x
1024x768	60	x	x	x
1280x1024	60	x	x	x

Dual Display Mode				
Display 1 (D1)	**Display 2 (D2)**	**Color Depth (Max Color Depth Display 2 bpp)**		
		when D1 is 8 bpp	**when D1 is 16 bpp**	**when D1[1] is 24 bpp**
640x480	640x480	24 (D2)	24 (D2)	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	16	16	-
800x600	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	16	16	-
1024x768	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	16	16	-

[1]Max color depth for display 1, 16bpp under dual display

Table 2: Lynx3DM+ (8MB): Display Support Modes

CRT Only				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
	75	x	x	x
	85	x	x	x
800x600	60	x	x	x
	75	x	x	x
	85	x	x	x
1024x768	60	x	x	x
	75	x	x	x
	85	x	x	x
1280x1024	60	x	x	x
	75	x	x	x
	85	x	x	x

LCD/Simultaneous Mode				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
800x600	60	x	x	x
1024x768	60	x	x	x
1280x1024	60	x	x	-

Dual Display Mode				
Display 1 (D1)	**Display 2 (D2)**	**Color Depth (Max Color Depth Display 2 bpp)**		
		when D1 is 8 bpp	**when D1 is 16 bpp**	**when D1[1] is 24 bpp**
640x480	640x480	24 (D2)	24 (D2)	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	24	24	-
800x600	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	24	24	-
1024x768	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	24	24	-

[1]Max color depth for display 1, 16bpp under dual display

Table 3: Lynx3DM+ (16MB): Display Support Modes

CRT Only				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
	75	x	x	x
	85	x	x	x
800x600	60	x	x	x
	75	x	x	x
	85	x	x	x
1024x768	60	x	x	x
	75	x	x	x
	85	x	x	x
1280x1024	60	x	x	x
	75	x	x	x
	85	x	x	x

LCD/Simultaneous Mode				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
800x600	60	x	x	x
1024x768	60	x	x	x
1280x1024	60	x	x	x

Dual Display Mode				
Display 1 (D1)	**Display 2 (D2)**	**Color Depth (Max Color Depth Display 2 bpp)**		
		when D1 is 8 bpp	**when D1 is 16 bpp**	**when D1[1] is 24 bpp**
640x480	640x480	24 (D2)	24 (D2)	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	24	24	-
800x600	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	24	24	-
1024x768	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
	1280x1024	24	24	-

[1]Max color depth for display 1, 16bpp under dual display

Chapter 2: Pins

The Lynx3DM+ is provided in a 316 BGA package.

Figure 3 illustrates the pinout diagram for the SM722/SM723 316 BGA package. Figure 55 illustrate the mechanical dimensions of the BGA package.

Lynx3DM+ Pin Descriptions

The following table, Table 4, provides brief description of each BGA ball of the Lynx3DM+. Signal names with ~ preceding are active "LOW" signals, whereas signal names without ~ preceding are active "HIGH" signals. Also, the following abbreviations are used for Pin Type.

Table 4 outlines the numerical SM722/723 BGA pins.

I - INPUT SIGNAL
O - Output Signal
I/O - Input or Output Signal
‘Note: All Outputs and I/O signals are tri-stated. Internal pull-up for I/O pad are all 100KΩ resistor. Internal pull-down for I/O pads are all 100KΩ resistors.

Table 4: Pin Description

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
Host Interface (PCI or AGP)					
AD [31:0]	I/O		TBD	120	Multiplexed Address and Data Bus. A bus transaction consists of an address cycle followed by one or more data cycles.
C/ ~BE [3:0]	I/O		TBD	120	Bus Command and Byte Enables. These signals carry the bus command during the address cycle and byte enable during data cycles.
PAR	I/O		TBD	120	Parity. Lynx3DM+ asserts this signal to verify even parity across AD [31:0] and C/~BE [3:0].
~FRAME	I/O		TBD	120	Cycle Frame. Lynx3DM+ asserts this signal to indicate the beginning and duration of a bus transaction. It is de-asserted during the final data cycle of a bus transaction.
~TRDY	I/O		TBD	120	Target Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~IRDY	I/O		TBD	120	Initiator Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~STOP	I/O		TBD	120	Stop. Lynx3DM+ asserts this signal to indicate that the current target is requesting the master to stop current transaction.
~DEVSEL	I/O		TBD	120	Device Select. Lynx3DM+ asserts this signal when it decodes its addresses as the target of the current transaction.
IDSEL	I				ID Select. This input is used during PCI configuration read/write cycles.
CLK	I				System Clock, 33MHz. for PCI and 66MHz for AGP
~RST	I				System Reset. Lynx3DM+ asserts this signal to force registers and state machines to initial default values
~REQ	O		TBD	120	Bus Request (bus master mode)
~GNT	I				Bus Grant (bus master mode)
~INTA	O		TBD	120	Interrupt
PME#	O		TBD	120	Power management event signals
~PIPE	O		TBD	120	Pipe signal. Initiates pipelined AGP request. Signal indicates beginning and duration of pipelined AGP access.
~RBF	O		TBD	120	Read Buffer Full. Indicates if graphics device can accept previously low priority read data
AD_STB[1:0]	I/O		TBD	120	Address strobes 1, 0 for 2X transfer support
ST[2:0]	I				Status bus for AGP support
SBA[7:0]	O		TBD	120	Sideband address bits 7-0
SB_STB	O		TBD	120	Sideband strobe
~AGP_BUSY	O		TBD	120	Power management signal for AGP bus.
~STP_AGP	I				Power management signal for AGP bus.
Power Down Interface					

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
~PDOWN	I	pull-up			Power down mode enable
~CLKRUN/ ACTIVITY	O	pull-up	TBD	60	~CLKRUN or Lynx3DM+ Memory and I/O activity detection depending on SCR18 [7] 0 = select ~CLKRUN 1 = select ACTIVITY
Clock Interface					
REFCLK	I	pull-up			32KHz refresh clock source for power down
PALCLK	I	pull-up			27MHz clock source for PAL TV
CKIN	I	pull-up			14.318MHz clock (~EXCKEN = 1) or Video Clock (~EXCKEN = 0)
MCKIN/ LVDSCLK	I/O	pull-up	TBD	60	Memory Clock In (~EXCKEN = 0) LVDSCLK Out (~EXCKEN = 1). LVDSCLK is a free running clock which can be used to drive LVDS transmitter for DSTN panels. Note: this pin is used as CLK2 for dual panel configuration. For this case configure as LVDSCLK.
~EXCKEN	I	pull-up		60	External Clock Enable. Select external VCLK from CKIN and MCLK from MCKIN.
External Display Memory Interface (for reference only)					
MA [10:0]	O	pull-down	TBD	50	External Memory Address Bus. The video memory row and column addresses are multiplexed on these lines.
MD [63:0]	I/O	MD [63:33] pull-down	TBD	20	
MD [63:0]	I/O	MD[32:0] pull-up	TBD	20	
~WE	O	pull-up	TBD	50	
~RAS	O	pull-up	TBD	50	
~CAS	O	pull-up	TBD	50	External SGRAM Column Address Select
~CS0	O	pull-up	TBD	50	External SGRAM Chip Select 0, select 1st 1MB within the 2MB memory, or select 1st 2MB within the 4MB memory
~DQM [7:0]	O	pull-up	TBD	50	External SGRAM I/O mask [7:0]. DQM [7:0] are byte specific. DQM0 masks MD [7:0], DQM1 masks MD [15:8],Ö,and DQM7 masks MD [63:58].
DSF	O	pull-up	TBD	50	External SGRAM Block write
BA[1:0]	O		TBD	50	External SGRAM Bank Select. SDRAM has 2/4 internal banks. Bank address defines to which bank the current command is being applied.
SDCK	I/O	pull-up	TBD	50	External SGRAM clock. SDCK is driven by the memory clock. All SDRAM input signals are sampled on the positive edge of SDCK.
SDCKEN	I/O	pull-up	TBD	50	External SGRAM clock enable. SDCKEN activates (HIGH) and deactivates (LOW) the SDCLK signal. Deactivating the SDCK provides POWER-DOWN and SELF-REFRESH mode. ~ROMEN
~ROMEN	O	pull-up	TBD	20	ROM Enable

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
Flat Panel Interface					
FDATA [23:0]	O	pull-down	TBD	50	Flat Panel Data Bit 23 to Bit 0 for single panel implementation.
LP/FHSYNC	O	pull-down	TBD	50	**DSTN LCD:** Line Pulse **TFT LCD:** LCD Horizontal Sync
FP/FVSYNC	O	pull-down	TBD	50	DSTN LCD: Frame Pulse TFT LCD: LCD vertical sync
M/DE	O	pull-down	TBD	50	M-signal or Display Enable. This signal is used to indicate the active horizontal display time. FPR3E [7] is used to select 1 = M-signal 0 = Display Enable
FPSCLK	O	pull-down	TBD	50	Flat Panel Shift Clock. This is the pixel clock for Flat Panel Data.
FPEN	O	pull-down	TBD	20	Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are supplied. This signal also needs to become inactive before any panel voltages or control signals are removed. FPEN is part of the VESA FPDI-1B specification.
FPVDDEN	O	pull-down	TBD	20	Flat Panel VDD Enable. This signal is used to control LCD logic power.
VBIASEN	O	pull-down	TBD	20	Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power.
LVDS Interface					
TX0+/-	O				LVDS Channel 1 Output
TX1+/-	O				LVDS Channel 2 Output
TX2+/-	O				LVDS Channel 3 Output
TX3+/-	O				LVDS Channel 4 Output
TXCLK+/-	O				LVDS Clock Output
CRT Interface					
RED	O				Analog Red Current Output
GREEN	O				Analog Green Current Output
BLUE	O				Analog Blue Current Output
IREF	I				Current Reference Input
CRTVSYNC	O	pull-up	TBD	50	CRT Vertical Sync
CRTHSYNC/ CSYNC	O	pull-up	TBD	50	CRT Horizontal Sync or Composite Sync depending on CCR65 [0] 0 = CRT Horizontal Sync 1 = Composite Sync
TV Interface					
Y	O				Luminance Output
C	O				Chrominance Output
CVBS	O				Composite Video Output
IREF2	I				Current Reference Input
Video Port Interface					

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
P [15:0]	I/O	pull-down	TBD	20	RGB or YUV input/ RGB digital output
PCLK	I/O	pull-up	TBD	20	Pixel Clock
VREF	I/O	pull-up	TBD	20	VSYNC input from PC Card or video decoder
HREF	I/O	pull-up	TBD	20	HSYNC input from PC Card or video decoder
BLANK	O	pull-up	TBD	20	Blank output 0 = BLANK output
General Purpose Registers / I²C					
USR3	I/O	pull-up	TBD	20	General Purpose I/O
USR2	I/O	pull-up	TBD	20	General Purpose I/O
USR1 / SDA	I/O	pull-up	TBD	20	General Purpose I/O. USR1/ DDC2/ I²C Data for CRT. Can be used to select different test modes.
USR0 / SCL	I/O	pull-up	TBD	20	General Purpose I/O. USR0/ DDC2/ I²C Clock for CRT. Can be used to select different test modes.
Test Mode Pins					
TEST [1:0]	I	pull-down			Test mode selects
VCC and GROUND Pins					
HVDD					Host Interface VDD on I/O Ring, 3.3V
MIVDD					Integrated Display Memory Interface VDD on I/O Ring, 3.3V (2.5V option)
MEVDD					External Display Memory Interface VDD on I/O ring, 3.3V (2.5V option)
FPVDD					Flat Panel Interface VDD on I/O Ring, 3.3V
VPVDD					VPort Interface VDD on I/O Ring 3.3V
PLLVDD					LVDS PLL Power Supply, 2.5V
PLLVSS					LVDS PLL Ground
LVDD					LVDS Power Supply, 2.5V
LVSS					LVDS Ground
CVDD					Clock (PLL) Analog Power, 2.5V
AVDD					DAC Analog Power, 3.3V
AVDD3					TVDAC Analog Power, 3.3V
RVDD					RAM Filtered Palette Power, 2.5V
CVSS					PLL Analog Ground
AVSS1					DAC Analog Ground
AVSS2					DAC Analog Ground
AVSS3					TVDAC Analog Ground
RVSS					RAM Filtered Palette Ground
VDD					Digital Core Power Supply, 2.5V
VCCA					Digital Memory Power Supply, 3.3V (2.5V option)

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
VSSA					Digital Internal Memory Ground
VSS					Digital Ground
Others					
RS[12:2]					Reserve pins
BA0					Memory Bank 0 select (Reserved)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	MD12	MD3	MD4	MD5	MD7	MD31	MD17	MD28	MD20	MD25	MD22	AD0	AD4	AD7	AD9	AD12	AD14	PAR	~FRAME	~BE2
B	MD2	MD0	MD11	MD9	MD8	~DQM3	MD30	MD18	MD27	MD21	MD24	AD1	AD5	~BE0	AD10	AD13	~BE1	~TRDY	~STOP	AD16
C	MD15	MD1	MD13	MD10	MD6	~DQM2	MD16	MD29	MD19	MD26	MD23	AD3	AD6	AD8	AD11	AD15	~DEVSEL	~IRDY	AD17	AD18
D	~CS0	~DQM1	MD14	VCCA	**VSS**	MVDD	**VSS**	MVDD	**VSS**	**VSS**	AD2	HVDD	**VSS**	HVDD	**VDD**	**VSS**	HVDD	AD19	AD20	AD21
E	~WE	BA	~DQM0	**VSS**	RBF#	BA0	RS2	AGP_BUSY#	STOP_AGP#	PIPE#	ST0	ST1	ST2	SBA7	SBA6	SBA5	**VSS**	AD22	AD23	IDSEL
F	MA5	~CAS	~RAS	MVDD	VCCA											SBA4	HVDD	~BE3	AD24	AD25
G	MA7	MA3	MA4	**VSS**	VSS											SBA3	**VDD**	AD26	AD27	AD28
H	MA1	MA8	MA2	MA6	MA10											SBA2	**VSS**	AD29	AD30	AD31
J	SDCKEN	SDCK	MA9	MA0	**VDD**											SBA1	HVDD	~REQ	~GNT	CLK
K	VCCA	~ROMEM	DSF	VCCA	PME#											SBA0	**VSS**	~RST	~INTA	REFCLK
L	MD55	MD56	MD54	VSS	VSS											SB_STB	MCKIN	~PDOWN	~CLKRUN	~EXCKEN
M	MD57	MD53	MD58	VCCA	RS3											VSS	PALCK	VREF	HREF	BLANK
N	MD52	MD59	MD51	**VSS**	RS4											AD_STB0	P4	P1	P0	PCLK
P	MD60	MD50	MD61	MVDD	VSS											AD_STB1	Y	P5	P3	P2
R	MD49	MD62	MD48	~DQM7	VCCA											LVDD	VPVDD	P8	P7	P6
T	MD63	~DQM6	MD39	**VSS**	FPVDD	VCCA	VSS	PLLVDD	tx3p	txclkp	txclkn	tx2n	tx1p	tx0p	tx0n	LVSS	C	P12	P10	P9
U	MD40	MD38	MD41	MD43	MVDD	RS12	FDA22	PLLVSS	FPVDD	tx3n	tx2p	FPVDD	tx1n	FPVDDEN	CVSS	AVSS1	USR0	TEST1	P13	P11
V	MD37	MD42	MD34	MD33	~DQM5	FPSCLK	FDA23	FDA19	FDA16	FDA13	FDA8	FDA5	FDA2	VBIASEN	CVDD	RVSS	BLUE	USR1	TEST0	P14
W	MD36	MD46	MD45	MD47	LP	DE	FDA21	FDA18	FDA15	FDA12	FDA9	FDA6	FDA3	FDA0	CRTHSYNC	**VDD**	IREF	RED	P15	USR2
Y	MD35	MD44	MD32	~DQM4	FP	FPEN	FDA20	FDA17	FDA14	FDA11	FDA10	FDA7	FDA4	FDA1	CRTVSYNC	CKIN	AVDD	GREEN	AVSS2	USR3

PINOUT SM722

VSS	VSS	AVSS3	IREF2
VSS	VSS	VSS	AVDD3
RS5	RS6	RS7	CVBS
RS8	RS9	RS10	RS11

TOP VIEW

Figure 3: SM722/723 Pin Diagram for 316 BGA Package

Table 5: Numerical SM722 BGA Pin List

(NOTE: signals which are in BOLD have different definitions from Lynx3DM)

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
A1	MD12	MD12				MVDD
A2	MD3	MD3	{ROM}			MVDD
A3	MD4	MD4	ROMD4			MVDD
A4	MD5	MD5	ROMD5			MVDD
A5	MD7	MD7	ROMD7			MVDD
A6	MD31	MD31				MVDD
A7	MD17	MD17				MVDD
A8	MD28	MD28				MVDD
A9	MD20	MD20				MVDD
A10	MD25	MD25				MVDD
A11	MD22	MD22				MVDD
A12	AD0	AD0				HVDD
A13	AD4	AD4				HVDD
A14	AD7	AD7				HVDD
A15	AD9	AD9				HVDD
A16	AD12	AD12				HVDD
A17	AD14	AD14				HVDD
A18	PAR	PAR				HVDD
A19	~FRAME	~FRAME				HVDD
A20	C/~BE2	C/~BE2				HVDD
B1	MD2	MD2	ROMD2			MVDD
B2	MD0	MD0	ROMD0			MVDD
B3	MD11	MD11				MVDD
B4	MD9	MD9				MVDD
B5	MD8	MD8				MVDD
B6	~DQM3	~DQM3				MVDD
B7	MD30	MD30				MVDD
B8	MD18	MD18				MVDD
B9	MD27	MD27				MVDD
B10	MD21	MD21				MVDD
B11	MD24	MD24				MVDD
B12	AD1	AD1				HVDD
B13	AD5	AD5				HVDD
B14	C/~BE0	C/~BE0				HVDD
B15	AD10	AD10				HVDD
B16	AD13	AD13				HVDD
B17	C/~BE1	C/~BE1				HVDD
B18	~TDRY	~TDRY				HVDD
B19	~STOP	~STOP				HVDD
B20	AD16	AD16				HVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
C1	MD15	MD15				MVDD
C2	MD1	MD1	ROMD1			MVDD
C3	MD13	MD13				MVDD
C4	MD10	MD10				MVDD
C5	MD6	MD6	ROMD6			MVDD
C6	~DQM2	~DQM2				MVDD
C7	MD16	MD16				MVDD
C8	MD29	MD29				MVDD
C9	MD19	MD19				MVDD
C10	MD26	MD26				MVDD
C11	MD23	MD23				MVDD
C12	AD3	AD3				HVDD
C13	AD6	AD6				HVDD
C14	AD8	AD8				HVDD
C15	AD11	AD11				HVDD
C16	AD15	AD15				HVDD
C17	~DEVSEL	~DEVSEL				HVDD
C18	~IDRY	~IDRY				HVDD
C19	AD17	AD17				HVDD
C20	AD18	AD18				HVDD
D1	~CS0	~CS0				MVDD
D2	~DQM1	~DQM1				MVDD
D3	MD14	MD14				MVDD
D4	VCCA	VCCA				
D5	VSS	VSS				
D6	**MIVDD**	**MVDD**				
D7	VSS	VSS				
D8	**MIVDD**	**MVDD**				
D9	VSS	VSS				
D10	VSS	VSS				
D11	AD2	AD2				HVDD
D12	HVDD	HVDD				
D13	VSS	VSS				
D14	HVDD	HVDD				
D15	VDD	VDD				
D16	VSS	VSS				
D17	HVDD	HVDD				
D18	AD19	AD19				HVDD
D19	AD20	AD20				HVDD
D20	AD21	AD21				HVDD
E1	~WE	~WE				MVDD
E2	BA	BA				MVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
E3	~DQM0	~DQM0				MVDD
E4	VSS	VSS				
E5	~RBF	~RBF				
E6	**Reserved**	**BA0**				
E7	RS2	RS2				
E8	~AGP_BUSY	~AGP_BUSY				HVDD
E9	~STOP_AGP	~STOP_AGP				HVDD
E10	~PIPE	~PIPE				HVDD
E11	ST0	ST0				HVDD
E12	ST1	ST1				HVDD
E13	ST2	ST2				HVDD
E14	SBA7	SBA7				HVDD
E15	SBA6	SBA6				HVDD
E16	SBA5	SBA5				HVDD
E17	VSS	VSS				
E18	AD22	AD22				HVDD
E19	AD23	AD23				HVDD
E20	IDSEL	IDSEL				HVDD
F1	MA5	MA5				MVDD
F2	~CAS	~CAS				MVDD
F3	~RAS	~RAS				MVDD
F4	MVDD	MVDD				
F5	VCCA	VCCA				
F16	SBA4	SBA4				HVDD
F17	HVDD	HVDD				
F18	C/~BE3	C/~BE3				HVDD
F19	AD24	AD24				HVDD
F20	AD25	AD25				HVDD
G1	MA7	MA7				MVDD
G2	MA3	MA3				MVDD
G3	MA4	MA4				MVDD
G4	VSS	VSS				
G5	**VSSA**	**VSS**				
G16	SBA3	SBA3				HVDD
G17	VDD	VDD				
G18	AD26	AD26				HVDD
G19	AD27	AD27				HVDD
G20	AD28	AD28				HVDD
H1	MA1	MA1				MVDD
H2	MA8	MA8				MVDD
H3	MA2	MA2				MVDD
H4	MA6	MA6				MVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
H5	MA10	MA10				MVDD
H16	SBA2	SBA2				HVDD
H17	VSS	VSS				
H18	AD29	AD29				HVDD
H19	AD30	AD30				HVDD
H20	AD31	AD31				HVDD
J1	SDCKEN	SDCKEN				MVDD
J2	SDCK	SDCK				MVDD
J3	MA9	MA9				MVDD
J4	MA0	MA0				MVDD
J5	VDD	VDD				
J9	VSS	VSS				
J10	VSS	VSS				
J11	AVSS3	AVSS3				
J12	IREF2	IREF2				
J16	SBA1	SBA1				HVDD
J17	HVDD	HVDD				
J18	~REQ	~REQ				HVDD
J19	~GNT	~GNT				HVDD
J20	CLK	CLK				HVDD
K1	VCCA	VCCA				
K2	~ROMEN	~ROMEN				MVDD
K3	DSF	DSF				MVDD
K4	VCCA	VCCA				
K5	~PME	~PME				HVDD
K9	VSS	VSS				
K10	VSS	VSS				
K11	VSS	VSS				
K12	AVDD3	AVDD3				
K16	SBA0	SBA0				HVDD
K17	VSS	VSS				
K18	~RST	~RST				HVDD
K19	~INTA	~INTA				HVDD
K20	REFCLK	REFCLK				HVDD
L1	MD55	MD55				MVDD
L2	MD56	MD56				MVDD
L3	MD54	MD54				MVDD
L4	VSS	VSS				
L5	VSS	VSS				
L9	**FDATA29**	**RS5**				
L10	**FDATA32**	**RS6**				
L11	**FDATA26**	**RS7**				

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
L12	CVBS	CVBS	{EXT CLK}			
L16	SB_STB	SB_STB				HVDD
L17	MCKIN/LVDSCK	MCKIN/LVDSCK	MCKIN			HVDD
L18	~PDOWN	~PDOWN				HVDD
L19	~CLKRUN/ ACTIVITY	~CLKRUN/ ACTIVITY				HVDD
L20	~EXCKEN	~EXCKEN				HVDD
M1	MD57	MD57				MVDD
M2	MD53	MD53				MVDD
M3	MD58	MD58				MVDD
M4	VCCA	VCCA				
M5	**FDATA47**	**RS3**				
M9	**FDATA31**	**RS8**				
M10	**FDATA33**	**RS9**				
M11	**FDATA28**	**RS10**				
M12	**FDATA25**	**RS11**				
M16	VSS	VSS				
M17	PALCK	PALCK				
			{ZV IN}		{TESTMODE1}	
M18	VREF	VREF	VS		TD19	VPVDD
M19	HREF	HREF	HREF	{External TV encoder}	TD18	VPVDD
M20	BLANK	BLANK		TVCLK	TD17	VPVDD
N1	MD52	MD52				MVDD
N2	MD59	MD59				MVDD
N3	MD51	MD51				MVDD
N4	VSS	VSS				
N5	**FDATA46**	**RS4**				
N16	AD_STB0	AD_STB0				HVDD
N17	P4	P4	UV4		TD4	VPVDD
N18	P1	P1	UV1		TD1	VPVDD
N19	P0	P0	UV0		TD0	VPVDD
N20	PCLK	PCLK	PCLK		TD16	VPVDD
P1	MD60	MD60				MVDD
P2	MD50	MD50				MVDD
P3	MD61	MD61				MVDD
P4	MVDD	MVDD				
P5	VSS	VSS				
P16	AD_STB1	AD_STB1				HVDD
P17	Y	Y	{ZV IN}			
P18	P5	P5	UV5		TD5	VPVDD
P19	P3	P3	UV3		TD3	VPVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
P20	P2	P2	UV2		TD2	VPVDD
R1	MD49	MD49				MVDD
R2	MD62	MD62				MVDD
R3	MD48	MD48				MVDD
R4	~DQM7	~DQM7				MVDD
R5	VCCA	VCCA				
R16	**FDATA36**	**LVDD**				
R17	VPVDD	VPVDD				
R18	P8	P8	Y0		TD8	VPVDD
R19	P7	P7	UV7		TD7	VPVDD
R20	P6	P6	UV6		TD6	VPVDD
T1	MD63	MD63				MVDD
T2	~DQM6	~DQM6	{ROM}			MVDD
T3	MD39	MD39	ROMA7			MVDD
T4	VSS	VSS				
T5	FPVDD	FPVDD				
T6	VCCA	VCCA				
T7	VSS	VSS				
T8	**FDATA45**	**PLLVDD**				
T9	**FDATA44**	**TX3+**				**LVDD**
T10	**FDATA43**	**TXCLK+**				**LVDD**
T11	**FDATA42**	**TXCLK-**				**LVDD**
T12	**FDATA41**	**TX2-**				**LVDD**
T13	**FDATA40**	**TX1+**				**LVDD**
T14	**FDATA39**	**TX0+**				**LVDD**
T15	**FDATA38**	**TX0-**				**LVDD**
T16	**FDATA37**	**LVSS**				
T17	C	C	{ZV IN}			
T18	P12	P12	Y4		TD12	VPVDD
T19	P10	P10	Y2		TD10	VPVDD
T20	P9	P9	Y1		TD9	VPVDD
			{ROM}			
U1	MD40	MD40	ROMA8			MVDD
U2	MD38	MD38	ROMA6			MVDD
U3	MD41	MD41	ROMA9			MVDD
U4	MD43	MD43	ROMA11			
U5	MVDD	MVDD				
U6	**FDATA35**	**RS12**	**{DSTN}**			
U7	FDATA22	FDATA22	UD10			FPVDD
U8	**FDATA34**	**PLVSS**				
U9	FPVDD	FPVDD				
U10	**FDATA30**	**TX3-**				**LVDD**

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
U11	**FDATA27**	**TX2+**				**LVDD**
U12	FPVDD	FPVDD				
U13	**FDATA24**	**TX1-**				**LVDD**
U14	FPVDDEN	FPVDDEN				FPVDD
U15	CVSS	CVSS				
U16	AVSS1	AVSS1	{I2C/DDC}	{USR CFG}		
U17	USR0/SCL	USR0/SCL	SCL (Prim)	USR0		VPVDD
U18	TEST1	TEST1	{ZV IN}		TEST1	VPVDD
U19	P13	P13	Y5		TD13	VPVDD
U20	P11	P11	Y3		TD11	VPVDD
			{ROM}			
V1	MD37	MD37	ROMA5			MVDD
V2	MD42	MD42	ROMA10			MVDD
V3	MD34	MD34	ROMA2			MVDD
V4	MD33	MD33	ROMA1			MVDD
V5	~DQM5	~DQM5	{DSTN}			MVDD
V6	FPSCLK	FPSCLK	XCK			FPVDD
V7	FDATA23	FDATA23	UD11			FPVDD
V8	FDATA19	FDATA19	UD7			FPVDD
V9	FDATA16	FDATA16	UD4			FPVDD
V10	FDATA13	FDATA13	UD1			FPVDD
V11	FDATA8	FDATA8	LD8			FPVDD
V12	FDATA5	FDATA5	LD5			FPVDD
V13	FDATA2	FDATA2	LD2			FPVDD
V14	VBIASEN	VBIASEN				FPVDD
V15	CVDD	CVDD				
V16	RVSS	RVSS				
V17	BLUE	BLUE	{I2C/DDC}	{USR CFG}		
V18	USR1/SDA	USR1/SDA	SDA (Prim)	USR1		VPVDD
V19	TEST0	TEST0	{ZV IN}		TEST0	VPVDD
V20	P14	P14	Y6		TD14	VPVDD
			{ROM}			
W1	MD36	MD36	ROMA4			MVDD
W2	MD46	MD46	ROMA14			MVDD
W3	MD45	MD45	ROMA13			MVDD
W4	MD47	MD47	ROMA15			MVDD
				{DSTN}		
W5	LP/FHSYNC	LP/FHSYNC		LP		FPVDD
W6	M/ DE	M/ DE		M/DE		FPVDD
W7	FDATA21	FDATA21		UD9		FPVDD
W8	FDATA18	FDATA18		UD6		FPVDD
W9	FDATA15	FDATA15		UD3		FPVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
W10	FDATA12	FDATA12		UD0		FPVDD
W11	FDATA9	FDATA9		LD9		FPVDD
W12	FDATA6	FDATA6		LD6		FPVDD
W13	FDATA3	FDATA3		LD3		FPVDD
W14	FDATA0	FDATA0		LD0		FPVDD
W15	CRTHSYNC	CRTHSYNC				VPVDD
W16	**RVDD**	**VDD**				
W17	IREF	IREF				
W18	RED	RED	{ZV IN}			
W19	P15	P15	Y7		TD15	VPVDD
			{I2C/DDC}	{USR CFG}		
W20	USR2	USR2	SCL	USR2/ NTSCPAL		VPVDD
			{ROM}			
Y1	MD35	MD35	ROMA3			MVDD
Y2	MD44	MD44	ROMA12			MVDD
Y3	MD32	MD32	ROMA0			MVDD
Y4	~DQM4	~DQM4		{DSTN}		MVDD
Y5	FP/ FVSYNC	FP/ FVSYNC		FP		FPVDD
Y6	FPEN	FPEN		FPEN		FPVDD
Y7	FDATD20	FDATD20		UD8		FPVDD
Y8	FDATA17	FDATA17		UD5		FPVDD
Y9	FDATA14	FDATA14		UD2		FPVDD
Y10	FDATA11	FDATA11		LD11		FPVDD
Y11	FDATA10	FDATA10		LD10		FPVDD
Y12	FDATA7	FDATA7		LD7		FPVDD
Y13	FDATA4	FDATA4		LD4		FPVDD
Y14	FDATA1	FDATA1		LD1		FPVDD
Y15	CRTVSYNC	CRTVSYNC				FPVDD
Y16	CKIN	CKIN				
Y17	AVDD	AVDD				
Y18	GREEN	GREEN				
Y19	AVSS2	AVSS2	{I2C/DDC2}	{USR CFG}		
Y20	USR3	USR3	SDA	USR3/TVONOFF		VPVDD

Notes: The reserved signals are for future use.

Table 6: Lynx3DM+ VCC and GROUND Connections

VCC Pin	Location	Supply Voltage	Description
HVDD	D12,D14,D17,F17,J17	3.3V	Host interface VDD
MVDD	D6, D8, F4 P4,U5	3.3V/2.5V[1]	Memory VDD. Allow option for 3.3V or 2.5V connection.
FPVDD	T5, U9, U12	3.3V	Flat panel interface VDD
VPVDD	R17	3.3V	ZVPort Interface VDD
CVDD	V15	2.5V	Clock PLL analog power
AVDD	Y17	3.3V	CRT DAC analog power
AVDD3	K12	3.3V	TVDAC analog power
LVDD	R16	2.5V	LVDS Power Supply
PLLVDD	T8	2.5V	LVDS PLL Power Supply
VDD	D15, G17, J5,W16	2.5V	Core Power
VCCA	D4,F5,K1,K4,M4,R5,T6	3.3V/2.5V[1]	Integrated memory power. Allow for 3.3V or 2.5V connection
Ground			
CVSS	U15		Clock PLL analog ground
LVSS	T16		LVDS ground
PLLVSS	U8		LVDS PLL ground
AVSS1	U16		DAC analog ground
AVSS2	Y19		DAC analog ground
AVSS3	J11		TVDAC analog ground
RVSS	V16		RAM palette ground
VSS	D5,D7,D9,D10,D13,D16,E4,E17,G4, G5,H17,J9,J10,K9,K10,K11,K17,L4, L5, M16,N4, P5,T4,T7		Digital ground

Lynx3DM+ NAND Tree Scan Testing

The LYNX3DM+ NAND Tree scan test circuit is designed for verifying the device being properly soldered to the board. It detects opened/shorted traces of a signal pin with a simple test pattern which, for this particular case, only ~220 vectors in length. Since the NAND Tree scan test circuit uses Combinational logic, therefore, no clock pulses are required during the testing.

General Information

The LYNX3DM+ NAND Tree scan test circuit is a long chain of 2-input NAND gates. The first pin of the NAND chain is an input (signal pin "PME#"), the last pin of the chain is an output (signal pin "BLANK"). In order to setup the device for NAND Tree scan testing, program USR[3:0] pins to 0010h and Test[1:0] pins to 10h. ALL VDD's, VSS's, and Analog pins RED, GREEN, BLUE, IREF, C, Y, CVBS, IREF2, TX[3:0]P, TX[3:0]N, TXCLK1P, TXCLK1N and Control pins USR[3:0], Test[1:0] are not included in the scan chain.

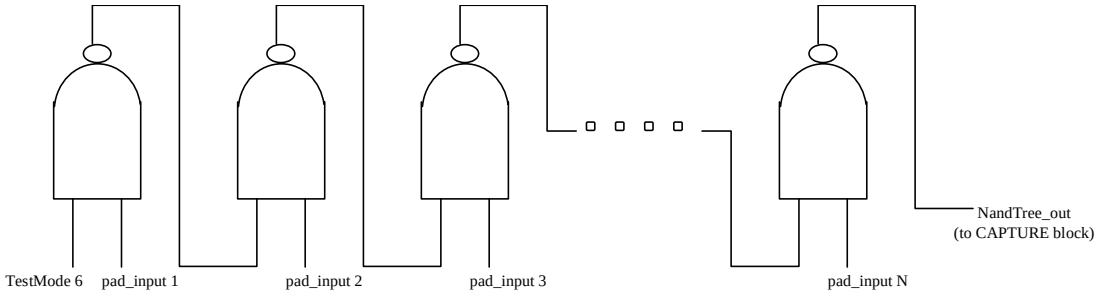


Figure 4: NAND Tree Connection

NAND Tree Simulation

In order to setup LYNX3DM+ to NAND Tree scan test mode, USR[3:0] and Test[1:0] pins are programmed to 0010h and 10h respectively. In NAND Tree mode, internal signal TestMode6 is a "1" (active "High" signal). In the beginning of the simulation, all inputs are forced to "1". Then, follow the NAND Tree PAD sequence and change each input to "0" every 400ns, starting with input_0 (signal "PME#"). The Output pin (signal "BLANK") should be a clock waveform that toggles every 400ns (a 2.5MHz square waveform) (See Figure 2). Any mismatch in the waveform would mean the device not properly soldered to the board.

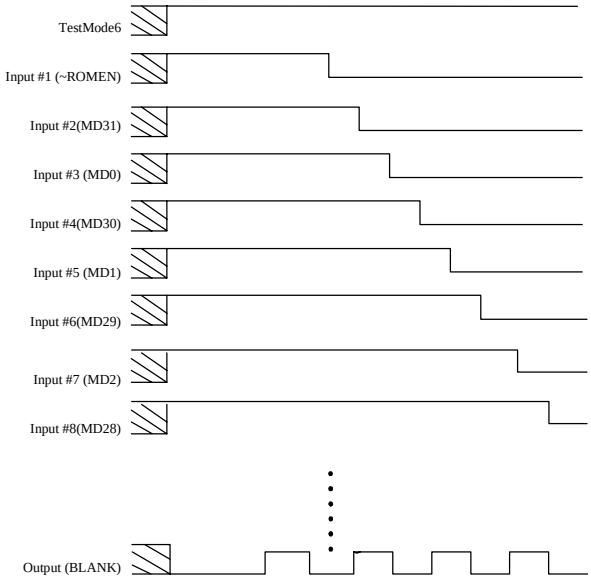


Figure 5: NAND Tree Simulation Timing Diagram

Table 7: NAND Tree Scan Test Order

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
1	PME#	In
2	RBF#	In
3	AGP_BUSY#	In
4	STOP_AGP#	In
5	PIPE#	In
6	ST0	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
7	AD2	In
8	ST1	In
9	AD3	In
10	AD1	In
11	AD0	In
12	ST2	In
13	AD6	In
14	AD5	In
15	AD4	In
16	SBA7	In
17	AD8	In
18	~CBE0	In
19	AD7	In
20	SBA6	In
21	AD11	In
22	AD10	In
23	AD9	In
24	AD13	In
25	AD12	In
26	AD14	In
27	~CBE1	In
28	PAR	In
29	~DEVSEL	In
30	~FRAME	In
31	~TRDY	In
32	~IRDY	In
33	AD16	In
34	~CBE2	In
35	AD17	In
36	~STOP	In
37	AD19	In
38	AD20	In
39	SBA5	In
40	AD22	In
41	~CBE3	In
42	AD23	In
43	AD15	In
44	AD24	In
45	CLK	In
46	AD18	In
47	SBA4	In
48	AD21	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
49	SBA3	In
50	IDSEL	In
51	AD26	In
52	AD25	In
53	AD_STB1	In
54	AD27	In
55	AD_STB0	In
56	AD28	In
57	SB_STB	In
58	AD31	In
59	SBA0	In
60	~INTA	In
61	~RST	In
62	~GNT	In
63	SBA2	In
64	AD30	In
65	SBA1	In
66	AD29	In
67	~REQ	In
68	CLKRUN/ACTIVITY	In
69	P0	In
70	P1	In
71	P2	In
72	P3	In
73	P4	In
74	P6	In
75	P5	In
76	P7	In
77	P8	In
78	PCLK	In
79	P9	In
80	P10	In
81	P11	In
82	P12	In
83	P13	In
84	P14	In
85	P15	In
86	VREF	In
87	HREF	In
88	PALCLK	In
89	MCKIN	In
90	~PDOWN	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
91	REFCLK	In
92	~EXCKEN	In
93	CRTHSYNC	In
94	CRTVSYNC	In
95	CKIN	In
96	FDA1	In
97	FDA4	In
98	FDA0	In
99	VBIASEN	In
100	FDA3	In
101	FDA2	In
102	FDVDDEN	In
103	FDA7	In
104	FDA10	In
105	FDA9	In
106	FDA6	In
107	FDA8	In
108	FDA5	In
109	FDA11	In
110	FDA12	In
111	FDA14	In
112	FDA15	In
113	FDA13	In
114	FDA17	In
115	FDA18	In
116	FDA16	In
117	FDA19	In
118	FDA21	In
119	FDA20	In
120	FDA23	In
121	FDA22	In
122	FPEN	In
123	FPDE	In
124	FPSCLK	In
125	FP/FPVSYNC	In
126	LP/FPHSYNC	In
127	MD63	In
128	MD32	In
129	MD62	In
130	MD33	In
131	MD61	In
132	MD34	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
133	MD60	In
134	MD35	In
135	MD36	In
136	MD59	In
137	MD37	In
138	MD58	In
139	MD38	In
140	MD57	In
141	MD39	In
142	MD56	In
143	MD48	In
144	MD47	In
145	MD49	In
146	MD46	In
147	MD50	In
148	MD45	In
149	MD51	In
150	MD44	In
151	MD52	In
152	MD43	In
153	MD53	In
154	MD42	In
155	MD54	In
156	MD41	In
157	MD55	In
158	MD40	In
159	~DQM4	In
160	~DQM6	In
161	~WE	In
162	~DQM7	In
163	~CAS	In
164	~DQM5	In
165	~RAS	In
166	MA10	In
167	~CS0	In
168	MA6	In
169	BA0	In
170	BA	In
171	MA8	In
172	MA5	In
173	SDCK	In
174	MA0	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
175	MA4	In
176	MA7	In
177	MA3	In
178	MA9	In
179	MA2	In
180	DSF	In
181	MA1	In
182	SDCKEN	In
183	~DQM2	In
184	~DQM1	In
185	~DQM0	In
186	~DQM3	In
187	MD23	In
188	MD8	In
189	MD22	In
190	MD9	In
191	MD10	In
192	MD21	In
193	MD11	In
194	MD20	In
195	MD12	In
196	MD19	In
197	MD13	In
198	MD18	In
199	MD14	In
200	MD17	In
201	MD15	In
202	MD16	In
203	MD7	In
204	MD6	In
205	MD24	In
206	MD5	In
207	MD25	In
208	MD4	In
209	MD26	In
210	MD27	In
211	MD3	In
212	MD28	In
213	MD2	In
214	MD29	In
215	MD1	In
216	MD30	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
217	MD0	In
218	MD31	In
219	~ROMEN	In
220	BLANK	Out

Chapter 3: Initialization

Lynx3DM+ generates an internal power-on reset during system power-on. After receiving the system ~RESET signal, Lynx3DM+ will release its internal power-on reset circuit and enter the RESET period until the host de-asserts the ~RESET signal. During the RESET period, Lynx3DM+ resets its internal state machines and registers to the power-on default states. During power-on, Lynx3DM+ is configured based on configuration lines MD [22:0].

Table 8 provides a detailed description of each configuration line. All MD (memory data) lines have internal pull-up resistors on I/O pads which are latched into the corresponding register as logic "1" on the rising edge (trailing edge) of the ~RESET. To set a specific bit as logic "0" during power-on reset, an external pull-down resistor must be added on the corresponding MD line.

In addition to power-on configuration, Lynx3DM+ performs an initialization sequence for the integrated memory.

After memory initialization has been completed, Lynx3DM+'s video BIOS is ready to service system BIOS requests. System BIOS passes a pointer to the Lynx3DM+ video BIOS to start the video BIOS initialization sequence.

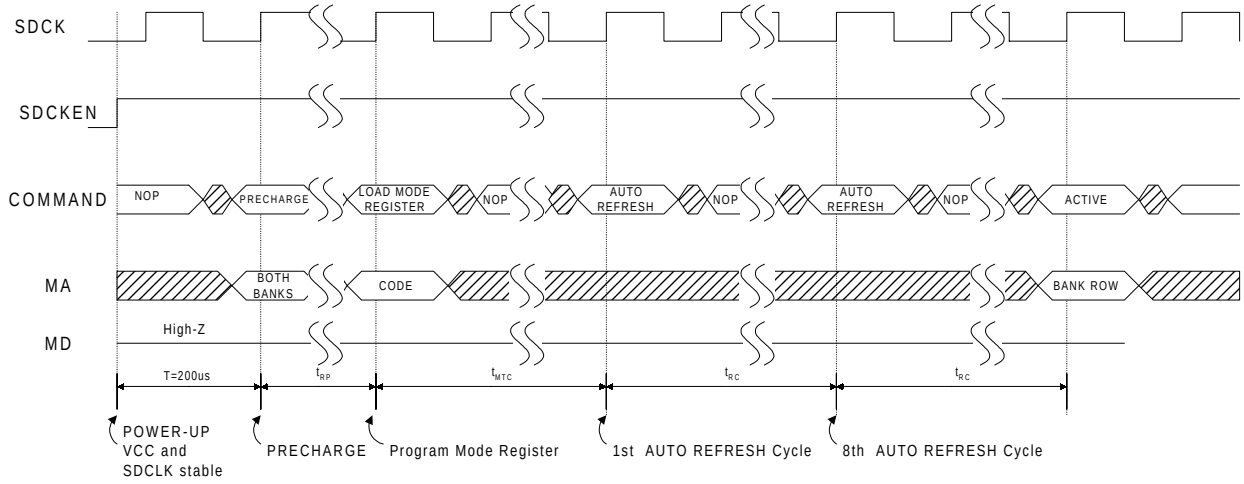


Figure 6: SGRAM Power-Up and Initialization Sequence

Figure 7 illustrates the Lynx3DM+ Video BIOS initialization flow. The initialization sequence consists of the following stages:

- Load configuration table
- Get panel 2D
- Initialize INT10 function
- Initialize hardware
- Query system BIOS via In 15 calls
- Set initial mode
- Enable the display

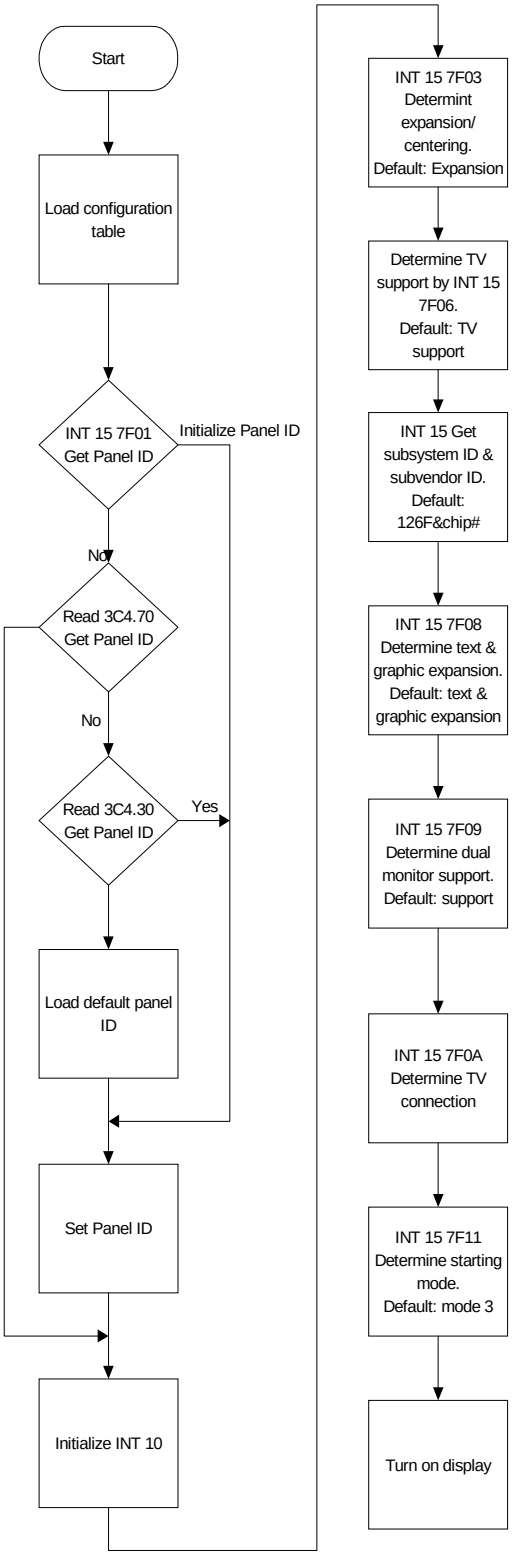


Figure 7: Lynx3DM+ Video BIOS Initialization Flow

Lynx3DM+ Power-On Configurations

- Memory data bit [63:33] have pull-down resisters on I/O pads
- Memory data bit [32:0] have internal pull-up resistors on I/O pads
- 0 = external pull-down resistor
- 1 = no external pull-down resistor

Table 8: Power-On Configurations

Signal Name	Read/Write	Register Bits	Address	Lynx3DM+ Description
MD [32]	CONFIG ONLY			**Enable AGP sideband signal**s 0 = Disable 1 = Enable
MD [31:30]	R/W	MCR76 [7:6]	3C5h.76	**MCB Memory Size** 00 = 8MB 01 = 16MB 10 = Reserved 11 = 4MB
MD [29:28]	R/W	MCR76 [5:4]	3C5h.76	**MCB memory Column Address Select** 11= 8-bit column address 10 = 9-bit column address 0x = 10-bit column address
MD [27]	R/W	MCR76 [3]	3C5h.76	**Reserved**
MD [26]	R/W	MCR76 [2]	3C5h.76	Reserved default = 1
MD [25]	R/W	MCR76 [1]	3C5h.76	**Reserved**
MD [24]	R/W	MCR76 [0]	3C5h.76	**Reserved**
MD [23]	CONFIG ONLY	CPR00 [25]		Reserved
MD [22]	CONFIG ONLY			Reserved
MD [21]	CONFIG ONLY			**EBROM Access** 0 = Enable C0000 access when expansion ROM is disabled (MD [20] = 1) 1 = Disable C0000 access (default)
MD [20]	CONFIG ONLY			**Expansion ROM** 0 = Expansion ROM 1 = no Expansion ROM (default)
MD [19:16]	R/W	GPR70 [3:0]	3C5h.70	**Panel ID Configuration** Refer to BIOS Spec for panel ID definition
MD15	R/W	FPR30 [7]	3C5h.30	**DSTN Interface Type** 0 = 16-bit interface 1 = 24-bit interface
MD [14:12]	R/W	FPR30 [6:4]	3C5h.30	**Color TFT Interface Type** 000 = 9-bit, 3-bit per R, G, B 001 = 12-bit, 4-bit per R, G, B 010 = 18-bit, 6-bit per R, G, B 011 = 24-bit, 8-bit per R, G, B 100 = RESERVED 101 = Analog TFT w/ analog R, G, B interface 110 = RESERVED 111 = RESERVED
MD [11:10]	R/W	FPR30 [3:2]	3C5h.30	**LCD Display Size** 00 = 640 x 480 01 = 800 x 600 10 = 1024 x 768 11 = 1280 x 1024
MD9	R/W	FPR30 [1]	3C5h.30	**TFT FPCLK Select** 0 = Normal 1 = Inverted
MD8	R/W	FPR30 [0]	3C5h.30	**Color LCD Type** 0 = color TFT 1 = color STN

Signal Name	Read/Write	Register Bits	Address	Lynx3DM+ Description
MD [7:6]	R/W	MCR62 [7:6]	3C5h.62	Reserved
MD [5:4]	R/W	MCR62 [5:4]	3C5h.62	Reserved
MD3	R/W	MCR62 [3]	3C5h.62	**MCB SDRAM Memory Bank Select** 0 = 4 memory bank 1 = 2 memory bank (default)
MD2	R/W	MCR62 [2],[0]	3C5h.62	Reserved
MD1	R/W	MCR62 [1]	3C5h.62	Reserved
MD0	R/W	MCR62 [2],[0]	3C5h.62	Reserved

Chapter 4: PCI/AGP Bus Interface

Lynx3DM+ provides a glue-less interface to the PCI and AGP system bus. The device is fully compliant with PCI Version 2.1. The PCI interface 5V tolerant. Lynx3DM+'s PCI Host Interface Unit supports both slave and master mode. To maximize performance, the Host Interface Unit also supports burst write, and burst read with Read Look Ahead. When connected to the AGP interface, Lynx3DM+ supports AGP 2X with sideband.

The Lynx3DM+'s PCI/AGP Host Interface Unit manages data transfer between the external PCI/AGP bus and internal Host Interface (HIF) bus. All functional blocks, with the exception of the Drawing Engine, are tied to the HIF bus through a proprietary protocol. Separate decode logic and a dedicated FIFO are used for the Drawing Engine.

In addition to PCI Configuration Space Registers, the PCI/AGP Host Interface Unit contains Power Down Control Registers (PDR20-PDR23) and System Control Registers (SCR10-SCR1A). These Registers may accessed by the CPU even while internal PLLs are turned off.

PCI Configuration Registers

The PCI configuration registers are designated CSR00 - CSR3D. A brief description of key elements of the register set follows:

- Vendor ID register (CSR00) - hardwired to 126Fh to identify Silicon Motion, Inc as the chip vendor.
- Device ID register (CSR02) - hardwired to 0720h to identify the Lynx3DM+ device.
- Status register (CSR06) - hardwired to 01b, which indicates medium speed for ~DEVSEL.
- Class Code register (CSR08) - hardwired to 030000h to specify Lynx3DM+ as a VGA compatible device. Bit [7:0] used to identify the revision of the Lynx3DM+.
- Memory Base Address register (CSR10) - specifies the PCI configuration space for address relocation. After power-on, the register defaults to 00h, which indicates the base register can be located anywhere in a 32-bit address space and that the base register is located in memory space.
- Subsystem Vendor ID and Subsystem ID (addressable at CSR2C and CSR2E respectively) - 32-bit read only registers. These registers are used to differentiate between multiple graphics adapters within the same system.

Chapter 5: Display Memory Interface

Memory Configuration

The Lynx3DM+ supports a total of 16MB of integrated memory. The memory interface is 32/64 bits wide and is clocked at up to 150 MHz, for a total bandwidth of 1.0GB/s peak. To accomplish this when configured with 16MB, Lynx3DM+ uses two 1Mx64 SGRAM memory devices running in parallel.

Page Break Look Ahead

For standard architectures, the memory controller will break cycle when bus agent changes. Lynx3DM+ can allow a "No Wait Cycle" during agent changes if the preceding and current agents are in the same page. Both the embedded memory bus and external memory bus support this capability.

Memory Timing Control

Memory timing control is configured via MD [7:0] and MD [31:24] during power-on reset. When equipped with 16MB, the configuration bits MD [7:0] control the first SGRAM timing, while MD [31:24] control the second SGRAM timing. They should always be set the same. See Reference Table 10 in the Initialization section for a complete description of these memory configuration bits.

Note: MD[63-33] has internal pull-down resistors and MD[32-0] has pull-up resistors on I/O pads. The default configuration is therefore a logical "1" during power-on reset. To set an MD line to 0, an external pull-down resistor needs to be added. After power-on initialization, software can be used to overwrite the initial setting by writing to MCR62 - bits [7:0] correspond to MD [7:0], and MCR76 - bits [7:0] correspond to MD [31:24].

Chapter 6: Drawing Engine

Lynx3DM+'s 128-bit Drawing Engine is designed to accelerate Microsoft's DirectDraw and Direct3D applications. The engine contains a 3-operand ALU with 256 raster operations, source and destination FIFOs, as well as a host data FIFO. The drawing engine pipeline allows single cycle operations and runs at the memory clock speed.

Lynx3DM+'s Drawing Engine includes several key functions to achieve the high GUI performance. The device supports color expansion with packed mono font, color pattern fill, host BLT, stretch BLT, short stroke, line draw, and others. Dedicated pathways are designed to transfer data between host interface (HIF) bus and Drawing Engine, and memory interface (MIF) bus and Drawing Engine. In addition, the drawing engine supports rotation BIBLT for any block size, and automatic self activate rotation BLIT. This feature allows conversion between landscape and portrait display without the need for special software drivers.

The Drawing Engine offers several 3D assist features. The Drawing Engine supports low-resolution modes and hardware arithmetic stretching to allow 3D to be rendered to a smaller back buffer and scaled up to the front buffer. Lynx3DM+ also supports fast DMA BLT, source clear during BLT, transparent BLT, programmable blter stride, page flip, and current scan line refresh.

Lynx3DM+'s Drawing Engine is also used to bus master captured data to the hard disk drive or to system memory during video capture. To accomplish this, the video capture driver turns on the Drawing Engine Capture Enable bit (DPR0E bit 4), selects HOST BLT Read command function (DPR0E [3:0]), and enables PCI bus master mode (SCR17 bit 6). The Video Capture Unit loads the incoming video stream into Capture Buffer 1 or 2, depending on which is idle (CPR00 bit 1 or bit 2 = 0 indicates idle status). The Drawing Engine resets Capture Buffer I or Capture Buffer II control/Status bit to 0 (CPR00 bit 1 or bit 2) after a transfer has completed.

Chapter 7: Video Processor

Lynx3DM+'s Video Processor manages video data streams, as well as graphics data streams in non-VGA modes. The Video Processor can process two independent video data streams. The two video windows (primary and secondary) can be displayed at any screen location with any size, and can be overlaid with graphics data. Lynx3DM+ also supports Bob and Weave for DVD playback.

Within the Video Processor, the Graphics Source Control block, Video Window I Control block, Video Window II Control block, and HW Pop-up Icon Control block all have independent Starting Address and Offset Address registers. This means that each control block can fetch data from any display memory location. Video Window I source control block supports double-buffered video capture. Internal logic automatically detects the control/status bits of the two capture buffers and fetches the captured video data from the buffer which is not used.

The Video Processor supports TV flicker reduction for direct color modes (64K colors or 16M colors), as well as index color modes (256 colors and 16 colors). A special data path is designed to feed the outputs of the color palette RAM back to the TV Flicker Reduction block. The TV Overscan & Underscan Control block is used to convert 480 lines into 400 visible lines on NTSC TV display. The same function can also be used on PAL TV display. When the TV display is enabled, the Shadow registers need to be locked as 640 x 480 mode (or 720 x 525 for PAL).

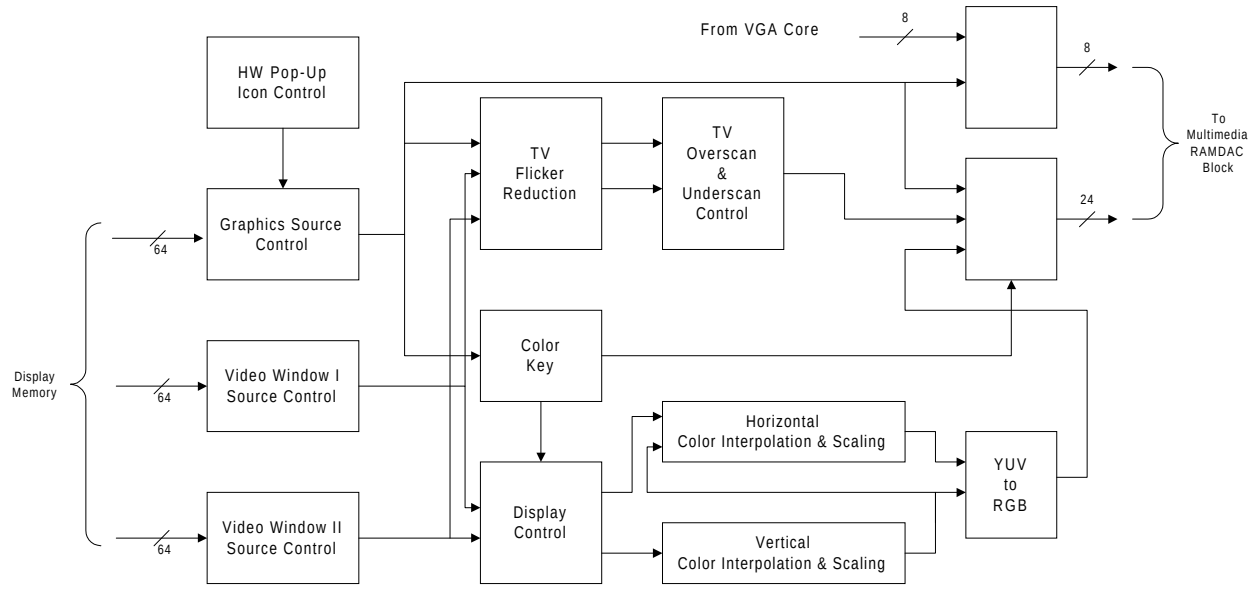


Figure 8: Video Processor Block Diagram

Chapter 8: Zoom Video Port and Video Capture Unit

Zoom Video Port

Lynx3DM+'s Zoom Video Port (ZV Port) is designed to interface with video solutions implemented as PCMCIA (or PC CardBus) cards: examples are NTSC/PAL decoders, MPEG-2 decoders, and JPEG Codecs. The ZV Port can also directly interface with an NTSC/PAL decoder, such as Philips 7111 or BT819. Figure 9 illustrates an example of the Philips video encoder interface via the ZV Port.

Incoming video data from the ZV Port interface can be YUV or RGB format. The data can be interlaced or non-interlaced. The ZV Port can be configured for output if the video capture function is disabled. 18-bit graphics and video data in RGB format can be sent out when the ZV Port is configured for output mode.

The ZV Port may also be configured as a test port. Up to 20 signals from each of the logic blocks within Lynx3DM+ can be brought out to an internal test bus (TD Bus) connected to the ZV Port. System designers or silicon validation engineers can access these signals by setting the TEST0, TEST1, USR0, USR1, and USR2 pins. This approach can bring out a total of 180 internal signals to the primary I/O pins. The test port capability can be used to enhance fault coverage, as well as reduce silicon validation or debugging time.

Table 9 lists signal definitions for the following ZV Port interface configurations: YUV input mode, RGB input mode, and graphics/video (output mode).

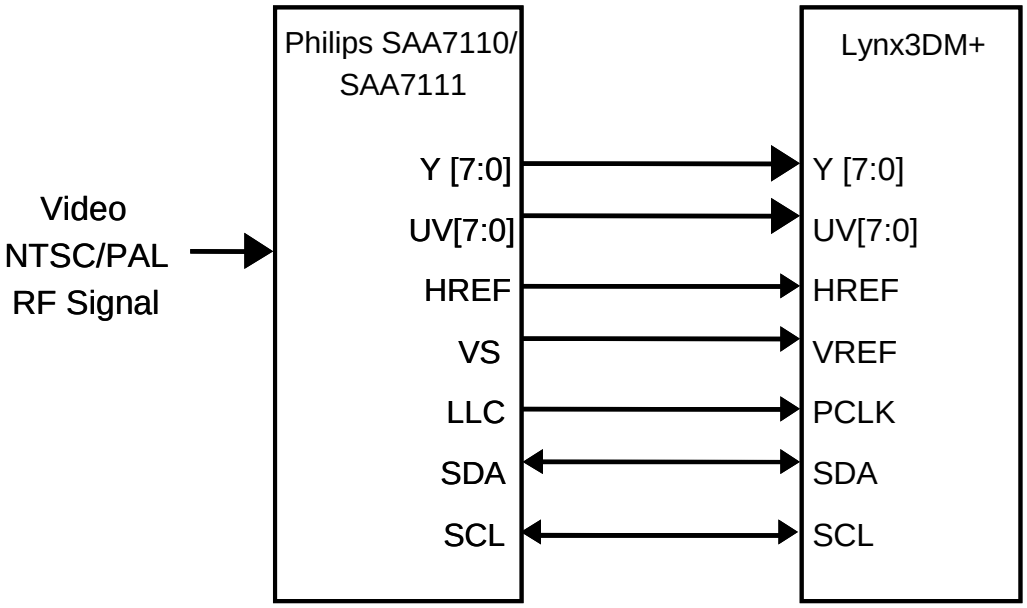


Figure 9: Video Encoder Interface via Video Port

Table 9: Lynx3DM+ Video Port Interface I/O Compliance

Video Port Interface	ZV Port (Input mode)	I/O	NTSC/PAL Decoder (Input mode)	I/O	Graphics/Video (Output mode)	I/O
VREF	VS	I	VS	I	R7	O
HREF	HREF	I	HREF	I	R6	O
BLANK	(note1)		(note1)		BLANK	O
PCLK	PCLK	I	PCLK	I	PCLK	O
P15	UV7	I	R7	I	R5	O
P14	UV6	I	R6	I	R4	O
P13	UV5	I	R5	I	R3	O
P12	UV4	I	R4	I	R2	O
P11	UV3	I	R3	I	G7	O
P10	UV2	I	G7	I	G6	O
P9	UV1	I	G6	I	G5	O
P8	UV0	I	G5	I	G4	O
P7	Y7	I	G4	I	G3/Vindex_[7]	O
P6	Y6	I	G3	I	G2/Vindex_[6]	O
P5	Y5	I	G2	I	G7/Vindex_[5]	O
P4	Y4	I	B7	I	G6/Vindex_[4]	O
P3	Y3	I	B6	I	G5/Vindex_[3]	O
P2	Y2	I	B5	I	G4/Vindex_[2]	O
P1	Y1	I	B4	I	G3/Vindex_[1]	O
P0	Y0	I	B3	I	G2/Vindex_[0]	O

Note 1: BLANK pin can used as TVCLK output, which is independent of ZV port.

Note 2: Vindex [7:0] is indexed video out

Note 3: SMI test bus is for internal use only

Video Capture Unit

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer. The Video Capture Unit support several features to maintain display quality, and balance the capture rate:

- 2-tap, 3-tap, and 4-tap horizontal filtering
- 2 to 1 and 4 to 1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swap, RGB 5:5:5, and RGB 5:6:5
- Multiple frame skipping methods
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

Lynx3DM+ uses the Video Processor block to display the captured data on the LCD, TV, or CRT display. The captured data can be displayed through Video Window I or Video Window II. The stretching, color interpolation, YUV-to-RGB conversion, and color key functions are performed in the Video Processor. Lynx3DM+'s Video Processor can simultaneously process captured video data and perform CD-ROM playback on two independent video windows.

Lynx3DM+ also supports real-time video capture to the hard drive or system memory through PCI master mode or slave mode. In PCI bus master mode, Lynx3DM+ uses the Drawing Engine's Host BLT and Host DMA functions to maximize performance.

Functional Description

Lynx3DM+'s Video Capture Unit supports the Video Port Extension (VPE) specification for video stream processing. This capture unit includes CLIP block, FILTER block, SHRINK block, and FIFO control block. Figure 10 and Figure 11 illustrate the Lynx3DM+ Video Capture Block Diagram and Data Flow. The CLIP functional block is used to select the desired rectangles from the video stream to be captured. VPR40 register (Video Source Clipping Control) is used to define the upper left corner of the rectangle from the video source. VPR44 register (Video Source Capture Size Control) is used to define the height and width of the rectangle from the video source.

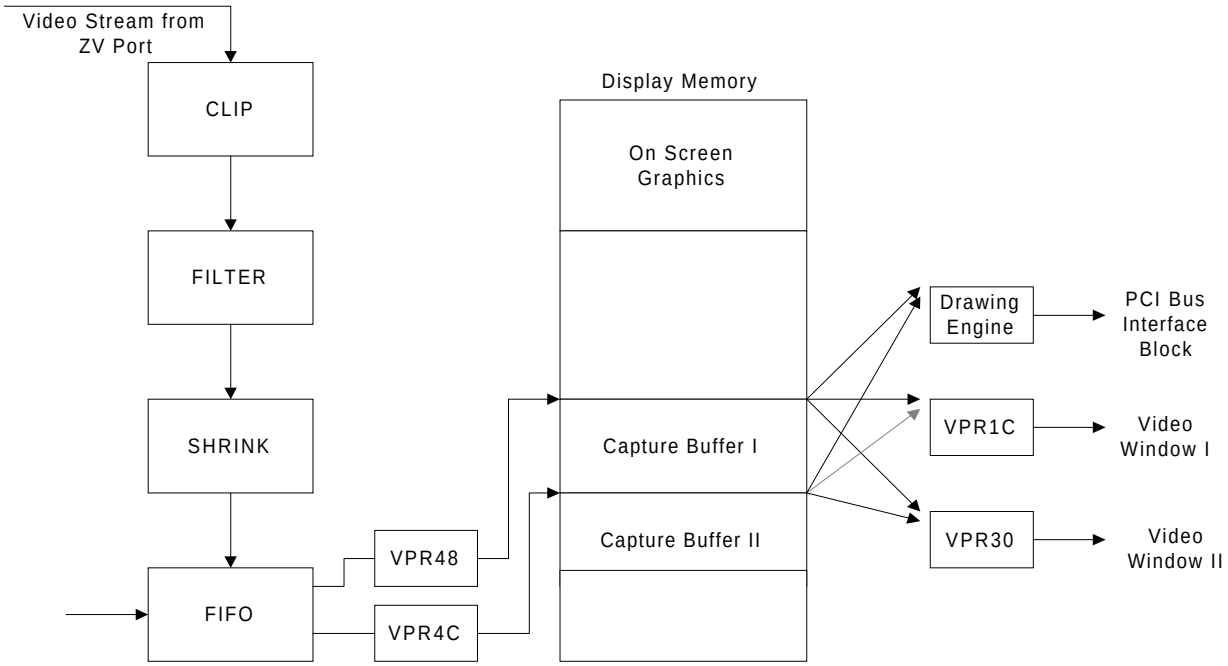


Figure 10: Video Capture Block Diagram

The FILTER functional block controls horizontal filtering logic. CPR00 (Capture Port Control) bit 21 and bit 20 are used to select 2 tap, 3 tap, and 4 tap filtering. The SHRINK functional block is used to not only reduce the storage area for both display memory and hard drive, but also increase performance of video capture and video playback. CPR00 bit 19 and 18 are used to enable vertical reduction, and bit 17 and bit 16 are used to enable horizontal reduction. With filter and shrink functions, Lynx3DM+ is able to achieve high video capture performance and maintain optimal video playback quality.

CPR00 bit 13 to bit 11 are use to select 8 different frame skipping options in the event the capture rate is less than the incoming video stream. CPR00 bit 10 and bit 9 are used to support interlaced capture and double buffer capture. CPR00 bit 1 and bit 2 are used as control/status bits for Buffer I and Buffer II.

The captured data can be displayed on either Video Window I or Video Window II. The video capture driver needs to program VPR1C (or VPR30), Video Window I (or II) Source Start Address, with the same address value from Capture Port Buffer I or II Start Address register. VPR00 (Miscellaneous Graphics and Video Control) bit 24 may be used to automatically display the capture data on Video Window I without programming VPR1C register. This feature is independent of single buffer or double buffer mode.

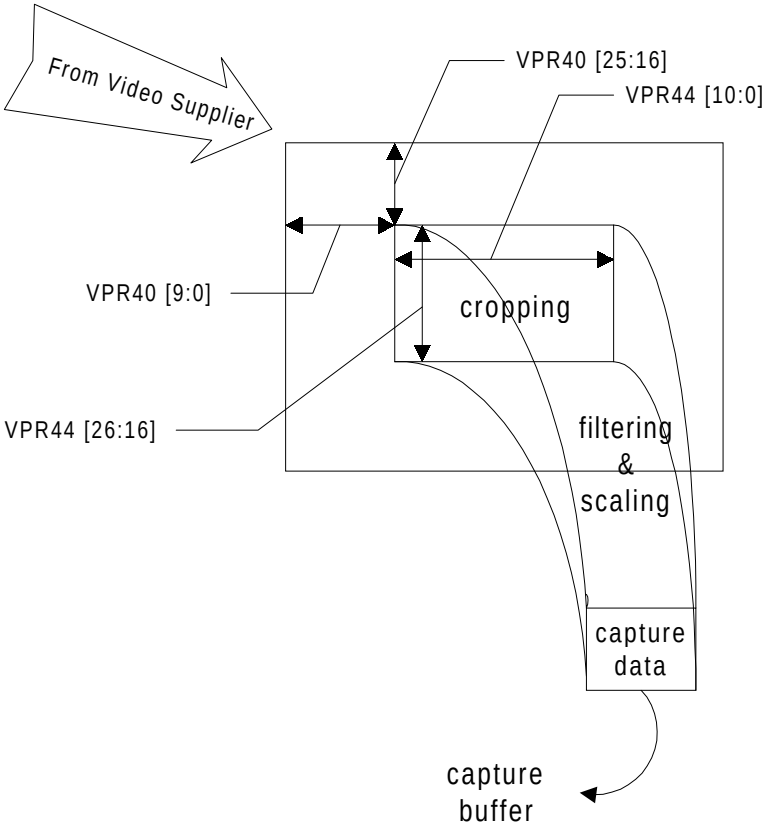


Figure 11: Video Capture Data Flow

Theory of Operation

Initialization

- Enable Video Capture (CPR00 bit 0 = 1)
- Preset Buffer I and Buffer II Status/Control bits (CPR00 [2:1] = 11b)
- Enable Drawing Engine (DPR0E bit 4 = 1)
- Select Host BLT Read Command function (DPR0E [3:0] =9h)
- Enable PCI bus master mode (SCR17 bit 6 = 1)
- Select Field Detection, VREF/HREF polarity, Vertical/Horizontal Reduction, Horizontal Filtering, Video Capture Input Data Format, Frame Skip, Interlaced/non-interlaced and other miscellaneous settings (CPR00, Capture Port Control Register)

Table 10: Bit Setting Summary for Video Capture

B1S	Buffer 1 Status/Control (CPR00 bit 1)
B2S	Buffer 2 Status/Control (CPR00 bit 2)
Continuous Capture	bit 8 = 0
Conditional Capture	bit 8 = 1
Single Buffer	bit 9 = 0
Double Buffer	bit 9 = 1
Non-interlaced Mode	bit 10 = 0
Interlaced Mode	bit 10 = 1

The Video Capture Unit supports the following types of capture modes:

- Single Buffer Mode with Continuous Capture
- Single Buffer Mode with Conditional Capture
- Double Buffer Mode with Continuous Capture
- Double Buffer Mode with Conditional Capture
- Interlace and Non-Interlaced Mode

A summary of each of the video capture modes follows:

- **Single Buffer Mode with Continuous Capture**

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
• Continuously capture incoming video data to capture buffer 1 • Independent of B1S and B2S bits	It is not recommended to use the Drawing Engine to transfer captured data from display memory to hard drive or system memory in this mode. This mode is used to view the captured data only.	• VPR00 bit 24 = 0 Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 Captured data is automatically displayed on Video Window I.

- **Single Buffer Mode with Conditional Capture**

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
bg) VCU monitors B1S bit bh) If B1S = 1, start capture bi) VCU will reset B1S to 0 after it completes a frame bj) Go to step “a”	a) Test b) If B1S = 0, SW will activate the DE to transfer captured data from capture buffer 1 to hard drive or system memory c) DE will set B1S bit to 1 after it completes a frame d) Go to step "a”	• VPR00 bit 24 = 0 • Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 • Captured data is automatically displayed on Video Window I

- **Double Buffer Mode with Continuous Capture**

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
• Continuously capture the incoming video data into capture buffer 1 or buffer 2 • Automatically switch from one buffer to the other when VCU completes a frame • Independent of B1S and B2S bits	It is not recommended to use DE to transfer captured data from display memory to hard drive or system memory in this mode. This mode is used to view the captured data only.	• VPR00 bit 24 = 0 Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 Captured data is automatically displayed on Video Window I. If capture buffer 1 is used by VCU, Video Window I will display captured data from capture buffer 2

- **Double Buffer Mode with Conditional Capture**

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
a) VCU monitors B1S and B2S bits b) If B1S (or B2S) = 1, start video capture and store into capture buffer 1 (or buffer 2). c) VCU will reset B1S (or B2S) to 0 after it completes a frame d) VCU will continue video capture if B1S or B2S = 1 e) Go to step "a" if both bits = 0	a) SW monitors B1S or B2S bit b) If B1S (or B2S) = 0, SW will activate the DE to transfer captured data from capture buffer 1(or buffer 2) to hard drive or system memory c) DE will set B1S (or B2S) bit to 1 after it completes a frame d) DE will continuously transfer e) Data from capture buffer 1 or 2 if B1S or B2S = 0 f) Go to step "a " if both bits = 1	• VPR00 bit 24 = 0 Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 Captured data is automatically displayed on Video Window I. If capture buffer 2 is used by VCU, Video Window I will display captured data from capture buffer 1.

- **Interlaced Capture**

CPR00 bits 10 are used to select the interlaced capture mode. In most of video capture applications, an interlaced video stream will be treated as non-interlaced video stream by dropping all even frames (CPR00[13:11] = 010b), or dropping all odd frames (CPR00[13:11] = 011). This approach will reduce artifacts when playing back the captured data. However, in some video capture applications, de-interlacing is needed to handle the incoming interlaced video stream.

For the de-interlacing case, CPR00 bit 10 needs to be set to 1 to enable interlaced capture for incoming interlaced video stream. The double buffer mode (CPR00 bit 9 = 1) needs to be turned on at the same time. Capture Buffer 1 and Capture Buffer 2 are combined together as a single buffer with one line offset. Figure 12 illustrates the capture buffer structure. The video capture driver will preset B1S and B2S bits to 1 to initialize the buffer 1 and 2 status/control bits. The Video Capture Unit will start video capture if any one of B1S and B2S = 1. After VCU fills capture buffer 1 and 2, both B1S and B2S bits are set to "0" by VCU. The video capture driver will activate Drawing Engine to transfer captured data in capture buffer 1 and 2 to system memory or hard drive when both B1S and B2S are "0". After the completion of the transfer, the Drawing Engine will set both B1S and B2S to "1". The Video Capture Unit then continues video capture and repeats the same protocol.

During video playback, the captured data can be displayed on either Video Window I or Video Window II. It is not recommended to display both even frame and odd frame for video playback. The video captured driver can program Video Window I (or II) Source Start Address Register and Video Window I (or II) Source Width and Offset Register in such a way that odd frame (or even frame) captured data will be dropped during video playback. The scaling, color interpolation, and YUV-to-RGB conversion functions can also be enabled at the same time.

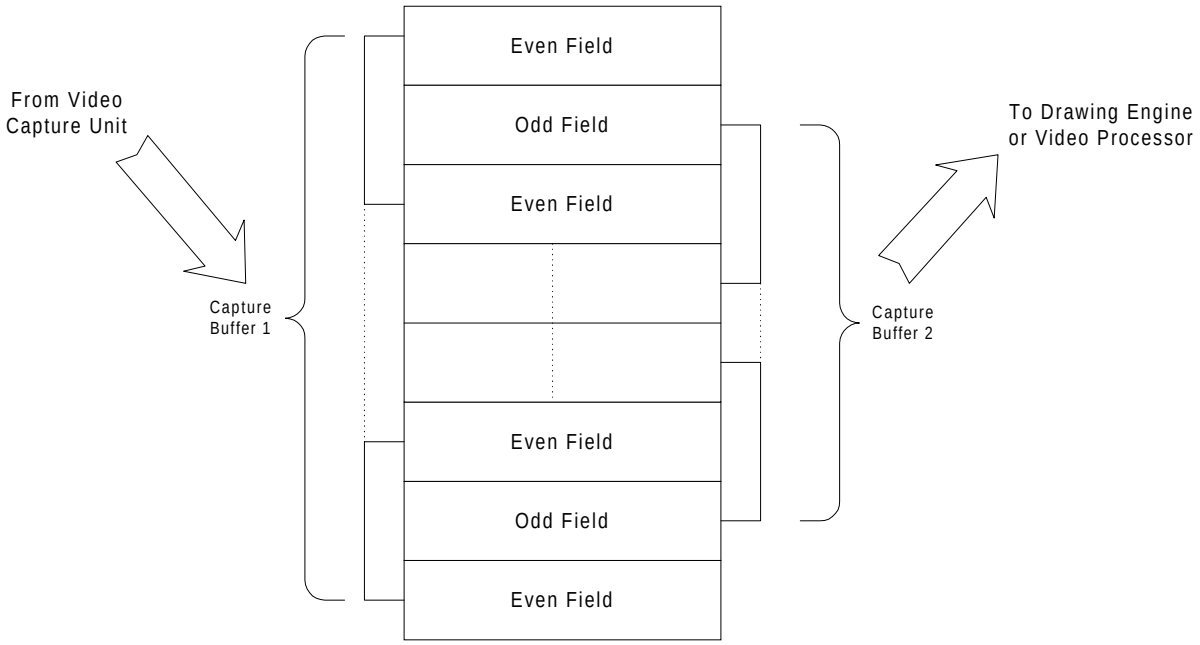


Figure 12: Capture Buffer Structure in Interlaced Mode

Chapter 9: Flat Panel Interface

Lynx3DM+ supports both color dual scan STN (passive) and color TFT (active) panel interface for notebook computers. It can also support color TFT panel with RGB analog interface. For color DSTN panel, Lynx3DM+ can support 16-bit and 24-bit interfaces up to 1280x1024 resolution. For color TFT panel, Lynx3DM+ can support single pixel per clock of 9-bit, 12-bit, 18-bit, 24-bit. In addition, Lynx3DM+ integrates one channel LVDS output. Table 11 lists the complete set of Lynx3DM+ panel interface pins for both color DSTN and TFT LCD. Figure 14 shows the single-pixel per clock TFT interface, Figure 16 shows the 16-bit DSTN interface, and Figure 17 shows the 24-bit DSTN interface.

Lynx3DM+ Flat Panel Enhancements

Lynx3DM+ integrates various flat panel enhancement features such as: LCD screen auto-centering, LCD screen expansion (including XY interpolated screen expansion), Virtual Refresh, and special dithering engines for TFT and DSTN flat panels.

Lynx3DM+ Flat Panel Enhancements

Lynx3DM+ integrates various flat panel enhancement features such as: LCD screen auto-centering, LCD screen expansion (including XY interpolated screen expansion), Virtual Refresh, and special dithering engines for TFT and DSTN flat panels.

Lynx3DM+ Graphics/Text Expansion Information

Introduction

Lynx3DM+ provides full expansion capability for text and graphics modes. Text as well as graphics expansion is supported up to XGA resolution. Expansion is supported on TFT and DSTN panels. A detailed description of the expansion algorithms of these devices follows:

Horizontal Expansion for Text and Graphics

Horizontal expansion is handled in 8 pixel pieces whether the mode is text or graphics. There are two expansion mechanisms: 10-dot expansion and 12-dot expansion. 10-dot expansion is used to expand to 800 pixels, 12-dot is used to expand to 960 pixels for XGA panel sizes.

For 10-dot expansion, every 4th pixel is duplicated. For example, for mode3h (80x25 text) or mode 12h(640x480 graphics), where p0 is pixel one and p7 is pixel 8 - p0p1p2**p3p3**p4p5p6**p7p7** - the 4th pixel (p3) is duplicated, as well as the 8th pixel (p7). The pattern repeats for each 8 pixel piece.

For 12-dot expansion, every other pixel, beginning with p1 is duplicated. For example, for mode 3h or mode 12h - p0**p1p1**p2**p3p3**p4**p5p5**p6**p7p7**. Again, the pattern repeats for each pixel piece.

So far, all examples assume 8x16 font size. There is also 9x16 font size to consider (in this case the actual font is still 8x16, but an additional 9th dot - either the background color or a repeat of the 8th pixel - is inserted). For 9x16 case, pixel p3 is duplicated just like 8x16 case. Pixel p7 is handled somewhat differently depending on whether the character is a text

character or graphics character - for text character case, the second p7 value becomes the background color. For graphics case, p7 is repeated.

Vertical Expansion for Text and Graphics

Vertical expansion for text or graphics uses a Dynamic Duplication Algorithm (DDA) method to achieve expansion. The same basic methodology is used independent of resolution. First, an initial DDA constant value (for Lynx3DM+ this is a 10-bit value) is loaded into the Vertical Screen Expansion DDA Constant Registers. This value is used as part of a logical algorithm to determine which lines on the display to duplicate. Figure 13 is a diagram of the algorithm.

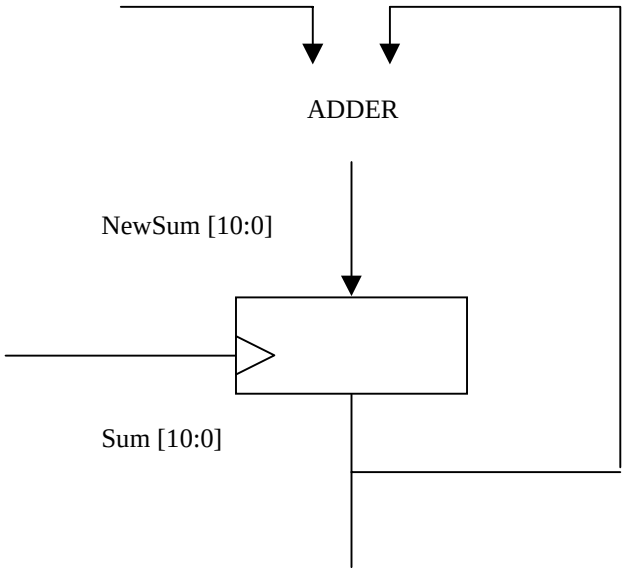


Figure 13: DDA Expansion Algorithm

For each line of the display, the following equation is calculated via the illustrated algorithm:

NewSum [10:0] = Sum[10:0] + DDA

If Sum [10:0] = NewSum [10:0], the given line is duplicated.

For text case, the DDA logic algorithm will reset each character block, so expansion is handled in terms of character rows (e.g. 25 character rows of 16 lines each). For the graphics case, the DDA logic algorithm will reset when the bottom of the display is reached.
The DDA constant may be calculated by the following equation:

$$\frac{1024}{DDA} = \frac{\text{Expanded Resolution}}{\text{Existing Resolution}}$$

For example, to expand a 480 line mode to 768, the equation would be:

$$\frac{1024}{DDA} = \frac{768\ \text{Lines}}{480\ \text{Lines}}$$

DDA constant may then be calculated and entered into the expansion algorithm.

DDA[9:0]

LCD Dithering Engine

Lynx3DM+ has separate dithering engines for color DSTN LCD and color TFT LCD. The DSTN dithering engine includes a set of 32 different dithering patterns which are developed with LCD's response time and contrast ratio in mind. FPR32 bit 5 is used to select 16 gray levels or 32 gray levels for each Red, Green, and Blue color. The TFT dithering engine includes a set of 8 different dithering patterns which combine frame rate modulation and space dithering algorithm. FPR32 bit 7 and 6 are used to select 4-gray level dithering, 8-gray level dithering, and no dithering.

Flat Panel Power ON/OFF Sequencing

Lynx3DM+ integrates logic for panel power ON/OFF sequencing during power down modes and display switching.

There are two ways to power ON/OFF the flat panel: hardware panel power sequencing and software panel power sequencing.

Hardware panel power sequencing:

Hardware panel power sequencing is selected when FPR34 bit 7 =1. Whenever FPR31 bit toggles, Lynx3DM+ automatically controls LCD data, LCD controls, FPEN, FPVDD, and VBIASEN pins. FPR33 [3:2] determines the time period from FPEN to VBIASEN, from VBIASEN to LCD controls/data, and from LCD controls/data to FPVDDEN.

FPR33[3:2]	Power On Sequencing Time Select
00	1 vertical frame
01	2 vertical frames
10	4 vertical frames
11	8 vertical frames

Figure 18 shows the auto panel power on sequencing timing relationship. Figure 19 shows the auto panel power off sequencing timing relationship.

For flat panels which have non-standard requirements for on/off power sequencing, Lynx3DM+ supports panel power on/off sequencing through software programming.

Below are examples of software programming for panel power on sequencing:

Software panel power sequencing- ON:

- Set FPR34 bit 7 = 0 (software panel power sequencing)
- Setup shadow registers: SVR40 to SVR4B
- Set FPR31 bit 0 = 1 (enable LCD display)
- After X vertical frames, set PDR22 bit 0 = 1 (turn on FPVDDEN)
- After X vertical frames, set PDR22 bit 1 = 0 (enable LCD controls and data)
- After X vertical frame, set PDR22 bit 2 = 1 (turn on VBIASEN)
- After X vertical frames, set PDR22 bit 3 = 1 (turn on FPEN)

Note: LCD backlight control is independent of power sequencing. The VBKLGT can be turned on at the same time as FPEN.

Software panel power sequencing - OFF:

- Set FPR34 bit 7 = 0 (software panel power sequencing)
- Select FPR33 [3:2] for panel power on/off timing:

- Set PDR22 bit 3 = 0 (turn off FPEN)
- After X vertical frames, set PDR22 bit 2 = 0 (turn off VBIASEN)
- After X vertical frames, set PDR22 bit 1 = 1 (disable LCD controls and data)
- After X vertical frames, set PDR22 bit 0 = 0 (turn off FPVDDEN)
- Set FPR31 bit 0 = 0 (disable LCD display)

Lynx3DM+ Dual Digital LCD Support

Lynx3DM+ can support two separate digital LCDs. Both LCDs need to be TFT interface. FP1 has to be the THine LVDS TFT interface and FP2 has to be 24-bit TFT interface. DSTN panel can not be supported under dual digital LCD mode.

Table 11 lists the Dual Digital LCD pin mapping for FP1 + FP2.

Dual Digital LCD mode is supported through the Virtual Refresh architecture. FP1 and FP2 must be in Virtual Refresh mode. FP1 clocks the data based on VRCLK (Virtual Refresh Clock); whereas FP2 clocks the data based on WFIFOCLK (based on Video Clock).

To enable FP1 + FP2, the following registers need to be programmed:

* FPR31[7] = 1 (virtual refresh enable)
* FPR4E[1] = 1 (enable second LCD panel)
* PDR21[5] = 0 (enable LCD frame buffer write)
* CCR69[5] = 1 (LVDSCLK source is from inverted WFIFO clock)
* FPR33[9] = 0 (enable LVDS for FP1)
* FPR33[4] = 0 (enable virtual refresh for FP2)

FP1's timing can be programmed via the Virtual Refresh Timing Registers. (FPR50 - FPR57) FP2's timing is directly derived from the CRT timing under Virtual Refresh mode via the Shadow VGA Registers (SVR40 - SVR4D).

Lynx3DM+ Flat Panel Interface Connections

Lynx3DM+ supports both color dual scan STN (passive) and TFT (active) panel interface for notebook computers. It supports DSTN in 16-bit 24-bit interface. For TFT interface, it can support either 9-bit, 12-bit, 18-bit, 24-bit and 12-bitx2. Furthermore, Lynx3DM+ can support two separate TFT interface: FP1 is LVDS TFT and FP2 is 24-bit TFT. The table listed below details the various pin mapping for different panel configuration

Table 11: Flat Panel Interface Pins listing for color DSTN and color TFT LCD

	DSTN		TFT				
Pin Name	**16-bit**	**24-bit**	**9-bit**	**12-bit**	**18-bit**	**24-bit**	**12-bit x2**
LP/FHSYNC	LP	LP	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
FP/FVSYNC	FP	FP	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
FPSCLK	XCK	XCK	CK	CK	CK	CK	CK
DE			ENAB	ENAB	ENAB	ENAB	ENAB
FPEN	FPEN	FPEN	FPEN	FPEN	FPEN	FPEN	FPEN
FPVDDEN	VDD	VDD	VDD	VDD	VDD	VDD	VDD
VBIASEN	VEE	VEE	VEE	VEE	VEE	VEE	VEE
FPDATA23		UD11				R7	RB3

Table 11: Flat Panel Interface Pins listing for color DSTN and color TFT LCD

	DSTN		TFT				
Pin Name	**16-bit**	**24-bit**	**9-bit**	**12-bit**	**18-bit**	**24-bit**	**12-bit x2**
FPDATA22		UD10				R6	RB2
FPDATA21		UD9			R5	R5	RB1
FPDATA20		UD8			R4	R4	RB0
FPDATA19	UD7	UD7		R3	R3	R3	RA3
FPDATA18	UD6	UD6	R2	R2	R2	R2	RA2
FPDATA17	UD5	UD5	R1	R1	R1	R1	RA1
FPDATA16	UD4	UD4	R0	R0	R0	R0	RA0
FPDATA15	UD3	UD3				G7	GB3
FPDATA14	UD2	UD2				G6	GB2
FPDATA13	UD1	UD1			G5	G5	GB1
FPDATA12	UD0	UD0			G4	G4	GB0
FPDATA11		LD11		G3	G3	G3	GA3
FPDATA10		LD10	G2	G2	G2	G2	GA2
FPDATA9		LD9	G1	G1	G1	G1	GA1
FPDATA8		LD8	G0	G0	G0	G0	GA0
FPDATA7	LD7	LD7				B7	BB3
FPDATA6	LD6	LD6				B6	BB2
FPDATA5	LD5	LD5			B5	B5	BB1
FPDATA4	LD4	LD4			B4	B4	BB0
FPDATA3	LD3	LD3		B3	B3	B3	BA3
FPDATA2	LD2	LD2	B2	B2	B2	B2	BA2
FPDATA1	LD1	LD1	B1	B1	B1	B1	BA1
FPDATA0	LD0	LD0	B0	B0	B0	B0	BA0

Table 12: Dual Panel Interface (One Digital Panel and One LVDS Panel)

Pin name	**Digital Panel & LVDS Panel**	**TFTs: FP1 + FP2**	**24-bit TFT**
DE	DE		DE
FP_FVSYNC	FP_FVSYNC		FP_FVSYNC
LP_FHSYNC	LP_FHSYNC		LP_FHSYNC
FPSCLK	FPSCLK		FPSCLK
FPEN	FPEN		FPEN
FPVDDEN	FPVDDEN		FPVDDEN
VBIASEN	VBIASEN		VBIASEN

Pin name	Digital Panel & LVDS Panel	TFTs: FP1 + FP2	24-bit TFT
FPDATA23	R7		R7
FPDATA22	R6		R6
FPDATA21	R5		R5
FPDATA20	R4		R4
FPDATA19	R3		R3
FPDATA18	R2		R2
FPDATA17	R1		R1
FPDATA16	R0		R0
FPDATA15	G7		G7
FPDATA14	G6		G6
FPDATA13	G5		G5
FPDATA12	G4		G4
FPDATA11	G3		G3
FPDATA10	G2		G2
FPDATA9	G1		G1
FPDATA8	G0		G0
FPDATA7	B7		B7
FPDATA6	B6		B6
FPDATA5	B5		B5
FPDATA4	B4		B4
FPDATA3	B3		B3
FPDATA2	B2		B2
FPDATA1	B1		B1
FPDATA0	B0		B0
TxOUT0±	RxIn0±		
TxOUT1±	RxIn1±		
TxOUT2±	RxIn2±		
TxOUT3±	RxIn3±		
TxCLKOUT±	RxCLKIN±		

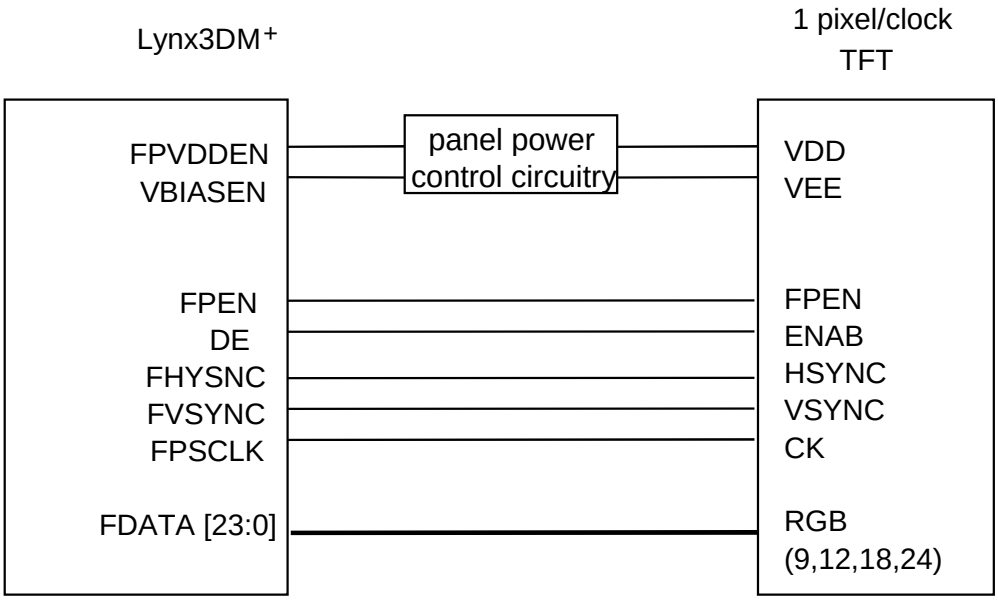


Figure 14: TFT (Single Pixel/Clock) Interface Diagram

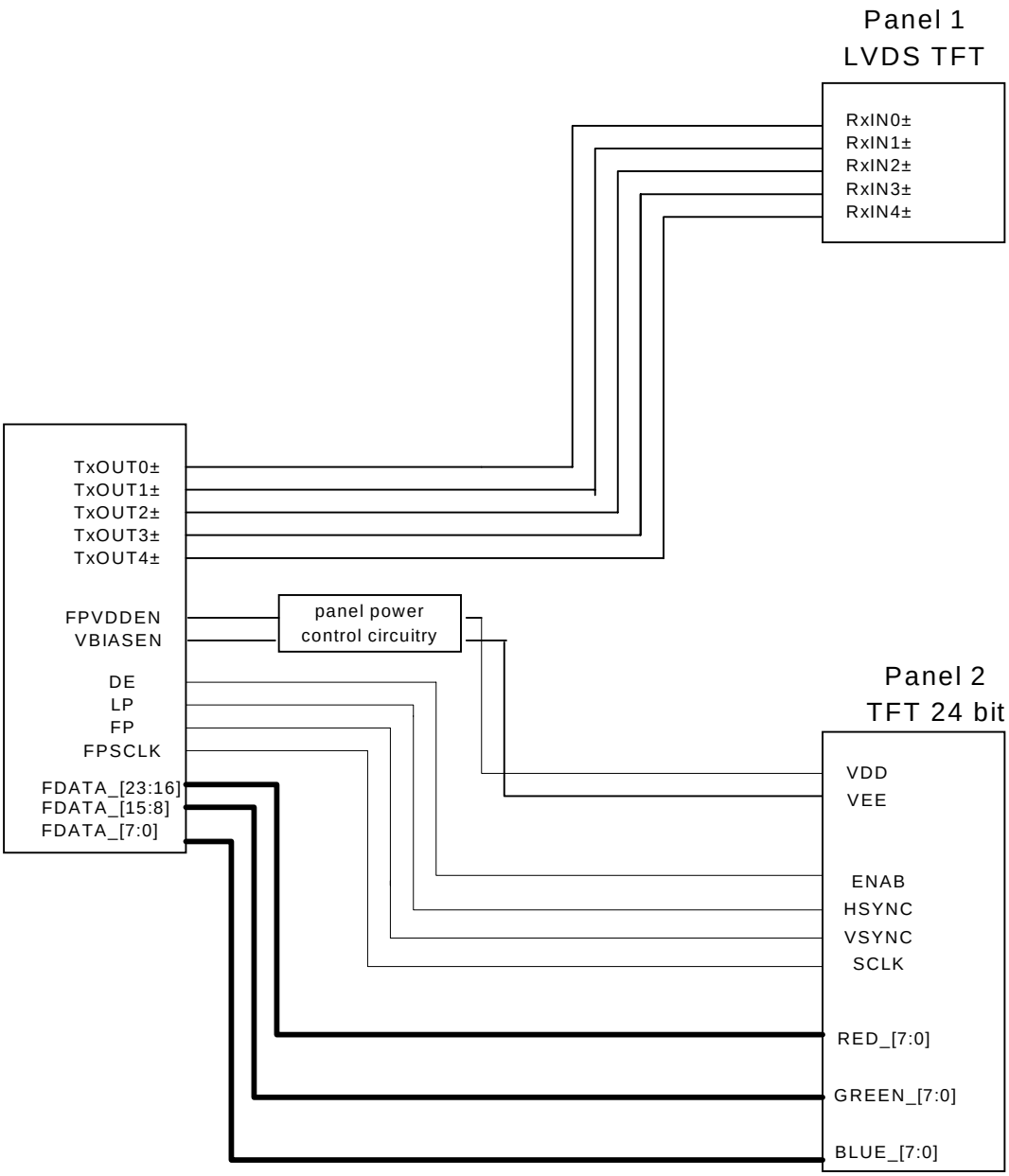


Figure 15: TFT Two Panel Interface Diagram

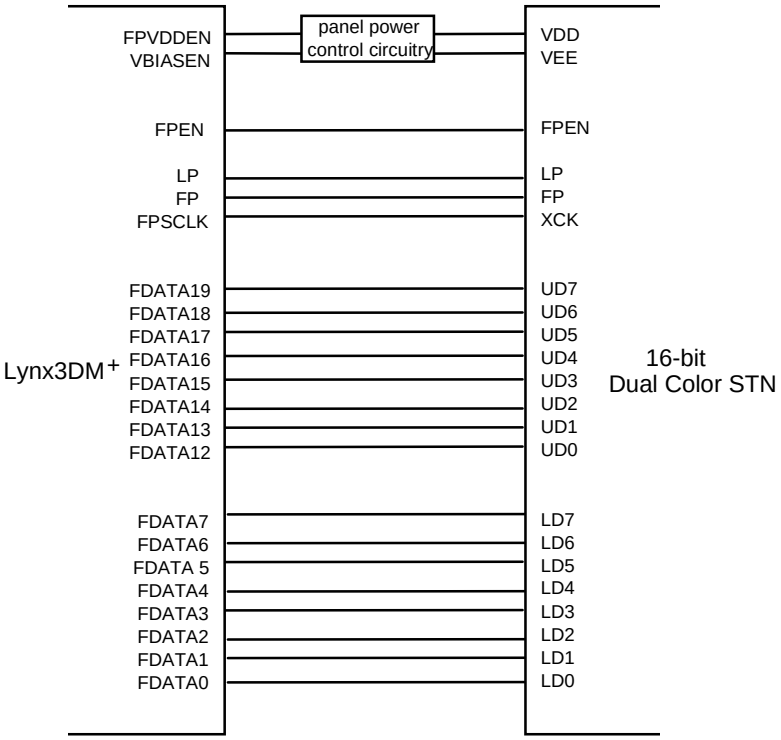


Figure 16: 16-bit DSTN Interface Configuration

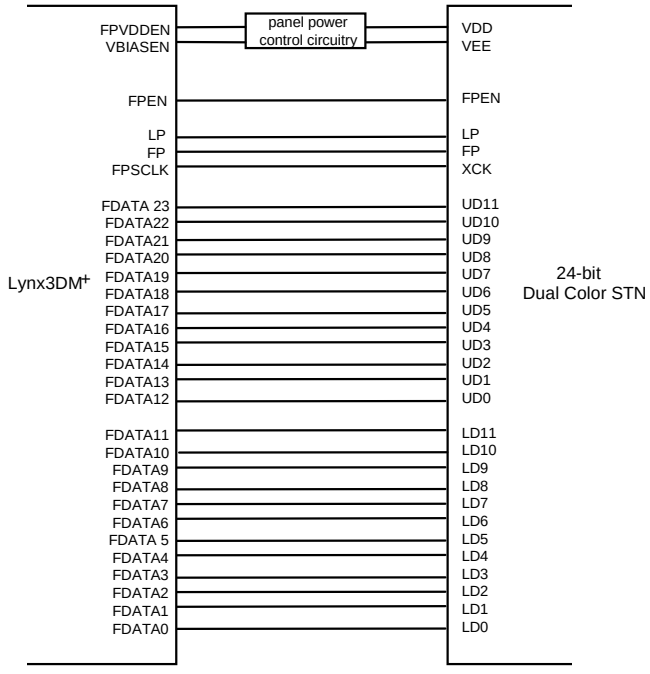
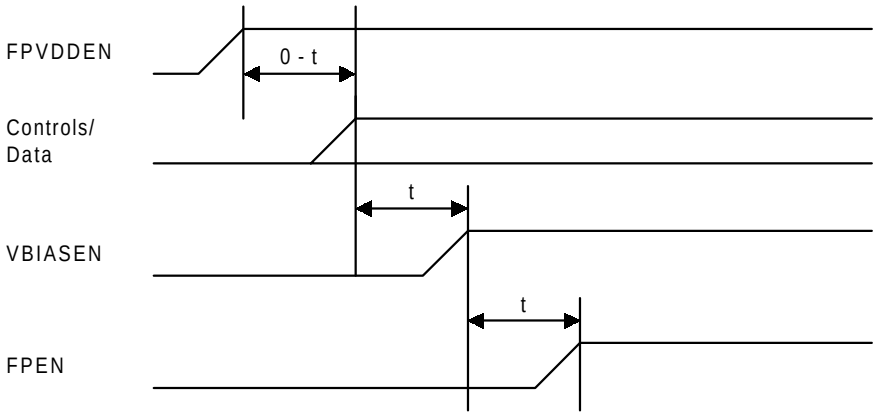
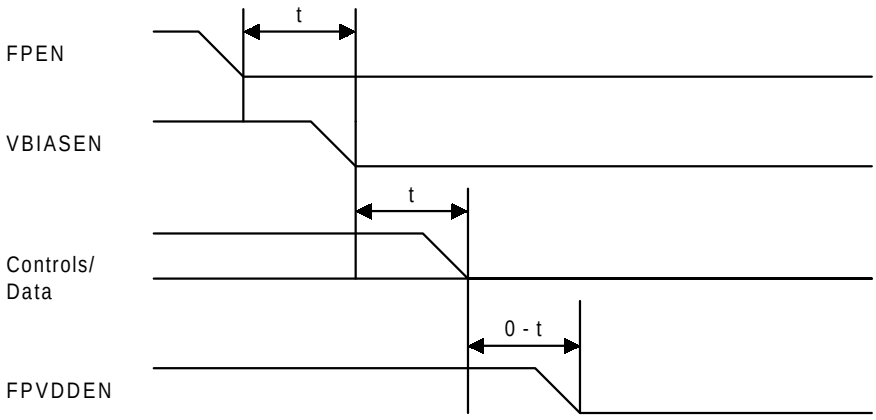


Figure 17: 24-bit Dual Color STN Interface Diagram



t is programmed via FPR33 [3:2]

Figure 18: Panel Power On Sequencing Timing Diagram



t is programmed via FPR33 [3:2]

Figure 19: Panel Power Off Sequencing Timing Diagram

FPR33[3:2]	Power On/Off Sequencing Time Select
00	1 vertical frame
01	2 vertical frames
10	4 vertical frames
11	8 vertical frames

Integrated LVDS Chipset Interface

In order to address EMI and cable issues associated with a wide, high speed TTL/CMOS panel interface, designers may choose to use an LVDS (Low Voltage Differential Signaling) chipset (each chipset type includes a transmitter and a receiver). Lynx3DM+ supports a integrated LVDS transmitter. Figure 20 and Figure 21 below illustrate the 24-bit interfaces for TFT LVDS panels and internal LVDS Panel Interface, respectively. Please note that DSTN LVDS panel is not supported.

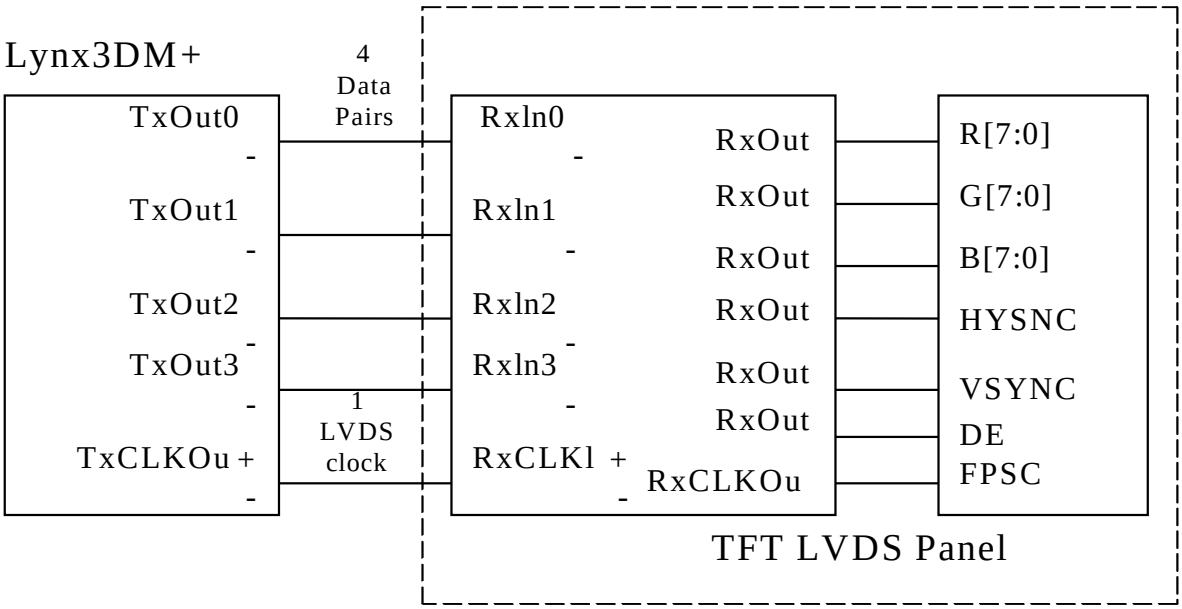


Figure 20: LVDS Interface with TFT LVDS Panel

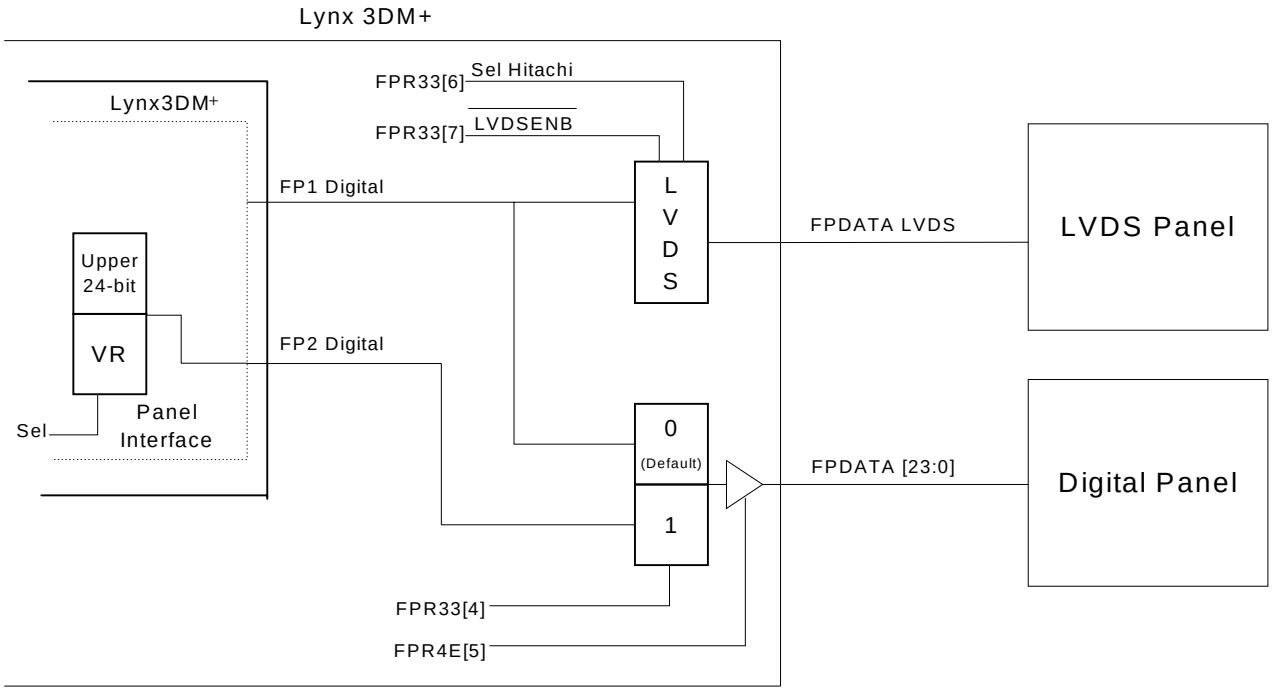


Figure 21: Lynx 3DM+ Internal LVDS Panel Interface

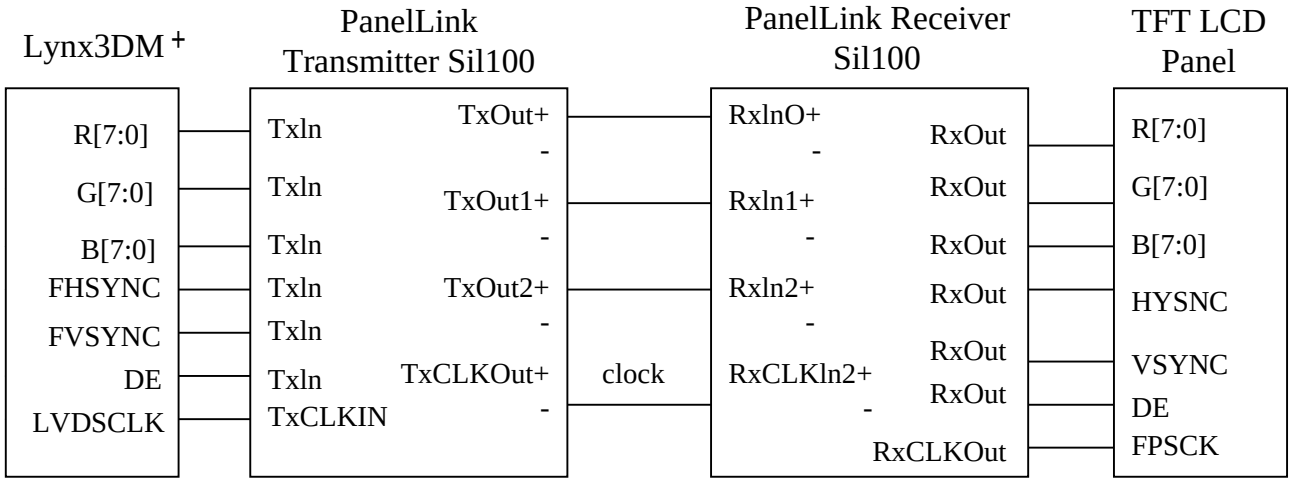


Figure 22: PanelLink Interface with TFT LCD Panel

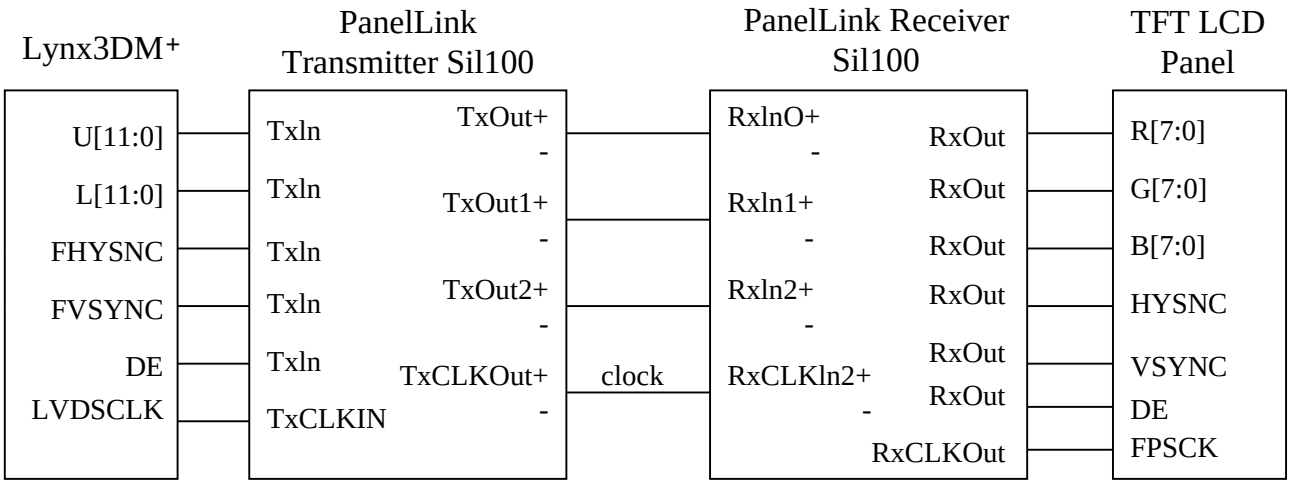


Figure 23: PanelLink Interface with DSTN LCD Panel

Table 13 lists the pin mapping for an LVDS transmitter with Lynx3DM+ for LVDS TFT. Table 14 lists the pin mapping for a PanelLink transmitter with Lynx3DM+ for PanelLink TFT panels.

Please consult your panel manufacturer to verify the pin mapping between the LVDS receiver and the panel. The pin mapping from the transmitter side must correspond with the pin mapping from the receiver side in order to ensure that the panel will function properly.

Table 13: LVDS Transmitter Pin Mapping for TFT Interface

Lynx3DM+ Pin Name	TFT interface	LVDS Transmitter SN75LVDS83/DS90C383 Pin #	LVDS Transmitter Pin Name
FPDATA16	R0	51	TxIN0
FPDATA17	R1	52	TxIN1
FPDATA18	R2	54	TxIN2
FPDATA19	R3	55	TxIN3
FPDATA20	R4	56	TxIN4
FPDATA21	R5	3	TxIN6
FPDATA22	R6	50	TxIN27
FPDATA23	R7	2	TxIN5
FPDATA8	G0	4	TxIN7
FPDATA9	G1	6	TxIN8
FPDATA10	G2	7	TxIN9
FPDATA11	G3	11	TxIN12
FPDATA12	G4	12	TxIN13
FPDATA13	G5	14	TxIN14
FPDATA14	G6	8	TxIN10
FPDATA15	G7	10	TxIN11
FPDATA0	B0	15	TxIN15
FPDATA1	B1	19	TxIN18
FPDATA2	B2	20	TxIN19
FPDATA3	B3	22	TxIN20
FPDATA4	B4	23	TxIN21
FPDATA5	B5	24	TxIN22
FPDATA6	B6	16	TxIN16
FPDATA7	B7	18	TxIN17
LP/FHSYNC	FHSYNC	27	TxIN24
FP/FVSYNC	FVSYNC	28	TxIN25
DE	DE	30	TxIN26
-	-	25	TxIN23
FPSCLK	FPSCLK	31	TxCLKIN

Table 14: PanelLink Transmitter Pin Mapping for TFT Interface

Lynx3DM+ Pin Name	TFT interface	PanelLink Transmitter Sil100 Pin #	PanelLink Transmitter Pin Name
FPDATA16	R0	63	D0
FPDATA17	R1	62	D1
FPDATA18	R2	61	D2
FPDATA19	R3	60	D3
FPDATA20	R4	59	D4
FPDATA21	R5	58	D5
FPDATA22	R6	57	D6
FPDATA23	R7	56	D7
FPDATA8	G0	55	D8
FPDATA9	G1	54	D9
FPDATA10	G2	52	D10
FPDATA11	G3	51	D11
FPDATA12	G4	50	D12
FPDATA13	G5	49	D13
FPDATA14	G6	48	D14
FPDATA15	G7	47	D15
FPDATA0	B0	46	D16
FPDATA1	B1	44	D17
FPDATA2	B2	43	D18
FPDATA3	B3	42	D19
FPDATA4	B4	41	D20
FPDATA5	B5	40	D21
FPDATA6	B6	38	D22
FPDATA7	B7	37	D23
LP/FHSYNC	FHSYNC	2	HSYNC
FP/FVSYNC	FVSYNC	3	VSYNC
DE	DE	1	DE
FPSCLK	FPSCLK	12	IDCK

Chapter 10: Miscellaneous Functions

This chapter describes functions of Lynx3DM+ such as the Video ROM BIOS interface, VESA DPMS, and I^2C / VESA DDC2B.

Video BIOS ROM Interface

The Video BIOS contains code for chip power-on initialization, graphics mode setup, and various read/write routines to the frame buffer. The Video BIOS can be burned into a separate video BIOS EPROM (this is the typical case for add-in cards) or be integrated into the system BIOS ROM (this is the typical case for a motherboard graphics implementation).

To support separate video BIOS ROM access, BIOS address decode must be enabled by setting CSR30 (Expansion ROM Enable Base Address Register) bit 0 = 1. For implementations where video BIOS is integrated into the system BIOS ROM, BIOS address decode access must be disabled by clearing CSR30 bit 0.

Figure 24 shows the external video BIOS ROM configuration interface for Lynx3DM+. The ~ROMEN (ROM Enable) signal from Lynx3DM+ connects to the OE and CE signals of the BIOS ROM. Since video BIOS ROM address and data are shared with the video memory data (MD) lines, programmers must ensure that the memory bus is inactive when reading from the Video BIOS ROM. For this case, the Video BIOS ROM must be read out and shadowed (typically in system memory at C0000) immediately after reset. Direct physical access to the Video BIOS must then be disabled to prevent interference with ensuing graphics operations.

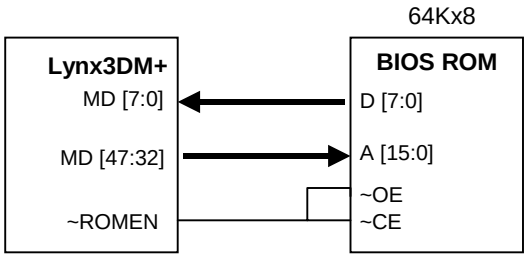


Figure 24: Video BIOS ROM Configuration Interface

VESA DPMS Interface

Lynx3DM+ supports the VESA Display Power Management Signaling (DPMS) via direct programming PDR22 (LCD Panel Control Select Register) bits 5, 4, or through implementation of the chip's power down states. Table 15 shows the VESA DPMS states and methods for entering each of the DPMS states.

Table 15: DPMS Summary

DPMS State	HSYNC State	VSYNC State	RGB State	Direct Programming Method	Power Down State Method
ON	Pulses	Pulses	Active	PDR22 [5:4] = 00	-
Standby	No pulses	Pulses	Blank	PDR22 [5:4] = 01	Automatic Standby DPMS state when enter Standby mode
Suspend	Pulses	No pulses	Blank	PDR22 [5:4] = 10	CCR69[2]=0 selects Suspend DPMS state when in Sleep mode
OFF	No pulses	No pulses	Blank	PDR22 [5:4] = 11	CCR69[2]=1 selects OFF DPMS state when in Sleep mode

I^2C Bus or VESA DDC2B Interface

Lynx3DM+ provides dual ports for I^2C-Bus through USR [3:0] I/O pins for various applications such as VESA's DDC2B monitor interface. It is recommended to use USR1 and USR0 as the primary port for SDA and SCL signals on I^2C Bus. USR3 and USR2 are reserved as a secondary port. GPR72 (User Defined Register 1) and GPR73 (User Defined Register 2) are defined to support I^2C/DDC2 bus protocol. Lynx3DM+, as an I^2C master controller only, is designed to initiate a transfer, generate clock signal, and terminate a transfer to a slave I^2C component.

Lynx3DM+'s I^2C-Bus interface is designed to interface with NTSC/PAL decoders, EEPROMs, audio decoders, and others. The operation voltage of USR [3:0] I/O pins is controlled by VPVDD, which can be configured as 5V or 3.3V. Each of the USR [3:0] I/O pins has an internal pull-up resistor. To enable the data (SDA) and the clock (SCL) from Lynx3DM+'s primary port, bit 5 and bit 4 of GPR72 (3C5h index 72h) must be set as "11". To drive a logic "0" to SDA line (USR1) and SCL line (USR0), program GPR72 bit 1 and bit 0 to "0". The SDA and SCL can be read back from bit 3 and bit 2 of GPR72.

Figure 25 shows the basic I^2C-Bus protocol of Lynx3DM+ as a master transmitter.

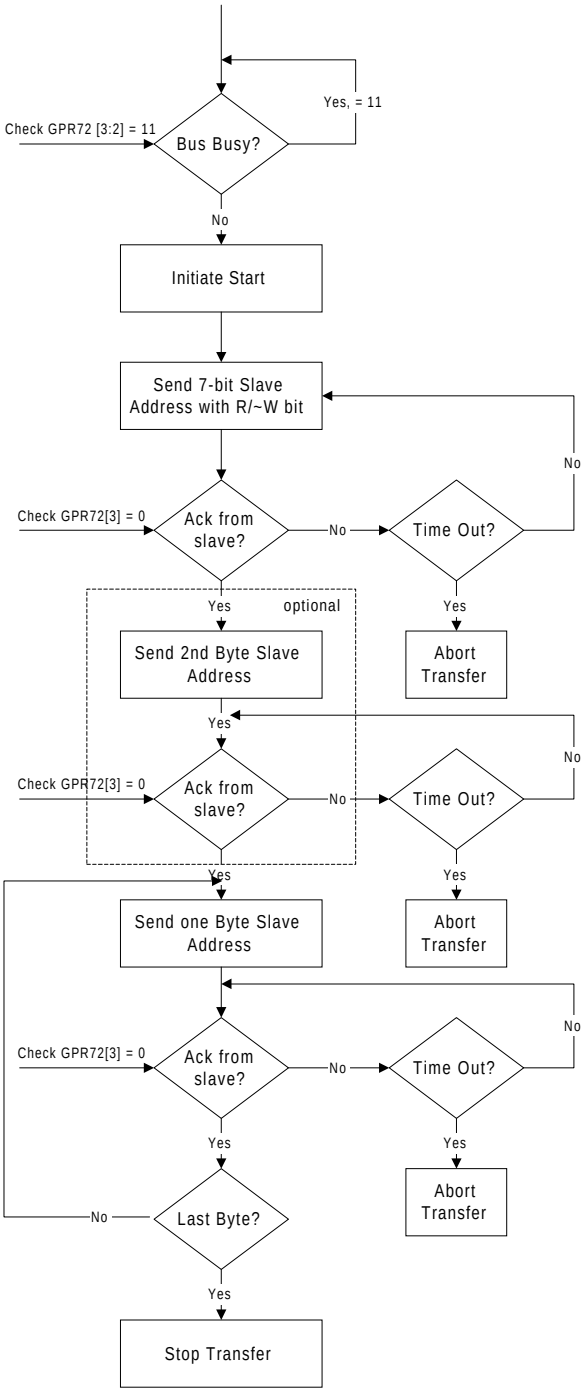


Figure 25: Lynx3DM+ I²C Bus Protocol Flow Chart

Chapter 11: Clock Synthesizers

Lynx3DM+ integrates three programmable clock synthesizers for memory clock (MCLK), Video Clock 1 (VCLK), and Video Clock 2(VCLK2). VCLK1 is utilized for standard CRT only, LCD only, or CRT/LCD display modes for which the refresh rate for both devices is the same. VCLK2 may be utilized when Virtual Refresh mode is implemented - for this case, VCLK1 is utilized for panel timing and to clock the panel display block within Lynx3DM+. VCLK2 may be utilized to clock the CRT interface independently for LCD/CRT display modes or to independently clock various functional blocks within the device to save power under LCD only display mode. Please see the Virtual Refresh discussion under the Power Management section for additional details regarding power saving capabilities under Virtual Refresh architecture.

Figure 26 illustrates the control logic for MCLK, VCLK, VCLK2. The figure also shows the clock generator module for WFIFO (WFIFOCLK), RFIFO (RFIFOCLK), RAM (RAMCLK), Video Capture (VCMCLK), Drawing Engine (DPMCLK), and Video Processor (VPCLK). TVCLK is used for an external analog TV encoder (this clock is either derived from 14.318MHz base clock - NTSC, or from separate 17.734480MHz clock source connected to input signal PALCLK - PAL).

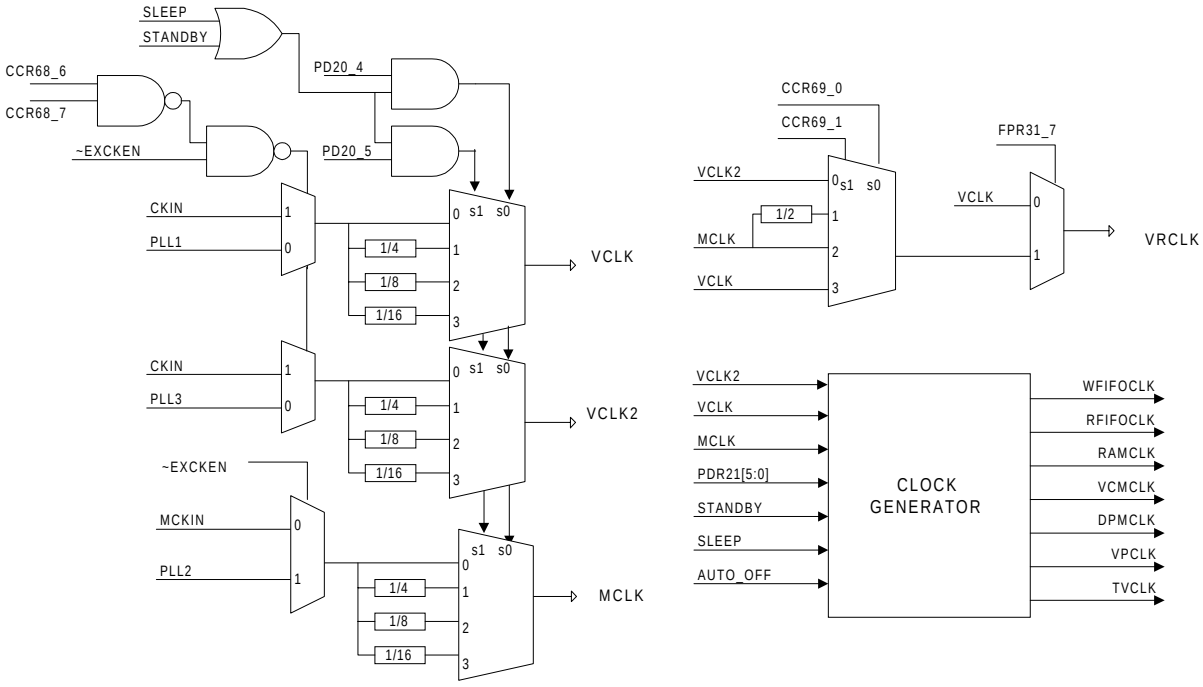


Figure 26: Clocks Generator Block Diagram

The VCLK PLL is programmed using the VCLK Numerator Register (VNR), CCR6C, and VCLK Denominator (VDR) and Post Scalar (PS) register, CCR6D. The VCLK frequency is based on the following equation:

$$VCLK = 14.31818\ MHz \cdot \frac{VNR}{VDR} \cdot \frac{1}{1+PS}$$

The post scalar is used to support VCLK frequencies which need a large VDR number. With PS enabled, the VDR number can be set to ½ of the original VDR number. This helps to reduce jitter and maintain accuracy.

The VCLK2 PLL is programmed using the VCLK2 Numerator Register (VCLK2NR), CCR6E, and VCLK Denominator (VCLK2DR) register CCR6F. The VCLK2 frequency is based on the following equation:

$$VCLK2 = 14.31818\ Mhz * \frac{VCLK2NR}{VCLK2DR}$$

Table 16: Recommended VNR and VDR Values for Common VCLK Settings

Mode	Ref. Rate	CCR68 [7]	CCR68 [6]	CCR68 [5]	3C2.3	3C2.2	VCLK (MHZ)	VNR	VDR
640x480	60Hz	0	01	0	0	0	25.180	33h	1Dh
720x400									
(text)	70Hz	0	0	0	0	1	28.325	5Bh	97h2
640x480	85Hz	0	0	1	0	0	31.500	2Ch	14h
800x600	56Hz	0	0	1	0	1	35.484	39h	17h
--	--	1	1	x	x	x	14.318	x	x
800x600	72Hz	0	1	x	x	x	49.517	53h	18h
1024x768	75Hz	0	1	x	x	x	78.750	6Eh	14h

Notes:
1. VNR and VDR numbers are hard coded in VGA modes.
2. Post scalar enabled.

The MCLK PLL is programmed using the MCLK Numerator Register (MNR), CCR6A, and MCLK Denominator Register (MDR), CCR6B. MCLK frequency is based on the following equation:

$$MCLK = 14.31818\ MHz \cdot \frac{MNR}{MDR}$$

Chapter 12: Multimedia RAMDAC

Lynx3DM+ contains a multimedia RAMDAC, which supports a maximum frequency of 200MHz (2.5V power supply). The multimedia RAMDAC includes two 256 x 18 color palette RAMs (RAM0 for CRT display, RAM1 for LCD display), RAM Sequencer, Hardware Cursor Registers (foreground and background), Hardware Pop-up Icon Registers (foreground and background), Data Mixer, Power-On Reset, Bias circuit, Monitor Detect circuit, and three 8-bit DACs (R, G and B). Anti-flicker logic for I/O read/writes is also built in the color palette RAM blocks. Figure 27 shows a block diagram of Lynx3DM+ Multimedia RAMDAC.

Lynx3DM+ uses an internal band gap voltage reference circuit to supply the reference voltage. This circuit automatically compensates for temperature and power supply variation. The external portion of the circuit consists of a single RSET resistor used to set the full scale voltage of RGB output from DAC.

The RAMDAC supports two types of modes, color palette index mode and direct color mode. In color palette index mode, the 8-bit input data of a given pixel goes to the color palette RAM block through VGA mask register. In direct color mode, pixel data bypasses the color palette RAM.

LCD Backend RAM (RAM1)

Lynx3DM+ includes a separate 18-bit RAM (6 bits each RGB) module for the LCD backend. The RAM allows support for color palette index modes for the LCD display. This RAM module is written concurrently with RAM0.

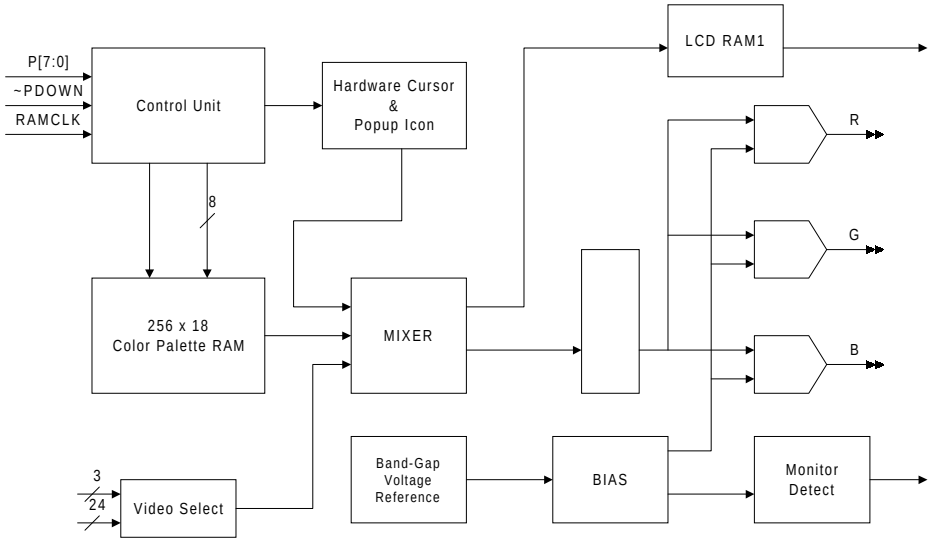


Figure 27: Lynx3DM+ RAMDAC Block Diagram

Chapter 13: Signature Analyzer

Lynx3DM+ includes several built-in test features to enhance testability and fault coverage. Lynx3DM+'s signature analyzer is designed to reduce LSI tester time and manufacturing test time. This signature analyzer resides within the Video Processor block and receives 24-bit RGB data from Multimedia RAMDAC block. It can be used to test CRT graphics modes, TV display modes, and motion video with single frame data. It can also be used to test data combinations such as: graphics, video 1, video 2, HW cursor, and HW pop-up icon at the same time.

The primary variables for a the signature analyzer are the length of the internal shift registers and the number of feedback terms. Lynx3DM+ implements the CRC-CCITT polynomial (X16 + X12 + X5 + 1) on a 16-bit signature shift register. VPR64 (Signature Analyzer Control and Status) register is used to define and control the operation of Lynx3DM+'s signature analyzer. Bit 3 is used as a Enable/Stop bit. Bit 2 is used as a Reset/Normal bit. Bit 1 and 0 are used to select 8-bit Red, Green, or Blue data from the 24-bit outputs of Multimedia RAMDAC. Bit 31 to bit 16 are used to read back the signature from the signature analyzer.

To turn on the signature analyzer, both bit 3 and bit 2 must be set as "11". The signature shift register will be reset to "0" as its initial value. On the rising edge of the 1st vertical sync pulse after VPR64 bit [3:2]=11, the state machine will start collecting signature data. Bit 2 is automatically reset to "0" at the same time. On the rising edge of the next vertical sync pulse, the signature analyzer stops and Bit 3 is automatically reset to "0". The test software can read back the 16-bit signature from Bit [31:16] to compare the golden signature for the test patterns. Figure 28 is a block diagram of the signature analyzer.

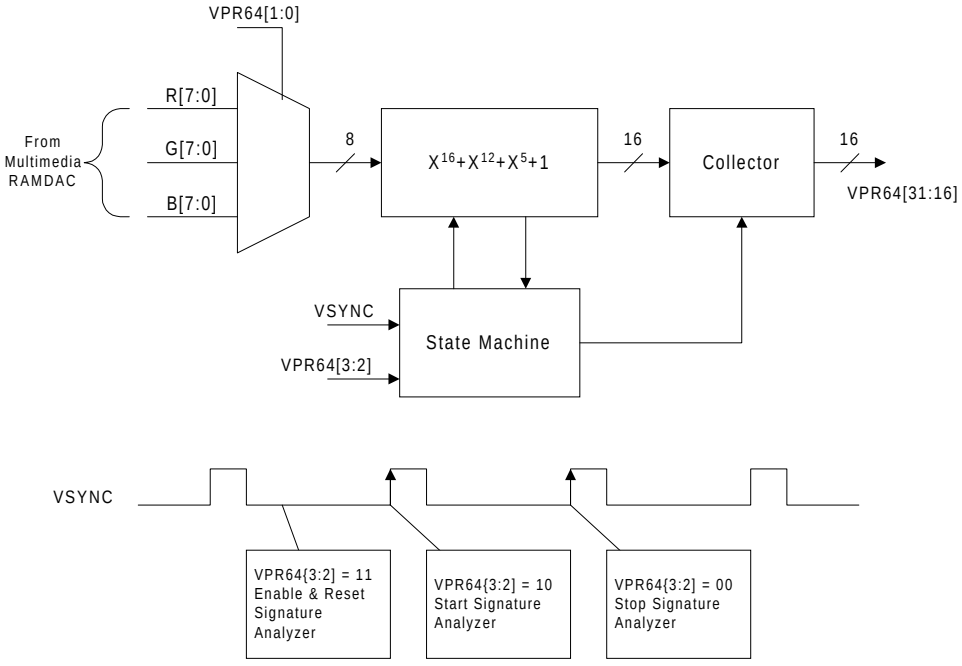


Figure 28: Signature Analyzer Block Diagram

Chapter 14: Power Management

Lynx3DM+ is designed to support ACPI requirements as defined in the PCI Bus Management Interface Specification 1.0 (PPMI v1.0) and Display device Class Power Management Specification v1.0a. Lynx3DM+ also supports a variety of adaptive power saving and clock management methods while in full operational mode. Finally, Lynx3DM+ supports traditional Standby and Suspend mode functionality for operating systems such as Windows 95 which do not have ACPI support built into the OS. A summary of these capabilities follows.

ACPI

Lynx3DM+ supports D0-D3 modes of operation via software programming of the Power Management Control/Status Register PMSCR[1:0]. As required by the PCI Bus Management Interface Specification, PCI Configuration Space Status Register (offset 06h) bit 4 is set to "1" to indicate new capabilities have been defined for Lynx3DM+. At offset 34h, the Cap_Ptr register stores the offset of the new capabilities (this register is hardwired to 40h). The first byte at offset 40h has a value of 01h, which indicates a Power Management capability (supports D1 and D2 states in addition to the required D0 and D3 power states). The second byte has a value of 00h indicating the no additional new capability features (Note: Lynx3DM+ does not offer support for optional ~PME capabilities as defined in PPMI v1.0).

Please refer to the PCI Bus Power Management Interface Specification 1.0 and Display Device Class Power Management Reference Specification v1.0a for additional details.

Display driver support for ACPI under Windows 98 and future versions of Windows 2000 will be provided by Silicon Motion in accordance with PC97 and PC98 requirements.

Adaptive Power Management

Lynx3DM+ provides intelligent power saving control during graphics/video operation. Two key methods through which power savings is achieved are Dynamic control of functional blocks, and dynamic clock control through Silicon Motion's Virtual Refresh architecture.

Dynamic Control of Functional Blocks

All major functional blocks within the device are laid out independently. There is no signal crossover between blocks. Special clock drivers are used to control each of the independent functional blocks. The clock drivers can be turned off by setting Power-Down Registers (PDR20 - PDR22), or by entering the internal auto-standby mode (PDR23 Bit 6). Functional blocks therefore can be turned on/off dynamically in response to how Lynx3DM+ is being utilized. Since the blocks shut down are unused functional blocks, this power saving feature is transparent to the end user.

Below are some programming recommendations for selected display configurations. These auto power saving features are implemented through video BIOS and system PMI. In addition to these display configuration recommendations, the drawing engine, ZV Port, video processor can be turned off through video driver control.

CRT is the only selected display

- Disable LCD frame buffer write operation (PDR21 bit 5 = 1)
- Disable LCD frame buffer read operation and DSTN dithering engine (PDR21 bit 4 = 1)

Color TFT is the only selected display with normal refresh

- Disable the DAC (PDR21 bit 7= 1)
- Disable LCD frame buffer write operation (PDR21 bit 5= 1)
- Disable LCD frame buffer read operation and DSTN dithering engine (PDR21 bit 4 = 1)

Color DSTN is the only selected display with Virtual Refresh

- Disable the DAC (PDR21 bit 7 = 1)
- Enable auto shut-down of display memory screen refresh cycle and LCD frame buffer write cycle (FPR31 bit 3 = 1)
- Set VCLK clock rate to 10 MHz (reduce clock rate to save power)

TV is the only selected display

- Set VCLK clock rate to 14.1 MHz and set interlaced mode (CRT30 bit 7 = 1)
- Disable LCD frame buffer write operation (PDR21 bit 5= 1)
- Disable LCD frame buffer read operation and DSTN dithering engine (PDR21 bit 4 = 1)

Dynamic Clock Control and Virtual Refresh

Dynamic clock control is made possible through Silicon Motion's Virtual Refresh architecture. Virtual Refresh is an intelligent architecture for dynamic clock control in LCD only mode, as well as independent display refresh control when multiple displays are enabled (e.g. CRT/LCD, TV/LCD). Virtual Refresh utilizes two independent clocks (VCLK, VRCLK): one clock, VRCLK drives the panel interface and maintains proper screen refresh. The second clock, VCLK is now independent of the panel and can be scaled according to user needs (e.g. scaled down for power savings, or scaled up to drive a higher refresh rate on CRT).

Virtual Refresh is enabled by setting FPR31 bit 7 to "1". When the LCD display is the only display viewed by the user, power saving can achieved via three key functions:

- Dynamically slows down the video clock (VCLK) to 25%~50% of the original clock rate
- Auto shut-down display memory screen refresh
- Auto shut-down the LCD write frame buffer

These functions can be automatically implemented when Lynx3DM+ detects the user has not performed any activity for selectable number of screen refresh cycles. Since a significant percentage of the logic is synchronized with VCLK, the average power consumption of the chip will drop dramatically. The LCD screen remains on with proper screen refresh, so the power savings is transparent to the end user.

Note: When multiple displays are used, Virtual Refresh architecture can also be used to simultaneously display CRT/TV and the LCD with different resolutions, and independent refresh rates.

Standard Power Management

Standby Mode

Lynx3DM+ supports Standby Mode in two ways: internal auto-standby and system standby from system PMI. The internal auto-standby is enabled and controlled by Activity Detection Register (PDR23). When the internal timer matches the selected condition (PDR23 bit [2:0]), Lynx3DM+ immediately enters standby mode Any CPU Memory or I/O access

to Lynx3DM+ will cause the device to exit standby mode, and reset as an internal counter timer. The system PMI can enable system standby mode by pulling Lynx3DM+'s "~PDOWN" signal low. (Note: To select standby mode, PDR20 bit 7 must be set to 0 before pulling ~PDOWN low) Lynx3DM+ will exit standby mode when "~PDOWN" goes high. When the system PMI standby is on, the internal auto-standby is ignored. Programming sequences for internal auto-standby and system standby follow.

Start Internal Auto-standby Mode

- PDR23 bit[7:6] = 11b
- PDR20 bit 7 = 0 to enter standby mode
- The internal timer count matches the setting from PDR23 bit[2:0]

Start System Standby Mode

- PDR20 bit 7 = 0 to enter standby mode
- "~PDOWN" input pin is driven low

Power Saving In Standby Mode

The standby mode is designed to provide an automatic power saving mechanism for the portable PC when the graphics display sub-system is idle for a short period of time. There is no need for BIOS or application software to program Lynx3DM+ registers. All power saving control are done by hardware. Both internal auto-standby and system PMI standby have the same power saving mechanisms listed below.

- Both memory clock and video clock switch to lower frequencies which are selected by bit [5:4] of PDR20 register
- Lynx3DM+ will continuously issue DRAM refresh cycles
- The following functional blocks are disabled (PDR21 bit 7, 5, 4, 3, 2, and 1)

  * DAC
  * LCD frame buffer write
  * LCD frame buffer read and DSTN dithering engine
  * Color Palette RAM
  * ZV Port
  * Drawing engine
  * Video processor

- LCD auto-power off sequence enabled
- VESA DPMS standby mode enabled

Sleep Mode

Sleep mode is the maximizes power-saving mode while maintaining display memory and register integrity. Sleep mode is selected when the whole system will be idle for a long period of time. All selected displays will be shutdown. PLLs can also be shutdown if the external 32 KHz refresh clock is selected (CCR69 bit 3 = 0) or memory self-refresh mode is selected. LCD panel on/off sequence will be done by simply programming the PDR22 register. The programming sequence for Sleep Mode follows.

Setting Before Entering Sleep Mode

- PDR20 bit 7 = 1 to enter sleep mode
- Set PDR20 bit 6 to select memory refresh type
- Set CCR69 bit 3 to select external or internal refresh clock

Enter Sleep Mode (Suspend)

- Power OFF the LCD panel if the LCD display is enabled. There are two ways to power OFF the LCD panel: hardware or software (selected by FPR34 bit 7). For software approach, the system PMI needs to program FPR34 bit 7 = 0 and PDR22 bit [3:0] to control FPEN, FPVDD, VBIAS,VBKLGT and panel interface pins. For hardware approach, one needs to program FPR34 bit 7 = 1 and panel ON/OFF timing select via FPR33 [3:2], then Lynx3DM+ will generate the proper panel sequencing.
- "~PDOWN" input pin is driven low. After ~PDOWN has been asserted for 2 vertical sync cycles, Lynx3DM+ will automatically shut-down the following blocks:

  * DAC
  * LCD frame buffer write
  * LCD frame buffer read and DSTN dithering engine
  * Color Palette RAM
  * ZV Port
  * 2D/3D drawing engine
  * Video processor
  * Memory screen refresh
  * Start power-down memory refresh cycle

Exit Sleep Mode (Resume)

- Drive "~PDOWN" input high. (200 ms after PLLs are turned on)
- After 200 ms, Power ON the LCD panel by either hardware or software. For software panel sequencing, enable LCD display by programming the PDR22 register. The whole system will be back to original state. For hardware panel sequencing, set FPR34 bit 7 = 1.

Activity Detection

The activity detection function is used to monitor Lynx3DM+ I/O and memory activity. System designer can select a fixed time period by programming PDR23 bit [2:0]. An internal timer will count the idle period of memory or I/O operation. If the idle period matches the selected value, Lynx3DM+ will generate a "Low-High" or "High-Low" signal to system through ACTIVITY output pin. Any Memory or I/O operation can reset the ACTIVITY signal and the internal counter.

After receiving the ACTIVITY signal from Lynx3DM+, the system power management unit can start Standby mode or Sleep Mode by pulling "~PDOWN" signal low. The activity detection function can also be used to enable internal auto-standby mode by setting PDR23 bit [7:6]. This power saving feature is independent of software and transparent to the end users.

Power-down Sleep Mode States

Table 17: Interface Signals Sleep Mode States

Signal Name	Sleep Mode
Host Interface	
AD [31:0]	tri-state
C/ ~BE [3:0]	tri-state
PAR	tri-state
~FRAME	tri-state
~TRDY	tri-state

Signal Name	Sleep Mode
~IRDY	tri-state
~STOP	tri-state
~DEVSEL	tri-state
IDSEL	x
CLK	x
~RST	H
~REQ	tri-state
~GNT	x
~INTA	tri-state
Power Down Interface	
~PDOWN	L
~CLKRUN	open-collector
Clock Interface	
REFCLK/PALCLK	x
CKIN	x
LVDSCLK	tri-state
~EXCKEN	H
Memory Interface	
MA [9:0]	H
MD [63:0]	H or L (note 2)
~WE	H
~RAS	L
~CAS	L
~CS [1:0]	L
~DQM [7:0]	H
DSF	L
BA	H
SDCKEN	L (self-refresh), H (CAS-b-RAS)
SCK	depends on PLL
~ROMEN	H
Flat Panel Interface	
FDATA [23:0]	L
FPSCLK	L
FPEN	L
FPVDDEN	L
VBIASEN	L
LP/FHSYNC	L

Signal Name	Sleep Mode
FP/FVSYNC	L
CRT Interface	
R, G, B	0 V
CRTVSYNC	L
CRTHSYNC	L
Video Port Interface	
P [15:0]	L
PCLK	H
VREF	H
HREF	H
BLANK/TVCLK	H
General Purpose Registers/I^2C	
USR3	H
USR2	H
USR1/SDA	H
USR0/SCL	H
Test Mode Pins	
TEST [1:0]	L

Notes:

1. This entry specifies when PDR20 bit 6 = 1 (self-refresh). When PDR20 bit 6 = 0 (CAS before RAS), both ~RAS and ~CAS control are based on 32K Hz refresh clock
2. MD lines have internal pull-up, therefore, without external pulldown resistors, MD lines will be at HIGH. With external pulldown resistors, MD lines will be at LOW.

Chapter 15: Motion Compensation Specification

Overview

The Motion Compensation block (MC) executes a series of instructions in a pipelined fashion. There is actually only one type of instruction with several flags that control the instruction execution. The MC instruction is similar to a CPU arithmetic instruction with three sources (imm - IMMediate operand, mrd - Memory ReaD and acc - ACCumulator) and one destination (mwr - Memory WRite). The main difference between standard CPU instructions and those used by the MC is that the MC instruction works on rectangular blocks of data instead of 8, 16, 32, or 64-bit integers.

The rectangular blocks of data (rectangles) used by the MC are 2-dimensional arrays containing 8-bit values. For the current implementation, the horizontal and vertical sizes (hsize and vsize) are limited to the following ranges: hsize = 8 or 16; vsize = 4 or 8. The MC requires one 128x16 SRAM for temporary storage of the input and output array values. It acts as a CPU accumulator.

The throughput of the MC pipeline is two pixels per cycle. Under worst case assumptions a MPEG-2 MP@ML picture will thus require 22 Mcycles/second.

Data Flow and External System Responsibilities

All instructions for motion compensation are generated by a software front-end and fed to the graphics controller via a standard software API. The instructions specify two different types of operations: (1) Memory accesses used for reading prediction data and writing reconstructed pels, and (2) Data processing operations used to combine predictions with the error terms generated by the IDCT operation.

The MC core handles all data processing operations required for motion compensation. The graphics memory controller handles the memory access operations. The memory controller must read the instructions generated by software, fetch prediction data, feed the data to the MC block and write the final reconstructed pels into the proper location.

MC Top Level Architecture

The top level architecture of the MC core is shown in Figure 29. It consists of a simplified quadrilinear filer (mc_qlf - this is the data path), a 128x16 dual port SRAM, and a controller (mc_ctl). The MC has four data busses: command (cmd), immediate operand (imm), memory read (mrd) and memory write (mwr).

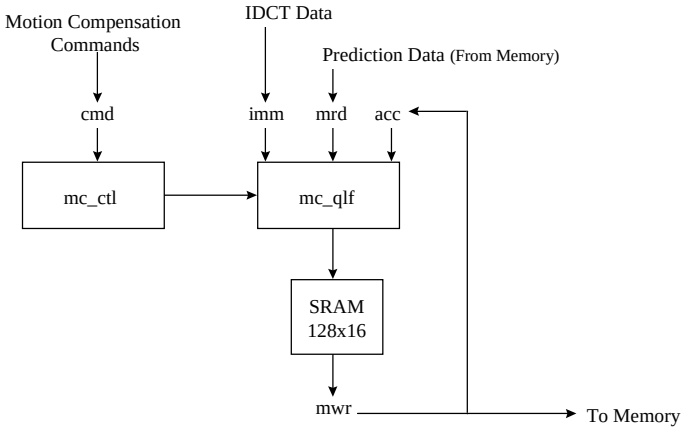


Figure 29: MC Top Level Architecture

In the current architecture all input and output busses are kept separate to offer the maximum processing throughput. Except for the command bus, all busses can operate continuously at one 16-bit or 18-bit value per cycle (two pixels/cycle). All busses use a rdy-ack protocol and can be stalled on any cycle.

For MPEG the IDCT output is fed through the imm bus and the prediction through the mrd bus. For bidirectionally interpolated macroblocks, first the forward prediction is read, half-pel interpolated, and stored in the 128x16 memory (block ACCumulator). Next, the backward prediction is read, half-pel interpolated, and added to both the acc (forward prediction) and imm (immediate or IDCT) data.

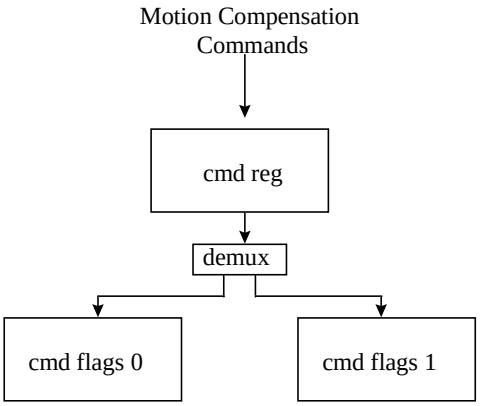


Figure 30: Control Block Diagram

Words from the cmd bus are loaded directly into the 16-bit cmd register as the command pipeline advances. The flags0 and flags1 registers each hold exactly one instruction each and together form a 2 instruction FIFO. One instruction is encoded as 2 or more 16-bit words, which means that it will take 2 or more pipeline advances before a flags register has accepted an entire instruction. Having 2 instructions queued at a time allows the MC to prepare an idle QLF pipeline with data ahead of time - before the current instruction has completed.

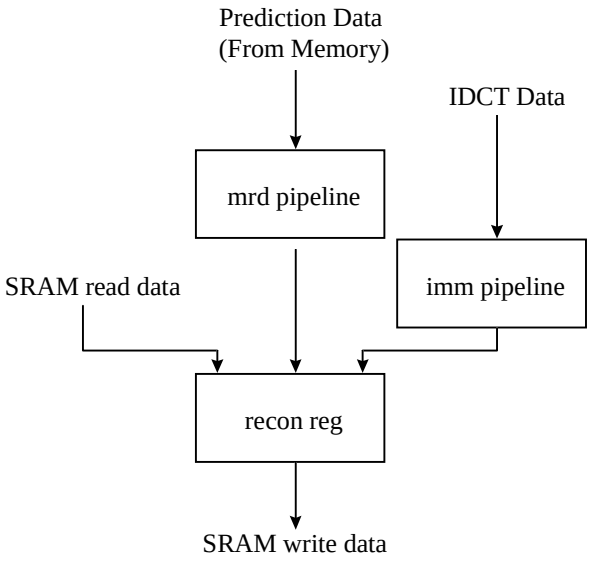


Figure 31: QLF Block Diagram

The Quadrilinear Filter consists of three pipelines, namely the acc, mrd, imm pipelines. The acc pipeline is not shown in block diagram because it consists of two stages external to the MC. The first stage is the synchronous SRAM read port while the second stage is a register that accepts SRAM read data. The width of this register matches the width of the reconstruction memory write back (mwr) data and is application dependent.

The mrd pipeline accepts prediction data from memory in a 16-bit wide format (2-pels). Pel alignment, horizontal half pel interpolation, and vertical half pel interpolation are handled in the pipeline.

The imm pipeline accepts IDCT data in a 18-bit (9-bit pel) or 16-bit (8-bit pel) format. The data is reformatted based on the flags in the current instruction.

Data from the three pipelines is combined and held in the reconstruction register. The data is added together, then saturated to values between 0 and 255. From this register the data is written to the local SRAM 16-bits (2 pels) at a time.

MC Instruction Format and Operation

Figure 33 shows the MC instruction format. The flags and parameters in the instructions are summarized in Table 18. All MC commands have the most significant bit (MSB) of word A set=1. Commands that have the MSB cleared=0, are intended for the memory controller or other control logic external to the MC. Currently, the only command with MSB=0 is used to indicate the end of stream:

	f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	0	0	10000					0	0	0	00000					0

Figure 32: End Stream Instruction

This End Stream command can occur anywhere in a command stream and should trigger an end to the command stream transfer. After this instruction is encountered by hardware, communication would then take place between hardware and the driver to determine what step to take next. This command is intended for logic external to the MC but should also be

passed on to the MC. The MC will see it as a Flush command and is required in order for the results from the last valid command to be written to memory.

The following table defines the format for MC instructions. Notice that the MSB of word A is set=1, indicating that this is an MC instruction.

	f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
A	1	-	ISL	IM8	MRD	IMM	ACC	MWR	THB	LHB	IH0	IH1	TVB	LVB	IV0	IV1
B	-	-	hsize [4:0]					HHP	-	-	vsize [4:0]					VHP
C	mrd_slot[1:0]		mrd_plane[1:0]		mrd_hadder [11:0]											
D	-			RVS	mrd_hadder [11:0]											
E	mrd_slot[1:0]		mrd_plane[1:0]		mrd_hadder [11:0]											
F	-			WVS	mrd_hadder [11:0]											

Figure 33: MC Instruction Format

Table 18: Instruction Flags and Parameters

Flag	Parameter	Meaning
ISL		Immediate Shift Left vs. sign extend left
IM8		IMmediate data 8-bits per pixel
MRD		Memory ReaD
IMM		IMMediate
ACC		ACCumulate
MWR		Memory WRite
THB		Two Horizontal Blocks
LHB		interLeaved Horizontal Blocks
IH0		Immediate operand for Horizontal block 0
IH1		Immediate operand for Horizontal block 1
TVB		Two Vertical Blocks
LVB		interLeaved Vertical Blocks
IV0		Immediate operand for Vertical block 0
IV1		Immediate operand for Vertical block 1
	hsize [4:0]	Horizontal SIZE
HHP		Horizontal Half Pel interpolation
	vsize [4:0]	Vertical SIZE
VHP		Vertical Half Pel interpolation
	mrd_slot [1:0]	Memory ReaD SLOT
	mrd_plane [1:0]	Memory ReaD PLANE
	mrd_haddr [11:0]	Memory ReaD Horizontal ADDRess
	mrd_vaddr [11:0]	Memory ReaD Vertical ADDRess

Flag	Parameter	Meaning
RVS	mrd_vstep	Memory ReaD Vertical STEP
	mwr_slot [1:0]	Memory WRite SLOT
	mwr_plane [1:0]	Memory WRite PLANE
	mwr_haddr [11:0]	Memory WRite Horizontal ADDRess
	mwr_vaddr [11:0]	Memory WRite Vertical ADDRess
RVS	mwr_vstep	Memory ReaD Vertical STEP

Each MC instruction consists of two, four or six 16-bit words. The first instruction, instruction A in Figure 33, contains the instruction flags. The second instruction contains the rectangle size. Depending on the flags in the first instruction, the remaining four instructions may or may not be present.

In instruction A, the most important flags are MRD, IMM, ACC, and MWR. These flags indicate what source operands are used and if the result should be stored to memory or to the accumulator (the 128x16 memory). All or none of these four flags can be set. If none of the source flags are set, the MC generates a rectangle of zeros.

If the MRD (Memory ReaD) flag is set, instructions C and D must be present. These instructions specify the address from which prediction data should be fetched. The memory slot (prediction slot) from which to read the data is given by the mrd_slot [1:0]. A slot contains one frame of video which can be broken down into two or three color planes: (Y, Cb, Cr) or (Y, Cb/Cr interleaved). Each color plane can be broken down into two fields. The top field is located in the even lines while the bottom field is located in the odd lines of the frame. The X-Y offset in the slot (frame) from which to fetch the data is given by the mrd_haddr [11:0} and mrd_vaddr [11:0]. The vertical step, mrd_vstep, indicates whether every line or every other line should be read from the slot. For frame prediction every line is read (mrd_vstep = 0) and for field prediction every other line is read (mrd_vstep = 1). The first line of a rectangle of prediction data is indicated by mrd_vaddr [11:0]. In field prediction (mrd_vstep = 1), which field the data must come from depends on the location the first line of the prediction rectangle. If that line is in the top field, then the data comes from the top field. Otherwise it comes from the bottom field.

The parameter mrd_plane (Memory ReaD PLANE) indicates which video plane is being processed (0=Y, 1=Cb, 2=Cr, 3=CbCr). For MPEG decompression the memory read plane, mrd_plane [1:0] and memorywrite plane, mwr_plane [1:0], are always equal. (Note: they are provided as different values to offer increased flexibility for other applications (read from one plane and write to a different plane).

If the MWR is set, instruction E and F must be present. These instructions specify the address to which the final computed pels should be written. Similar to the data read instructions, the write slot is indicated by mwr_slot [1:0]. The X-Y offset is indicated by mwr_haddr [11:0] and mdr_vaddr [11:0]. The mwr_vstep bit specifies whether or not to skip a line between successive rows written in the same way that the mrd_vstep does for the prediction data. In MPEG-2 decode, mwr_vstep setting reflects the motion type for the macroblock being processed.

In instruction B, if HHP is set, Horizontal Half Pel interpolation is performed and the mrd horizontal size shall be hsize pixels plus one. If VHP is set, Vertical Half Pel interpolation is performed and mrd vertical size shall be vsize rows plus one.

If the ACC flag is set, the MC adds the content of the ACCumulator (the 128x16 memory to be memory read data (if present).

If the IMM flag is set, the MC adds the immediate data, supplied on the imm bus, to the interpolated data, (mrd = acc)/2. The immediate data is the error term calculated by the IDCT. All the other nine flags have a meaning only if IMM is set.

IM8 indicates if the immediate data is only 8 bits wide. If IM8=0 the MC will accept IDCT data in a 9-bit per pixel format. MPEG-2 defines a range for IDCT data from -256 to =255 which is covered by a 9-bit two's complement number. A setting of IM8=1 indicates that the data is in an 8-bit per pixel format which approximates the full range. The ISL flag is used in conjunction with IM8 and differentiates between two 8-bit modes. ISL is ignored when IM8=0. 8-bit approximations allow data to be packed more efficiently into standard word widths. At issue is the sign bit. Intra-coded macroblocks never use the sign bit since values are restricted to the range of 0 to +255, while predicted to bidirectional IDCT values take the range of -256 to +255. For this reason, commands are separated into two different categories: intra-coded and non intra-coded.

If IM8=1 and ISL=0, the MC first determines the type of command currently being executed, then generates the sign bit based on the category. Intra-coded values are zero extended, while non intra-coded values are sign extended to the full 9 bits. Software that decodes the IDCT data must remove the sign bit in the intra-coded case while saturating the lower 7 bits and removing the 8th bit in the non intra-coded case. Non-intra coded data retains its sign bit since the saturation process results in a 8-bit twos complement number whose most significant bit represents its sign.

The IM8=1/ISL=0 setting will put an upper limit on the amount of correction that can be made to prediction data though. After the correction IDCT error terms can be no greater than =127 and no less than -128. As mentioned before, MPEG-2 specifies the range to be between +255 and -256. Under normal conditions values rarely exceed the smaller range since motion is relatively slow from picture to picture. When they do, it will be almost impossible for an observer to notice since the corrupted pels will be located in an area where a great deal of motion is occurring. In some rare cases though this range clipping can cause visible artifacts. They can be corrected though, with a second IMM data "pass". Instructions with settings of MRD=1, ACC=1 and IMM=1 calculate results as follows:

acc = (mrd+acc) / 2 = imm
Instructions with settings of MRD=0, ACC=1 and IMM=1 calculate results differently:

acc = acc + imm

This allows for a correction of IMM data terms that were saturated to the range of [-128, +127]. The first IMM pass would correct to this smaller range while the second pass would allow for a correction to a range of [-256 +254]. To reach a correction of +255, a third pass can be generated but would not be required very often.

If IM8=1 and ISL=1, the MC shifts the 8-bit IMM data left one bit before performing calculations with it. Intra coded an non-intra coded commands both treat the IMM data this way. Software must drop the least significant bit of the original 9-bit terms to convert to the format of the data required in this mode. This is the fastest way to generate 8-bit IMM data but will result in lower quality video. Images that contain large areas of a single color will suffer contour lines.

The remaining eight flags are needed to accommodate all possible combinations of coded_block_pattern and dct_type. The immediate data is present only if indicated by these flags. The term "reconstruction plane" in the following paragraphs refers to data that is written to the MC block's local SRAM as a result of a given command. Each reconstructed pel has a horizontal and vertical component that make up its position in the plane.

IH0 and IH1 indicate that the coded_block_pattern flag is set (IDCT data is present) for the one or two horizontal blocks that are processed. IH0 is used for the left most pels while IH1 is used for the right most. Pel locations in the reconstruction plane are assigned to one of the coded block pattern (cbp) bits, namely IH0, IH1, or IV1. IDCT data is only used in the reconstruction calculation for a given location when its cbp bit is 1. Otherwise, the IDCT data is either masked out or missing from the immediate data stream.

IV0 and IV1 are the cbp bits used when two vertical blocks are present. In MPEG terms, IV0 can be thought of as indicating that block Y2 is coded. IV1 can be thought of as indicating whether Y3 is coded. IDCT data is re-ordered to be combined with prediction data (MRD bus). For this reason, the cbp bits may not apply evenly to adjacent blocks as they

do in the MPEG bitstream. Their assignment to locations in the reconstruction plane reflect the change in the order of the IDCT data.

TVB indicates that Two Vertical Block as are processed at the same time. If TVB is high, IH0 and IH1 are used for the top half of the rows while IV0 and IV1 are used for the bottom half. In the top half, whether IH0 and IH1 is used will be dependent on the horizontal reconstruction pel position, THB and LHB. The same is true of IV0 and IV1 in the bottom half. TVB is not an indicator of the number of vertical rows for a command. The vsize [3:0] bits indicate this. Although if TVB is high, vsize [3:0] bits indicate this. Although if TVB is high, vsize [3:0] is used to determine the vertical half-way point for a command.

LVB indicates that two Blocks are Vertically interLeaved. This is needed when frame prediction and field DCT type data are used in a frame picture. When LVB is high, the even rows in the reconstruction plane are assigned to IH0 and IH1 while the odd rows are assigned to IV0 and IV1.

For MPEG related applications, TVB and LVB will never both be set high. A command generator that sets them both will not cause a failure in the MC though. The result will be a union of the two modes. The top half of the rows will be interleaved while the bottom half will not. All of the bottom rows will be assigned to the IV0 and IV1 cbp bits.

THB indicates that Two Horizontal Blocks are processed at the same time. When THB is high, either IH0 and IV0 will be assigned to the left most half of a reconstruction row, while IH1 or IV1 will be used for the right most half. In the left half, whether IH0 and IV0 is used will be dependent on the row number, TVB and LVB. The same is true of IH1 and IV1 in the right half. THB is not an indicator of the number of horizontal pels in a row. The hsize [4:0] bits indicate this. Although if THB is high, hsize [4:0] is used to determine the half-way point in a row.

LHB indicates that two Blocks are Horizontally interLeaved. This is needed when chroma (Cb and Cr) is stored in a single plane to save memory bandwidth. When LHB is high, the upper 9 or 8 bits of the imm [17:0] bus are interpreted as a Cb IDCT pel and IH0 and IV0 is used as a mask while the lower 9 or 8 bits are interpreted as Cr with IH1 or IV1 as a mask. When a coded block pattern bit is 0 the corresponding immediate data is masked to 0 before being used in reconstruction calculations. Unlike non-interleaved cases, data for the pels masked to 0 must be present in the immediate data stream even though their values are thrown out. When LHB is set high, the THB bit is ignored. Setting both bits high has the same effect as setting LHB high and THB low.

Chapter 16: 3D Engine

The Lynx3DM+ engine consists of a triangle setup engine, triangle fill engine, texture engine and pixel engine.

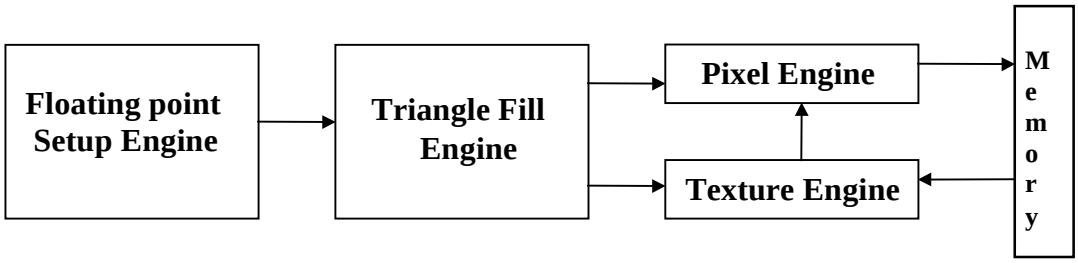


Figure 34: 3D Engine Block Diagram

IEEE 754 Floating Point Setup Engine

Lynx3DM+ incorporates a full triangle setup engine in hardware, relieving the host processor of these duties, as well as the need to transfer the setup data across the PCI Bus (43 double words per triangle). This frees up the host processor to perform tasks such as game logic and setting up data for the next frame. The result is higher triangle rates, and lower CPU utilization.

The setup engine computes triangle slope parameters (x, y, z, color (rgba) and texture parameters (s,t,w)). The triangle engine uses this information to walk along the edge of the triangle and generate span lines to be shaded or textured. Slope computation require divide operations in floating point to achieve maximum precision. The setup engine also performs subpixel correction (fractional adjustment calculations of the slope parameters to the pixel center) to eliminate polygon and texture misalignment.

The key components of the setup engine are 2 floating points units which work in parallel to perform triangle slope computations. In addition there is a hardware vertex sorting function to sort triangle vertices based on Y coordinates, as well as vertex transfer DMA to free the host CPU from transferring thousands of triangle vertices from host memory to the setup engine.

The vertex buffers within the setup engine (V0,V1,V2) consist of x,y,z,r,g,b,a,s,t,w (10) triangle parameters whose formats (floating point) are matched to Direct3D or OpenGL requirements. There is fixed to floating point format hardware conversion capability for color, as the data is specified as fixed point format in D3D.

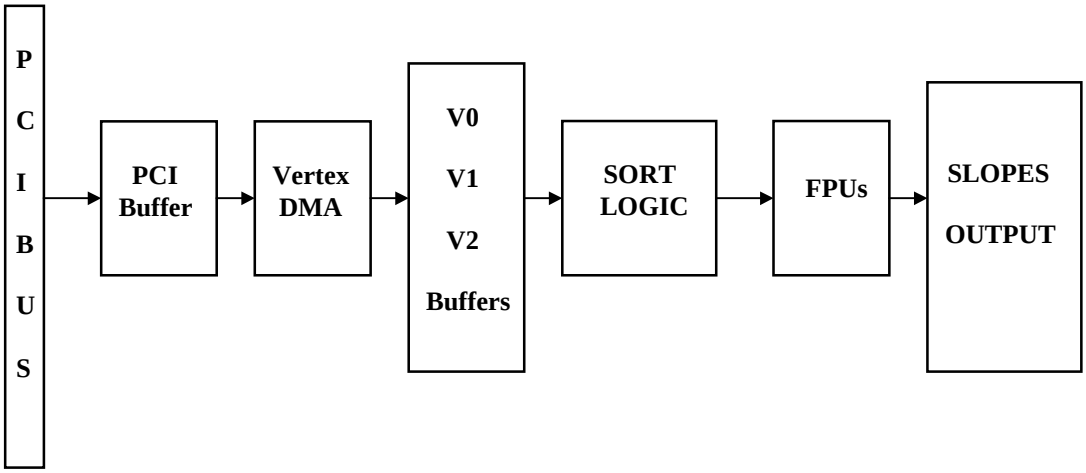


Figure 35: Setup Engine Block Diagram

Triangle Engine

The slope data from the triangle setup engine is passed to the edge walker within the triangle setup engine. The edge walker interpolates along the major edge of a triangle, generating horizontal Z, Gouraud and texture span lines simultaneously and calculating their starting values (RGBA and STW). The span engine interpolates the lines into pixels (Gouraud shading) and texels (via texture engine) to be combined (modulated, added, blended) in the pixel pipeline stages within the Pixel Engine.

Significant parallelism is achieved by running the span engine, texture engine and Z engine in parallel.

All pixel rendering is calculated internally as 32-bit RGBA data. Triangle engine supports 2 separate interpolators for diffuse and specular color.

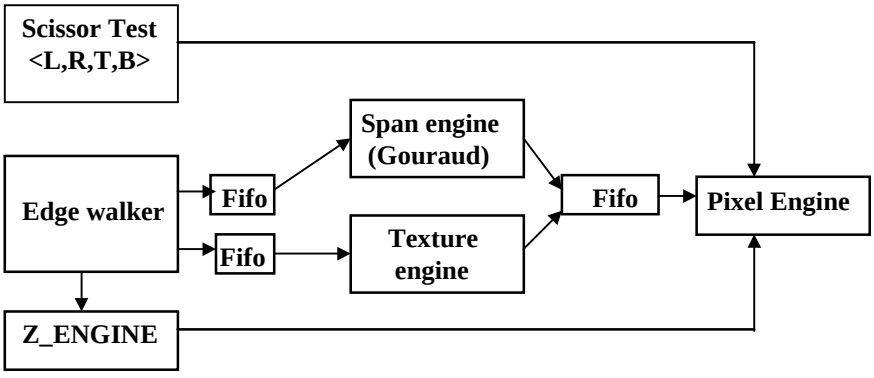


Figure 36: Triangle engine block diagram

Z Engine

The Z buffer (16bpp) process is performed in parallel with other triangle engine operations. The Z_engine whose output determines if pixel is to be drawn or not.

Z relational operation:

000 = Z disabled
001 = pass if Zi .GT. Zzb
010 = pass if Zi .EQ. Zzb
011 = pass if Zi .GE. Zzb
100 = pass if Zi .LT. Zzb
101 = pass if Zi .NE. Zzb
110 = pass if Zi .LE. Zzb
111 = Z always passes

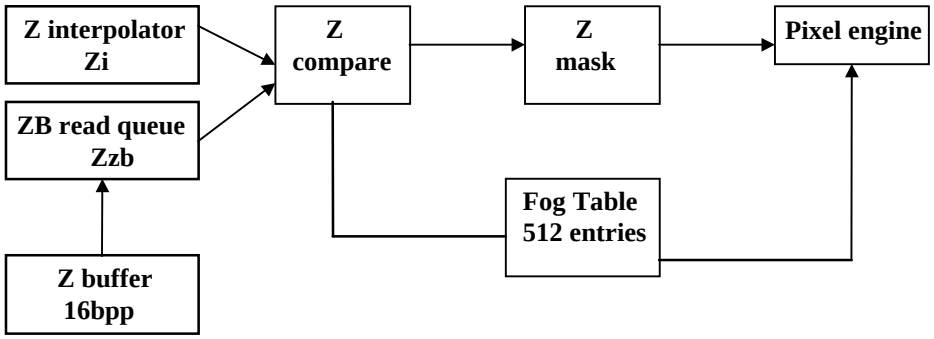


Figure 37: Z Engine Block Diagram

Texture Engine

Lynx3DM+ supports perspective correct texture mapping (divide per pixel), various texture filtering such as point sampling, bilinear, and trilinear mip-mapping (per pixel LOD) to eliminate texture aliasing.

Point sampling and bilinear texture filtering are done in a single pass. Trilinear mip-mapping and texture compositing (multiple texture map) are done in 2 passes.

Texture engine supports the following source texture formats: RGBA_8888, RGBA_4444, RGB_1555, RGB_565 and 8-bit color index with separate look up table.

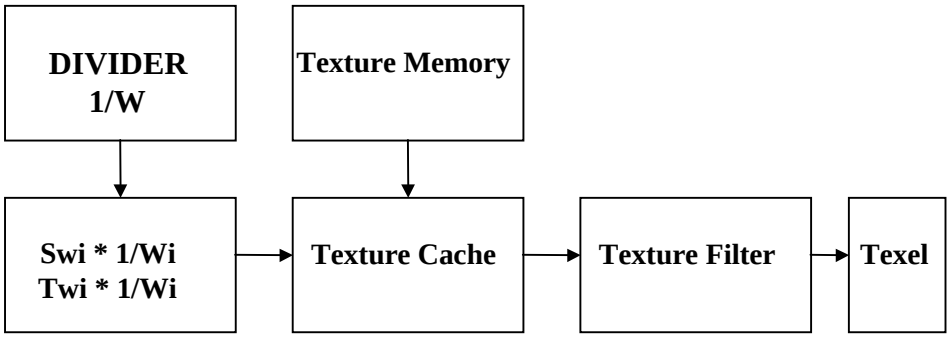


Figure 38: Texture Engine Block Diagram

Pixel Engine

The Pixel Engine consists of a series of pipeline stages (operations) to combine texture color and diffuse color (highlighting), add specular color, and create transparency and atmospheric fog/haze effects. In addition, the Pixel Engine performs edge anti alias to eliminate jaggedness.

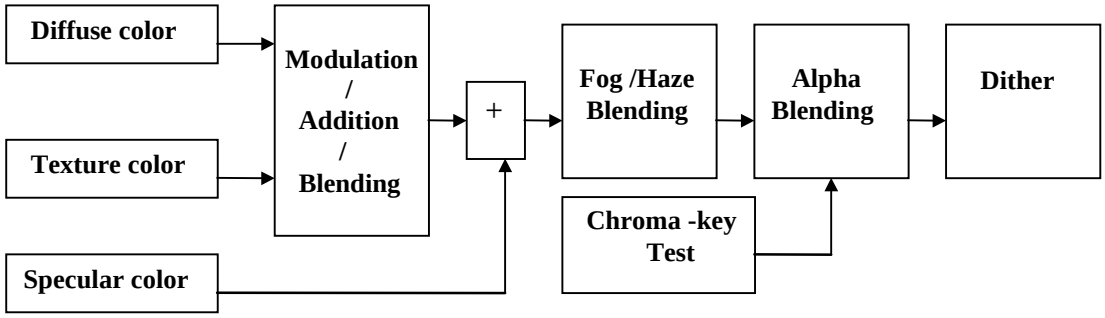


Figure 39: Pixel pipeline block diagram

Modulation/Addition Unit

Combine pixel (diffuse color) from gouraud span engine with texel from texture engine. Includes modulation (multiplication), addition and blending operations.

Fog Blending Unit

Fog blend factor per pixel is computed based on Z distance. Lynx3DM+ supports both local fog (fog blend factor is derived from iterated fog blend factor at vertex level) and global fog (fog blend factor is from fog table indexed by z at that pixel). Global fog gives more realistic effect as local fog tends to give fog band effect due to linearly interpolated fog factor at the vertex level.

Chroma-Key Test Unit

Chroma-key is used in conjunction with transparency (alpha blend). If enabled, the texel from texture engine is compared to the chroma-key value and if within range then the alpha blending factor is set to 0, which essentially means disable pixel write.

Alpha Blending Unit

The Alpha Blending unit blends incoming source pixels with destination pixels. One of the most common function of alpha blend is to create a translucent object. Lynx3DM+ supports most of the blend functions specified by microsoft D3D API and OpenGL.

Dithering Unit

The Dithering unit is used to improve 16-bit RGB (5:6:5) color representation on the display without actually storing the pixel data as 24 Bit data in the frame buffer. Dithering matrixes are used to represent the 16-bit RGB data as 24-bit RGB data on screen.

Chapter 17: TV Encoder

The TV Encoder is an NTSC/PAL Composite Video/S-video Encoder. It receives RGB inputs and converts to digital video signals based on CCIR 624 format.

The input video signal of the TV Encoder is RGB 8-bit each. The sampling rate is corresponding to CCIR 601, Square pixel and 4Fsc (NTSC only).

The output video signals of the TV Encoder are Composite video signal and S-video signals of 10-bit each. These output signals are over-sampled by a double frequency clock called CLKX2. This feature helps to simplify external analog filtering.

The TV Encoder video timing is controlled by vertical sync and the horizontal sync input signals. The blank signal input is optional. If the blank signal input signal is pulled up, internal blanking control will be performed.

Macrovision 7.01 and closed captioning functions are included.

Key Feature Summary

- NTSC/PAL interlace mode digital video encoder
- Composite Video and S-Video digital output
- CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- Slave timing operation
- Interlace mode operation
- 2x over-sampling data output to simplify external analog filtering
- Selectable pedestal level OIRE/7.5IRE for NTSC
- Macrovision function (version 7.01)
- Closed captioning function

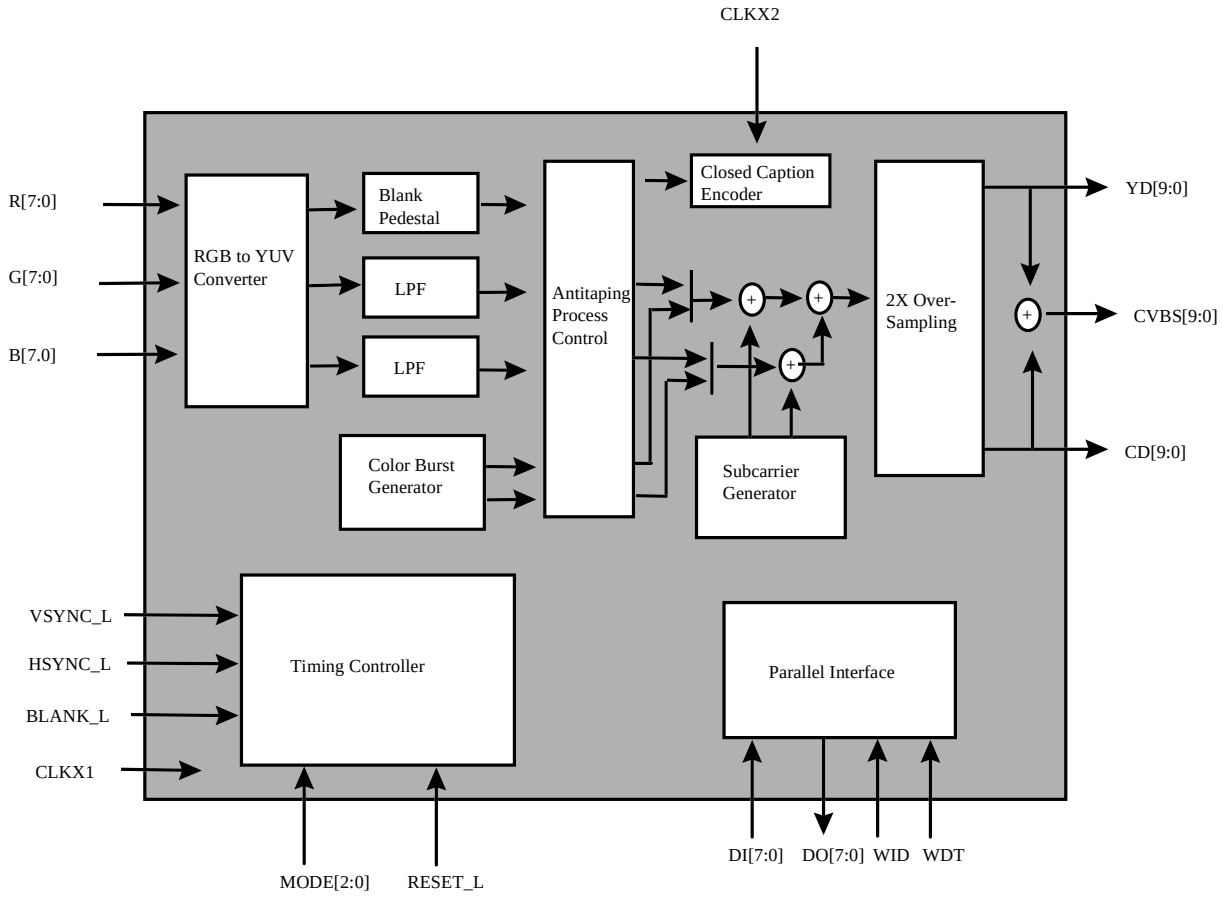


Figure 40: TV Encoder Block Diagram

Table 19: TV Encoder Block Interface Description

Excore-TV Encoder for SMI pin list

Pin name	Width	I/O	Description
R	8	I	4:4:4 sampled Red data This data should be synchronized to the CLKX1.
G	8	I	4:4:4 sampled Green data This data should be synchronized to the CLKX1.
B	8	I	4:4:4 sampled Blue data This data should be synchronized to the CLKX1.
VSYNC_L	8	I	Vertical sync input, active low This goes low during the vertical sync intervals.
HSYNC_L	1	I	Horizontal sync input, active low This goes low during the horizontal sync intervals.
BLANK_L	1	I	Composite blanking input, active low. This goes low during the composite blanking intervals. If this signal is low, the RGB input data will be masked.
CLKX1	1	I	Pixel rate clock input This clock should be free-running, and will be synchronized to the CLKX2.

Pin name	Width	I/O	Description
CLKX2	1	I	2X Pixel rate clock input This clock should be free-running.
MODE	3	1	Mode select When MR[7] is set to 1, the mode is controlled by these input pins, otherwise the mode register (MR) setting will be taken. 000: NTSC CCIR 100: PAL CCIR 001: NTSC Square Pixel 101: PAL Square pixel 010: NTSC 4Fsc
RESET_I	1	I	Reset input, active low
MV_EN	1	I	Macrovision function Enable
DI	8	I	Parallel I/F data input
DO	8	0	Parallel I/F data output
WID	1	I	Parallel I/F index strobe
WDT	1	I	Parallel I/F data strobe
CVBS	10	O	S-video Luminance data output
YD	10	O	Composite video data output
CD	10	O	S-video Chrominance data output

Function Descriptions

Video data input and sampling rate

The video input data is RGB. Each R, G, or B data is an 8-bit value. The range for the data is 0 to 255 respectively. The data is latched at positive edge of the CLKX1.

The TV Encoder supports the following sampling rates:

Table 20: TV Encoder Sampling Rates

Video Mode		Frequency	Total pixel/line	Total lines/frame
NTSC	CCIR 601	13.5 MHz	858	525
	Square pixel	12.27 MHz	780	525
	4Fsc	14.32 MHz	910	525
PAL	CCIR 601	13.5 MHz	864	625
	Square pixel	14.75 MHz	944	625

Macrovision Antitaping process

The TV Encoder supports the Macrovision Antitaping process function (U7.01). Macrovision involves 3 functions which are the colorstripe process, Pseudo Sync/AGC pulses with sync pulse amplitude reduction and EOF back porch pulses.
If the same line is assigned for closed captioning and the Macrovision process, all Macrovision functions at the line are disabled for the closed captioning function.

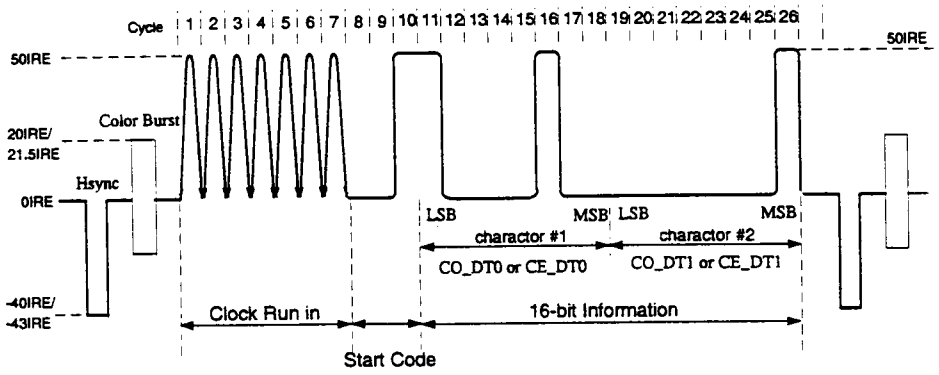
The color stripe process function is applied to the composite video output and the Chrominance signal output. This activated by MCR0[3] and controlled by MCR1 to MCR7 and MCR16 to MCR21. This function controls the color burst length and polarity. When this process is invoked during the burst blanking lines, no color burst signal is put. When the color burst length is assigned beyond the active video time, the color burst completes at the end of the blanking time. Active video data then starts. The blanking time is controlled by the BLANK-L input pin and internal blanking.

The Pseudo Sync/AGC pulse function is applied to the composite video output and the S-video Luminance output. The Pseudo Sync pulse is applied to the Luminance signal. The AGC pulses is a super-white positive going pulse. Both of these pulses are output after color burst signal. The Sync Pulse amplitude reduction changes the synchronizing level. This function is activated by MCR0[5] and MCR0[1:0], and controlled by MCR0[2], MCR8 to MCRI4.

The EOF back porch pulse function generates a high level signal immediately after the trailing edge of the H-sync pulse. The value is 100IRE for NTSC mode and 7OOmV for PAL mode. This function is activated by MCR0[4], and controlled by MCR[15].

Closed Captioning

The closed captioning function is applied to the Luminance data, and is shown at the composite video output and the S-video Luminance output as follows. The level and timing corresponds to the EIA standard EIA-608.



This function is controlled by the closed captioning registers. The closed captioned line is controlled as follows.

Table 21: Closed Captioning Lines

Video Mode	Odd field	Even field
NTSC	CCL + 4	CCL + 263 + 4
PAL	CCL + 1	CCL + 313 + 1

When the closed captioning function is enabled by the CCEN register, the captioning data will be placed on the assigned line. When there is new data, the TV Encoder outputs the new data. When there is no new data, a null code (80h) will be output.

The odd field and even field are controlled separately. When one of 2 odd (even) data registers is written, the TV Encoder recognizes new data for odd (even) field. The status bit OST(EST) is set to 1. For normal usage, the new data is written when the status bit is 1.

Table 22: Closed Captioning Odd Field Output Data

Enable	Status	1st Output Data	2nd Output Data
CCE[0] = 0	-	no data	no data
CCE[0] = 1	OST = 0	CO_DT0	CO_DT1
CCE[0] = 1	OST = 1	80 (hex)	80 (hex)

Table 23: Closed Captioning Even Field Output Data

Enable	Status	1st Output Data	2nd Output Data
CCE[0] = 0	-	no data	no data
CCE[0] = 1	EST = 0	CO_DT0	CE_DT1
CCE[0] = 1	EST = 1	80 (hex)	80 (hex)

Video data output and Over-sampling

The TV Encoder outputs composite video, Luminance and Chrominance signals. These outputs have 10-bit each, and are 2X over-sampled by the double frequency clock designated CLKX2. This over-sampling simplifies external analog filtering. The output level and timing depend on the mode selected.

Synchronization

This TV Encoder operates in a slave mode. This means that the vertical sync and the horizontal sync are required for operation. The blanking signal is optional. The TV Encoder will calculate the composite blanking time using the sync information. If the blank signal BLANK-L is pulled up, input data at the blanking time will be masked by the internal blanking signal. When the blanking signal is controlled, it's possible to shorten the active time for the input data. The TV Encoder will mask the input data when the BLANK-L is low. The TV Encoder automatically detects the Odd/Even field by sync information.

Sub-carrier Generation

The sub-carrier is internally generated using CLKX1. Depending on the sampling rate, the TV Encoder will automatically calculate exact frequency. The sub-carrier phase is reset under the following conditions:

- RESET-L is low.
- The first field changes to field 1 after RESET- goes high.
- The first field changes to field 1 after the TV Encoder detects the mode change.
- When genlock control is on. For this case, the sub-carrier phase will be reset on every 4 fields for NTSC mode and 8 fields for PAL mode.

Parallel bus I/F

For internal register access, the parallel bus I/F is used. When the write index signal designated WID is high, the register address is latched. When the write data signal designated WDT is high, the data will be written to the latched address.

Chapter 18: Register Overview & Usage

There are generally 3 types of registers:

PCI Configuration Registers

The PCI Configuration registers are listed in Chapter 19: PCI Configuration Space Registers and accessed via the standard PCI read/write protocols specified in the PCI specification.

Memory Mapped I/O Registers

All the I/O mapped registers within Lynx3DM+ have been designed to be memory mapped as well. They are listed in Chapter 20: Standard VGA Registers and Chapter 21: Extended SMI Registers. “I/O” or “Memory” Mapping is selected through PCI configuration registers CSR04 bit 0 and bit 1.

- Access via “I/O” space is done by first writing the index value into the I/O register 3C4. Thereafter, the indexed register can be accessed via I/O read/write to I/O address 3C5

  Example: Register with Index 0/H
  I/O write 0/H to 3C4
  I/O read/write to/from 3C5

- The procedure to access these registers via “Memory” Mapped space is similar to “I/O” space in that the index register is moved to memory address C0xxx and the access register is moved to C0xxx (where “xxx” represents the VGA control numbers.

  Example: Register with Index 0/H
  Memory write 0/H to C03C4
  Memory read/write to/from C03C5

Memory Mapped Registers

All the advanced functions of Lynx3DM+ are controlled through Memory Mapped registers. Such as the 2D and 3D Motion Comp Registers in Chapter 22: 2D & Video Registers, Chapter 23: Motion Comp Video Registers, Chapter 24: PCI Bus Master Control Registers, Chapter 25: 3D Registers, and Chapter 26: TV Encoder Registers. The following diagram illustrates the Memory Mapped register address assignment.

I/O Mapped Register Mapped Summary

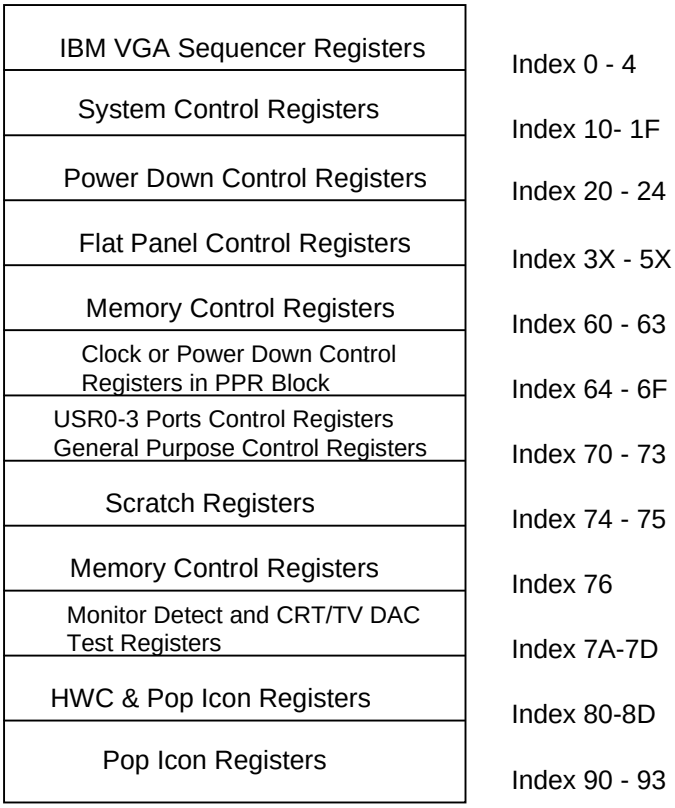


Figure 41: I/O Port 3C4

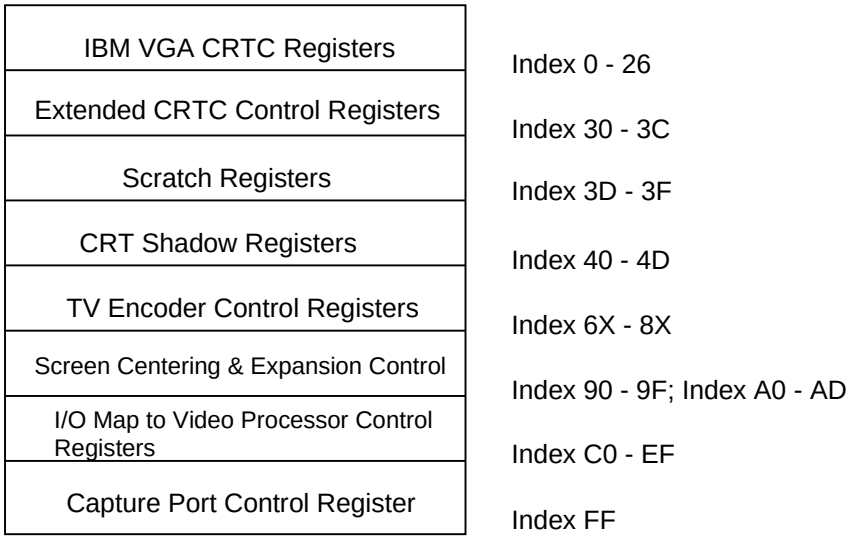


Figure 42: I/O Port 3?4

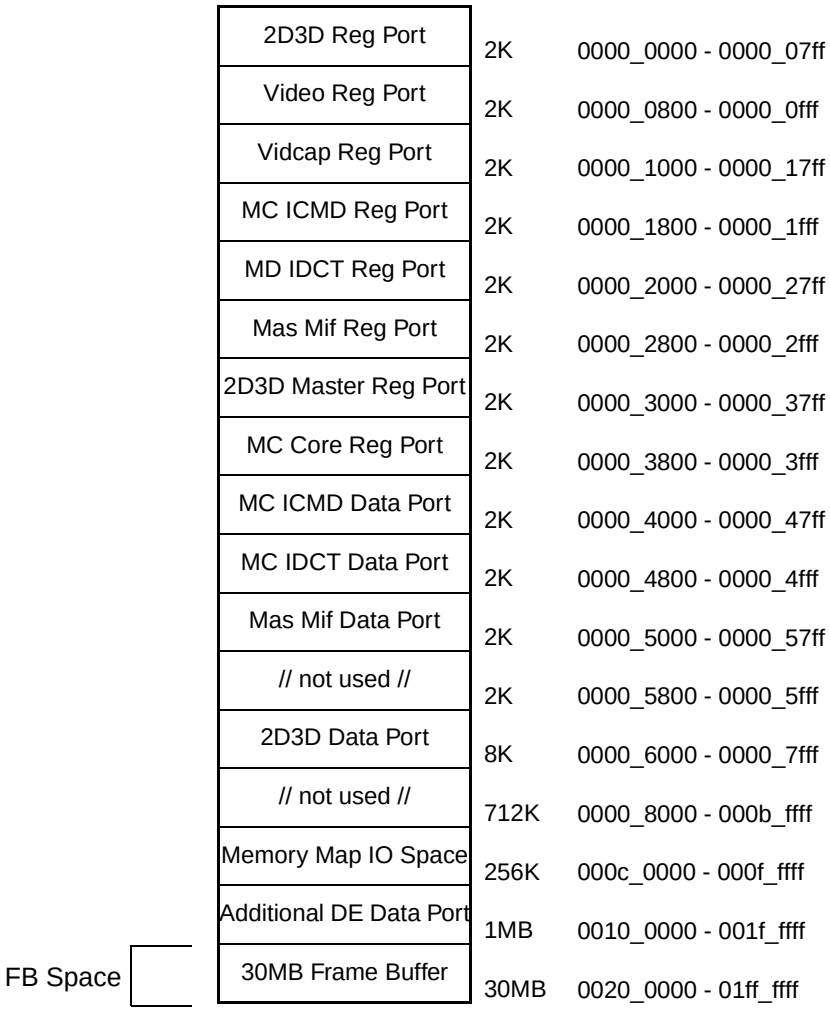


Figure 43: Memory Mapped Address Diagram

Chapter 19: PCI Configuration Space Registers

Table 24: PCI Configuration Registers Quick Reference

PCI Configuration Space Registers

The PCI specification defines the configuration space for auto-configuration (plug-and-play), device and memory relocation.

CSR00: Vendor ID

Read Only Address: 00h
Power-on Default: 126Fh

This register specifies the vendor ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR ID															

Bit 31:16 Reserved

Bit 15:0 Vendor ID
This register is hardwired to 126Fh to identify as Silicon Motion®, Inc.

CSR02: Device ID

Read Only Address: 02h
Power-on Default: 0720h

This register specifies the device ID.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DEVICE ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit 31:16 Device ID
This register is hardwired to 0720h to identify the device as Lynx3DM++.

Bit 15:0 Reserved

CSR04: Command

Read/Write Address: 04h Note: Reserved bits are read only
Power-on Default: 00h

This register controls which types of PCI command cycles are supported by Lynx3DM++.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										**PSE**	**MWR**	**R**	**PCI**	**MS**	**IO**

Bit 31:6 Reserved

Bit 5 Palette Snooping Enable (PSE)
0 = Disable
1 = Enable

Bit 4 Memory Write Invalidate Enable for PCI master (MWR)
0 = Disable
1 = Enable

Bit 3 Reserved (R)

Bit 2 PCI Master Enable (PCI)
0 = Disable
1 = Enable

Bit 1 Memory Space Access Enable (MS) (Note: This bit needs to be set to "1" in order to enable BIOS addressing decoding)
0 = Disable
1 = Enable

Bit 0 I/O Space Access Enable (IO)
0 = Disable
1 = Enable

CSR06: Status

Read Only Address: 06h
Power-on Default: 20h

This register controls device select timing status, detect parity status, and detects target abort status for Lynx3DM++. In order to clear any bit of this register, you must write a "1" to that particular bit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	**RESERVED**		**DTA**	**R**	**TS**		**RESERVED**								

Bit 31:16 Reserved

Bit 15 Detect Parity Error (DPE)

Bit 14:13 Reserved (R)

Bit 12 Detect Target Abort for Master Mode (DTA)

Bit 11 Reserved (R)

Bit 10:9 ~DEVSEL Timing Select (TS)
01 = medium speed (hardwired)

Bit 8:0 Reserved

CSR08: Revision ID and Class Code

Read Only Address: 08h
Power-on Default: 030000A0h

This register specifies the silicon revision ID and the Class Code that the silicon supports.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE CLASS CODE								**SUBCLASS CODE**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG LEVEL PROGRAMMING INTERFACE								**REVISION ID**							

Bit 31:24 Base Class Code
03h = for Video Controller

Bit 23:16 Subclass Code
00h = VGA

Bit 15:8 Register Level Programming Interface
00h = hardwired setting

Bit 7:0 Revision ID
For example, A0h = revision A; B0h = revision B

CSR0D: Latency Timer

Read Only Address: 0Dh
Power-on Default: 00h

This register specifies the latency timer that Lynx3DM++ supports for burst master mode.

7	6	5	4	3	2	1	0
LATENCY TIMER							

Bit 7:0 Latency Timer for burst capable master

CSR10: Memory Base Address Register

Read/Write Address: 10h (Note: Reserved bits are read only)
Power-on Default: 00h

This register specifies the PCI configuration space for address relocation

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LINEAR ADDRESSING MEMORY BASE						**RESERVED**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**MSI**

Bit 31:26 Linear Addressing Memory Base Address. Memory segment allocated within 64 MB boundary

Bit 25:1 Reserved

Bit 0 Memory Space Indicator (MSI) (Read only)
0 = memory base

CSR2C: PCI Configuration Space Subsystem Vendor ID

Read Only Address: 2Ch
Power-on Default: 00h

This register specifies the Subsystem device ID.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM DEVICE ID															

Bit 15:0 Subsystem ID. This System ID is written by system BIOS during POST

CSR2E: PCI Configuration Space Subsystem ID

Read Only Address: 2Eh
Power-on Default: 0720h

This register specifies the Subsystem Vendor ID.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM VENDOR ID															

Bit 15:0 Subsystem Vendor ID

CSR30: Expansion ROM Base Address

Read/Write Address: 30h
Power-on Default: 00h

This register specifies the expansion ROM base address. Note: Reserved bits are read only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM BASE ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**BIOS**

Bit 31:16 ROM Base Address. Memory segment allocated for BIOS ROM in 64KB boundary [15:0]

Bit 15:1 Reserved

Bit 0 BIOS Address Decode Enable. This bit is valid only if memory space access is enabled. (CSR04 bit 1 = 1)
0 = Disable
1 = Enable

CSR34: Power Down Capability Pointer

Read Only Address: 34h
Power-on Default: 40h

This register contains the address where PCI power down management registers are located

7	6	5	4	3	2	1	0
CAPABILITY POINTER/PCI POWER DOWN MGMT							

Bit 7:0 Capability pointer contains the address where PCI Power Down Management Register are located.

CSR3C: Interrupt Line

Read/Write Address: 3Ch
Power-on Default: 00h

This register specifies the PCI Interrupt Line.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bit 7:0 Interrupt Line

CSR3D: Interrupt Pin

Read Only Address: 3Dh
Power-on Default: 01h

This register specifies the PCI Interrupt Pin.

7	6	5	4	3	2	1	0
RESERVED							IP

Bit 7:1 Reserved

Bit 0 Interrupt Pin (IP) (~INTA)

CSR40: Power Down Capability Register

Read Only Address: 40h
Power-on Default: 0601_5001h

This register contains the address where PCI power down management Capabilities.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI POWER DOWN MANAGEMENT CAPABILITY (0601h)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT CAPABILITY POINTER LINK LIST								**PCI POWER DOWN MGMT CAPABILITY (01h)**							

Bit 31:16 PCI Power Down Management Capability = 0601h
Offset 2

Bit 15:8 Next Capability Pointer Link List = 50h
Offset 1

Bit 7:0 PCI Power Down Management Capability ID= 01h
Offset 0

CSR44: Power Down Capability Data

Read/Write Address: 44h
Power-on Default: 00h

This register contains the address where PCI power down management Control, Status and Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI POWER DOWN MGMT CONTROL/STATUS															

Bit 31:24 Data
Read Only. Offset 7

Bit 23:16 Reserved =00
Offset 6

Bit 15:0 PCI Power Down Management Control/Status
Offset 4

CSR50: AGP Capability Pointer

Read/Write Address: 50h
Power-on Default: 02h

7	6	5	4	3	2	1	0
AGP CAPABILITY POINTER							

Bit 7:0 AGP Capability Pointer

CSR51: Next Capability Pointer

Read/Write Address: 51h
Power-on Default: 00h

7	6	5	4	3	2	1	0
NEXT CAPABILITY POINTER							

Bit 7:0 Next Capability Pointer

CSR52: Major Minor Revision

Read/Write Address: 52h
Power-on Default: 00h

7	6	5	4	3	2	1	0
MAJOR MINOR REVISION							

Bit 7:0 Major Minor Revision

CSR53: Reserved

Read/Write Address: 53h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED							

Bit 7:0 Reserved

CSR54: AGP Status Pointer

Read Only Address: 54h
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQUEST DEPTH								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**SBA**	**RESERVED**			**4GS**	**FWE**	**R**	**DATA RATE**		

Bit 31:24 Request Depth

Bit 23:10 Reserved

Bit 9 Side Bus Addressing Enabled (SBA)

Bit 8:6 Reserved

Bit 5 4 GB Support

Bit 4 Fast Write Enabled

Bit 3 Reserved (R)

Bit 2:0 Data Rate

CSR58: AGP Command Register

Read/Write Address: 58h
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQUEST DEPTH								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**SBA**	**AGP**	**RESERVED**		**4GS**	**FWE**	**R**	**DATA RATE**		

Bit 31:24 Request Depth

Bit 23:10 Reserved

Bit 9 Side Bus Addressing Enabled (SBA)

Bit 8 AGP Enabled

Bit 7:6 Reserved

Bit 5 4 GB Support

Bit 4 Fast Write Enabled

Bit 3 Reserved (R)

Bit 2:0 Data Rate

Extended SMI Registers

LOCK: Extended Register Write Protect Control

Read/Write Address: 3C3h
Power-on Default: 00h

This register specifies write protect controls for the SMI extended registers. SMI extended registers are write-protected. In order to write to the SMI extended registers, one must write Bit [7:5] = 010b.

7	6	5	4	3	2	1	0
WPE			**RESERVED**				

Bit 7:5 Write Protect Enable (WPE)
101 = All SMI Extended registers are Write-Protected
010 = Enable writes to SMI Extended registers
Others = Maintain previous state

Bit 4:0 Reserved

Chapter 20: Standard VGA Registers

Table 25: Standard VGA Registers Quick Reference

Standard VGA Registers

In the following registers description, a '?' in an address stands for a hexadecimal value of either 'B' or 'D'. If Bit 0 of the Miscellaneous Output Register is set to 1, the address is based at 3Dxh for color emulation. If Bit 0 of the Miscellaneous Output Register is set to 0, the address is based at 3Bxh for monochrome emulation.

General Registers

MISC: Miscellaneous Output Register

Write Only Address: 3C2h
Read Only Address: 3CCh
Power-on Default: 00h

7	6	5	4	3	2	1	0
VSP	**HSP**	**OEM**	**R**	**VIDEO CLOCK**		**EVR**	**IO**

Bit 7 Vertical Sync Polarity Select (VSP)
0 = positive vertical sync polarity
1 = negative vertical sync polarity

Bit 6 Horizontal Sync Polarity Select (HSP)
0 = positive horizontal sync polarity
1 = negative horizontal sync polarity

Bit 5 Odd/Even Memory Page Select (OEM)
0 = Select lower 64K page of memory
1 = Select upper 64K page of memory

Bit 4 Reserved (R)

Bit 3:2 Video Clock Select
00 = Select 25.175MHz for 640 dots/line mode
01 = Select 28.322MHz for 720 dots/line mode
10 = Reserved (enable external clock source)
11 = Reserved (enable external clock source)

Bit 1 Enable Video RAM Access from CPU (EVR)
0 = Disable Video RAM access from CPU
1 = Enable Video RAM access from CPU

Bit 0 I/O Address Select (IO)
0 = Select monochrome mode. Address based at3Bxh.

1 = Select for color mode. Address based at 3Dxh

ISR0: Input Status Register 0

Read Only Address: 3C2h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
CRT	**RESERVED**		**MDS**	**RESERVED**			

Bit 7 CRT Vertical Retrace Interrupt (CRT)
0 = Vertical Retrace Interrupt is cleared
1 = Vertical Retrace Interrupt is pending.

Bit 6:5 Reserved

Bit 4 Monitor Detect Status (MDS)
0 = Monochrome display is detected
1 = Color display is detected

Bit 3:0 Reserved

ISR1: Input Status Register 1

Read Only Address: 3?Ah
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED		**COLOR PLANE**		**VRS**	**R**	**DISPLAY ENABLE**	

Bit 7:6 Reserved

Bit 5:4 Color Plane Diagnostics
These bits return two of the 8 video outputs VID0-VID7, as selected by Color Plane Enable Register [5:4]

Bit 3 Vertical Retrace Status (VRS)
0 = In display mode
1 = In vertical retrace mode

Bit 2:1 Reserved (R)

Bit 0 Display Enable
0 = In display mode
1 = Not in display mode. (it is either in horizontal or vertical retrace mode)

FCR: Feature Control Register

Write Only Address: 3?Ah
Read Only Address: 3CAh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				VSC	RESERVED		

Bit 7:4 Reserved

Bit 3 Vertical Sync Control
0 = VSYNC output is enabled
1 = VSYNC output is logical 'OR' of VSYNC and Vertical Display Enable

Bit 2:0 Reserved

Sequencer Register

SEQX: Sequencer Index Register

Read/ Write Address: 3C4h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED				SEQUENCER ADDRESS/INDEX			

Bit 7:4 Reserved

Bit 3:0 Sequencer Address/Index
The Sequencer address register is written with the index value of the sequencer register to be accessed.

SEQ00: Reset Register

Read/ Write Address: 3C5h, Index: 00h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED						SR	AR

Bit 7:2 Reserved

Bit 1 Synchronous Reset (SR)
0 = Sequencer is cleared and halted synchronously

1 = Normal operating mode

Bit 0 Asynchronous Reset (AR)
0 = Sequencer is cleared and halted asynchronously
1 = Normal operating mode

SEQ01: Clocking Mode Register

Read/ Write Address: 3C5h, Index: 01h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SO**	**VS**	**DCS**	**SL**	**R**	**DC**

Bit 7:6 Reserved

Bit 5 Screen Off (SO)
0 = Normal operating mode
1 = Screen is turned off but SYNC signals remain active

Bit 4 Video Serial Shift Select (VS)
0 = Load video serializer every or every other character or clock, depending on Bit2 of this register.
1 = Load video serializer every 4th character clock

Bit 3 Dot Clock Select (DCS)
0 = Normal dot clock select by VCLK input frequency
1 = Dot clock is divided by 2 (320/360 pixel mode)

Bit 2 Shift Load (SL)
0 = Load video serializer every character or clock
1 = Load video serializer every other character or clock

Bit 1 Reserved (R)

Bit 0 8/9 Dot Clock (DC)
0 = 9 dot wide character clock
1 = 8 dot wide character clock

SEQ02: Enable Write Plane Register

Read/ Write Address: 3C5h, Index: 02h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**ENABLE WRITING**			

Bit 7:4 Reserved

Bit 3:0 Enable Writing to Memory Maps 3 through 0 (respectively)
0 = Disable writing to corresponding plane
1 = Enable writing to corresponding plane

SEQ03: Character Map Select Register

Read/ Write Address: 3C5h, Index: 03h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SCM**	**SCMB**	**SCMA**	**SCMA**	**SCMB**	**SCMB**

Bit 7:6 Reserved

Bit 5,3,2 Select Character Map A (SCMA)

This value select the portion of plane 2 used to generate text character when bit 3 of this register = 0, according to the following table:

Bit 5,3,2	Font Table Location
000	First 8K of plane 2
100	Second 8K of plane 2
001	Third 8K of plane 2
101	Fourth 8K of plane 2
010	Fifth 8K of plane 2
110	Sixth 8K of plane 2
011	Seventh 8K of plane 2
111	Eighth 8K of plane 2

Bit 4,1,0 Select Character Map B (SCMB)

This value select the portion of plane 2 used to generate text character when bit 3 of this register = 1, according to the same table as character Map A

SEQ04: Memory Mode Register

Read/ Write Address: 3C5h, Index: 04h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**CM**	**SSA**	**EVM**	**R**

Bit 7:4 Reserved

Bit 3 Chained 4 Map (CM)
0 = Enable odd/even mode
1 = Enable Chain 4 mode. Uses the two lower bits of CPU address to select plane in video memory as follows:

MA1	MA0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Select Sequential Addressing Mode (SSA). This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enable the odd/even addressing mode. Even addresses access planes 0 and 2, and odd addresses access plane 1 and 3
1 = Enable system to use a sequential addressing mode

Bit 1 Extended Video Memory Enable (EVM)
0 = Memory access restricted to 16/32K
1 = Enable extended video memory access. Allows complete memory access to 256K

Bit 0 Reserved (R)

CRTC Controller Registers

The CRTC registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register (3?4h), then writing to the data register (3?5h). The I/O address is either 3Bxh or 3Dxh depending on bit 0 of the Miscellaneous Output Register at 3C2h.

CRTX: CRTC Controller Index Register

Read/Write Address: 3?4h
Power-on Default: 00h

This register is loaded with a binary value that indexes the CRTC controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED			**CRTC ADDRESS INDEX**				

Bit 7:5 Reserved

Bit 4:0 CRTC Address Index
These bits specify the CRTC register to be addressed. Its value is programmed in hexadecimal.

CRT00: Horizontal Total Register

Read/Write Address: 3?5h, Index 00h
Power-on Default: Undefined

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bit 7:0 Horizontal Total
This value = (number of character clocks per scan line) - 5.

CRT01: Horizontal Display End Register

Read/Write Address: 3?5h, Index 01h
Power-on Default: Undefined

This register defines the number of character clocks for one horizontal line active display. This register is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY ENABLE							

Bit 7:0 Horizontal Display Enable
This value = (number of character clocks during active display) - 1.

CRT02: Horizontal Blank Start Register

Read/Write Address: 3?5h, Index 02h
Power-on Default: Undefined

This register defines the number of character clocks at which horizontal ~Blank is asserted.

7	6	5	4	3	2	1	0
HORIZONTAL BLANK START							

Bit 7:0 Horizontal Blank Start
This value = character value at which ~Blank signal becomes active.

CRT03: Horizontal Blank End Register

Read/Write Address: 3?5h, Index 03h
Power-on Default: Undefined

This register defines the display enable skew and pulse width of ~Blank signal.

7	6	5	4	3	2	1	0
R	**DISPLAY ENABLE**		**HORIZONTAL BLANK END**				

Bit 7 Reserved

Bit 6:5 Display Enable Skew. These 2 bits define the display enable signal skew timing in relation to horizontal synchronization pulses.

DESKW1	DESKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Horizontal Blank End
Horizontal Blank End has a 6-bit value. This register contains the least significant 5-bits of this value. Bit 6 of this value is at CRTC index 05 bit 7.

CRT04: Horizontal Sync Pulse Start Register

Read/Write Address: 3?5h, Index 04h
Power-on Default: Undefined

This register is used to adjust screen position horizontally and to specify the position at which HSYNC is active.

7	6	5	4	3	2	1	0
HORIZONTAL SYNC PULSE START							

Bit 7:0 Horizontal Sync Pulse Start
This value = character clock count value at which HSYNC becomes active.

CRT05: End Horizontal Sync Pulse Register

Read/Write Address: 3?5h, Index 05h
Power-on Default: Undefined

This register defines the horizontal sync skew and pulse width of HSYNC signal.

7	6	5	4	3	2	1	0
HBE	**HSS**		**HORIZONTAL SYNC END**				

Bit 7 Horizontal Blank End Bit 5. This bit is End Horizontal Blank Bit 5. (HBE)

Bit 6:5 Horizontal Sync Skew. (HSS)
These 2-bits define the HSYNC signal skew timing in relation to horizontal synchronization pulses.

HSSKW1	HSSKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Horizontal Sync End
Horizontal Sync End has a 5-bit value. This value defines the character clock counter value at which HSYNC signal becomes inactive.

CRT06: Vertical Total Register

Read/Write Address: 3?5h, Index 06h
Power-on Default: Undefined

This register defines the number of scan lines from VSYNC going active to the next VSYNC going active. Vertical total has a 11-bit value. Bit 8 of this value is located at CRT07 bit 0. Bit 9 of this value is located at CRT07 bit 5. Bit 10 of this value is located at CRT30 bit 3.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bit 7:0 Vertical Total
Vertical Total has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines from VSYNC going active to the next VSYNC) - 2. Bit 8 is in CRT07 bit 0. Bit 9 is in CRT 07 bit 5. Bit 10 is in CRT30 bit 3.

CRT07: Overflow Vertical Register

Read/ Write Address: 3?5hIndex: 07h
Power-on Default: Undefined

This register specifies the CRTC vertical overflow registers.

7	6	5	4	3	2	1	0
VSS	**VDE**	**VT**	**LC**	**VBS**	**VSS**	**VDE**	**VT**

Bit 7 Vertical Sync Start Bit 9 (VSS)

Bit 6 Vertical Display Enable End Bit 9. This bit is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register. (VDE)

Bit 5 Vertical Total Bit 9 (VT)

Bit 4 Line Compare Bit 8 (LC)

Bit 3 Vertical Blank Start Bit 8 (VBS)

Bit 2 Vertical Sync Start Bit 8 (VSS)

Bit 1 Vertical Display Enable End Bit 8. This bit is locked when FPR33 (SC5h, index 33) bit 5 = 1. (VDE)

Bit 0 Vertical Total Bit 8 (VT)

CRT08: Preset Row Scan Register

Read/Write Address: 3?5h, Index 08h
Power-on Default: Undefined

This register is used for panning and text scrolling.

7	6	5	4	3	2	1	0
R	**BYTE PLANNING**		**PRESET ROW SCAN COUNT**				

Bit 7 Reserved (R)

Bit 6:5 Byte Panning Control. These 2-bits controls the number of bytes to pan.

BPC1	BPC0	Operation
0	0	Normal
0	1	1 Byte left shift
1	0	2 Bytes left shift
1	1	3 Bytes left shift

Bit 4:0 Preset Row Scan Count
These bits preset the vertical row scan counter once after each vertical retrace. This counter is automatically incremented by 1 after each horizontal sync period. Once the maximum row scan count is reached, this counter is cleared. This is useful for smoothing vertical text scrolling.

CRT09: Maximum Scan Line Register

Read/Write Address: 3?5h, Index 09h
Power-on Default: Undefined

This register defines the maximum number of scan lines per character row and provides one scanning control and two overflow bits

7	6	5	4	3	2	1	0
EDS	**LC**	**VB**	**MAXIMUM SCAN LINE**				

Bit 7 Enable Double Scan (EDS)
0 = Normal Operating
1 = Enable Double Scan. The row scan counter is clocked at half of the horizontal scan rate.

Bit 6 Line Compare Register Bit 9 (LC)

Bit 5 Vertical Blank Start Register Bit 9 (VB)

Bit 4:0 Maximum Scan Line
This value equals to the total number of scan lines per character row - 1

CRT0A: Cursor Start Scan Line Register

Read/Write Address: 3?5h, Index 0Ah
Power-on Default: Undefined

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
RESERVED		**EC**	**CURSOR START SCAN LINE**				

Bit 7:6 Reserved

Bit 5 Enable Cursor (EC)
0 = Cursor is on
1 = Cursor is off

Bit 4:0 Cursor Start Scan Line
This value equals to the starting cursor row within the character box. If this value is programmed with a value greater than the Cursor End Scan Line Register (3?5h, index 0Bh), no cursor will be displayed.

CRT0B: Cursor End Scan Line Register

Read/Write Address: 3?5h, Index 0Bh
Power-on Default: Undefined

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
R	**CURSOR SKEW**		**CURSOR END SCAN LINE**				

Bit 7 Reserved (R)

Bit 6:5 Cursor Skew. These 2 bits defines the cursor delay skew, which moves the cursor to the right, in character clock.

CSKW1	CSKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Cursor End Scan Line
This value equals to the ending cursor row within the character box. If this value is programmed with a value less than the Cursor Start Scan Line Register (3?5h, index 0Ah), no cursor will be displayed.

CRT0C: Display Start Address High Register

Read/Write Address: 3?5h, Index 0Ch
Power-on Default: Undefined

This register defines the high order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are located in CRT30 bit [6:4]. Bit [7:0] are located in CRT0D.

7	6	5	4	3	2	1	0
DIPLAY START ADDRESS [15:8]							

Bit 7:0 Display Start Address [15:8]
This register is the high order byte of the address [15:8].

CRT0D: Display Start Address Low Register

Read/Write Address: 3?5h, Index 0Dh
Power-on Default: Undefined

This register defines the low order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are in CRT30 bit [6:4]. Bit [15:8] are in CRT0C.

7	6	5	4	3	2	1	0
START ADDRESS [7:0]							

Bit 7:0 Start Address [7:0]
This register is the low order byte of the address [7:0].

CRT0E: Cursor Location High Register

Read/Write Address: 3?5h, Index 0Eh
Power-on Default: Undefined

This register defines the high order cursor location address. This value is a 19-bit value along with CRT30 bit[6:4] are the high order bits of the address.

7	6	5	4	3	2	1	0
CURSOR LOCATION HIGH							

Bit 7:0 Cursor Location High
This register is the high order byte of the cursor location address.

CRT0F: Cursor Location Low Register

Read/Write Address: 3?5h, Index 0Fh
Power-on Default: Undefined

This register defines the low order cursor location address.

7	6	5	4	3	2	1	0
CURSOR LOCATION LOW							

Bit 7:0 Cursor Location Low
This register is the low order byte of the cursor location address.

CRT10: Vertical Sync Pulse Start Register

Read/Write Address: 3?5h, Index 10h
Power-on Default: Undefined

This register is used to adjust screen position vertically and to specify the position at which VSYNC is active. Bit 10 of this value is in CRT30 bit 0. Bit 9 of this value is in CRT07 bit 7. Bit 8 of this value is in CRT07 bit 2.

7	6	5	4	3	2	1	0
VERTICAL SYNC PULSE START							

Bit 7:0 Vertical Sync Pulse Start
Vertical Sync Start has a 11-bit value. This register contains the least significant 8 bits of this value. This value = number of scan lines at which VSYNC becomes active.

CRT11: Vertical Sync Pulse End Register

Read/Write Address: 3?5h, Index 11h
Power-on Default: 0xh.

This register is used to control vertical interrupt, vertical sync end CRT0-7 Write protect.

7	6	5	4	3	2	1	0
LW	**RCS**	**DVI**	**CVI**	**VERTICAL SYNC PULSE END**			

Bit 7 Lock writing to CRTC registers: CRT00-07. (LW)
0 = Enable writing to CRTC registers are
1 = Disable writing to CRTC registers, except CRT07 bit 4 (line compare)

Bit 6 Refresh Cycle Select (3/5) (RCS)
0 = 3 DRAM refresh cycles per horizontal scan line
1 = 5 DRAM refresh cycles per horizontal scan line

Bit 5 Disable Vertical Interrupt (DVI)
0 = vertical retrace interrupt enabled
1 = vertical retrace interrupt disabled

Bit 4 Clear Vertical Interrupt (CVI)
0 = vertical retrace interrupt is cleared
1 = vertical retrace interrupt. This allows an interrupt to be generated at the end of active vertical display.

Bit 3:0 Vertical Sync Pulse End
This value = number of scan lines at which VSYNC becomes inactive.

CRT12: Vertical Display End Register

Read/Write Address: 3?5h, Index 12h
Power-on Default: Undefined

This register defines the number of scan line where the display on the screen ends. Bit 10 of this value is in CRT30 bit 2. Bit 9 of this value is in CRT07 bit 6. Bit 8 of this value is in CRT07 bit 1. This register is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7:0 Vertical Display End
Vertical Display End has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines during active display) - 1.

CRT13: Offset Register

Read/Write Address: 3?5h, Index 13h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

This register defines the logical line width of the screen. The starting memory address for the next display row is larger than the current row by two (in byte mode), four (in word mode), or eight (in double word mode) times this offset.

Bit 7:0 Logical Screen Width
Logical Screen Width has a 10-bit value. This register contains the least significant 8-bits of this value. The addressing mode is specified by bit 6 of CRT14 and bit 3 of CRT17.

CRT14: Underline Location Register

Read/Write Address: 3?5h, Index 14h
Power-on Default: Undefined

This register defines the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
R	**DWS**	**CS**	**UNDER LINE LOCATION**				

Bit 7 Reserved (R)

Bit 6 Double Word Mode Select (DWS)
0 = the memory address are byte or word addresses
1 = the memory address are double word addresses

Bit 5 Count by 4 Select (CS)
0 = the memory address counter depends on bit 3 of CRT17
1 = the memory address counter is incremented every four character clocks

Bit 4:0 Under Line Location
Under Line Location has a 5-bit value. This value = (scan line count of a character row on which an underline occurs) - 1.

CRT15: Vertical Blank Start Register

Read/Write Address: 3?5h, Index 15h
Power-on Default: Undefined

This register defines the number of scan lines at which vertical blank is asserted. Bit 10 of this value is in CRT30 bit 1. Bit 9 of this value is in CRT09 bit 5. Bit 8 of this value is in CRT07 bit 3.

7	6	5	4	3	2	1	0
VERTICAL BLANK START							

Bit 7:0 Vertical Blank Start
Vertical Blank Start has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (scan line count at which vertical blank signal becomes active) - 1.

CRT16: Vertical Blank End Register

Read/Write Address: 3?5h, Index 16h
Power-on Default: Undefined

This register defines the number of scan lines at which vertical blank is de-asserted.

7	6	5	4	3	2	1	0
VERTICAL BLANK END							

Bit 7:0 Vertical Blank End
Vertical Blank End is a 8-bit value. This value = [(scan line count at which vertical blank signal becomes active) -1)] + (desired width of vertical blanking pulse in scan lines)

CRT17: CRT Mode Control Register

Read/Write Address: 3?5h, Index 17h
Power-on Default: Undefined

This register defines the controls for CRT mode.

7	6	5	4	3	2	1	0
HR	**BAS**	**AW**	**R**	**WS**	**HCS**	**EGA**	**CGA**

Bit 7 ~RST Hardware Reset for Horizontal and Vertical Sync (HR)
0 = horizontal and vertical sync outputs inactive
1 = horizontal and vertical sync outputs active

Bit 6 Byte Address Mode Select (BAS)
0 = word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB
1 = byte address mode

Bit 5 Address Wrap is useful in implementing CGA mode. (AW)
0 = In word address mode, memory address counter bit 13 appears on the memory address output signal of the CRT controller and the video memory address wraps around at 16KB.
1 = In word address mode, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRTC controller.

Bit 4 Reserved (R)

Bit 3 Word Mode Select (WS)

0 = byte mode addressing is selected and memory address counter is clocked by the character clock input
1 = word mode addressing is selected and memory address counter is clocked by the character clock divided by two.

Bit 2 Horizontal Retrace Clock Select (HCS)
0 = select horizontal retrace clock rate
1 = select horizontal retrace clock rate divided by two.

Bit 1 EGA Emulation (EGA)
0 = Row scan counter bit 1 is replaced by memory address bit 14 during active display time
1 = Memory address bit 14 appear son the memory address output bit 14 signal of the CRT controller.

Bit 0 CGA Emulation (CGA)
0 = Row scan counter bit 0 is replaced by memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller.

CRT18: Line Compare Register

Read/Write Address: 3?5h, Index 18h
Power-on Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0.

7	6	5	4	3	2	1	0
LINE COMPARE REGISTER							

Bit 7:0 Line Compare Register
This value = number of scan lines at which the screen is split into screen 1 and screen 2.

CRT22: Graphics Controller Data Latches Readback Register

Read Only Address: 3?5h, Index 22h
Power-on Default: Undefined

This register is used to read the CPU latches in the graphics controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU DATA LATCHES							

Bit 7:0 Graphics Controller CPU Data Latches
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

CRT24: Attribute Controller Toggle Readback Register

Read Only Address: 3?5h, Index 24h

Power-on Default: Undefined

This register is used to provide access to the attribute controller toggle.

7	6	5	4	3	2	1	0
ACS	**RESERVED**						

Bit 7 Attribute Controller Index Select (ACS)
0 = the attribute controller reads or writes an index value on the next access
1 = the attribute controller reads or writes a data value on the next access

Bit 6:0 Reserved

CRT26: Attribute Controller Index Readback Register

Read Only Address: 3?5h, Index 26h
Power-on Default: Undefined

This register is used to provide access to the attribute controller index.

7	6	5	4	3	2	1	0
RESERVED		**VES**	**ATTRIBUTE CONTROLLER INDEX**				

Bit 7:6 Reserved

Bit 5 Video Enable Status (VES)

This bit provides status of the video display enable bit in Attribute Controller (3C0h) index bit 5.

Bit 4:0 Attribute Controller Index

This value is the attribute controller index data at 3C0h.

Graphics Controller Registers

The graphics controller registers are located at a two byte I/O address space. The registers are accessed by first writing an index to 3CEh and followed by writing a data to 3CFh.

GRXX: Graphics Controller Index Register

Read/Write Address: 3CEh
Power-on Default: Undefined

This register is loaded with a binary value that indexes the graphics controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED				GRAPHICS CONTROLLER			

Bit 7:4 Reserved

Bit 3:0 Graphics Controller Address Index
These bits specify the graphics controller register to be addressed. Its value is programmed in hexadecimal.

GRX00: Set/Reset Register

Read/Write Address: 3CFh, Index: 00h.
Power-on Default: Undefined

This register represents the value written to all 8-bits of the corresponding memory planes when CPU executes a memory write in write mode 0.

7	6	5	4	3	2	1	0
RESERVED				SET/RESET PLANE			

Bit 7:4 Reserved

Bit 3:0 Set/Reset Plane3:0
In write mode 0, the set/reset data can be enabled on the corresponding bit of the bit of the Enable Set/Reset Data register. These bits become the color value for CPU memory write operations.

GRX01: Enable Set/Reset Register

Read/Write Address: 3CFh, Index: 01h.
Power-on Default: Undefined

This register enable the set/reset register in write mode 0.

7	6	5	4	3	2	1	0
RESERVED				ENABLE SET/RESET PLANE			

Bit 7:4 Reserved

Bit 3:0 Enable Set/Reset Plane3:0
In write mode 0, the enable set/reset bits allow writing to the corresponding planes with the data in set/reset register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

GRX02: Color Compare Register

Read/Write Address: 3CFhIndex: 02h.
Power-on Default: Undefined

This register is to used to compare with the CPU memory read data. This register works in conjunction with the Color Don't Care Register.

7	6	5	4	3	2	1	0
RESERVED				**COLOR COMPARE PLANE**			

Bit 7:4 Reserved

Bit 3:0 Color Compare Plane [3:0]
These bits represent the reference color used to compare each pixel in corresponding plane. A logical 1 is returned in each plane bit position when color matches.

GRX03: Data Rotate/ROP Register

Read/Write Address: 3CFhIndex: 03h.
Power-on Default: Undefined

This register is to used to control rotation and raster operations.

7	6	5	4	3	2	1	0
RESERVED			**ROS**		**ROTATE COUNT**		

Bit 7:5 Reserved

Bit 4:3 Raster Operations Select (ROS)
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

Bit 2:0 Rotate Count
These bits specifies the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0. To write non-rotated data, the CPU must present a count with 0.

GRX04: Read Plane Select Register

Read/Write Address: 3CFhIndex: 04h.
Power-on Default: Undefined

This register is selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
RESERVED						**READ PLANE**	

Bit 7:2 Reserved

Bit 1:0 Read Plane Select is as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

GRX05: Graphics Mode Register

Read/Write Address: 3CFhIndex: 05h.
Power-on Default: Undefined

This register is selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
R	**CS**	**OES**	**OEA**	**ERC**	**R**	**WRITING MODE**	

Bit 7 Reserved (R)

Bit 6 256 Color Shift Mode Select (CS)
0 = Enable bit 5 of this register to control loading of the shift registers.
1 = The shift registers are loaded in a manner that support the 256 color mode.

Bit 5 Odd/Even Shift Mode Select (OES)
0 = Normal shift mode
1 = The video shift registers are directed to format the serial data stream with even numbered bits from both planes on the even numbered planes and odd numbered bits from both planes on the odd planes.

Bit 4 Odd/Even Addressing Select (OEA)
0 = Normal addressing
1 = CGA Odd/even addressing mode is selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3.

Bit 3 Enable Read Compare (ERC)
0 = System read data from memory planes selected by read map select register (3CFh index 04h). This is called read mode 0.
1 = System read the results of logical comparison between the data in 4 memory planes selected by the Color Don't Care Register and the Color Compare Register. The results is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1.

Bit 2 Reserved (R)

Bit 1:0 Write Mode Select

00 = Write mode 0. Each of four video planes is written with CPU data rotated by the number of counts in rotate register. If Set/Reset register is enabled for any of the four planes, the corresponding planes is written with the data stored in the Set/Reset register.
01 = Write mode 1. Each of four video planes is written with CPU data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, Set/Reset data, enable Set/Reset data and bit mask registers are ignored.
10 = Write mode 2. Video planes [3:0] are written with the value of CPU write data [3:0]. The 32-bit output from the four planes is then operated on by the Bit Mask register and the resulting data are written into the four planes. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored.
11 = Write mode 3. Each of the four video planes is written with 8-bit of the color value in the Set/Reset register for the corresponding plane. The bit-position-enable field is formed with the logical AND of the Bit Mask register and rotated CPU data. The Enable Set/Reset register is ignored.

GRX06: Graphics Miscellaneous Register

Read/Write Address: 3CFhIndex: 06h.
Power-on Default: Undefined

This register controls video memory addressing.

7	6	5	4	3	2	1	0
RESERVED				**MEMORY MAP**		**OES**	**GMS**

Bit 7:4 Reserved

Bit 3:2 Memory Map Mode. These bits control the address mapping of video memory into the CPU address space.
00 = A0000h to BFFFFh (128KB)
01 = A0000h to AFFFFh (64KB)
10 = B0000h to B7FFFh (32KB)
11 = B8000h to BFFFFh (32KB)

Bit 1 Odd/Even Mode Select (OES)
0 = CPU address bit A0 is the memory address bit MA0
1 = CPU address A0 is replaced by a higher order address bit. A0 is then used to select odd or even maps. A0=0, selects Map 2 or 0; A0 = 1, select Map 3 or 1.

Bit 0 Graphics Mode Select (GMS)
0 = Select Text mode
1 = Select Graphics mode

GRX07: Color Don't Care Plane Register

Read/Write Address: 3CFhIndex: 07h.
Power-on Default: Undefined

This register controls whether the corresponding bit of the Color Compare Register, GRX02, is to be ignored or used for color comparison. This register is used with GRX02 for Read Mode 1 accesses.

7	6	5	4	3	2	1	0
RESERVED				**COMPARE PLANE SELECT**			

Bit 7:4 Reserved

Bit 3:0 Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1.
1 = The corresponding color plane is used for color comparison with the data in the Color Compare Register, GRX02.

GRX08: Bit Mask Register

Read/Write Address: 3CFhIndex: 08h.
Power-on Default: Undefined

This register controls bit mask operations which applies simultaneously to all four maps. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bit 7:0 Bit Mask
0 = corresponding bit of each plane in memory is set to the corresponding bit in the processor latches.
1 = corresponding bit of each plane in memory is set as specified by other conditions.

Attribute Controller Registers

The attribute controller registers are located at the same byte I/O address for writing address and data. The Attribute Index Register has an internal flip-flop rather than an input bit to control the selection of the address and data registers. Reading the Input Status Register 1 at Port 3?Ah clears the flip-flop and selects the Address Register, which is read at address 3C1h and written at address 3C0h. Once the Address Register has been loaded with an index, the next write operation to 3C0h loads the Data Register. The flip-flop toggles between the Address and the Data Register after every write to address 3C0h, but does not toggle for reads from address 3C1h. Furthermore, the attribute controller index register is read at 3C0h, and the attribute controller data register is read at address 3C1h.

ATRX: Attribute Controller Index Register

Read/Write Address: 3C0h
Power-on Default: Undefined

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED		**PAS**	**ATTRIBUTE CONTROLLER ADDRESS**				

Bit 7:6 Reserved

Bit 5 Palette Address Source (PAS)
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers
1 = Enable internal color palette and normal video translation.

Bit 4:0 Attribute Controller Address
A binary value that points to the attribute controller register where data is to be written.

ATR00-0F: Palette Register

Read/Write Address: 3C1h/3C0hIndex 00h - 0Fh.
Power-on Default: Undefined

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED		**PALETTE COLORS**					

Bit 7:6 Reserved

Bit 5:0 Palette Colors
0 = corresponding pixel color is de-selected
1 = corresponding pixel color is enabled

ATR10: Attribute Mode Control Register

Read/Write Address: 3C1h/3C0hIndex: 10h.
Power-on Default: 00h

This register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
VID	**CS**	**PPE**	**R**	**BIS**	**LGC**	**MCE**	**TGM**

Bit 7 VID5, VID4 Select (VID)
0 = VID5 and VID4 palette register outputs are selected
1 = Color Select Register Port 3C1h/3C0h, Index 14h, bit 1 and bit 0 are selected for outputs.

Bit 6 256 Color Select (CS)

0 = Disable 256 color mode pixel width. PCLK rate = internal dot clock rate.
1 = Enable 256 color mode pixel width. PCLK rate = internal dot clock rate / 2

Bit 5 Pixel Panning Enable (PPE)
0 = Line compare will have no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC is active

Bit 4 Reserved (R)

Bit 3 Blinking and Intensity Select (BIS)
0 = Select background intensity from the text attribute byte.
1 = Select blink attribute in text modes

Bit 2 Line Graphics Character Enable (LGC)
0 = Forces the ninth dot to be the same color as the background in line graphics character codes.
1 = Enable special line graphics character codes.

Bit 1 Mono/Color Emulation (MCE)
0 = Select color display text attributes
1 = Select monochrome display text attributes

Bit 0 Text /Graphics Mode Select (TGM)
0 = Select text attribute control mode
1 = Select graphics control mode

ATR11: Overscan Color Register

Read/Write Address: 3C1h/3C0hIndex: 11h.
Power-on Default: 00h

This register controls the overscan or border color. This register will be locked if CRT3C register (3?5h, index 3Ch) bit 5 is set to 1. Please refer to CRT3C register for details.

7	6	5	4	3	2	1	0
OVERSCAN COLOR REGISTER							

Bit 7:0 OverScan Color register determines the overscan or border color displayed on the CRT screen.

ATR12: Color Plane Enable Register

Read/Write Address: 3C1h/3C0hIndex: 12h.
Power-on Default: 00h

This register enables the respective video memory color plan 0-3 and selects the video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
RESERVED		**VIDEO SATUS**		**COLOR PLANE ENABLE**			

Bit 7:6 Reserved

Bit 5:4 Video Status Multiplexer. These bits select two out of the 8 color outputs which can be read by the Input Status Register 1 at port 3?Ah, bit 5 and bit 4.

Color Plane Register		**Input Status Register 1**	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID7

Bit 3:0 Color Plane Enable
0 = disable the corresponding color planes. Forces pixel bit to be 0 before it address palette.
1 = enables the corresponding color planes.

ATR13: Horizontal Pixel Panning Register

Read/Write Address: 3C1h/3C0hIndex: 13h.
Power-on Default: 00h

This register specifies the number of pixels to shift the display data horizontally to the left. Horizontal pixel panning is available in text and graphics modes.

7	6	5	4	3	2	1	0
RESERVED				**HORIZONTAL PIXEL PLANNING**			

Bit 7:4 Reserved

Bit 3:0 Horizontal Pixel Panning. These 4 bits determine the horizontal left shift of the video data in number of pixels. In the 9 pixel/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixel/character text mode and all graphics modes, except for 256 color mode, a maximum shift of 7 pixels is allowed. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

Bits 3:0	9 pixel/character	8 pixel/character	256 color modes
0000	1	0	0
0001	2	1	-
0010	3	2	1
0011	4	3	-
0100	5	4	2
0101	6	5	-
0110	7	6	3
0111	8	7	-
1000	0	-	-

ATR14: Color Select Register

Read/Write Address: 3C1h/3C0h, Index: 14h.
Power-on Default: 00h

This register specifies the high-order bits of video output when pixel padding is enable/disabled for 256 color modes.

7	6	5	4	3	2	1	0
RESERVED				**SC7/6**		**SC5/4**	

Bit 7:4 Reserved

Bit 3:2 Select Color 7 and Color 6 (SC7/6)
These are the two most significant bits of the 8 bits color value for video DAC. These are normally used in all modes except 256 color modes.

Bit 1:0 Select Color 5 and Color 4 (SC5/4)
These bits can be substituted for VID5 and VID4 from the palette registers to form the 8-bit color value for video DAC.

RAMDAC Registers

The section describes the RAMDAC registers. Special programming sequences are used to read or write data to and from the RAMDAC.

Writing data to DAC:

Write the color code to DAC Write Address Register at 3C8h.
Three bytes: Red, Green, Blue values are written into DAC Data Register at 3C9h.
Following the third write, the values are transferred to Color Lookup Table.

- The DAC Write Address Register is auto incremented by 1.

Reading data from DAC:

- Write the color code to DAC Read Address Register at 3C7h.
- Three bytes: Red, Green, Blue values are read from the DAC Data Register at 3C9h.

3C6: DAC Mask Register

Read/Write Address: 3C6h
Power-on Default: Undefined

This register is the pixel read mask register to select pixel video output.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bit 7:0 DAC Address Mask
This field is the pixel mask for palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry I the Color Lookup Table. This register is initialized to FFh by the BIOS during a video mode set.

3C7W: DAC Address Read Register

Write Only Address: 3C7h
Power-on Default: Undefined

This register contains the pointer to one of the 256 palette data registers and is used when reading the color palette. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bit 7:0 DAC Read Address
After a color code is written into this register, the chip will identifies that a DAC read sequence will occur. A read sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C7R: DAC Status Register

Read Only Address: 3C7h
Power-on Default: Undefined

This register specifies the DAC Status: read or write cycles.

7	6	5	4	3	2	1	0
RESERVED						**DAC STATUS**	

Bit 7:2 Reserved

Bit 1:0 DAC Status bits
00 = DAC write operation in progress
11 = DAC read operation in progress

3C8: DAC Address Write Register

Read/Write Address: 3C8h
Power-on Default: Undefined

This register contains the pointer to one of the 256 palette data registers and is during a palette load. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS							

Bit 7:0 DAC Write Address
After a color code is written into this register, the chip identifies that a DAC write sequence will occur. A write sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C9: DAC Data Register

Read/Write Address: 3C9h
Power-on Default: Undefined

This register is the data port to read or write the contents of the location in the Color Lookup Table pointed to by the DAC Read Address or the DAC Write Address registers. An access to this register will cause 01b to be driven to RAMDAC outputs.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bit 7:0 DAC Read/Write Data
These read/write register bits store the Pixel data for the Palette DAC

Chapter 21: Extended SMI Registers

Table 26: Extended SMI Registers Quick Reference

Extended SMI Registers

This chapter describes the extended SMI registers including:

- System control registers
- Power down control register
- Flat panel registers
- Memory control registers
- Clock control registers
- General purpose registers
- Popup-Icon and hardware cursor registers
- Extended CRT registers
- Shadow VGA registers

All extended SMI registers are accessed through 3C3h, 3C5h, or 3?5h address. (? = B for monochrome mode and D for color mode) or through their MMI0 location. In order to access extended SMI registers, one must unlock the extended SMI register by writing 010xxxxxb to Lock register (3C3h).

The name of the register consists of the index which the register resides in. For example, SCR10 can be accessed through index 10h of 3C5h.

System Control Registers

All system control registers are controlled by PCI system clock, rather than memory clock (MCLK) or video clock (VCLK). During Lynx3DM+ power down (when MCLK and VCLK are shutdown), the system control registers can still be accessed through PCI bus.

SCR15: PCI Miscellaneous Control Register

Read Only Address: 3C5h, Index: 15h
Power-on Default: 00h

This register defines the various PCI control registers.

7	6	5	4	3	2	1	0
BRE	**ABORT**	**SDE**	**DEA**	**PCI**	**BIOS**	**XFER**	

Bit 7 PCI Burst Read Enable (BRE)
0 = Disable
1 = Enable. SCR17 bit 5 needs to be set to 1 in order for this bit to take effect. For example, if SCR17 bit 5 = 0, even this bit is set to 1, PCI burst read will not be enabled.

Bit 6 Abort 3D Engine (ABORT)
0 = 3D Engine Normal Operation
1 = Abort 3D Engine Activities

Bit 5 Software Abort Drawing Engine Enable (SDE)
0 = Normal
1 = Enable. This bit has no effect unless bit 4 is set to 1.

Bit 4 Drawing Engine Abort Enable (DEA)
0 = Normal

1 = Enable

Bit 3 PCI Configuration Space: Subsystem ID Lock Enable (PCI)
0 = Disable
1 = Enable

Bit 2 Full range for BIOS access (BIOS)

Bit 1:0 # of Double word transfer during burst read = for performance tuning purpose
00 = 2 3D-bit double words
01 = 4 3D-bit double words
IX = 8 3D-bit double words

SCR16: Status for Drawing Engine and Video Processor

Read Only Address: 3C5h, Index: 16h
Power-on Default: Undefined

This register specifies status of Lynx3DM+ including Drawing Engine Status, Video Processor Status, and Drawing Engine FIFO Available.

7	6	5	4	3	2	1	0
GES	**VWI**	**VWII**	**DE**	**DEBS**	**3DEBS**	**VPR**	**VPRCB**

Bit 7 Graphics Engine Status (GES)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 6 Video Window I Status (VWI)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 5 Video Window II Status (VWII)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 4 Drawing Engine is Empty and Ready (DE
0 = Drawing Engine not empty
1 = Drawing Engine empty

Bit 3 2D Drawing Engine Busy Status (DEBS)
0 = Drawing Engine Idle
1 = Drawing Engine Busy

Bit 2 3D Engine Busy Status (3DEBS)
0 = 3D Engine Idle
1 = 3D Engine Busy

Bit 1 VPR53_7 (VPR)
Sub picture Status
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 0 VPRcb_7

SCR17: General Graphics Command Register 1

Read/Write Address: 3C5h, Index: 17h
Power-on Default: 00h

This register specifies command controls for Memory Access Disable, PCI bus master status, PCI bus burst write and burst read enable, Big-Endian Swap mode Select, Direct 3D Data Buffer Select, Memory mapped access enable and BIOS ROM size select.

7	6	5	4	3	2	1	0
MAD	**PCI**	**PCI1**	**BESM**	**DIRECT3D**		**MMA**	**DLT**

Bit 7 Memory Access Disable when Drawing Engine Busy (MAD)
0 = Normal
1 = Disable memory access when Drawing Engine is busy

Bit 6 Start PCI Bus Master (PCI)
0 = Stop PCI
1 = Start PCI

Bit 5 PCI burst read and write enable. (PCI1)
0 = Disable
1 = Enable

Bit 4 Big Endian Swap Mode Select (BESM)

0 = Big Endian with byte swap

1 = Big Endian with word swap

Before	[31:24]	[23:16]	[15:8]	[7:0}
↓				
After	**[7:0]**	**[15:8]**	**[23:16]**	**[31:24]**

Before	[31:16]	[15:0]
↓		
After	**[15:0]**	**31:16]**

Bit 3:2 Direct3D Z-Buffer Data Select

00 = Normal (use all 32-bit data)

01 = Use low word [15:0]

10 = Use high word [31:16]

11 = Normal (use all 32-bit data)

Bit 1 Memory Mapped Aperture Select (MMA)
0 = Select Banking Aperture. No Memory Mapped registers access allowed.
1 = Select Memory Mapped Aperture

Bit 0 Disable Latency Timer (DLT)
0 = Normal
1 = Disable latency timer count

SCR18: General Graphics Command Register 2

Read/Write Address: 3C5h, Index: 18h
Power-on Default: 00h

This register specifies command control for aperture select, graphics modes select, 32/64 memory data path select and linear addressing mode enable.

7	6	5	4	3	2	1	0
SCLK	**ECLK**	**AS**	**GRAPHICS MODE**		**MDP**	**ERH**	**LMM**

Bit 7 Select ~CLKRUN or ACTIVITY (SCLK)
0 = Select ~CLKRUN as input for Pin 161
1 = Select ACITIVITY as output for Pin 161

Bit 6 Enable ~CLKRUN Function (ECLK)
0 = disable
1 = enable

Bit 5 Aperture Select. This bit is only valid in linear memory mode (bit 0 = 1) (AS)
0 = Select dual aperture. Allow 0A0000h-0AFFFFh and linear aperture to coexist.
1 = Select single aperture. Only linear aperture can be used.

Bit 4:3 Graphics Modes Select for Memory Access
00 = Standard VGA mode. The memory access only uses the lower 32-bit of the 64-bit internal memory bus. The memory address wraps after 256 KB.
01 = VESA Super VGA 16 color (4-bit) mode. The memory access only uses the low 32-bit of the 64-bit internal memory bus. The memory address does not wrap after 256 KB.
1x = Extended packed pixel graphics modes (8/16/24/32-bit). The memory access always use the internal 64-bit memory bus.

Bit 2 32/64 memory data path select. This bit is only valid in VGA or VESA Super VGA 16 color modes (bit 4 of this register = 0) (MDP)
0 = CPU access VGA memory. All host memory access goes through VGA aperture: 0A0000h - 0BFFFFh (controlled by 3CFh index 6 Bit [3:2]). The memory access only uses the low 32-bit of the 64-bit memory bus.
1 = CPU access graphics memory. All host memory access does not goes through VGA aperture. This bit is used to allow 64-bit memory access even in VGA or super VGA 16 color modes.
For example, when programming pop-up icon in VGA mode or VESA super VGA 16 color mode, one must set bit 2 = 1 and bit 4 = 0 of this register, in order to access full range of the display memory.

Bit 1 Enable Repeat Hardware Rotation BLT function (ERH)
0 = disable
1 = enable

Bit 0 Linear Memory Mode Enable (LMM)
0 = disable. Nonlinear addressing (banking) mode is selected, and MCR61 register will be used for memory bank select. Memory will be accessed according to 3CF index 6 Bit [3:2]:

3CF.6 Bit [3:2]Memory Range

00 0A0000-0BFFFF
01 0A0000-0AFFFF
10 0B0000-0B7000
11 0B8000-0BFFFF

1 = enable. Linear memory mode is selected, and memory will be accessed according to the PCI base address register.

SCR19: Interrupt Enable and Mask I

Read/Write Address: 3C5h, Index: 19h
Power-on Default: 00h

This register specifies interrupt enables and interrupt masks for PCI master, Zoom Video Port, and Drawing Engine. Each interrupt mask will block out its particular interrupt when the interrupt mask is enabled. When the interrupt mask is disabled, the corresponding interrupt will be generated when its particular interrupt is enabled.

7	6	5	4	3	2	1	0
IEVGA	**R**	**IEZVP**	**IEDE**	**RESERVED**		**IMZVP**	**IMDE**

Bit 7 Interrupt Enable for VGA (IEVGA)

Bit 6 Reserved (R)

Bit 5 Interrupt Enable for Zoom Video Port (IEZVP)
0 = Disable
1 = Enable

Bit 4 Interrupt Enable for 2D/3D Drawing Engine (IEDE)
0 = Disable
1 = Enable

Bit 3:2 Reserved

Bit 1 Interrupt Mask for Zoom Video Port (IMZVP)
0 = Disable
1 = Enable

Bit 0 Interrupt Mask for 2D/3D Drawing Engine (IMDE)
0 = Disable
1 = Enable

SCR1A: Interrupt Status

Read Only Address: 3C5h, Index: 1Ah
Power-on Default: Undefined

This register specifies Interrupt Status of Drawing Engine, Video Port, PCI Master, and VGA. The interrupt enable and mask bits for these interrupts are located in SCR19 register, with the exception of VGA's enable and mask bits which reside within the VGA block.

7	6	5	4	3	2	1	0
ICMD	**IDCT**	**3D TE**	**VGA**	**HMCIS**	**R**	**ZVP**	**DEI**

Bit 7 ICMD Interrupt Status (ICMD)
0 = No interrupt
1 = ICMD interrupt is detected

Bit 6 IDCT Interrupt Status (IDCT)

Bit 5 3D Texture Engine Interrupt Status (3D TE)
0 = No interrupt
1 = 3D Texture Engine interrupt detected

Bit 4 VGA Interrupt Status. VGA's interrupt enable and mask bits are in the VGA block. (VGA)
0 = No interrupt
1 = VGA Interrupt is detected

Bit 3 Host Memory Control Interrupt Status (HMCIS)
0 = No interrupt
1 = Master Control

Bit 2 Reserved

Bit 1 Zoom Video Port Interrupt Status (ZVP)
0 = No interrupt
1 = Zoom Video Port Interrupt is detected

Bit 0 2D/3D Drawing Engine Interrupt Status (DEI)
0 = No interrupt
1 = Drawing Engine Interrupt is detected

SCR1B: Interrupt Status Enable and Mask II

Read Only: Address: 3C5h, Index: 1Bh
Power-on Default: 00h

7	6	5	4	3	2	1	0
ICMDIE	**IDCTIE**	**TEXTURE**	**HMCIE**	**ICMDIM**	**IDCTIM**	**TEXTURE**	**HMIMM**

Bit 7 ICMD Interrupt Enable (ICMDIE)
0 = Disable ICMD interrupt (hardware interrupt to system)
1 = Enable ICMD interrupt (hardware interrupt to system)

Bit 6 IDCT Interrupt Enable (IDCTIE)
0 = Disable IDCT interrupt (hardware interrupt to system)
1 = Enable IDCT interrupt (hardware interrupt to system)

Bit 5 Text 3D Interrupt Enable (TEXTURE)
0 = Disable Text 3D interrupt (hardware interrupt to system)
1 = Enable Text 3D interrupt (hardware interrupt to system)

Bit 4 Host Master Control Interrupt Enable (HMCIE)
0 = Disable Host Master interrupt (hardware interrupt to system)
1 = Enable Host Master interrupt (hardware interrupt to system)

Bit 3 ICMD Interrupt Mask (ICMDIM)
0 = Allow ICMD interrupt signal to be latched into interrupt register
1 = Will not allow ICMD interrupt signal to be into interrupt register

Bit 2 IDCT Interrupt Mask (IDCTIM)
0 = Allow IDCT interrupt signal to be latched into interrupt register
1 = Will not allow IDCT interrupt signal to be into interrupt register

Bit 1 Texture (TEXTURE)
0 = Allow Texture interrupt signal to be latched into interrupt register
1 = Will not allow Texture interrupt signal to be into interrupt register

Bit 0 Host Control Interrupt Mask Master (HCIMM)
0 = Allow Host Control interrupt signal to be latched into interrupt register
1 = Will not allow Host Control interrupt signal to be into interrupt register

SCR1C: Interrupt Status

Read Only: Address: 3C5h, Index: 1Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**Usr3**	**Usr2**	**RESERVED**	

Bit 7:4 Reserved

Bit 3 Usr3 Interrupt Status

Bit 2 Usr2 Interrupt Status

Bit 1:0 Reserved

Bit 0 Usr0 Interrupt Status

SCR1F: Interrupt Mask and Hardware Interrupt Enable

Read Only: Address: 3C5h, Index: 1Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
USR3	**USR2**	**RESERVED**		**USR3IM**	**USR2IM**	**RESERVED**	

Bit 7 Usr3 to enable system hardware interrupt
0 = Disable USR3 Pin as interrupt (default)
1 = Enable USR3 Pin as interrupt input

Bit 6 Usr2 to enable system hardware interrupt
0 = Disable USR3 Pin as interrupt (default)
1 = Enable USR3 Pin as interrupt input

Bit 5:4 Reserved

Bit 3 Usr3 Interrupt Mask

Bit 2 Usr2 Interrupt Mask

Bit 1:0 Reserved

SCR24: Reserved

Read Only: Address: 3C5h, Index: 24h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**RESERVED**		**RESERVED**			

Bit 5:4 11 = Default

Power Down Control Registers

The power down control registers are controlled by system clock only. The power down control registers can still be read or written by CPU even when internal PLL is off.

PDR20: Power Down Control for Memory, Flat Panel, PLL, and Video Port

Read/Write Address: 3C5h, Index: 20h
Power-on Default: 04h

This register defines the different power down control for Memory, Flat Panel Interface, PLL, and Video Port. This register can still be read or written by CPU even when PLL is off.

7	6	5	4	3	2	1	0
SPDM	**SMR**	**SICLK**		**LVDS**	**VPO**	**FPI**	**DMI**

Bit 7 Select Power Down Mode. External "~PDOWN" pin needs to be pulled "Low" to enable the selected power down mode. For more details on power down modes, please refer to the power down management chapter of this data book. (SPDM)
0 = Standby mode
1 = Sleep mode

Bit 6 Select Memory Refresh Type During Sleep Mode (Bit 7 of this register = 1). (SMR)
0 = Auto Refresh
1 = Self Refresh

Bit 5:4 Select internal VCLK and MCLK frequencies to control DRAM refresh during standby or sleep mode (CCR69 bit 3 = 1). This register setting will be ignored when the chip is in operation mode. (SICLK)
00 = No change.
01 = Both VCLK and MCLK are divided by 4 (standby and sleep mode)
10 = Both VCLK and MCLK are divided by 8 (standby and sleep mode)
11 = Both VCLK and MCLK are divided by 16 (sleep mode only)

Bit 3 Tri-state LVDSCLK output pin. When ~EXCKEN = 0, Pin 159 (MCKIN) becomes an input pin. When ~EXCKEN = 1, Pin 159 (LVDSCLK) becomes an output pin. This register is only valid when ~EXCKEN = 1. This bit is used to test the silicon. (LVDS)
0 = Enable LVDSCLK output pin
1 = Tri-state LVDSCLK output pin

Bit 2 Tri-state Video Port Output. When this bit = 0, 20-bit outputs (R[7:2], G[7:2], B[7:2], BLANK, and PCLK) will be driven out. When Video Capture is enabled (CPR00 [0] = 1), video port output will be tri-stated automatically, except for BLANK/TVCLK output pin. This bit is used to test the silicon. (VPO)
0 = Enable output pins
1 = Tri-state output pins (default)

Bit 1 Tri-state Flat Panel Interface Output Pins. This bit is used to test the silicon (FPI)
0 = Enable output pins
1 = Tri-state output pins

Bit 0 Tri-state Display Memory Interface output pins. This bit can also be used to isolate Lynx3DM+ from display memory. All display memory interface pins: control signals, output clock, data bus and address bus are tri-stated. This bit is used to test the silicon. (DMI)
0 = Enable display memory interface output pins
1 = Tri-state display memory interface output pins

PDR21: Functional Blocks Disable Control

Read/Write Address: 3C5h, Index: 21h
Power-on Default: B0h

This register is designed to achieve optimum power saving in operation mode. Special clock drivers are built-in to control major functional blocks independently. This power saving feature will not affect the graphics and video performance, or LCD display quality. This register could be read or written by CPU even when PLL is off.

7	6	5	4	3	2	1	0
MHZ	**PLLS**	**FBWO**	**FBRO**	**CPR**	**ZVP**	**DE**	**VP**

Bit 7 Disable 200 MHz DAC (MHZ)
0 = Enable DAC
1 = Disable DAC

Bit 6 Disable PLLs (PLLS). This is only effective at power down mode.
0 = Enable PLLs
1 = Disable PLLs

Bit 5 Disable LCD Frame Buffer Write Operation. This bit is used to shut-down the (FBWO)
64 x 8 LCD write FIFO and remove the display memory bus request for LCD frame buffer write from arbitration control.
This bit needs to be set to "1" in Dual View Mode -- displaying different graphics data on CRT (or TV) and LCD.
This bit should be set to "1" when LCD display is not enabled or when TFT is selected in standard refresh mode in order to obtain optimum power saving.
0 = Enable LCD frame buffer write
1 = Disable LCD frame buffer write

Bit 4 Disable LCD Frame Buffer Read Operation and DSTN Dithering Engine. This bit is used to shut-down the 64 x 8 LCD read FIFO1 and LCD read FIFO2, turn off DSTN dithering engine and remove the display memory bus request from LCD Read FIFO1 and LCD read FIFO2. (FBRO)
This bit should be set to "1" when LCD display is not enabled, or when TFT is selected in standard refresh mode.
0 = Enable LCD frame buffer read and DSTN dithering engine
1 = Disable LCD frame buffer read and DSTN dithering engine

Bit 3 Disable 256 x 18 Color Palette RAM. Color Palette RAM will be automatically disabled by hardware in standby mode or sleep mode. (CPR)
0 = Enable Color Palette RAM
1 = Disable Color Palette RAM

Bit 2 Disable Zoom Video Port. This bit is used when there is no external video source which is connected to the Lynx3DM+. The Lynx3DM+ will block input data from external video port, turn off the clock driver of ZV Port, and remove the ZV Port display memory bus request from memory controller. (ZVP)
0 = Enable Zoom Video Port
1 = Disable Zoom Video Port

Bit 1 Disable 2D/3D Drawing Engine. This bit is used to turn-off the 2D/3D drawing engine block. For optimum power saving, this bit should be set to "1" in standard VGA mode since 2D/3D drawing engine is not in use. (DE)
0 = Enable 2D/3D drawing engine
1 = Disable 2D/3D drawing engine

Bit 0 Disable Video Processor. This bit is used to turn-off the video processor block which includes graphics FIFO, V0FIFO, V1FIFO, horizontal/vertical color interpolation, YUV-to-RGB conversion, TV flicker reduction, HW pop-up icon, and related control logic. For optimum power saving, This bit could be set to "1" in standard VGA mode since video processor is not in use. (VP)
0 = Enable video processor
1 = Disable video processor

PDR22: LCD Panel Control Select

Read/Write Address: 3C5h, Index: 22h
Power-on Default: x0h

This register specifies the flat panel control and data: FPEN, VBIASEN, FPVDDEN. This register is not valid when panel S/W power ON/OFF sequence is selected during display switching - FPR34 bit 7 = 0. For panel power ON/OFF sequence, please refer to the flat panel interface chapter of this data book.

7	6	5	4	3	2	1	0
RESERVED		**DPMS CONTROL**		**FPEN**	**VOP**	**FP**	**FOP**

Bit 7:6 Reserved

Bit 5:4 DPMS Control

	DPMS State	VSYNC	HSYNC
00 =	Normal	Pulses	Pulses
01 =	Standby	Pulses	No Pulse
10 =	Suspend	No Pulse	Pulses
11 =	Off	No Pulse	No Pulse

Bit 3 Control FPEN output pin. This function is disabled when LCD H/W auto-power ON/OFF sequence is enabled (FPR34 bit 7 = 1). This pin can also be used to control LCD back light (VBKLGT) at the same time. FPEN is part of the VESA FDPI-1B specification. (FPEN)
0 = Driven low
1 = Driven high

Bit 2 Control VBIASEN output pin. This function is disabled when LCD H/W auto-power ON/OFF sequence is enabled (FPR34 bit 7 = 1). (VOP)
0 = Driven low
1 = Driven high

Bit 1 Disable Flat Panel control signals and data lines. All Control signals and data lines from output pins will be forced to logic "Low". (FP)

0 = Enable Flat Panel control signals and data
1 = Disable Flat Panel control signals and data

Bit 0 Control FPVDDEN output pin. This function is disabled when LCD H/W auto-power ON/OFF sequence is enabled (FPR34 bit 7 = 1). (FOP)
0 = Driven low
1 = Driven high

PDR23: Activity Detection Control Register

Read/Write Address: 3C5h, Index: 23h
Power-on Default: 00h

The activity detection function is used to monitor I/O write and memory write activities. System designer can select a fixed time period by programming bit [2:0] of this register. An internal timer will count the idle period of memory write or I/O write operation. If the idle period is equal or greater than the selected value, a "Low-High" or "High-Low" on the ACTIVITY output signal will generate to the system. Any Memory write or I/O write operation will reset the ACTIVITY output signal and the internal counter. Please note that the internal counter will not start unless video capture is disabled (CPR00 bit 0 = 0). The activity detection can also be used to enable internal auto-standby mode.

7	6	5	4	3	2	1	0
ECAD	**EIAS**	**SA**	**SELECT I/O**		**INTERNAL TIMER SELECT**		

Bit 7 Enable chip activity detection (ECAD)
0 = Disable
1 = Enable

Bit 6 Enable internal auto-standby mode. This bit has no effect if chip activity detection is disabled (PDR23 bit 7 = 0). This bit is used to enable internal auto-standby mode through activity detection function. Before enabling this function, the internal timer bit [2:0] of this register needs to be programmed first. (EIAS)0 = Disable
1 = Enable

Bit 5 Select active "LOW" or "HIGH" signal for the ACTIVITY output (SA)
0 = Select active "LOW"
1 = Select active "HIGH"

Bit 4:3 Select I/O Write Activity Detection or Host Memory Write Activity Detection
00 = No detection
01 = Enable Host Memory Write detect
10 = Enable I/O Write detect
11 = Enable both I/O Write and Host Memory Write detect

Bit 2:0 Internal Timer Select
000 = Select 0 minute
001 = Select 1 minute (4K vertical frames period in standard setting)
010 = Select 2 minutes
.....
110 = Select 32 minutes

111 = Select 64 minutes (256K vertical frames period)

PDR24: Power Down Register Select

Read/Write Address: 3C5h, Index: 24h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED							**(PDMS)**

Bit 7:1 Reserved

Bit 0 Power Down Mode Select (PDMS)
0 = VESA Compliance power down mode
1 = ACPI power down Spec 1.0 compliance

Flat Panel Registers

FPR30: Flat Panel Type Select

Read/Write Address: 3C5h, Index: 30h
Power-on Default: This is a power-on configurable register (by RESET)

This register specifies different types of flat panel.

7	6	5	4	3	2	1	0
DSTN	**COLOR TFT**			**LCD DISPLAY**		**TFT**	**LCD**

Bit 7 Color DSTN interface type select. This bit is power-on configured by MD15. (DSTN)
0 = 16-bit interface
1 = 24-bit interface

Bit 6:4 Color TFT interface type select. This is a power-on configurable bit by MD [14:12]. For detailed interconnection for different type of LCD panels, please refer to the Flat Panel Interface Chapter of this data book.
000 = 9-bit, 3-bit per R, G, B
001 = 12-bit, 4-bit per R, G, B
010 = 18-bit, 6-bit per R, G, B
011 = 24-bit, 8-bit per R, G, B
100 = 12+12-bit, or 24-bit (two pixels/clock)
101 = analog TFT interface
110 = 18+18-bit, or 36-bit (two pixels/clock)
111 = 24+24-bit (two pixels/clock)

Bit 3:2 LCD display size select for DSTN and TFT LCD. This is a power-on configurable bit by MD [11:10].
00 = 640 x 480
01 = 800 x 600

10 = 1024 x 768
11 = 1280 x 1024 (reserved for color TFT only)

Bit 1 TFT FPSCLK Clock Phase Select. To adjust TFT flat panel data timing, one may wish to change the TFT FPSCLK phase by inverting the TFT FPSCLK. This register is only valid for TFT panel in single pixel/clock mode and 2 pixels/clock mode. (TFT)
This is a power-on configurable bit by MD9.
0 = Normal
1 = Inverted clock

Bit 0 Color LCD type select. This is a power-on configurable bit by MD8. (LCD)
0 = color TFT
1 = color DSTN

FPR31: Virtual Refresh and Auto Shut Down Control

Read/Write Address: 3C5h, Index: 31h
Power-on Default: 00h

This register defines the control for display select, Virtual Refresh mode enable and auto shut-down.

7	6	5	4	3	2	1	0
VRE	**VRES**	**SELECT AUTO S/D**		**EASD**	**DISPLAY SELECT**		

Bit 7 Virtual Refresh Enable. This bit is independent of FPR31 bit [2:0]. (VRE)
0 = Disable
1 = Enable

Bit 6 Virtual Refresh Encode Select (VRES)
0 = Select 8-bit per pixel encode, RGB = 3:3:2
1 = Select 16-bit per pixel encode, RGB = 5:6:5

Bit 5:4 Select Auto Shut-Down Period. Define a period to start auto shut-down of display memory screen refresh cycle and LCD frame buffer write cycle. Auto shut-down mode can only be used when the display is in LCD mode only and Virtual Refresh is enabled. This function is only valid when auto shut-down of memory screen refresh and LCD frame buffer write cycles are enabled (bit 3 of this register = 1).
00 = 8 frames
01 = 16 frames
10 = 32 frames
11 = 64 frames

Bit 3 Enable auto shut-down of display memory screen refresh cycle and LCD frame buffer write cycle in Virtual Refresh mode. This bit is only valid when Virtual Refresh mode is enabled (FPR31 bit 7 = "1"). If the display memory write operation is idle for more than the selected period specified by FPR31 bit [5:4], the display memory screen refresh cycle and LCD frame buffer write cycle will be automatically shut-down when auto shut-down is enabled. The graphics FIFO and video FIFO are also shut-down. Any Host memory write operation to Lynx3DM+ will turn on the display memory screen refresh and LCD frame buffer write cycle at the end of a vertical sync signal. (EASD)

0 = Disable auto shut-down
1 = Enable auto shut-down

Bit 2:0 Display Select. (Note: TV and CRT can not be enabled at the same time.)
000 = Disable all displays (default value)
001 = Enable LCD display
010 = Enable CRT display
011 = Enable both CRT and LCD display
100 = Enable TV display
101 = Enable both TV and LCD display
others = Reserved

FPR32: Dithering Engine Select, Polarity, and Expansion Control

Read/Write Address: 3C5h, Index: 32h
Power-on Default: 00h

This register defines the TFT and DSTN dithering engines select, LCD signal polarities, and screen auto-centering or vertical expansion select.

7	6	5	4	3	2	1	0
TFT DITHERING		**STN**	**LCDV**	**LCDH**	**ACE**	**VLEE**	**HPEE**

Bit 7:6 TFT Dithering Engine Select
00 = No dithering
01 = 4-gray level dithering patterns (for 9-bit, 12-bit, and 18-bit TFT only)
10 = 8-gray level dithering patterns (for 9-bit and 12-bit TFT only)
11 = Reserved

	FPR30 [6:4]			
	= 000	= 001 or 100	= 010 or 110	= 011
Bit [7:6]	**9-bit**	**12-bit**	**18-bit**	**24-bit**
00	512 colors	4K colors	256K colors	16M colors
01	24,389 colors	226,981 colors	16M colors	16M colors
10	185,193 colors	1,771,561 colors	16M colors	16M colors

Bit 5 STN Dithering Engine Select (STN)
0 = Select 16 gray levels for each R, G, and B
1 = Select 32 gray levels for each R, G, and B

Bit 4 LCD VSYNC/FP Polarity Select (LCDV)
0 = Select active "LOW"
1 = Select active "HIGH"

Bit 3 LCD HSYNC/LP polarity Select (LCDH)
0 = Select active "LOW"
1 = Select active "HIGH"

Bit 2 Auto Centering Enable. This register is used to control screen centering for VGA modes. (ACE)
0 = Disable
1 = Enable. This bit needs to be set to "1" and CRT shadow registers need to be reprogrammed to allow screen centering.

Bit 1 Vertical Line Expansion Enable for VGA modes (VLEE)
0 = Disable
1 = Enable

Bit 0 Horizontal Pixel Expansion Enable for VGA modes (HPEE)
0 = Disable
1 = Enable. Character clock is forced to 10-dot timing.

FPR33: Panel Power Sequence and LCD Character/Cursor Blink Control

Read/Write Address: 3C5h, Index: 33h
Power-on Default: 05h

This register defines the control for LCD power ON/OFF sequence timing, lock VGACRT horizontal and vertical display enable, and blinking rate for LCD character/cursor.

7	6	5	4	3	2	1	0
LVDS CONTROL		**VDE**	**PIC**	**PANEL ON/OFF**		**SELECT LCD**	

Bit 7 LVDS Control
0 = LVDS module in power down mode
1 = LVDS module in power-on

Bit 6 Selects TFT LVDS mapping
0 = Generic TFT 24-bit or 18-bit LVDS mapping
1 = Hitachi TFT 24-bit LVDS mapping (for Hitachi 18-bit LVDS panels, this bit should be set to 0)

Bit 5 Lock VGA CRT Vertical and Horizontal Display Enable registers used in Virtual Refresh mode (FPR31 bit 7 = 1) to lock the control signals to LCD BKEND. When this bit is set to 1, it will lock the following registers: CRT01 (3?5h, index1) [Horizontal Display Enable], CRT07 (3?5h, index 07) bit 6 [Vertical Display Enable bit 9] and bit 1[Vertical Display Enable bit 8], CRT12 (3?5h, index12) [Vertical Display Enable]. (VDE)
This register is also used to lock Shadow VGA CRT Horizontal Display Enable and Vertical Display Enable Registers.
0 = unlock (default)
1 = lock

Bit 4 Select panel to drive the digital panel interface (Please see Figure 21: on page 12) (PIC)
0 = FP1 interface drives the digital panel interface
1 = FP2 (virtual) interface drives the digital panel interface
(Note: only FP1 interface connects to the LVDS interface)

Bit 3:2 Panel ON/OFF timing select. These two bits are used to control the time period from FPEN to VBIASEN, from VBIASEN to LCD control signals, and from LCD control signals to FPVDDEN. These two bits are only valid when LCD H/W auto-power ON/OFF sequence is selected (FPR34 bit 7 =1).
00 = 1 vertical frame
01 = 2 vertical frames
10 = 4 vertical frames
11 = 8 vertical frames

Bit 1:0 Select LCD character/cursor blink rate

Bit [1:0]	Cursor	Character
00	16 frames	32 frames
01	32 frames	64 frames
10	64 frames	128 frames

FPR34: LCD Panel ON/OFF Sequence Select and DSTN LCD Control

Read/Write Address: 3C5h, Index: 34h
Power-on Default: 80h

This register defines LCD panel ON/OFF sequence select during display switching and color DSTN panel control, such as: LP pulse width, additional line pulse in odd and even frame.

7	6	5	4	3	2	1	0
SHS	**SLP**	**SELPO**		**SELECT EXTRA LP EVEN FRAME**			

Bit 7 Select Hardware or Software LCD auto-power ON/OFF sequence during display switching in operation or power down modes. This bit can be used to select two different ways to turn ON/OFF LCD panel. For special programming sequences, please refer to the Power Down Management chapter of this data book. (SHS)
0 = Select software LCD power sequencing
1 = Select hardware LCD power sequencing

Bit 6 Select LP (DSTN) Pulse Width in Pixel Clocks (SLP)
0 = 16 pixel clocks
1 = 32 pixel clocks

Bit 5:4 Select Extra LP in Odd Frame for DSTN LCD in Standard Refresh Mode (SELPO)
00 = 0 extra line pulses
01 = 1 extra line pulses
10 = 2 extra line pulses
11 = 3 extra line pulses

Bit 3:0 Select Extra LP in Even Frame for DSTN LCD in Standard Refresh Mode, or Extra LP in Every Frame for DSTN LCD in Virtual Refresh Mode.
0000 = 0 extra line pulses

0001 = 1 extra line pulses
0010 = 2 extra line pulses
.....
1111 = 15 extra line pulses

FPR3E: DSTN LCD Panel Height- High

Read/Write Address: 3C5h, Index: 3Eh
Power-on Default: 00h

This register defines bit 9 and bit 8 of DSTN LCD panel height register. This 10-bit register needs to be programmed as "DSTN LCD panel height ⎪2". This 10-bit register also has to be an even number. For example, DSTN LCD panel height register equals to "12Ch" for a 800x600 DSTN.

7	6	5	4	3	2	1	0
DES	**RESERVED**				**LP**	**DSTN LCD PANEL**	

Bit 7 M-Signal or Display Enable Select (DES)
0 = Select Display Enable as output for Pin 81
1 = Select M-Signal as output for Pin 81

Bit 6:3 Reserved

Bit 2 Free running LP enable for OSTN (LP)
0 = Disable
1 = Enable

Bit 1:0 Bit 9 and bit 8 of the 10-bit DSTN LCD Panel Height Register.

FPR3F: DSTN LCD Panel Height- Low

Read/Write Address: 3C5h, Index: 3Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
BIT [7:0] OF THE 10-BIT DSTN LCD PANEL HEIGHT REGISTER							

This register defines lower 8-bit of DSTN LCD panel height register. This 10-bit register needs to be programmed as "DSTN LCD panel height ⎪2". This 10-bit register also has to be an even number. For example, DSTN LCD panel height register equals to "180h" for a 1024x768 DSTN LCD.

Bit 7:0 Bit [7:0] of the 10-bit DSTN LCD Panel Height Register.

FPR40: Read FIFO1 Start Address Low for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 40h
Power-on Default: Undefined

This register defines the lower 8-bit of the read FIFO1 start address for LCD frame buffer. This Read FIFO1 start address is used for DSTN LCD in standard refresh mode or TFT LCD in Virtual Refresh mode. When DSTN LCD is selected and in Virtual Refresh mode, this register defines the lower 8-bit of the read FIFO1 start address for upper panel of the DSTN LCD.

7	6	5	4	3	2	1	0
BIT [7:0] OF DISPLAY MEMORY READ FIFO1							

Bit 7:0 Select bit [7:0] of display memory read FIFO1 address bus for the LCD frame buffer of DSTN LCD in standard refresh mode or for TFT LCD in Virtual Refresh mode. When Virtual Refresh is enabled (FPR31 bit 7 = 1) and when DSTN LCD is selected (FPR30 [1:0] = 01b), this register selects bit [7:0] of the display memory read FIFO1 address for the upper panel of DSTN LCD.

FPR41: Read FIFO1 Start Address High for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 41h
Power-on Default: Undefined

This register defines the higher 8-bit of the read FIFO1 start address for LCD frame buffer. This Read FIFO1 start address is used for DSTN LCD in standard refresh mode or TFT LCD in Virtual Refresh mode. When DSTN LCD is selected and in Virtual Refresh mode, this register defines the higher 8-bit of the read FIFO1 start address for upper panel of the DSTN LCD.

7	6	5	4	3	2	1	0
BIT [15:8] OF DISPLAY MEMROY READ FIFO1							

Bit 7:0 Select bit [15:8] of display memory read FIFO1 address bus for the LCD frame buffer of DSTN LCD in standard refresh mode or for TFT LCD in Virtual Refresh mode. When Virtual Refresh is enabled (FPR31 bit 7 = 1) and when DSTN LCD is selected (FPR30 [1:0] = 01b), this register selects bit [15:8] of the display memory read FIFO1 address for the upper panel of DSTN LCD.

FPR42: Read FIFO2 Start Address Low for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 42h
Power-on Default: Undefined

This register defines the lower 8-bit of the read FIFO2 start address for LCD frame buffer. This register is only valid when DSTN LCD is selected (FPR30 [1:0] = 01b) and Virtual Refresh is enabled (FPR31 bit 7 = 1).

7	6	5	4	3	2	1	0
BIT [7:0] OF DISPLAY MEMORY READ FIFO2							

Bit 7:0 Select bit [7:0] of display memory read FIFO2 address bus for lower panel of DSTN LCD.

FPR43: Read FIFO2 Start Address High for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 43h
Power-on Default: Undefined

This register defines the higher 8-bit of the read FIFO2 start address for LCD frame buffer. This register is valid only when DSTN LCD is selected (FPR30 [1:0] = 01b) and Virtual Refresh is enabled (FPR31 bit 7 = 1).

7	6	5	4	3	2	1	0
BIT [15:8] OF DISPLAY MEMORY READ FIFO2							

Bit 7:0 Select bit [15:8] of display memory read FIFO2 address bus for lower panel of DSTN LCD.

FPR44: Read FIFO1 Offset Value of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 44h
Power-on Default: Undefined

This register defines the read FIFO1 offset value of LCD Frame buffer. This offset value is used to calculate the read start address of the next line of LCD Frame buffer from the current line. The offset register is a 10-bit register. Bit [3:2] of Read Offset Value Register are in FPR4C register.

7	6	5	4	3	2	1	0
BIT [7:0] OF READ FIFO1							

Bit 7:0 Bit [7:0] of read FIFO1 offset value for LCD frame buffer. This offset value is a direct mapping from bit [10:3] of display memory read address bus.

FPR45: Read FIFO1 Address Offset for LCD Frame Buffer Overflow

Read/Write Address: 3C5h, Index: 45h
Power-on Default: Undefined

This register defines the MSB of the read FIFO1 start address. In additional, this register specifies the MSB of the LCD frame buffer read offset value.

7	6	5	4	3	2	1	0
DISPLAY MEM READ FIFO1				**DISPLAY MEM READ FIFO2**			

Bit 7:4 Bit [19:16] of display memory read FIFO1 address bus. The lower [15:0] of display memory read FIFO1 address is located in FPR41 and FPR40 registers.

When TFT LCD is in Virtual Refresh mode, or DSTN LCD is in standard refresh mode, this register specifies bit [18:16] of display memory read address. This register is used for upper panel of DSTN LCD when Virtual Refresh is enabled (FPR 31 bit 7 = 1) and DSTN LCD (FPR30 [1:0] = 01b) is selected.

Bit 3:0 Bit [19:16] of display memory read FIFO2 address bus for lower panel of DSTN LCD. The lower [15:0] of display memory read FIFO1 address is located in FPR43 and FPR42 registers. This register is valid only when DSTN LCD is selected (FPR30 [1:0] = 01b) and Virtual Refresh is enabled (FPR31 bit 7 = 1).

FPR46: Write Start Address Low of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 46h
Power-on Default: Undefined

This register defines the lower 8-bit of the start address for LCD Write Frame Buffer.

7	6	5	4	3	2	1	0
BIT [7:0] OF START ADDRESS LCD							

Bit 7:0 Bit [7:0] of start address for LCD write frame buffer. This register is a direct mapping from bit [10:3] of display memory write address bus.

FPR47: Write Start Address High of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 47h
Power-on Default: Undefined

This register defines the high byte start address of LCD Write Frame Buffer.

7	6	5	4	3	2	1	0
BIT [7:0] OF START ADDRESS LCD WRITE FRAME BUFFER							

Bit 7:0 Bit [15:8] of start address for LCD write frame buffer. This register is a direct mapping from bit [18:11] of display memory write address bus.

FPR48: Write Offset Value of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 48h
Power-on Default: Undefined

This register defines the offset value of LCD Write Frame Buffer. This offset value is used to calculate the start address of the next line of LCD Write Frame Buffer from the current line. The offset register is a 10-bit register. Bit [9:8] of the write offset value is in FPR49 register.

7	6	5	4	3	2	1	0
BIT [7:0] OF OFFSET VALUE LCD WRITE FRAME BUFFER							

Bit 7:0 Bit [7:0] of offset value for LCD write frame buffer. This offset value is a direct mapping from bit [10:3] of display memory write address bus.

FPR49: LCD Frame Buffer Write Overflow

Read/Write Address: 3C5h, Index: 49h
Power-on Default: Undefined

This register specifies the MSB of the LCD frame buffer write offset address. The lower 8-bit of the LCD frame buffer write offset address is in FPR48.

7	6	5	4	3	2	1	0
START ADDRESS LCD						**OVR**	

Bit 7:2 Bit [21:16] of start address for LCD Write Frame Buffer. This register is a direct mapping from bit [21:19] of display memory write address bus.

Bit 1:0 Bit [9:8] of offset value register of LCD Write Frame Buffer. These two bits are mapped to bit 12 and 11 of display memory write address bus. The lower 8 bits are in FPR48. (OVR)

FPR4A: LCD Read and Write FIFOs Request Level Control

Read/Write Address: 3C5h, Index: 4Ah
Power-on Default: 44h

This register controls the LCD Read and Write FIFOs Request Level. These bits can be used to maximize the available memory bandwidth.

7	6	5	4	3	2	1	0
LCD READ FIFO2		**LCD READ FIFO1**		**RESERVED**		**LCD WRITE FIFO**	

Bit 7:6 LCD Read FIFO2 Request Level. When the LCD Read FIFO2 empty level reaches the level specified by this register, a LCD Read FIFO2 Request will be generated.
00 = RFIFO2 has 4 or more entries empty
01 = RFIFO2 has 8 or more entries empty
1x = RFIFO2 has 12 or more entries empty

Bit 5:4 LCD Read FIFO1 Request Level. When the LCD Read FIFO1 empty level reaches the level specified by this register, a LCD Read FIFO1 Request will be generated.
00 = RFIFO1 has 4 or more entries empty
01 = RFIFO1 has 8 or more entries empty
1x = RFIFO1 has 12 or more entries empty

Bit 3:2 Reserved

Bit 1:0 LCD Write FIFO Request Level. When the LCD Write FIFO filled level reaches the level specified by this register, a LCD Write Request will be generated.
00 = WFIFO has 4 or more entries filled
01 = WFIFO has 8 or more entries filled
1x = WFIFO has 12 or more entries filled

FPR4B: Read FIFO2 Offset Value of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 4Bh
Power-on Default: Undefined

This register defines the read FIFO2 offset value of LCD Frame buffer. This offset value is used to calculate the read start address of the next line of LCD Frame buffer from the current line. The offset register is a 10-bit register.

7	6	5	4	3	2	1	0
BIT [7:0] OF READ FIFO2 OFFSET VALUE							

Bit 7:0 Bit [7:0] of read FIFO2 offset value for LCD frame buffer. This offset value is a direct mapping from bit [10:3] of display memory read address bus. The upper two bits are in FPR4C register.

FPR4C: Read FIFO Offset Value of LCD Frame Buffer Overflow

Read/Write Address: 3C5h, Index: 4Ch
Power-on Default: Undefined

This register defines the read FIFO offset value of LCD Frame buffer. This offset value is used to calculate the read start address of the next line of LCD Frame buffer from the current line.

7	6	5	4	3	2	1	0
READ FIFO2		**RESERVED**		**FPR44**		**RESERVED**	

Bit 7:6 Bit [9:8] of Read FIFO2 offset value register of LCD Frame buffer. These two bits are mapped to bit [12:11] of display memory address bus. The lower 8 bits are in FPR4B register.

Bit 5:4 Reserved

Bit 3:2 Bit [9:8] of Read FIFO 1 offset Lower 8-bit are in FPR44 (FPR44)

Bit 1:0 Reserved

FPR4D: MSB Read FIFO Address

Read/Write Address: 3C5h, Index: 4Dh
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED		**MSB READ FIFO2**		**RESERVED**		**MSB READ FIFO1**	

Bit 7:6 Reserved

Bit 5:4 MSB of Read FIFO2 Address

Bit 3:2 Reserved

Bit 1:0 MSB of Read FIFO1 Address

FPR4E: LCD2 Control Register

Read/Write Address: 3C5h, Index: 4Eh
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED		**DPO**	**VSYNC**	**HSYNC**	**FPSCLK**	**LCD2**	**STN**

Bit 7:6 Reserved

Bit 5 Enable/disable digital panel output (DPO)
0 = Normal. Digital Panel interface connected. (default)
1 = Digital Panel interface is not connected. Fpdata[23:0] pad is in tri-state mode.

Bit 4 VSYNC Sync Phase (VSYNC)
0 = LCD2_VSYNC sync phase same as LCD1_VSYNC
1 = LCD2_VSYNC sync phase invert

Bit 3 HSYNC Sync Phase (HSYNC)
0 = LCD2_HSYNC sync phase same as LCD1_HSYNC
1 = LCD2_HSYNC sync phase invert

Bit 2 FPSCLK Clock (FPSCLK)
0 = LCD2_FPSCLK clock invert
1 = LCD2_FPSCLK clock phase same as LCD1_FPSCLK

Bit 1 LCD2 Panel (LCD2)
0 = Disable LCD2 panel
1 = Enable LCD2 panel

Bit 0 Continuos line pulse for STN (STN)

FPR50: LCD Overflow Register 1 for Virtual Refresh

Read/Write Address: 3C5h, Index: 50h
Power-on Default: Undefined

This register defines the high order MSB bits of LCD Horizontal Sync Start (FPR54), and LCD Vertical Total (FPR55) registers which are used to control Virtual Refresh timing.

7	6	5	4	3	2	1	0
RESERVED				**[10:8] FPR55**			**FPR54**

Bit 7:4 Reserved

Bit 3:1 Bit [10:8] of FPR55, Vertical Total of LCD in Virtual Refresh mode

Bit 0 Bit 8 of FPR54, Horizontal Sync Start of LCD in Virtual Refresh mode (FPR54)

FPR51: LCD Overflow Register 2 for Virtual Refresh

Read/Write Address: 3C5h, Index: 51h
Power-on Default: Undefined

This register defines the overflow bits of FPR52, FPR53, FPR56, and FPR57 registers which are used to control Virtual Refresh timing.

7	6	5	4	3	2	1	0
[10:8] FPR57			**[10:8] FPR 56**			**FPR53**	**FPR4\52**

Bit 7:5 Bit [10:8] of FPR57, Vertical Sync Start of LCD in Virtual Refresh mode

Bit 4:2 Bit [10:8] of FPR56, Vertical Display End of LCD in Virtual Refresh mode

Bit 1 Bit 8 of FPR53, Horizontal Display End of LCD in Virtual Refresh mode (FPR53)

Bit 0 Bit 8 of FPR52, Horizontal Total of LCD in Virtual Refresh mode (FPR52)

FPR52: LCD Horizontal Total for Virtual Refresh

Read/Write Address: 3C5h, Index: 52h
Power-on Default: Undefined

This register defines the bit [7:0] of LCD Horizontal Total. This register is used in Virtual Refresh mode only. It represents one line in TFT LCD and two lines in DSTN LCD. The LSB bit represents a 8-pixel period. The equation to calculate the LCD horizontal total in Virtual Refresh mode is as follows:

For TFT: LCDHT = (LCD panel width + horizontal blanking pixels) ⎪8 - 1
For DSTN: LCDHT = (LCD panel width * 2 + horizontal blanking pixels) ⎪8 - 1

7	6	5	4	3	2	1	0
LCD HORIZONTAL TOTAL							

Bit 7:0 LCD Horizontal Total [7:0] in Virtual Refresh mode. Bit 8 of LCD horizontal total is in FPR51 register.

FPR53: LCD Horizontal Display Enable for Virtual Refresh

Read/Write Address: 3C5h, Index: 53h
Power-on Default: Undefined

This register defines the active horizontal display period of LCD in Virtual Refresh mode. It represents one line in TFT LCD and two lines in DSTN LCD. The equation to calculate the LCD horizontal display enable in Virtual Refresh mode:

For TFT: LCDHDE = (LCD panel width pixels) ⎪ 8 - 1
For DSTN: LCDHDE = (LCD panel width * 2) ⎪ 8 - 1

7	6	5	4	3	2	1	0
LCD HORIZONTAL DISPLAY ENABLE PERIOD							

Bit 7:0 LCD Horizontal display enable period [7:0] in Virtual Refresh mode. Bit 8 of LCD horizontal display enable is in FPR51 register.

FPR54: LCD Horizontal Sync Start for Virtual Refresh

Read/Write Address: 3C5h, Index: 54h
Power-on Default: Undefined

This register defines the LCD horizontal sync start in Virtual Refresh mode. This register is used to generate the start timing of HYSNC for TFT LCD, or the start timing of LP for DSTN LCD. The value in LCDHSS needs to be larger than the value in LCDHDE. The horizontal sync pulse width is 8 pixels or 16 pixels wide, which is dependent on FPR34 bit 6.

7	6	5	4	3	2	1	0
LCD HORIZONTAL SYNC START PERIOD							

Bit 7:0 LCD Horizontal sync start period [7:0] in Virtual Refresh mode. Bit 8 of LCD horizontal sync start is in FPR50 register.

FPR55: LCD Vertical Total for Virtual Refresh

Read/Write Address: 3C5h, Index: 55h
Power-on Default: Undefined

This register defines the bit [7:0] of LCD Vertical Total. This register is used in Virtual Refresh mode only. The calculation equation of LCD vertical total in Virtual Refresh mode is as follows:

For TFT: LCDVT = (LCD panel height + vertical blank lines) - 1

For DSTN: LCDVT = ((LCD panel height ⎪ 2) + vertical blank lines) - 1

7	6	5	4	3	2	1	0
LCD VERTICAL TOTAL							

Bit 7:0 LCD Vertical Total [7:0] in Virtual Refresh mode. Bit [10:8] of LCD vertical total are in FPR50 register.

FPR56: LCD Vertical Display Enable for Virtual Refresh

Read/Write Address: 3C5h, Index: 56h
Power-on Default: Undefined

This register defines the LCD active vertical display period in Virtual Refresh mode. The calculation equation of LCD vertical display enable in Virtual Refresh mode is as follows:

For TFT: LCDVDE = (LCD panel height) - 1

For DSTN: LCDVDE = (LCD panel height ⎪ 2) - 1

7	6	5	4	3	2	1	0
LCD VERTICAL DISPLAY ENABLE PERIOD							

Bit 7:0 LCD vertical display enable period [7:0] in Virtual Refresh mode. Bit [10:8] of LCD vertical display enable are in FPR51 register.

FPR57: LCD Vertical Sync Start for Virtual Refresh

Read/Write Address: 3C5h, Index: 57h
Power-on Default: Undefined

This register defines the LCD vertical sync start in Virtual Refresh mode. This register is used to generate the start timing VSYNC for TFT LCD, or the start timing of FP for DSTN LCD. The value in LCDVSS needs to be larger than the value in LDVDE. The vertical sync pulse width is equal to one horizontal scan line.

7	6	5	4	3	2	1	0
LCD VERTICAL SYNC START PERIOD							

Bit 7:0 LCD Vertical sync start period [7:0] in Virtual Refresh mode. Bit [10:8] of LCD vertical sync start are in FPR51 register.

FPR58: EMI Control Register

Read/Write Address: 3C5h, Index: 58h
Power-on Default: 00h

This register defines the EMI control register for LCD flat panels, including LCD Panel I/O pad drive strength, FSPCLK clock delay control.

7	6	5	4	3	2	1	0
RESERVED					**LCD**	**FPSCLK**	

Bit 7:2 Reserved

Bit 1:0 FPSCLK Clock Control. Each unit of clock is approximately 1.2ns best case or 2.0ns best case.
00 = normal
01 = FPSCLK delays by 1 unit of clock
10 = FPSCLK delays by 2 unit of clock
11 = FPSCLK delays by 3 unit of clock

FPR59: Panel M-Signal Control Register

Read/Write Address: 3C5h, Index: 59h
Power-on Default: 00h

This register defines the panel M-signal control such as modulation clock and modulation count.

7	6	5	4	3	2	1	0
MCS	**MODULATION COUNT**						

Bit 7 Modulation Clock Select (MCS)
0 = Select Frame Clock
1 = Select Line Clock

Bit 6:0 Modulation Count. The modulation is generated at a rate that is specified by the modulation count and modulation clock.

FPR5A: SYNC Pulse-widths Adjustment

Read/Write Address: 3C5h, Index: 5Ah
Power-on Default: 00h

This register allows adjust to the HSYNC and VSYNC Pulsewidths.

7	6	5	4	3	2	1	0
HSYNC					**VSYNC**		

Bit 7:3 Additional HSYNC pulse width in # of character clocks

Bit 2:0 Additional VSYNC pulse width in # of HSYNCs

FPRA0: Panel HW Video Control

Read/Write Address: 3C5h, Index: A0h
Power-on Default: 00h

This register defines the panel video display logic during Virtual Refresh mode. The video display logic will only be activated during Virtual Refresh mode with TFT panel.

7	6	5	4	3	2	1	0
EPV	**EHPD**	**ECK**	**RGB**	**EFS**	**EIC**	**RESERVED**	

Bit 7 Enable Panel Video (EPV)
0 = Disable
1 = Enable

Bit 6 Enable Horizontal Pixel Duplication (EHPD)
0 = Disable
1 = Enable

Bit 5 Enable Color Key (ECK)
0 = Disable
1 = Enable

Bit 4 RGB Format (RGB)
0 = YUV Format
1 = RGB Format

Bit 3 Enable Full screen video (EFS)
0 = Disable
1 = Enable

Bit 2 Enable 8-bit index color mode (only works in Virtual Refresh mode) (EIC)
0 = Disable
1 = Enable

Bit 1:0 Reserved

FPRA1: Panel Video Color Key

Read/Write Address: 3C5h, Index: A1h
Power-on Default: 00h

This register defines the panel video color key [7:0]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY [7:0]							

Bit 7:0 Panel Video Color Key[7:0]

FPRA2: Panel Video Color Key

Read/Write Address: 3C5h, Index: A2h
Power-on Default: 00h

This register defines the panel video color key [15:8]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY [15:8]							

Bit 7:0 Panel Video Color Key[15:8]

FPRA3: Panel Video Color Key Mask

Read/Write Address: 3C5h, Index: A3h
Power-on Default: 00h

This register defines the panel video color key mask [7:0]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY MASK [7:0]							

Bit 7:0 Panel Video Color Key Mask[7:0]

FPRA4: Panel Video Color Key Mask

Read/Write Address: 3C5h, Index: A4h
Power-on Default: 00h

This register defines the panel video color key mask [15:8]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY MASK [15:8]							

Bit 7:0 Panel Video Color Key Mask[15:8]

FPRA5: Panel Video Red Constant

Read/Write Address: 3C5h, Index: A5h
Power-on Default: EDh

This register defines the panel video Red Constant

7	6	5	4	3	2	1	0
PANEL VIDEO RED CONSTANT [7:0]							

Bit 7:0 Panel Video Red Constant [7:0]

FPRA6: Panel Video Green Constant

Read/Write Address: 3C5h, Index: A6h
Power-on Default: EDh

This register defines the panel video green constant

7	6	5	4	3	2	1	0
PANEL VIDEO GREEN CONSTANT [7:0]							

Bit 7:0 Panel Video Green Constant [7:0]

FPRA7: Panel Video Blue Constant

Read/Write Address: 3C5h, Index: A7h
Power-on Default: EDh

This register defines the panel video Blue Constant

7	6	5	4	3	2	1	0
PANEL VIDEO BLUE CONSTANT [7:0]							

Bit 7:0 Panel Video Blue Constant [7:0]

FPRA8: Panel Video Top Boundary

Read/Write Address: 3C5h, Index: A8h
Power-on Default: 00h

This register defines the panel video top boundary

7	6	5	4	3	2	1	0
PANEL VIDEO TOP BOUNDARY [7:0]							

Bit 7:0 Panel Video Top Boundary [7:0]

FPRA9: Panel Video Left Boundary

Read/Write Address: 3C5h, Index: A9h
Power-on Default: 00h

This register defines the panel video left boundary

7	6	5	4	3	2	1	0
PANEL VIDEO LEFT BOUNDARY [7:0]							

Bit 7:0 Panel Video Left Boundary [7:0]

FPRAA: Panel Video Bottom Boundary

Read/Write Address: 3C5h, Index: AAh
Power-on Default: 00h

This register defines the panel video bottom boundary

7	6	5	4	3	2	1	0
PANEL VIDEO BOTTOM BOUNDARY [7:0]							

Bit 7:0 Panel Video Bottom Boundary [7:0]

FPRAB: Panel Video Right Boundary

Read/Write Address: 3C5h, Index: ABh
Power-on Default: 00h

This register defines the panel video Right boundary

7	6	5	4	3	2	1	0
PANEL VIDEO RIGHT BOUNDARY [7:0]							

Bit 7:0 Panel Video Right Boundary [7:0]

FPRAC: Panel Video Top and Left Boundary Overflow

Read/Write Address: 3C5h, Index: ACh
Power-on Default: 00h

This register defines the panel video top and left boundary overflow

7	6	5	4	3	2	1	0
PVLB			**RESERVED**			**PVTB**	

Bit 7:5 Panel Video Left Boundary [10:8] (PVLB)

Bit 4:3 Reserved

Bit 2:0 Panel Video Top Boundary [10:8] (PVTB)

FPRAD: Panel Video Bottom and Right Boundary Overflow

Read/Write Address: 3C5h, Index: ADh
Power-on Default: 00h

This register defines the panel video bottom and right boundary overflow

7	6	5	4	3	2	1	0
PVRB			**RESERVED**		**PVBB**		

Bit 7:5 Panel Video Right Boundary [10:8] (PVRB)

Bit 4:3 Reserved

Bit 2:0 Panel Video Bottom Boundary [10:8] (PVBB)

FPRAE: Panel Video Vertical Stretch Factor

Read/Write Address: 3C5h, Index: AEh
Power-on Default: 00h

This register defines the panel video vertical stretch factor.

7	6	5	4	3	2	1	0
PANEL VIDEO VERTICAL STRETCH FACTOR [7:0]							

Bit 7:0 Panel Video Vertical Stretch Factor [7:0]. The stretch factor equals to:
S/D * 256.
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch.

FPRAF: Panel Video Horizontal Stretch Factor

Read/Write Address: 3C5h, Index: AFh
Power-on Default: 00h

This register defines the panel video horizontal stretch factor

7	6	5	4	3	2	1	0
PANEL VIDEO HORIZONTAL STRETCH FACTOR [7:0]							

Bit 7:0 Panel Video Horizontal Stretch Factor [7:0] The stretch factor equals to:
S/D * 256. Note: when stretch factor is set to 0, it becomes a 1-to-1 stretch.

Memory Control Registers

MCR60: Memory Control

Read/Write Address: 3C5h, Index: 60h
Power-on Default: 00h

This register specifies memory control for Memory Address Wrap Around, DRAM refresh, VGA to memory burst write, and synchronization. This register also includes RAMDAC Write/Read Command Pulse Width select.

7	6	5	4	3	2	1	0
TRDL	**BWC**	**RAM**	**DVGA**	**VGAF**	**R**	**DDRR**	**DRC**

Bit 7 TRDL - Procreate termination cycle (TRDL)
0 = TRDL 2 clock (default)
1 = TRDL 1 clock

Bit 6 Block Write Control (BWC)
0 = Block write enabled
1 = Block Write not enabled (default)

Bit 5 RAMDAC Write/Read Command Pulse Width Select (RAM)
0 = Command Pulse is 4 MCLK high and 12 MCLK low
1 = Command Pulse is 8 MCLK high and 24 MCLK low

Bit 4 Disable VGA to memory burst write (DVGA)
0 = Enable
1 = Disable

Bit 3 VGA FIFO Empty Level Request Select. VGA FIFO is 8 level deep. (VGAF)
0 = VGA FIFO request if VGA FIFO is two level empty
1 = VGA FIFO request if VGA FIFO is four level empty

Bit 2 Reserved (R)

Bit 1 Disable DRAM Refresh Request (DDRR)
0 = Enable
1 = Disable

Bit 0 DRAM Refresh Control (DRC)
0 = Normal DRAM refresh
1 = Force to 1 DRAM refresh per scan line

MCR61: Memory Bank Address High

Read/Write Address: 3C5h, Index: 61h
Power-on Default: 00h

This register specifies the high order memory bank address for non-linear addressing (or banking) mode (SCR18 bit 0 = 0).

7	6	5	4	3	2	1	0
MEMORY BANK ADDRESS HIGH							

Bit 7:0 Memory Bank Address High

Specifies the high-order address for memory access in non-linear addressing (or banking) mode. The host will take these bits append with address [15:0] to form a 22 bits address (4Mbyte).

MCR62: Memory Type and Timing Control

Read/Write Address: 3C5h, Index: 62h
Power-on Default: This is a power-on configurable register (by RESET)

Lynx3DM+ supports both internal and external memory. This register specifies the memory type and memory timing control. This register is power-on configurable by MD [7:0] of memory data bus.

7	6	5	4	3	2	1	0
RESERVED							

Bit 7:0 Reserved

MCR76: Memory Type and Timing Control

Read/Write Address: 3C5h, Index: 76h
Power-on Default: This is a power-on configurable register (by RESET)

7	6	5	4	3	2	1	0
EMDS		**EMDC**		**TBWC**	**EEM**	**EMPD**	**EMR**

Bit 7:6 MCB Memory Size
00 = 8MB
01 = 16MB
10 = Reserved
11 = 4MB

Bit 5:4 MCB memory Column Address Select
11= 8-bit column address
10 = 9-bit column address
0x = 10-bit column address

Bit 3 MCB Memory Block Write Cycle time
0 = 1 MCLK
1 = 2 MCLK

Bit 2 Reserved (Default = 1)

Bit 1 MCB Memory Active to Precharge Delay (tras)
0 = 4 MCLK
1 = 3 MCLK

Bit 0 MCB Memory Refresh to Command Delay (trc)
0 = 4 MCLK
1 = 3 MCLK

Clock Control Registers

CCR65: TV Encoder Control Register

Read/Write Address: 3C5h, Index: 65h
Power-on Default: 00h

This register specifies the various TV controls.

7	6	5	4	3	2	1	0
SVHS	**CVBS**	**TVEE**	**CRTDAC**	**CRRC**	**CRTDAC**	**TVCS**	**CHOS**

Bit 7 SVHS TV enable (SVHS)
0 = SVHS TV off
1 = SVHS TV on

Bit 6 CVBS TV enable (CVBS)
0 = CVBS TV off
1 = CVBS TV on

Bit 5 TV Encoder Enable (TVEE)
0 = Disable TV Encoder (TVCLK disable)
1 = Enable TV Encoder

Bit 4, 2 00 = Connect CRTRGB from video mixer to CRTDAC
01 = Connect TVRGB (CRTRGB go through flicker reduction) to CRTDAC
10 = Connect LCDRGB from fpbkend to CRTDAC

Bit 3 Color RAM read control (CRRC)
0 = Read from CRT color RAM
1 = Read from LCD color RAM

Bit 1 TV clock select (TVCS)
0 = TVCLK generated from VCLK
1 = TVCLK generated from REFCLK input

Bit 0 CRT HSYNC output select (CHOS)

0 = CRTHYSNC output to CRTHSYNC pin
1 = CRT composite SYNC to CRTHSYNC pin

CCR66: RAM Control and Function On/Off Register

Read/Write Address: 3C5h, Index: 66h
Power-on Default: 00h

7	6	5	4	3	2	1	0
ROOC		**RWCB2**		**CRT RAM**		**MCE**	**DEE**

Bit 7:6 RAMLUT On/Off Control (ROOC)

0	0	Both RAM ON*~
1	0	LCD RAM OFF
0	1	CRT RAM OFF
1	1	Both RAM OFF

Bit 5:4 RAM Write Control Bits (RWCB2)

0	0	Write both RAM (CRT/LCD)
1	0	Write CRT RAM only
0	1	Write LCD RAM only
1	1	Reserve

Bit 3:2 CRT RAM 8/6 Bits and Gamma Control

0	0	6-bits RAM
1	0	8-bits RAM
x	1	Gamma correct ON

Bit 1 Motion Comp Enable (MCE)
1 = Disable MComp*~
0 = Enable MComp
Include MCCLK off

Bit 0 3D DrawEng Enable (DEE)
1 = Disable 3DEng*~
0 = Enable 3DEng
Include 3DMCLK and 3DMCLKB off

CCR67: For Test Purpose Only

Read/Write Address: 3C5h, Index: 67h
Power-on Default: 00h

7	6	5	4	3	2	1	0
PDFC		**TIFC**	**LPDFC**	**BHPS**	**RESERVED**		

Bit 7:6 11 = The power down frame counter is incremented by toggle CCR67_5 (PDFC)

10 = The power down frame counter is incremented by Vsync

Bit 5 Toggle this bit will increment the frame counter in test mode (CCR67_[7:6] = 11) (TIFC)

Bit 4 1 = To load the power down frame counter the following value will be loaded into the frame counter: (CCR67_[2:0], CCR66_[7:0], CCR65_[7:4], 4'b0000) (LPDFC)
0 = Normal operation. The frame counter increment by Vsync

Bit 3 1 = Bypass hardware power sequencer for the FPdata. If select software power sequence this bit will not function (BHPS)
0 = LCD power sequencer will function

Bit 2:0 Reserved

CCR68: Clock Control 1

Read/Write Address: 3C5h, Index: 68h
Power-on Default: C0h

This register is used to select clock frequencies and pulse-width control.

7	6	5	4	3	2	1	0
VCLKF		**ISO**	**CLK**	**SELECT VCLK**		**SELECT MCLK**	

Bit 7:6 Select VCLK frequency based on the following table (VCLKF)

Bit [7:6]	~EXCKEN	VCLK frequency
00	1	VCLK is selected from VGA 3C2h register
01	1	VCLK is selected from programmable VCLK registers: CCR6C and CCR6D
10	1	VCLK is selected from 17.734 MHz
11	1	VCLK is selected from 14.131818 MHz
xx	0	VCLK is selected from CKIN input

Bit 5 Enable ISO standard at VGA modes. This bit is designed to increase the CRT screen refresh rate to ISO standard at VGA modes. This bit is used only when CCR68 bit [7:6] = 00b. (ISO)
0 = Standard VGA frequency which controlled by 3C2h bit [3:2]
1 = ISO frequency which selected by 3C2h bit [3:2]

CCR68 Bit 5	3C2h Bit [3:2]	VCLK frequency
0	00	25.180 MHz
0	01	28.325 MHz
1	00	31.500 MHz
1	01	35.484 MHz

Bit 4 Select 8-dot character clock and disable dot clock divided by 2 function. This bit is used when LCD or TV is selected (determined by FPR31 [2:0]). When this bit set to "1", the bit 3 and bit 0 setting of VGA Clocking Mode Register will be ignored. (CLK)
0 = Character clock and dot clock are controlled by VGA clocking mode register
1 = Select 8-dot character clock and non-divided by 2 dot clock

Bit 3:2 Select MCLK high pulse width
00 = default value
01 = reduce 1 ns high time
10 = increase 1 ns high time
11 = increase 2 ns high time

Bit 1:0 Select VCLK high pulse width
00 = default value
01 = reduce 1 ns high time
10 = increase 1 ns high time
11 = increase 2 ns high time

CCR69: Clock Control 2

Read/Write Address: 3C5h, Index: 69h
Power-on Default: 80h

This register is used to select Virtual Refresh clock frequency, DRAM refresh clock frequency during sleep mode and standby mode, and HSYNC & VSYNC control during sleep mode.

7	6	5	4	3	2	1	0
TVCLK	**TDSS**	**LVDSCLK**		**DRAM**	**SHVSM**	**SELECT VRCLK**	

Bit 7 TVCLK or BLANK Select (TVCLK)
0 = Select BLANK output for pin 158
1 = Select TVCLK to external analog NTSC/PAL TV encoder via pin 158. TVCLK is equal to ¼ of VCLK, where VCLK is programmable by CCR6C and CCR6D registers.

Bit 6 Test Data Source Select. This bit is used for LSI testing only. (TDSS)
0 = Select index color data for test data
1 = Select direct color data for test data

Bit 5:4 Select LVDSCLK output clock source when ~EXCKIN = 1.
00 = Select inverted VRCLK
01 = Output is always low
10 = Select inverted WFIFO clock (same as inverted VCLK)
11 = Select WFIFO clock (same as VCLK)

Bit 3 Select refresh clock source to control DRAM refresh during sleep mode and standby mode. It is recommended to select external 32 KHz refresh clock to achieve highest power saving. (DRAM)
0 = Select external 32 KHz refresh clock
1 = Select internal PLL. During standby or sleep mode, the VCLK and MCLK frequency are selected by PDR20 [5:4]. MCLK is used to replace external 32 KHz refresh clock to control DRAM refresh.

Bit 2 Select HSYNC and VSYNC during Sleep Mode. (PDR20 bit 7 = 1) This bit is used to support VESA DPMS during Sleep Mode. Lynx3DM+ will automatically support VESA DPMS Standby Mode during its internal Standby Mode. (SHVSM)

Bit 2	DPMS STATE	HSYNC	VSYNC
0	Suspend	Pulses	No Pulses
1	Off	No Pulses	No Pulses

Bit 1:0 Select Virtual Refresh clock (VRCLK). The VRCLK is used to generate the timing sequence of LCD interface signals and control logic during Virtual Refresh mode.

Bit [1:0]	VRCLK Frequency
00	VCLK2
01	½ MCLK
10	MCLK
11	programmable Video Clock[1]

Notes:

1. In TV display mode, VCLK is set up as 14.31818 MHz clock from CKIN input (CCR68 [7:6] = 11b) to control TV timing. VRCLK could be chosen from programmable Video Clock which is selected by CCR6C and CCR6D registers by programming CCR69 [1:0] = 11b.

2. In non-Virtual Refresh mode (FPR31 bit 7 = 0), VRCLK is the same as VCLK.

CCR6A: MCLK Numerator Register

Read/Write Address: 3C5h, Index: 6Ah
Power-on Default: 0Fh

This register specifies the 8-bit numerator value of MCLK frequency (MNR). The MNR value is used to calculate the programmable MCLK frequency as follow:

7	6	5	4	3	2	1	0
CALCULATE MCLK FREQUENCY [8]							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected MCLK frequency. The power-on default of this register is 5Ah. Along with CCR6B, the default frequency is set to 40.27 MHz.

CCR6B: MCLK Denominator Register

Read/Write Address: 3C5h, Index: 6Bh
Power-on Default: 04h

This register specifies the 6-bit denominator value of MCLK frequency (MDR). The MDR value is used to calculate the programmable MCLK frequency as follow:

7	6	5	4	3	2	1	0
RESERVED		**CALCULATE MCLK FREQUENCY [6]**					

Bit 7:6 Reserved

Bit 5:0 Specify the 6-bit denominator value to calculate the selected MCLK frequency. The power-on default of this register is 20h. Along with CCR6A, the default frequency is set to 40.27 MHz.

CCR6C: VCLK Numerator Register

Read/Write Address: 3C5h, Index: 6Ch
Power-on Default: 1Fh

This register specifies the numerator value of VCLK frequency (VNR). The VNR value is used to calculate the programmable VCLK frequency as follow:

7	6	5	4	3	2	1	0
CALCULATE VCLK FREQUENCY							

Bit 7:0 Specify the numerator value to calculate the selected VCLK frequency. The power-on default setting of this register is 5Bh. Along with CCR6D, the default frequency is set to 28.325 MHz.

CCR6D: VCLK Denominator Register

Read/Write Address: 3C5h, Index: 6Dh
Power-on Default: 0Fh

This register specifies the 6-bit denominator (VDR) value of and 1 bit post scalar (PS) value of VCLK frequency. The VDR value is used to calculate the programmable VCLK frequency. The post scalar is used to support VCLK frequencies which originally need high and even VDR value. With PS enabled, the revised VDR value should be set half of the original VDR value in order to reduce potential jitters.

7	6	5	4	3	2	1	0
EPS	**EVC0**	**VCLK FREQUENCY [6]**					

Bit 7 Enable Post Scalar. When post scalar is enabled, the revised VDR value is 1/2 of its original VDR value. (EPS)
0 = Disable
1 = Enable

Bit 6 Enable second VC0 (EVC0)
0 = Disable
1 = Enable

Bit 5:0 Specify the 6-bit denominator value to calculate the selected VCLK frequency. The power-on default setting of this register is 2Eh. Along with CCR6C, the default frequency is set to 28.325 MHz.

CCR6E: VCLK2 Numerator Register

Read/Write Address: 3C5h, Index: 6Eh
Power-on Default: 5Ah

This register specifies the 8-bit numerator value of VCLK2 frequency (VCKL2NR). The VCLK2NR value is used to calculate the programmable VCLK2 frequency as follow:

7	6	5	4	3	2	1	0
VCLK2 FREQUENCY [8]							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected VCLK2 frequency. Along with CCR6F, the default frequency is set to 40.27 MHz.

CCR6F: VCLK2 Denominator Register

Read/Write Address: 3C5h, Index: 6Fh
Power-on Default: 20h

This register specifies the 6-bit denominator value of VCLK2 frequency (VCLK2DR). The VCLK2DR value is used to calculate the programmable VCLK2 frequency as follow:

7	6	5	4	3	2	1	0
EPS	**EVC0**	**CALCULATE VCLK2 FREQUENCY [6]**					

Bit 7 Enable Post Scalar. When post scalar is enabled, the revised VDR value is 1/2 of its original VDR value. (EPS)
0 = Disable
1 = Enable

Bit 6 Enable second VC0 (EVC0)
0 = Disable
1 = Enable

Bit 5:0 Specify the 6-bit denominator value to calculate the selected VCLK2 frequency. Along with CCR6E, the default frequency is set to 40.27 MHz.

CCR7A-CCR7C: TV and RAMDAC Testing Power

Read/Write Address: 3C5h, Index: 7Ah-7Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
TV AND RAMDAC TESTING POWER ON RESET = 00							

Bit 7:0 TV and RAMDAC testing power on reset = 00

Note: See Appendix E for further details.

CCR7D: Control Registers for TV and RAMDAC Testing

Read/Write Address: 3C5h, Index: 7Dh
Power-on Default: 00h

7	6	5	4	3	2	1	0
TV	**SVHS**	**CVBS**	**MD**	**VCLK**	**MCLK**	**RESERVED**	

Bit 7 TV Detect (TV)
0 = Normal operation
1 = Use CCR7A, CCR7B, and CCR7C data to check for TV detect

Bit 6 Read only for SVHS Detect (SVHS)

Bit 5 Read only for CVBS detect (CVBS)

Bit 4 Monitor Detect (MD)
0 = Normal operation
1 = Use CCR7A, CCR7B, and CCR7C data to check for monitor detect

Bit 3 External VCLK
0 = Normal operation
1 = Enable external VCLK

Bit 2 External MCLK
0 = Normal operation
1 = Enable external MCLK

Bit 1:0 Reserved
Note: See Appendix E for further details.

General Purpose Registers

GPR70: Scratch Pad Register 1

Read/Write Address: 3C5h, Index: 70h
Power-on Default: Undefined except for bit [3:0] which are power-on configurable (by RESET)

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD REG BITS				**SCRATCH PAD REG BITS MD [19:16]**			

Bit 7:4 Scratch pad register bits. This register can be used as general purpose bits.

Bit 3:0 Scratch pad register bits. These lower 4 bits are also connected to MD [19:16] of memory data bus. The external pull-down on MD lines will generate a logic "0", and internal pull-up will generate a logic "1" during power-on reset period. For power-on configuration, please refer to Initialization chapter of this data book.

GPR71: Scratch Pad Register 2

Read/Write Address: 3C5h, Index: 71h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 2 REGISTER							

Bit 7:0 Scratch Pad 2 register. This register can be used as general purpose scratch bits.

GPR72: User Defined Register 1 for DDC2/ I2C

Read/Write Address: 3C5h, Index: 72h
Power-on Default: 00h

This register is used for user defined registers: USR1/SDA and USR0/SCL. The SDA and SCL can be used for VESA DDC2 / I2C serial communication port.

7	6	5	4	3	2	1	0
RESERVED		**EUSR1**	**EUSR0**	**USR1S**	**USR0S**	**USR1W**	**USR0W**

Bit 7:6 Reserved

Bit 5 Enable USR1/SDA Port (EUSR1)
0 = Disable use of bit 1 of this register
1 = Enable use of bit 1 of this register

Bit 4 Enable USR0/SCL Port (EUSR0)
0 = Disable use of bit 0 of this register
1 = Enable use of bit 0 of this register

Bit 3 USR1/SDA Status (Read only). This bit can be used for DDC2/I2C Data. (USR1S)
0 = pin USR1/SDA is low
1 = pin USR1/SDA is tri-stated

Bit 2 USR0/SCL Status (Read only). This bit can be used for DDC2/I2C Clock. (USR0S)
0 = pin USR0/SCL is low
1 = pin USR0/SCL is tri-stated

Bit 1 USR1/SDA Write. Pin 131 can be used for DDC2/I2C Data. When pin USR1/SDA is tri-stated, other devices may drive this line. The actual state of the pin USR1/SDA is read via bit 3 of this register. (USR1W)
0 = pin USR1/SDA is driven low
1 = pin USR1/SDA is tri-stated

Bit 0 USR0/SCL Write. Pin 132 can be used for DDC2/I2C Clock. When pin USR0/SCL is tri-stated, other devices may drive this line. The actual state of the pin USR0/SCL is read via bit 2 of this register. (USR0W)0 = pin USR0/SCL is driven low
1 = pin USR0/SCL is tri-stated

Note: See Appendix D for further details.

GPR73: User Defined Register 2

Read/Write Address: 3C5h, Index: 73h
Power-on Default: 00h

This register can be used to control user programmable outputs: USR2 and USR3 pins.

7	6	5	4	3	2	1	0
RESERVED		**USR3P**	**USR2P**	**USER3**	**USER2**	**USR3W**	**USR2W**

Bit 7:6 Reserved

Bit 5 Enable USR3 Port (USR3P)
0 = Disable use of bit 1 of this register
1 = Enable use of bit 1 of this register

Bit 4 Enable USR2 Port (USR2P)
0 = Disable use of bit 0 of this register
1 = Enable use of bit 0 of this register

Bit 3 USER3 Status (Read only) (USER3)
0 = pin USR3 is low
1 = pin USR3 is tri-stated

Bit 2 USER2 Status (Read only) (USER2)
0 = pin USR2 is low
1 = pin USR2 is tri-stated

Bit 1 USR3 Write. When pin USR3 is tri-stated, other devices may drive this line. The actual state of the pin USR3 is read via bit 3 of this register. (USR3W)
0 = pin USR3 is driven low
1 = pin USR3 is tri-stated

Bit 0 USR2 Write. When pin USR2 is tri-stated, other devices may drive this line. The actual state of the pin USR2 is read via bit 2 of this register. (USR2W)
0 = pin USR2 is driven low

1 = pin USR2 is tri-stated

GPR74: Scratch Pad Register 3

Read/Write Address: 3C5h, Index: 74h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 3 REGISTER							

Bit 7:0 Scratch Pad 3 register. This register can be used as general purpose scratch bits.

GPR75: Scratch Pad register 4

Read/Write Address: 3C5h, Index: 75h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 4 REGISTER							

Bit 7:0 Scratch Pad 4 register. This register can be used as general purpose scratch bits.

Pop-up Icon and Hardware Cursor Registers

PHR80: Pop-up Icon and Hardware Cursor Pattern Location Low

Read/Write Address: 3C5h, Index: 80h
Power-on Default: Undefined

This register specifies the low 8 bits of the address for pop-up icon and Hardware Cursor Pattern Location, which is a 11-bit register. The high order 3 bits are specified in the PHR81 [2:0] register.

7	6	5	4	3	2	1	0
POP-UP ICON AND HARDWARE CURSOR PATTERN							

Bit 7:0 Pop-up Icon and Hardware Cursor Pattern Location Low. The PHR80 and PHR81 [2:0] registers allocate 2KB off-screen memory within the maximum 4MB of physical memory. The lower 1KB is used to store Pop-up Icon image. The upper 1KB is used to store Hardware Cursor image

PHR81: Hardware Cursor Enable & PI/HWC Pattern Location High

Read/Write Address: 3C5h, Index: 81h
Power-on Default: 0xh

This register specifies the hardware cursor enable and the high-order 3 bits of the address for pop-up icon and Hardware Cursor Pattern Location, which is a 11-bit register. The low order 8 bits are specified in the PHR80 register.

7	6	5	4	3	2	1	0
HCE	**R**	**POP-UP ICON**					

Bit 7 Hardware Cursor Enable (HCE)
0 = Disable (default)
1 = Enable

Bit 6 Reserved (R)

Bit 5:0 Pop-up Icon and Hardware Cursor Pattern Location High. The PHR80 and PHR81 [2:0] registers allocate 2KB off-screen memory within the maximum 32MB of physical memory. The lower 1KB is used to store Pop-up Icon image. The upper 1KB is used to store Hardware Cursor image.

Pop-up Icon Registers

POP82: Pop-up Icon Control

Read/Write Address: 3C5h, Index: 82h
Power-on Default: 00h

This register specifies the control for pop-up icon.

7	6	5	4	3	2	1	0
PUIE	**PUIZE**	**RESERVED**					

Bit 7 Pop-up Icon Enable (PUIE)
0 = Disable
1 = Enable

Bit 6 Pop-up Icon Zoom Enable (PUIZE)
0 = Normal. (Pop-up Icon size is 64x64x2)
1 = zoom up the Pop-up Icon size by 2. (Pop-up Icon size is 128x128x2)

Bit 5:0 Reserved

POP83: Reserved

Read/Write Address: 3C5h, Index: 83h
Power-on Default: Undefined

This register is reserved.

7	6	5	4	3	2	1	0
RESERVED							

Bit 7:0 Reserved

POP84: Pop-up Icon Color 1

Read/Write Address: 3C5h, Index: 84h
Power-on Default: Undefined

This register specifies the color1 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR1							

Bit 7:0 Pop-up icon color1.

POP85: Pop-up Icon Color 2

Read/Write Address: 3C5h, Index: 85h
Power-on Default: Undefined

This register specifies the color2 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR2							

Bit 7:0 Pop-up icon color2.

POP86: Pop-up Icon Color 3

Read/Write Address: 3C5h, Index: 86h
Power-on Default: Undefined

This register specifies the color3 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR3							

Bit 7:0 Pop-up icon color3.

POP90: Pop-up Icon Start X - Low

Read/Write Address: 3C5h, Index: 90h
Power-on Default: Undefined

This register specifies Pop-up icon location X start [7:1]. The pop icon can only be moved in X direction by increments of 2 pixels. Bit [0] has no effect

7	6	5	4	3	2	1	0
POP-UP ICON X START [7:0]							**NE**

Bit 7:1 Pop-up icon X start [7:1]

Bit 0 Has no effect (NE)

POP91: Pop-up Icon Start X - High

Read/Write Address: 3C5h, Index: 91h
Power-on Default: Undefined

This register specifies Pop-up icon location X start [11:8]

7	6	5	4	3	2	1	0
RESERVED					**POP-UP ICON X START**		

Bit 7:3 Reserved

Bit 2:0 Pop-up icon X start [10:8]

POP92: Pop-up Icon Start Y - Low

Read/Write Address: 3C5h, Index: 92h
Power-on Default: Undefined

This register specifies Pop-up icon location Y start [7:0]

7	6	5	4	3	2	1	0
POP-UP ICON Y START							

Bit 7:0 Pop-up icon Y start [7:0]

POP93: Pop-up Icon Start Y - High

Read/Write Address: 3C5h, Index: 93h
Power-on Default: Undefined

This register specifies Pop-up icon location Y start [11:8]

7	6	5	4	3	2	1	0
RESERVED					**POP-UP ICON Y START**		

Bit 7:3 Reserved

Bit 2:0 Pop-up icon Y start [10:8]

Hardware Cursor Registers

HCR88: Hardware Cursor Upper Left X Position - Low

Read/Write Address: 3C5h, Index: 88h
Power-on Default: 00h

This register specifies the lower 8-bit upper left X position for hardware cursor.

7	6	5	4	3	2	1	0
HARDWARE CURSOR X POSITION LOW ORDER							

Bit 7:0 Hardware Cursor X position low order 8 bits. The high order 3 bits are in HCR89[2:0].

HCR89: Hardware Cursor Upper Left X Position- High

Read/Write Address: 3C5h, Index: 89h
Power-on Default: 00h

This register specifies the upper left X position for hardware cursor.

7	6	5	4	3	2	1	0
RESERVED				**HCUL**	**HCXP**		

Bit 7:4 Reserved

Bit 3 Hardware Cursor Upper Left X Position Boundary Select (HCUL)
0 = hardware cursor is within the screen left side boundary. {HCR89[2:0], HCR88[7:0]} specify the X position of the hardware cursor from the left side boundary.
1 = hardware cursor is partially or totally outside of the left side screen boundary. HCR88 [4:0] specify how many pixels of the hardware cursor are outside the left side screen boundary.

Bit 2:0 Hardware Cursor X position high-order 3 bits. The low order 8 bits are specified in the HCR88 register. (HCXP)

HCR8A: Hardware Cursor Upper Left Y Position - Low

Read/Write Address: 3C5h, Index: 8Ah
Power-on Default: 00h

This register specifies the upper left Y position for hardware cursor.

7	6	5	4	3	2	1	0
HARDWARE CURSOR Y POSITION LOW ORDER							

Bit 7:0 Hardware Cursor Y position low order 8 bits. The high order 3 bits are in HCR8B [2:0].

HCR8B: Hardware Cursor Upper Left Y Position - High

Read/Write Address: 3C5h, Index: 8Bh
Power-on Default: 00h

This register specifies the upper left Y position for hardware cursor.

7	6	5	4	3	2	1	0
RESERVED				**HCUL**	**HCYP**		

Bit 7:4 Reserved

Bit 3 Hardware Cursor Upper Left Y Boundary Select (HCUL)
0 = hardware cursor is within the screen top side boundary. {HCR8B[2:0], HCR8A[7:0]} specify the Y position of the hardware cursor from the top side boundary.
1 = hardware cursor is partially or totally outside of the top side screen boundary. HCR8A [4:0] specify how many pixels of the hardware cursor are outside the top side screen boundary.

Bit 2:0 Hardware Cursor Y position high-order 3 bits. The low order 8 bits are specified in the HCR8A register. (HCYP)

HCR8C: Hardware Cursor Foreground Color

Read/Write Address: 3C5h, Index: 8Ch
Power-on Default: 00h

This register specifies the foreground color for hardware cursor. Hardware Cursor is always in 24-bit color. The 24-bit color is the expansion of 3:3:2 RGB into 8:8:8 RGB color.

7	6	5	4	3	2	1	0
HARDWARE CURSOR FOREGROUND COLOR							

Bit 7:0 Hardware Cursor foreground color
This register defines 3:3:2 8-bit RGB of the Hardware Cursor foreground color.

HCR8D: Hardware Cursor Background Color

Read/Write Address: 3C5h, Index: 8Dh
Power-on Default: 00h

This register specifies the background color for hardware cursor. Hardware Cursor is always in 24-bit color. The 24-bit color is the expansion of 3:3:2 RGB into 8:8:8 RGB color.

7	6	5	4	3	2	1	0
HARDWARE CURSOR BACKGROUND COLOR							

Bit 7:0 Hardware Cursor background color
This register defines 3:3:2 8-bit RGB of the Hardware Cursor background color.

Extended CRT Control Registers

CRT30: CRTC Overflow and Interlace Mode Enable

Read/Write Address: 3?5h, Index: 30h
Power-on Default: 00h

This register specifies the CRTC overflow registers and Interlace Mode Enable.

7	6	5	4	3	2	1	0
IME	**CRTHR**	**CRT DISPLAY**		**CVTR**	**CVDER**	**CVBS**	**CVRS**

Bit 7 Interlace Mode Enable (IME)
0 = Disable
1 = Enable

Bit 6 Bit 8 of the horizontal register. Bit [7:0] are located at CRTC register index 00.

Bit 5:4 Bit [17:16] of the CRT display starting address. The lower order 16-bit are located in CRTC register index 0Ch and 0Dh.

Bit 3 Bit 10 of the CRT vertical total register. The lower bit [9:0] are defined in CRTC register index 07h and 06h. (CVTR)

Bit 2 Bit 10 of the CRT vertical display end register. The lower bit [9:0] are defined in CRTC register index 12h and 07h. (CVDER)

Bit 1 Bit 10 of the CRT vertical blank start. The lower bit [9:0] are defined in CRTC register index 15 h, 09h, and 07h. (CVBS)

Bit 0 Bit 10 of the CRT vertical retrace start. The lower bit [9:0] are defined in CRTC register index 10h and 07h. (CVRS)

CRT31: Interlace Retrace

Read/Write Address: 3?5h, Index: 31h
Power-on Default: 00h

This register specifies when vertical retrace begins. This register is only valid if interlace mode is enabled (CRT30 Bit 7 = 1).

7	6	5	4	3	2	1	0
SPECIFIY # CHARACTER UNITS IN HORIZONTAL TIMING							

Bit 7:0 Specify the number of character units in horizontal timing when vertical retrace begins.

CRT32: TV Vertical Display Enable Start

Read/Write Address: 3?5h, Index: 32h
Power-on Default: 00h

This register specifies the vertical display enable start for TV timing.

7	6	5	4	3	2	1	0
TV VERTICAL DISPLAY ENABLE							

Bit 7:0 When CRT vertical count = CRT32 [7:0], TV vertical display enable become active.

CRT33: TV Vertical Display Enable End - High

Read/Write Address: 3?5h, Index: 33h
Power-on Default: 00h

This register specifies the vertical display enable end for TV timing. This register is a 11-bit register. The lower 8-bit of this register resides in CRT34.

7	6	5	4	3	2	1	0
ITE	**HBE**		**VBE**		**CRT VERTICAL COUNT**		

Bit 7 Interlace Timing Enable for double scan modes (i.e.: mode 13, etc.) (ITE)
0 = Disable
1 = Enable

Bit 6:5 Bit [7:6] of Horizontal Blank End. Bit 5 is located in bit 7 of CRTC register, 3?5h, index 5. Bit [4:0] is located in CRTC register, 3?5h, index 3. (HBE)

Bit 4:3 Bit [9:8] of Vertical Blank End. Bit [7:0] of Vertical Blank End is located in CRTC register, 3?5h, index 16. (VBE)

Bit 2:0 When CRT vertical count = {CRT33 [2:0],CRT34 [7:0]}, TV vertical display enable becomes inactive.

CRT34: TV Vertical Display Enable End - Low

Read/Write Address: 3?5h, Index: 34h
Power-on Default: 00h

This register specifies the vertical display enable end for TV timing.

7	6	5	4	3	2	1	0
CRT VERTICAL COUNT							

Bit 7:0 When CRT vertical count = {CRT33 [2:0],CRT34 [7:0]} TV vertical display enable becomes inactive.

CRT35: Vertical Screen Expansion DDA Control Constant - Low

Read/Write Address: 3?5h, Index: 35h
Power-on Default: 00h

This register specifies bit [7:0] the DDA control constant (DDACC) which is used for vertical screen expansion in VGA modes. Bit [9:8] of the DDACC is located in CRT36.

To enable vertical screen expansion in VGA graphics modes, one needs to program the DDA control constant (DDACC) equal to:

$$\text{DDACC} = \frac{1024 * \text{actual vertical size}}{\text{expanded vertical size}}$$

To enable vertical expansion in VGA text mode, one must program DDACC [2:0] = # of times the last character row should be repeated.

7	6	5	4	3	2	1	0
VERTICAL SCREEN EXPANSION							

Bit 7:0 This register defines the lower 8 bits of the vertical screen expansion DDA control constant. The upper 2 bits of the DDACC register is located in CRT36. For VGA text modes, only the lower [2:0] are valid.

CRT36: Vertical Screen Expansion DDA Control Constant - High

Read/Write Address: 3?5h, Index: 36h
Power-on Default: 00h

This register the vertical screen expansion DDA control constant lower 8 bits.

7	6	5	4	3	2	1	0
RESERVED					**VBE_10**	**VSE**	

Bit 7:3 Reserved

Bit 2 Blank End Control Bits_10. Bit [7:0] of Vertical Blank End is located in CRTC register, 3?5h, index 16. (VBE_10)
Bit [9:8] of VBE is located in CRTC register 3?5h, index 33, Bit [4:3]
Bit [7:0] of VBE is located at 3?5h, index 16 [7:0]

Bit 1:0 This register defines bit [9:8] of the vertical screen expansion DDA control constant. The lower 8-bit are located in CRT35. (VSE)

CRT37: Hardware/VGA Test Selection

Read/Write Address: 3?5h, Index: 37h
Power-on Default: 00h

7	6	5	4	3	2	1	0
HARDWARE TEST			**VGA HARDWARE TEST SELECTION**				

Bit 7:5 Reserved for hardware test bus selection

Bit 4:0 Reserved for VGA hardware testing

CRT38: TV Equalization Pulse Control - *For use with an external TV encoder only*

Read/Write Address: 3?5h, Index: 38h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CSS	**R**	**EQUALIZATION PULSE WIDTH**					

Bit 7 Composite Sync Select (CSS)
0 = CSYNC is generated by SYNCs (HSYNC NOR VSYNC)
1 = CSYNC is generated by equalizer state machine

Bit 6 Reserved (R)

Bit 5:0 Equalization pulse width in units of four VCLK

CRT39: TV Serration Pulse Control - *For use with an external TV encoder only*

Read/Write Address: 3?5h, Index: 39h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SERRATION PULSE WIDTH**					

Bit 7:6 Reserved

Bit 5:0 Serration pulse width in units of four VCLK

CRT3A: TV Total Timing Control for the Internal TV Encoder

Read/Write Address: 3?5h, Index: 3Ah
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**HSYNC**			**DOT CLOCKS**		

Bit 7:6 Reserved

Bit 5:3
00 = Normal
01 = HSYNC delayed by one pixel clock
02 = HSYNC delayed by two pixel clock
03 = HSYNC delayed by three pixel clock
04 = HSYNC delayed by four pixel clock
05 = HSYNC delayed by five pixel clock

Bit 2:0
07 = One character clock contains 7 dot clocks
06 = One character clock contains 6 dot clocks
05 = One character clock contains 5 dot clocks
04 = One character clock contains 4 dot clocks
03 = One character clock contains 3 dot clocks
02 = One character clock contains 2 dot clocks
01 = One character clock contains 1 dot clocks
00 = One character clock contains 0 dot clocks

For example, to program 910 pixel horizontal total for 4fc NTSC TV mode:
Program CRT horizontal total register to be 109 character clock
Program 3?4 index 3A bit [2:0] = 06
The actual total number of characters per horizontal line is 109 + 5 = 114
The horizontal total in pixel clock is: 113 x 8 + 6 = 910

CRT3B: Miscellaneous Lock Register I

Read/Write Address: 3?5h, Index: 3Bh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED FOR VGA HARDWARE TESTING							

Bit 7:0 Reserved for VGA Hardware testing

CRT3C: Miscellaneous Lock Register II

Read/Write Address: 3?5h, Index: 3Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**BSS**	**VGALC**	**RESERVED**			

Bit 7:6 Reserved VGA hardware debug test bus selection

Bit 5 Blanking signal selection (BSS)
0 = The blanking signal sent to RAMDAC is reversed active display. Outside of active display the blanking is active (black color). The border color register has no effect.
1 = The blank signal sent to RAMDAC is the normal blank signal from CRT. When both the blank and dispen are inactive the border color is displayed.

Bit 4 VGA line compare register (CRT09 [6] and CRT07 [4]) force (VGALC)
0 = normal (default)
1 = Enable. Force line compare [9:8] to be high. The original line compare control bits [9:8] have no effect. This register is used for Japanese DOS hardware scrolling compatibility purpose.

Bit 3:0 Reserved

CRT3D Scratch Register Bits

Read/Write Address: 3?5h, Index: 3Dh
Power-on Default:

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bit

CRT3E: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Eh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT3F: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT9E: Expansion/Centering Control Register 2

Read/Write Address: 3?4h, Index: 9Eh
Power-on Default: 00h

7	6	5	4	3	2	1	0
FE	**HSCRT**	**HSRW**	**VE**	**VC**	**VEE**	**VCE**	**HCE**

Bit 7 Font expansion control bit (FE)
This bit is effective if the following is true: CRT9E_[4] = 0 and the text mode plus the vertical expansion is on and CRT09_[4:0] < H0F
0 = The font vertical expansion will repeat the last character row
1 = The font vertical expansion will insert lines (with screen background color) between the last scan line of the current character row and the first scan of the next character row.

Bit 6 Horizontal shadow register selection for CRT timing control (HSCRT)
0 = There are two sets of horizontal shadow registers (primary and secondary). The selection switch is at the beginning of the vsync. If CR9F_[0] or CR9F [1] or FPR32_[0] is equal to 1 the second set is selected. If these registers are not equal to 1 then the primary set is selected.
1 = To force the selection of the second set of horizontal shadow register

Bit 5 Horizontal shadow register read/write selection (HSRW)

The following register update are effected
SVR40_[7:0] - Horizontal total shadow
SVR41_[7:0] - Horizontal blank start shadow
SVR42_[4:0] - Horizontal blank end shadow
SVR44_[7] - Horizontal blank end bit 5 shadow
CRT33_[6:5] - Horizontal blank end bit 7 & 6
SVR43_[7:0] - Horizontal sync start shadow
SVR44_[4:0] - Horizontal sync end
CRT9F_[0] - 10 dots expansion
CRT9F_[1] - 12 dots expansion

These registers have two sets - primary and secondary.
Bit 5=0: The primary registers are selected for W/R and control crt
Bit 5=1: The secondary registers are selected for W/R and control crt

Bit 4 Vertical expansion DDA value selection (VE)
0 = Vertical expansion will select the DDA value from the DDA look up table (3?4.35&36). This bit has no effect if bit 2 of this register = 0.
1 = Vertical expansion will select the DDA value from the DDA look up table (3?4.90-91B).

Bit 3 Vertical centering offset value selection (VC)
0 = Select vertical centering offset value from vertical center offset register (3?4, Index A6). This bit has no effect if bit 1 of this register = 0
1 = Select vertical centering offset value from a look-up table (look up by vdispend)

Bit 2 Vertical expansion enable selection (VEE)
0 = Vertical expansion disable
1 = Vertical expansion enable

Bit 1 Vertical centering enable selection (VCE)
0 = Vertical centering disable
1 = Vertical centering enable

Bit 0 Horizontal centering enable selection (HCE)
0 = Horizontal centering disable
1 = Horizontal centering enable

CRT9F: Expansion/Center Control Register 1

Read/Write Address: 3?4h, Index: 9Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**HT**	**16DOT**	**CC12**	**CC10**

Bit 7:4 Reserved

Bit 3 For hardware testing only (HT)
0 = VGA mode use non divide by 2 video clock. Extended VGA mode use divide by 2 video clock
1 = Reserved for 16 dot expansion. Should set to 0.

Bit 2 Reserved for 16 dot expansion. Should set to 0. (16DOT)

Bit 1 12 dot expansion (CC12)
0 = 12 dots expansion disabled
1 = Character clock expand to 12 dots regardless of bit 0 of this register

Bit 0 10 dot expansion (CC10)
0 = 10 dots expansion
1 = Character clock expand to 10 dots

CRT90-9B Vertical DDA Look Up Table & CRTA0-A5: Vertical Centering Offset Look Up Table

Read/Write Address: 3?4, Index A0h-A5h
Power-on Default: 00h

3?4.90								3?4.91								3?4.A0					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	5	4	3	2	1	0
FIELD 3								FIELD 2								FIELD 1					

Field 3: This field compared with Vdisp_end (3?4.12 bit_[7:2])

Field 2: This field is selected DDA value if field 3 compares

Field 1: This field is selected vertical centering offset value if field 3 compares. The actual offset value = 3?4.A0_[5:0] x 4

The vertical expansion/centering using look up table is enabled only if the following conditions are true: CR9E_[3:1] = 111; if the compare fails to match with any entry, the value from 3?4.A6 will be used for vertical centering and the 3?4.35&36 will be used for DDA.

The following register groups behave the same:

3?4.92; 3?4.93; 3?4.A1
3?4.94; 3?4.95; 3?4.A2
3?4.96; 3?4.97; 3?4.A3
3?4.98; 3?4.99; 3?4.A4
3?4.9A; 3?4.9B; 3?4.A5

CRTA0-A5: Vertical Centering Offset Look Up Table

Read/Write Address: 3?4, Index A0h-A5h
Power-on Default: 00h

3?4.90								3?4.91								3?4.A0					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	5	4	3	2	1	0
FIELD 3								FIELD 2								FIELD 1					

Field 3: This field compared with Vdisp_end (3?4.12 bit_[7:2])

Field 2: This field is selected DDA value if field 3 compares

Field 1: This field is selected vertical centering offset value if field 3 compares. The actual offset value = 3?4.A0_[5:0] x 4

The vertical expansion/centering using look up table is enabled only if the following conditions are true: CR9E_[3:1] = 111; if the compare fails to match with any entry, the value from 3?4.A6 will be used for vertical centering and the 3?4.35&36 will be used for DDA.

The following register groups behave the same:

3?4.92; 3?4.93; 3?4.A1
3?4.94; 3?4.95; 3?4.A2
3?4.96; 3?4.97; 3?4.A3
3?4.98; 3?4.99; 3?4.A4
3?4.9A; 3?4.9B; 3?4.A5

CRTA6: Vertical Centering Offset Register

Read/Write Address: 3?4, Index: A6h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**LINE SHIFT DOWN**					

Bit 7:6 Reserved

Bit 5:0 Specifies how many lines the screen image will shift down. This register will have no effect if 3?4.9E bit_[1]=1

CRTA7: Horizontal Centering Offset Register

Read/Write Address: 3?4h, Index: A7h
Power-on Default: 00h

7	6	5	4	3	2	1	0
R	**CHARACTER UNIT SHIFT RIGHT**						

Bit 7 Reserved (R)

Bit 6:0 Specifies how many character units the screen image will shift to the right. This register has no effect if 3?4.9E BIT_[0] = 0.

0 = Use to specify how many character units the screen image will shift to the right to center position. The horizontal screen centering look up table has no effect.

1 = To enable horizontal shift look up table (CRT9E_[0] has to be 1). One of the table entry will be select and the value in the entry specifies how many character units the screen image will shift to the right center position.

The selection of the look up is as follows:

IF CRT01_[7:1] = CRTA8_[6:0] control screen centering. Else if CRT01_[7:1] = CRTAA_[6:0], CRTAB_[6:0] control screen centering. Else if CRT01_[7:1] = CRTAC_[6:0], CRTAD_[6:0] control screen centering. Else CRA7_[6:0] will be used as default to control screen centering.

CRTA8-AD: Horizontal Screen Centering Look Up Table

Read/Write Address: 3?4, Index A8h-ADh
Power-on Default: 00h

7	6	5	4	3	2	1	0
R	**HORIZONTAL SCREEN CENTERING LOOK UP TABLE**						

Bit 7: Reserved

Bit 6:0 Horizontal Screen Centering Look Up Table

Shadow VGA Registers

The Shadow VGA Registers are designed to control CRT, LCD and TV timing, and maintain VGA compatibility. Lynx3DM+ shadows 12 VGA CRT registers. When these shadow registers are unlocked, the CPU I/O write operation can write into both standard CRT registers and shadow registers through standard VGA CRTC I/O location. When these shadow registers are locked, the CPU I/O write can only write into the standard CRT registers through CRTC I/O location. These 12 shadow registers also have specific I/O location which is not controlled by Shadow Lock/Unlock Register.

SVR40 - Horizontal Total	SVR45 - Vertical Total	SVR4A - Overflow (bit 7, 6,5, 3, 2, 1,and 0)
SVR41 - Start Horizontal Blanking	SVR46 - Start Vertical Blank	SVR4B - Maximum Scan Line (bit 5 only)
SVR42 - End Horizontal Blanking	SVR47 - End Vertical Blank	SVR4C - Horizontal Display End
SVR43 - Start Horizontal Retrace	SVR48 - Vertical Retrace Start	SVR4D - Vertical Display End
SVR44 - End Horizontal Retrace	SVR49 - Vertical Retrace End	

Automatic Lock/Unlock Scheme for Shadow Registers

There are two ways to access shadow registers. One is through standard VGA CRTC I/O location when CRT is the only selected display. These VGA CRT I/O write operations will write to both standard VGA CRT registers and shadow registers. The other way to access shadow registers is through their dedicated I/O locations. The shadow registers can only be read through their dedicated I/O locations.

When LCD or TV display is selected, the shadow registers will be automatically locked. The VGA CRT I/O write operation will write only to the standard VGA CRT registers. The shadow registers have to be accessed from their dedicated I/O location. This approach will reduce programming difficulty and maintain VGA compatibility.

SVR40: Shadow VGA Horizontal Total

Read/Write Address: 3?5h, Index: 40h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Total register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL TOTAL							

Bit 7:0 Defines the total character count minus 5 characters per horizontal scan line. This register only depends on the resolution of LCD, not the type of LCD.

SVR41: Shadow VGA Horizontal Blank Start

Read/Write Address: 3?5h, Index: 41h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Blank Start register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL BLANK							

Bit 7:0 When the horizontal character = SVR41 [7:0], shadow VGA horizontal blank become active.

SVR42: Shadow VGA Horizontal Blank End

Read/Write Address: 3?5h, Index: 42h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Blank End register.

7	6	5	4	3	2	1	0
R	**SDES**		**SHADOW VGA HORIZONTAL BLANK INACTIVE**				

Bit 7 Reserved (R)

Bit 6:5 Shadows display enable skew control (SDES)

Bit 4:0 When the horizontal character = {SVR44 [7],SVR42 [4:0]}, shadow VGA horizontal blank become inactive.

SVR43: Shadow VGA Horizontal Retrace Start

Read/Write Address: 3?5h, Index: 43h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Retrace Start register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL RETRACE INACTIVE							

Bit 7:0 When the horizontal character = SVR43 [7:0], shadow VGA horizontal retrace become active.

SVR44: Shadow VGA Horizontal Retrace End

Read/Write Address: 3?5h, Index: 44h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Retrace End register.

7	6	5	4	3	2	1	0
SVHB	**SHRD**		**SHADOW VGA HORIZONTAL RETRACE INACTIVE**				

Bit 7 When the horizontal character = {SVR44 [7],SVR41 [4:0]}, shadow VGA horizontal blank become inactive. (SVHB)

Bit 6:5 Shadows horizontal retrace delay (SHRD)

Bit 4:0 When the horizontal character = SVR44 [4:0], shadow VGA horizontal retrace become inactive.

SVR45: Shadow VGA Vertical Total

Read/Write Address: 3?5h, Index: 45h
Power-on Default: 00h

This register shadows VGA CRT Vertical Total register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL TOTAL							

Bit 7:0 Shadows the least significant 8 bits of 11 bits count of raster scan lines for display frame.

SVR46: Shadow VGA Vertical Blank Start

Read/Write Address: 3?5h, Index: 46h
Power-on Default: 00h

This register shadows VGA CRT Vertical Blank Start register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL BLANK START							

Bit 7:0 Shadows the least significant 8-bit of the 11-bit VGA CRT vertical blank start register.

SVR47: Shadow VGA Vertical Blank End

Read/Write Address: 3?5h, Index: 47h
Power-on Default: 00h

This register shadows VGA CRT Vertical Blank End register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL BLANK END							

Bit 7:0 Shadows the least significant 8-bit VGA CRT vertical blank end register.

SVR48: Shadow VGA Vertical Retrace Start

Read/Write Address: 3?5h, Index: 48h
Power-on Default: 00h

This register shadows VGA CRT Vertical Retrace Start register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL RETRACE START							

Bit 7:0 Shadows the least significant 8-bit of the 11-bit vertical retrace start register.

SVR49: Shadow VGA Vertical Retrace End

Read/Write Address: 3?5h, Index: 49h
Power-on Default: 00h

This register shadows VGA CRT Vertical Retrace End register.

7	6	5	4	3	2	1	0
RESERVED				**SHADOW VGA/CRT VERTICAL RETRACE**			

Bit 7:4 Reserved

Bit 3:0 Shadows bit [3:0] of VGA CRT vertical retrace end register.

SVR4A: Shadow VGA Vertical Overflow

Read/Write Address: 3?5h, Index: 4Ah
Power-on Default: 00h

This register shadows VGA CRT Vertical Overflow register.

7	6	5	4	3	2	1	0
SVRS9	**SVDE9**	**SVTB9**	**R**	**SVBS**	**SVRS8**	**SVDE8**	**SVTB8**

Bit 7 Shadows vertical retrace start bit 9 (SVRS9)

Bit 6 Shadow vertical display enable bit 9 (3?5h, index 7 [6]). When FPR33[5] = 1, can only access this bit through 3?5h, index 4Ah. (SVDE9)

Bit 5 Shadows vertical total bit 9 (SVTB9)

Bit 4 Reserved (R)

Bit 3 Shadows vertical blank start bit 8 (SVBS)

Bit 2 Shadows vertical retrace start bit 8 (SVRS8)

Bit 1 Shadow vertical display enable bit 8 (3?5h, index 7 [1]). When FPR33[5] = 1, can only access this bit through 3?5h, index 4Ah. (SVDE8)

Bit 0 Shadows vertical total bit 8 (SVTB8)

SVR4B: Shadow VGA Maximum Scan Line

Read/Write Address: 3?5h, Index: 4Bh
Power-on Default: 00h

This register shadows VGA CRT Maximum Scan Line register.

7	6	5	4	3	2	1	0
SSP		**SVBS**	**RESERVED**				

Bit 7:6 Shadow 3C2 bit_[7:6] for sync polarity (SSP)

Bit 5 Shadows vertical blank start bit 9 (SVBS)

Bit 4:0 Reserved

SVR4C: Shadow VGA Horizontal Display End

Read/Write Address: 3?5h, Index: 4Ch
Power-on Default: 00h

This register shadows VGA CRT Horizontal Display end.

7	6	5	4	3	2	1	0
SHADOW HORIZONTAL DISPLAY END							

Bit 7:0 Shadows Horizontal Display End register (3?5h, index 01). When FPR33[5] = 1, it locks access to this register only through 3?5h, index 4Ch.

SVR4D: Shadow VGA Vertical Display End

Read/Write Address: 3?5h, Index: 4Dh
Power-on Default: 00h

This register shadows VGA CRT Vertical Display end.

7	6	5	4	3	2	1	0
SHADOW VERTICAL DISPLAY END							

Bit 7:0 Shadows Vertical Display End register [7:0] (3?5h, index 12) When FPR33[5] = 1, it locks access to this register only through 3?5h, index 4Dh.

Chapter 22: 2D & Video Registers

Table 27: Memory Mapped Registers Quick Reference

Note: Some VPR registers can be accessed using memory mapped register space, or can be accessed using I/O mapped register space. Please see register descriptions for detailed information.

The drawing processor and video processor registers are all memory mapped. The following diagram illustrates the memory mapped register address assignment.

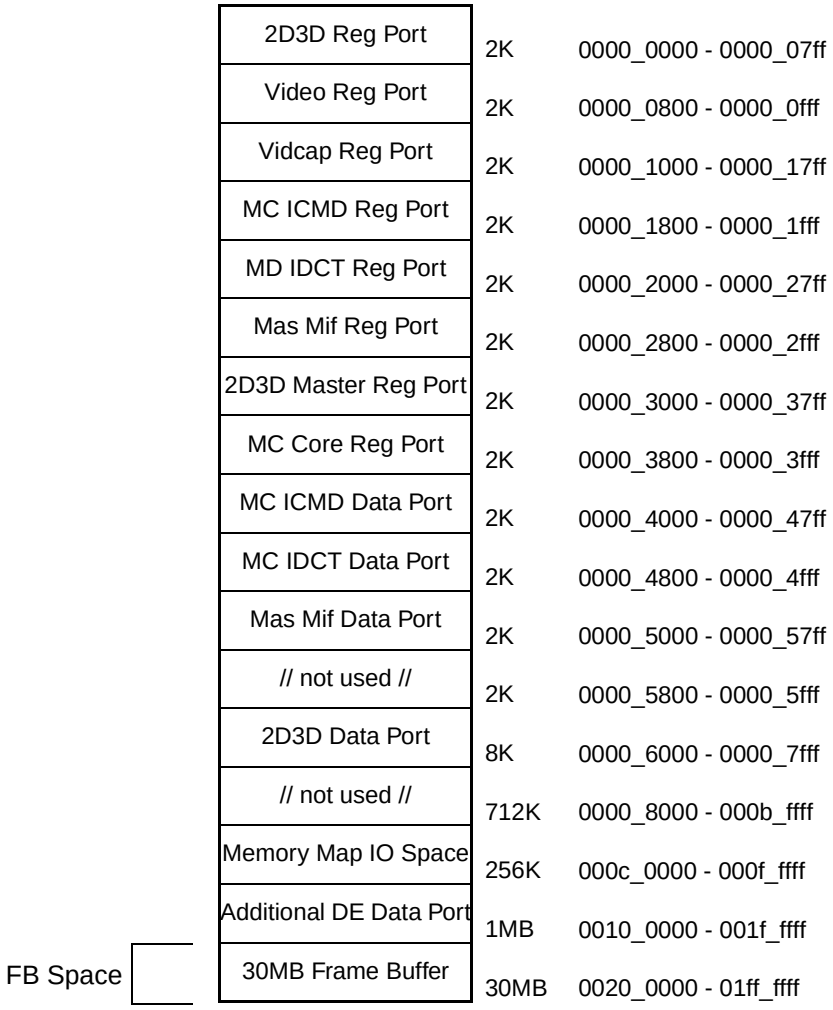


Figure 44: Memory Mapped Address Diagram

Drawing Engine Control Registers

The Drawing Engine supports various drawing functions, including Bresenham line draw, short stroke line draw, BITBLT, rectangle fill, HOSTBLT, Rotation Blit, and others. Hardware clipping is supported by 4 registers, DPR2C-DPR32, which defines a rectangular clipping area.

The drawing engine supports two types of format for its source and destination locations. One can specifies location format in X-Y coordinate, where the upper left corner of the screen is defined to be (0,0); this method is referred as X-Y addressing. Also, one can specify the location format based on its position in the display memory sequentially from the first pixel of the visible data; this method is referred as DE linear addressing. To select DE linear addressing, one must set DPR1E bit [3:0] = 1111.

All Drawing Engine control registers can be accessed via memory-mapped.

DPR00: Source Y or K2

Read/Write Address: DP_Base+00h
Power-on Default: Undefined

This register specifies the 12-bit Source Y position in x-y addressing mode, or low-order source address in DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify the 14-bit for K2 constant of Bresenham line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**SOURCE Y FOR X-Y ADDRESSING**													

Bit 15:14 Reserved

Bit 13:0 Source Y for X-Y addressing. In 24-bit packed modes, Source Y needs to be multiplied by 3.
OR
High-order source address SA[23:12] for DE linear addressing. Low-order 12-bit are in DPR02.

Bresenham Line (DPR0E bit [3:0] = 0111b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**AXIAL DIAGONAL CONSTANT (K2)**													

Bit 15:14 Reserved

Bit 13:0 Axial Diagonal Constant (K2) = 2 * (min(|dx|,|dy|) - max(|dx|,|dy|))

DPR02: Source X or K1

Read/Write Address: DP_Base+02h
Power-on Default: Undefined

This register specifies the 12-bit Source X position in x-y addressing mode, or low-order source address in linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify the 14-bit for K1 constant of Bresenham line when DPR0E bit [3:0] = 0111b to select Bresenham line command function. For HOSTBLT write command function (when DPR0E bit [3:0] = 1000b), this register is also used to specify the 3-bit HOST mono source for alignment.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE X FOR X-Y ADDRESSING**											

Bit 12:15 Reserved

Bit 11:0 Source X for X-Y addressing mode. In 24-bit packed modes, Source X needs to be multiplied by 3.
OR
Low-order source address SA [11:0] for DE linear addressing mode. Higher order 12-bit are in DPR00.

Note: For 24-bit color pattern, Xs = (PatXs * 3) LOGIC_OR (Yd[2:0] *3, shift 3 bits to left)
For 32-bit color pattern, Xs = (PatXs) LOGIC_OR (Yd[2:0], shift 3 bits to left)

Bresenham Line (DPR0E bit [3:0] = 0111b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**AXIAL STEP CONSTANT K1**													

Bit 15:14 Reserved

Bit 13:0 Axial Step Constant (K1) = 2 * min (|dx|, |dy|)

HOSTBLT Write (DPR0E bit [3:0] = 1000b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**HMSA**		

Bit 15:3 Reserved

Bit 2:0 Host mono source alignment for 8, 16, or 32-bit color modes. For 24-bit color mode, software needs to adjust for alignment. (HMSA)

DPR04: Destination Y or Start Y

Read/Write Address: DP_Base+04h
Power-on Default: Undefined

This register specifies the 12-bit Destination Y position in x-y addressing mode or higher-order destination address for DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify Vector Y start address for Bresenham Line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**DESTINATION Y OR START Y**													

Bit 15:14 Reserved

Bit 13:0 Destination Y for X-Y addressing. In 24-bit packed modes, Destination Y needs to be multiplied by 3.
OR
High-order 12 bits destination address DA[23:12] for DE linear addressing.

Bresenham Line (DPR0E bit [3:0] = 0111b
Vector Y start address

DPR06: Destination X or Start X

Read/Write Address: DP_Base+06h
Power-on Default: Undefined

This register specifies 12-bit Destination X position in x-y addressing mode or low-order 12-bit destination address in DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify Vector X start address for Bresenham Line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DESTINATION X OR START X**											

Bit 15:12 Reserved

		Bresenham Line (DPR0E bit [3:0] = 0111b
Bit 11:0	Destination X for X-Y addressing. In 24-bit packed modes, Destination X needs to be multiplied by 3. OR Low-order 12 bits destination address DA[11:0] for DE linear addressing.	Vector X start address

DPR08: Dimension Y or Error Term

Read/Write Address: DP_Base+08h
Power-on Default: Undefined

This register specifies the rectangle height or Dimension Y in pixels. When Bresenham line command function is selected (DPR0E bit [3:0] = 0111b), this register specifies the Vector Error Term. When Short Stroke Line command function is selected (DPR0E bit [3:0] = 0110b), this register specifies the short stroke line length for non-horizontal short stroke line

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DIMENSION Y OR ERROR TERM**											

		Short Stroke (DPR0E bit [3:0] = 0110b)	**Bresenham Line (DPR0E bit [3:0] = 0111b)**
Bit 15:14	Reserved	Reserved	Reserved
Bit 13:12	Reserved	Reserved	Vector Error Term
Bit 11:0	Dimension Y	Short Stroke Length if not a horizontal line (≠ 0° or ≠ 180°)	(ET)*

* Vector Error Term is determined based on the following logic:
ET = 2 * min (|dx|,|dy|) - max (|dx|,|dy|) if starting X > ending X.
ET = 2 * min (|dx|,|dy|) - max (|dx|,|dy|) -1 if starting X <= ending X.

DPR0A: Dimension X or Vector Length

Read/Write Address: DP_Base+0Ah
Power-on Default: Undefined

This register specifies the rectangle width or Dimension X in pixels. When Bresenham line command function is selected (DPR0E bit [3:0] = 0111b), this register specifies the Vector Length. When Short Stroke Line command function is selected (DPR0E bit [3:0] = 0110b), this register specifies the short stroke line length for horizontal short stroke line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DIMENSION X OR VECTOR LENGTH**											

Bit 15:12 Reserved

	.	**Bresenham Line (DPR0E bit [3:0] = 0111b)**	**Short Stroke (DPR0E bit [3:0] = 0110b)**
Bit 11:0	Dimension X. In 24-bit packed mode, Dimension X needs to be multiplied by 3. (note: Dimension Y does not need to be multiplied by 3)	Vector Length = Dmax + 1.Where Dmax is the dimension of Vector length which is on the major axis. Major axis is determined to be the axis which has longer length.	Short Stroke Length for horizontal short stroke line. (= 0° or = 180°)

DPR0C: ROP and Miscellaneous Control

Read/Write Address: DP_Base+0Ch
Power-on Default: Undefined

This register specifies the ROP2/ROP3 select, ROP2 source select, mono data format, pixel control, and 3 ROP operands.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROP	**ROPS**	**MDS**		**ERR**	**MPC**	**PCTS**	**TE**	**ROP3 RESERVED**				**ROP CODE**			

Bit 15 ROP2 or ROP3 select (ROP)
0 = select ROP3
1 = select ROP2

Bit 14 ROP2 source select. This bit is only valid when bit 15 of this register is set to "1". (ROPS)
0 = ROP2 source is not pattern
1 = ROP2 source is pattern

Bit 13:12 Mono Data Select. Mono data format is used to optimize font performance. Driver selects particular mono data format for particular font sizes. (MDS)
00 = No packed mono data
01 = Mono data packed at 8-bit
10 = Mono data packed at 16-bit
11 = Mono data packed at 32-bit

Bit 11 Enable Repeat Rotation BLT. This bit is only valid when DPR0E[3:0] = 1011b. (ERR)
0 = disable
1 = enable

Bit 10 Matching Pixel Control. This bit is only valid when transparency is enabled (bit 8 of this register = 1) (MPC)
0 = Matching pixel is opaque
1 = Matching pixel is transparent

Bit 9 Pixel Control Transparency Select (PCTS)
0 = Source controls transparency
1 = Destination controls transparency

Bit 8 Transparency Enable (TE)
0 = disable
1 = enable

Bit 7:4 ROP3 code[1] Reserved

Bit 3:0 ROP3 code[1] ROP2 code[2]

Notes:
[1] 3 Operands 256 operations ROP codes table reference listed below. For details on ROP codes, please refer to the Microsoft's device driver adaptation guide.

ROP3 Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pattern	1	1	1	1	0	0	0	0
Source	1	1	0	0	1	1	0	0
Destination	1	0	1	0	1	0	1	0

[2] 2 Operands 16 operations ROP codes table listed below:

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
Zero	0	0	0	0
~(D+ S)	0	0	0	1
D * ~S	0	0	1	0
~ S	0	0	1	1
S * ~D	0	1	0	0
~D	0	1	0	1
D ⊕ S	0	1	1	0
~(D * S)	0	1	1	1

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
D * S	1	0	0	0
~(D ⊕ S)	1	0	0	1
D	1	0	1	0
D + ~S	1	0	1	1
S	1	1	0	0
S + ~D	1	1	0	1
D + S	1	1	1	0
One	1	1	1	1

DPR0E: Drawing Engine Commands and Control

Read/Write Address: DP_Base+0Eh
Power-on Default: Undefined (except for Bit 15 and Bit 12 = 0)

This register specifies the drawing engine command and control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEA	**PS**	**DUE**	**DEQS**	**SSL**	**BMA**	**XYS**		**GSE**	**HBSC**	**PSB**	**DECE**	**COMMAND FUNCTIONS**			

Bit 15 Drawing Engine Activate (DEA)
0 = Idle (Power-on default = 0)
1 = Start Activate Drawing Engine

Bit 14 Pattern Select (PS)
0 = mono pattern
1 = color pattern

Bit 13 Destination X Update Enable (DUE)

0 = Do not update destination X on completion of a drawing engine function
1 = Update destination X on completion of a drawing engine function

Bit 12 Drawing Engine Quick Start Enable. If this bit is set, drawing engine will be activated right after dimension X is provided. One does not need to activate the drawing engine by setting bit 15 = 1 if quick start is already enabled. (DEQS)
0 = disable (Power-on default = 0)
1 = enable

Bit 11 Direction for Short Stroke Line and BITBLT For diagonal and vertical line, this bit needs to be set to "0". (SSL)

Bit 11	Short Stroke Line Direction	BITBLT Direction
0	not horizontal	Left to Right
1	horizontal	Right to Left

Bit 10 Bresenham Major Axis (Y) (BMA)
0= major axis is X
1= major axis is Y. For vertical line, this bit needs to be set.

Bit 9:8 X-Step and Y-Step (XYS)
01 = Counter Clock Wise Rotate 90 degree (CCW90)
10 = Clock Wise Rotate 90 degree (CW90)
00 = Right_Top and Left_Bottom as axis flip
11 = Left_Top and Right_Bottom as axis flip

Bit 7 Graphics Stretch Enable (only for Y direction) (GSE)

0 = disable
1 = enable

Bit 6 HOST BITBLT Source Color Select (HBSC)
0 = Source is color
1 = Source is monochrome

Bit 5 Last Pixel Select for Bresenham line (PSB)
0 = Vector not draw last pixel
1 = Vector draw last pixel

Bit 4 Drawing Engine Capture Enable (DECE)
0 = Normal Operation. No HOSTBLT capture operation.
1 = Enable HOSTBLT Read capture operation

Bit 3:0 Command Functions
0000 = BITBLT
0001 = Rectangle Fill
0010 = Reserved
0011 = Trapezoid Pattern Fill
0100 = Reserved
0101 = Run Length Encoding (RLE) Strip Draw
0110 = Short Stroke
0111 = Bresenham Line Draw
1000 = Host BLT Write
1001 = Host BLT Read
1010 = Host BLT Write from Left_Bottom
1011 = Rotation BLT
1111 = 3D Operation
1100 = AGP HbitW (master mode)* - with texture master engine
1101 = Reserved
1110 = Reserved

DPR10: Source Row Pitch

Read/Write Address: DP_Base+10h
Power-on Default: Undefined

This register specifies the source row offset in pixel unit for 8/16/32-bit color modes. In 24-bit color mode, source row offset needs to be multiplied by 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE ROW OFFSET**											

Bit 15:12 Reserved

Bit 11:0 Source Row Offset. In 24-bit color mode, source row offset needs to be multiplied by 3.

DPR12: Destination Row Pitch

Read/Write Address: DP_Base+12h
Power-on Default: Undefined

This register specifies the destination row offset in pixel unit for 8/16/32-bit color modes. In 24-bit color mode, destination row offset needs to be multiplied by 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DESTINATION ROW OFFSET**											

Bit 15:12 Reserved

Bit 11:0 Destination Row Offset. In 24-bit color mode, destination row offset needs to be multiplied by 3.

DPR14: Foreground Colors

Read/Write Address: DP_Base+14h
Power-on Default: Undefined

The register specifies the foreground graphics color for 8-bit color (DPR1E bit [5:4] = 00b), 16-bit color (DPR1E bit [5:4] = 01b), and 24-bit color (DPR1E bit [5:4] = 11b) modes.

8-bit color mode

31	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**FOREGROUND COLOR**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR HIGH BYTE								**FOREGROUND COLOR LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**FOREGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR GREEN								**FOREGROUND COLOR BLUE**							

Bit 31:24 Reserved

	8-bit color mode	16-bit color mode	24-bit color mode
Bit 23:16	Reserved	Reserved	Foreground Color Red
Bit 15:8	Reserved	Foreground Color High Byte	Foreground Color Green
Bit 7:0	Foreground Color 8-bit index	Foreground Color Low Byte	Foreground Color Blue

DPR18: Background Colors

Read/Write Address: DP_Base+18h
Power-on Default: Undefined

The register specifies the background graphics color for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.

Note: in monochrome transparency mode (font operation), the background color needs to be programmed to equal to the invert of foreground color in DPR14.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BACKGROUND COLOR**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR HIGH BYTE								**BACKGROUND COLOR GREEN**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**BACKGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR GREEN								**BACKGROUND COLOR BLUE**							

Bit 31:24 Reserved

	8-bit color mode	16-bit color mode	24-bit color mode
Bit 23:16	Reserved	Reserved	Background Color Red
Bit 15:8	Reserved	Background Color High Byte	Background Color Green
Bit 7:0	Background Color	Background Color Low Byte	Background Color Blue

8-bit index

DPR1C: Stretch Source Height Y

Read/Write Address: DP_Base+1Ch
Power-on Default: Undefined

This register specifies the height of source block for stretch BITBLT.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE Y DIMENSION FOR STRETCH BLT**											

Bit 15:12 Reserved

Bit 11:0 Source Y dimension for stretch BLT. (only for Y direction)

DPR1E: Drawing Engine Data Format and Location Format Select

Read/Write Address: DP_Base+1Eh
Power-on Default: Undefined

The register specifies drawing engine source & destination locations select and data format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**XY**	**PATTERN START Y**			**PATTERN START X**				**R**	**DEDF**		**DRAWING ENG LOCATION**			

Bit 15 Reserved (R)

Bit 14 Pattern XY Overwrite Select (XY)
0 = Normal. Drawing Engine uses Bit [13:8] as pattern address only when it is in linear addressing mode (Bit [3:0] = 1111b]
1 = Overwrite. Drawing Engine uses Bit [13:8] as pattern address no matter what addressing mode it is in.

Bit 13:11 Pattern Start Y Address (Yd [2:0]). This address is only valid if Bit 14 = 1 or Bit [3:0] = 11xxb (linear addressing).

Bit 10:7 Pattern Start X Address (Xd [2:0]). This address is only valid if Bit 14 = 1 or Bit [3:0] = 11xxb (linear addressing). It is based on the top left corner of screen as (0,0) coordinate address. Rotation is needed for pattern source if Xd is non-zero. All 4 bits (bit 10:7) are used at 24bpp. Only 3 bits (bit 9:7) are used at 8, 16, and 32 bpp.

Bit 6 Reserved

Bit 5:4 Drawing Engine Data Format (DEDF)
00 = 8-bit per pixel
01 = 16-bit per pixel

10 = 32-bit per pixel
11 = 24-bit per pixel (24-bit packed)

Bit 3:0 Drawing Engine Locations (Source and Destination) Format Select. The drawing engine supports two types of format for its source and destination locations. One can specifies location format in X-Y coordinate, where the upper left corner of the screen is defined to be (0,0); this method is referred as X-Y addressing. Also, one can specifies the location format based on its position in the display memory sequentially from the first pixel of the visible data; this method is referred as DE linear addressing. This register selects the pixel width for X-Y addressing and DE linear addressing.
1111 = DE linear addressing
else = XY screen width depends on DPR3C register

DPR20: Color Compare

Read/Write Address: DP_Base+20h
Power-on Default: Undefined

The register specifies the color compare for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.
Note, in monochrome transparency mode for font operations, the color compare needs to be programmed to equal to the foreground color in DPR14.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**COLOR COMPARE 8-BIT INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE HIGH BYTE								**COLOR COMPARE LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**COLOR COMPARE RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE GREEN								**COLOR COMPARE BLUE**							

	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 31:24	Reserved	Reserved	Reserved
Bit 23:16	Reserved	Reserved	Color Compare Red
Bit 15:8	Reserved	Color Compare High Byte	Color Compare Green

Bit 7:0	Color Compare 8-bit index	Color Compare Low Byte	Color Compare Blue

DPR24: Color Compare Masks

Read/Write Address: DP_Base+24h
Power-on Default: Undefined

The register specifies the color compare mask for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**COLOR COMPARE 8-BIT INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE MASK HIGH BYTE								**COLOR COMPARE MASK LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**COLOR COMPARE MASK RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE MASK GREEN								**COLOR COMPARE MASK BLUE**							

	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 31:24	Reserved	Reserved	Reserved
Bit 23:16	Reserved	Reserved	Color Compare Mask Red
	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 15:8	Reserved	Color Compare Mask High Byte	Color Compare Mask Green
Bit 7:0	Color Compare Mask 8-bit index	Color Compare Mask Low Byte	Color Compare Mask Blue

DPR28: Bit Mask

Read/Write Address: DP_Base+28h
Power-on Default: Undefined

The register specifies the Bit Mask for 8-bit color (DPR1E bit [5:4] = 00) and 16-bit color (DPR1E bit [5:4] = 01) modes.

8-bit color mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BIT MASK 8-BIT INDEX**							

16-bit color mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT MASK HIGH BYTE								**BIT MASK LOW BYTE**							

	8-bit color mode	**16-bit color mode**
Bit 15:8	Reserved	Bit Mask High Byte
Bit 7:0	Bit Mask 8-bit index	Bit Mask Low Byte

DPR2A: Byte Mask Enable

Read/Write Address: DP_Base+2Ah
Power-on Default: Undefined

The register specifies the byte mask enable register for 64-bit datapath.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BYTE MASK FOR 64-BIT DATAPATH**							

Bit 15:8 Reserved

Bit 7:0 Byte Mask for 64-bit datapath. Each bit enables the corresponding byte data.
0 = disable write
1 = enable write

DPR2C: Scissors Left and Control

Read/Write Address: DP_Base+2Ch
Power-on Default: Undefined

The register specifies the Scissors left boundary and control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**SE**	**SBS**	**SCISSORS BOUNDARY LEFT**											

Bit 15:14 Reserved

Bit 13 Scissors Enable (SE)
0 = disable

1 = enable

Bit 12 Scissors Boundary Select (SBS)
0 = Write disable outside the Scissors boundary
1 = Write disable inside the Scissors boundary

Bit 11:0 Scissors Boundary Left. In 24-bit color mode, the scissors boundary left position needs to be multiplied by 3.

DPR2E: Scissors Top

Read/Write Address: DP_Base+2Eh
Power-on Default: Undefined

The register specifies the scissors top boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SCISSORS BOUNDARY TOP**											

Bit 15:12 Reserved

Bit 11:0 Scissors Boundary Top. In 24-bit color mode, the scissors boundary top position needs to be multiplied by 3.

DPR30: Scissors Right

Read/Write Address: DP_Base+30h
Power-on Default: Undefined

The register specifies the right boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SCISSORS BOUNDARY RIGHT**											

Bit 15:12 Reserved

Bit 11:0 Scissors Boundary Right. In 24-bit color mode, the scissors boundary right position needs to be multiplied by 3.

DPR32: Scissors Bottom

Read/Write Address: DP_Base+32h
Power-on Default: Undefined

The register specifies the bottom boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SCISSORS BOUNDARY BOTTOM											

Bit 15:12 Reserved

Bit 11:0 Scissors Boundary Bottom. In 24-bit color mode, the scissors boundary bottom position = scissors boundary top position DPR2E [11:0] + height of the clipping window.

DPR34: Mono Pattern Low

Read/Write Address: DP_Base+34h
Power-on Default: Undefined

The register specifies the monochrome pattern lower double word. It is 32-bit access only. The higher 32-bit are in DPR38.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MONO PATTERN TOP 4 LINES															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONO PATTERN TOP 4 LINES															

Bit 31:0 Mono pattern top 4 lines. Line 3 data is located in the most significant byte where as line 0 data is located in the least significant bye.

DPR38: Mono Pattern High

Read/Write Address: DP_Base+38h
Power-on Default: Undefined

The register specifies the monochrome pattern higher double word. It is 32-bit access only. The lower 32-bit are in DPR34.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MONO PATTERN LAST 4 LINES															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONO PATTERN LAST 4 LINES															

Bit 31:0 Mono pattern last 4 lines. Line 7 data is located in the most significant byte where as line 4 data is located in the least significant bye.

DPR3C: XY Addressing Destination & Source Window Widths

Read/Write Address: DP_Base+3Ch
Power-on Default: Undefined

The register specifies the XY width for source and destination window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				DESTINATION WINDOW WIDTH IN PIXEL											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SOURCE WINDOW WIDTH IN PIXEL											

Bit 31:28 Reserved

Bit 27:16 Destination Window width in pixel for XY addressing mode (max. = 4096 pixel)

Bit 15:12 Reserved

Bit 11:0 Source Window width in pixel for XY addressing mode (max. = 4096 pixel)

DPR40: Source Base Address

Read/Write Address: DP_Base+40h
Power-on Default: Undefined

The register specifies the Source base address in 64-bit unit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												SOURCE BASE ADDRESS			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE BASE ADDRESS															

Bit 31:20 Reserved

Bit 19:0 Source Base address

DPR44: Destination Base Address

Read/Write Address: DP_Base+44h
Power-on Default: Undefined

The register specifies the destination base address in 64-bit unit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												DESTINATION BASE ADDRESS			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BASE ADDRESS															

Bit 31:20 Reserved

Bit 19:0 Destination Base address

Video Processor Control Registers

Lynx3DM+ integrates a concurrent video processor. It can support 2 independent video windows using hardware scaling for any size of video windows at any location of the screen display. The Video Processor Control Registers specify the control registers for Video Processor. The Video Processor Control Registers can only be accessed through memory-mapped.

VPR00: Miscellaneous Graphics and Video Control

Read/Write Address: VP_Base+00h/3?5, Index c0, c1, c2, c3
Power-on Default: 00h

This register specifies the controls for graphics and video window I/II. (where x = don't care)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**CKEII**	**ESD**	**FR**	**VVWI**	**FVIE**	**FRIM**	**VIE**	**CKEI**	**TVWS**	**GDF**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**EVWII**	**EVW HII HR**	**VWII AE**	**VWIIE**	**VWFII**			**R**	**EVWI**	**EVWIH**	**VWIAE**	**VWIE**	**VWIF**		

Bit 31:28 Reserved

Bit 27 Color Key Enable for Video Window II (CKEII)
0 = Disable
1 = Enable

Bit 26 Enable separate data (graphics or video) to DAC/TV. This bit is used to implement "Dual View" in index color mode. This bit needs to also be set when enabling flicker reduction for TV display in VGA index-color mode. (ESD)
0 = Disable
1 = Enable

Bit 25 Enable V0FIFO to fetch 8-bit index color data to LCD BKEND in non-VGA mode. Normally, the 8-bit index color data is fetched by graphics FIFO in non-VGA mode. This bit is designed to enable flicker reduction on TV display in non-VGA, 8-bit index color mode. (FR)
0 = Disable
1 = Enable

Bit 24 Select video window I source start address same as video capture buffer start address. This bit is used to automatically display captured data on video window I without programming video window I source start address register (SVWI).
0 = Normal. Video window I source start address is from VPR1C register.
1 = Video window I source start address is equal to capture port buffer I source start address (VPR48) or capture port buffer II source start address (VPR4C). If single buffer is selected for video capture, video window I source start address is equal to capture port buffer I source address. If double buffer is selected for video capture and capture port buffer I is busy, video window I source start address is equal to capture port buffer II source address.

Bit 23 Fixed Vertical Interpolation Enable. Scale factor is fixed to 80. (FVIE)
0 = Disable
1 = Enable

Bit 22 Flicker Reduction in Interlace Modes for TV display. V1FIFO will be used together with the graphics FIFO for flicker reduction. Therefore, only one video Window is allowed for this feature to be enabled. (FRIM)
0 = Disable
1 = Enable

Bit 21 Vertical Interpolation Enable. This bit can only be set when single window is enabled. (VIE)
0 = Disable (line duplication)
1 = Enable

Bit 20 Color Key Enable for Video Window I (CKEI)
0 = Disable
1 = Enable

Bit 19 Top Video Window Select (TVWS)
0 = video window I is on top
1 = video window II is on top

Bit 18:16 Graphics Data Format (GDF)
000 = 8-bit index
001 = 15 -bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
11x = Reserved

Bit 15 Reserved (R)

Bit 14 Enable Video Window II data doubling. This bit is in 8-bit index color mode when the VCLK is larger than 85 MHz. The V1FIFO will shift out data every 2 VCLK. (EVWII)
0 = Disable
1 = Enable

Bit 13 Enable Video Window II Horizontal Replication (EVWII HR)
0 = Disable (horizontal interpolation)
1 = Enable (pixel duplication)

Bit 12 Video Window II YUV Averaging Enable. 2 YUV pixels will be averaged and the result will become single pixel. (VWII AE)
0 = Disable
1 = Enable

Bit 11 Video Window II Enable (VWIIE)
0 = Disable

1 = Enable

Bit 10:8 Video Window II Format (VWFII)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
11x = YUV 4:2:2

Bit 7 Reserved (R)

Bit 6 Enable Video Window I data doubling. This bit is used in 8-bit index color mode when the VCLK is larger than 85 MHz. The V0FIFO will shift out data every 2 VCLK. (EVWI)
0 = Disable
1 = Enable

Bit 5 Enable Video Window I Horizontal Replication (EVWIH)
0 = Disable (horizontal interpolation)
1 = Enable (pixel duplication)

Bit 4 Video Window I YUV Averaging Enable. 2 YUV pixels will be averaged and the result will become single pixel. (VWIAE)
0 = Disable
1 = Enable

Bit 3 Video Window I Enable (VWIE)
0 = Disable
1 = Enable

Bit 2:0 Video Window I Format (VWIF)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
11x = YUV 4:2:2

VPR04: Color Keys

Read/Write Address: VP_Base+04h/3?5, Index c4, c5, c6, c7
Power-on Default: Undefined

This register specifies color keys for the two video windows

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VIDEO WINDOW II COLOR KEY INDEX**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**VIDEO WINDOW I COLOR KEY INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY [15:8]								**VIDEO WINDOW II COLOR KEY [7:0]**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY [15:8]								**VIDEO WINDOW I COLOR KEY [7:0]**							

	8-bit color mode	**16-bit color mode**[1]
Bit 31:24	Reserved	Video Window II Color Key [15:8]
Bit 23:16	Video Window II Color Key Index	Video Window II Color Key [7:0]
Bit 15:8	Reserved	Video Window I Color Key [15:8]
Bit 7:0	Video Window I Color Key Index	Video Window I Color Key [7:0]

Note[1]: for 24-bit or 32-bit color mode, software will need to repack the color key data into RGB - 5:6:5 (16-bit) format.

VPR08: Color Key Masks

Read/Write Address: VP_Base+08h/3?5h, Index c8, c9, ca, cb
Power-on Default: Undefined

This register specifies color key masks for the two video window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY MASK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY MASK															

Bit 31:16 Video Window II Color Key Mask
0 = Disable color mask
1 = Enable color mask

Bit 15:0 Video Window I Color Key Mask
0 = Disable color mask
1 = Enable color mask

VPR0C: Data Source Start Address for Extended Graphics Modes

Read/Write Address: VP_Base+0Ch/3?5h, Index cc, cd, ce, cf
Power-on Default: Undefined

This register specifies data source start address for extended graphics modes

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GDSB	**RESERVED**									**GDSSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GDSSA															

Bit 31 Graphic Data Status Bit (GDSB)

Bit 30:22 Reserved

Bit 21:0 Graphics Data Source Starting Address, in 64-bit segment (GDSSA)

VPR10: Data Source Width and Offset for Extended Graphics Modes

Read/Write Address: VP_Base+10h/3?5h, Index d0, d1, d2, d3
Power-on Default: Undefined

This register specifies data source data line width and offset address for extended graphics modes.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**GRAPHICS DATA SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**GRAPHICS DATA START ADDRESS OFFSET**									

Bit 31:26 Reserved

Bit 25:16 Graphics Data Source data line width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Graphics Data Start Address Offset, in 64-bit segment

VPR14: Video Window I Left and Top Boundaries

Read/Write Address: VP_Base+14h/3?5h, Index d4, d5, d6, d7
Power-on Default: Undefined

This register specifies left and top boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, top boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, left boundary

VPR18: Video Window I Right and Bottom Boundaries

Read/Write Address: VP_Base+18h/3?5h, Index d8, d9, da, db
Power-on Default: Undefined

This register specifies right and bottom boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, bottom boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, right boundary

VPR1C: Video Window I Source Start Address

Read/Write Address: VP_Base+1Ch/3?5h, Index dc, dd, de, df
Power-on Default: Undefined

This register specifies video start address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIS	**RESERVED**									**VWISS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWISS															

Bit 31 Video Window I Status Bit (VWIS)

Bit 30:22 Reserved

Bit 21:0 Video Window I source start address for, in 64-bit segment. (VWISS)

VPR20: Video Window I Source Width and Offset

Read/Write Address: VP_Base+20h/3?5h, Index e0, e1, e2, e3
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW I SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW I SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window I Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window I Source Address Offset, in 64-bit segment

VPR24: Video Window I Stretch Factor:

Read/Write Address: VP_Base+24h/3?5h, Index e4, e5, e6, e7
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window I. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1. The two high bytes of this register can be used to enable the “Bob” function.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I HORIZONTAL STRETCH								**VIDEO WINDOW I VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window 1 Horizontal Stretch Factor (W1HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window 1 Vertical Stretch Factor (W1VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1VSF = \left(1 - \frac{Source}{Destination}\right) * 256$$

VPR28: Video Window II Left and Top Boundaries

Read/Write Address: VP_Base+28h
Power-on Default: Undefined

This register specifies left and top boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Top Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Left Boundary

VPR2C: Video Window II Right and Bottom Boundaries

Read/Write Address: VP_Base+2Ch
Power-on Default: Undefined

This register specifies right and bottom boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Right Boundary

VPR30: Video Window II Source Start Address

Read/Write Address: VP_Base+30h
Power-on Default: Undefined

This register specifies video start address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIIS	**RESERVED**									**VWIIDS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIIDS															

Bit 31 Video Window II Status Bits (VWIIS)

Bit 30:22 Reserved

Bit 21:0 Video Window II Data Source Starting Address (VWIIDS)

VPR34: Video Window II Source Width and Offset

Read/Write Address: VP_Base+34h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW II SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW II SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window II Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window II Source Address Offset, in 64-bit segment

VPR38: Video Window II Stretch Factor

Read/Write Address: VP_Base+38h/3?5h, Index f8, f9, fa, fb

Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window II. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II HORIZONTAL STRETCH								**VIDEO WINDOW II VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window II Horizontal Stretch Factor (W2HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window II Vertical Stretch Factor (W2VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2VSF = \left(1 - \frac{Source}{Destination}\right) * 256$$

VPR3C: Graphics and Video Control II

Read/Write: Address: VP_Base+3Ch/3?5h, Index fc, fd, fe
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									**ESP 2-1**	**ESP 4-3**	**ESPV**	**R**	**SPVW**	**ESP 2-Bit**	**ESP**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**EGHS 2-1**	**EGHS 4-3**	**EGVS**	**EGVSF**	**EGHR**	**EGVI**	**EGFR**	**EVWII 420i**	**EVWII 2-1**	**EVWII 4-3**	**EVWII VS**	**EVWI 420i**	**EVWI 2-1**	**EVWI 4-3**	**EVWI VS**

Bit 31:23 Reserved

Bit 22 Enable Sub-Picture 2-to-1 Horizontal Shrink (ESP 2-1)

Bit 21 Enable Sub-Picture 4-to-3 Horizontal Shrink (ESP 4-3)

Bit 20 Enable Sub-Picture Vertical Shrink (ESPV)

Bit 19 Reserved (R)

Bit 18 Sub-Picture on Video Window II (SPVW)

Bit 17 Enable 2-bit/pixel Sub-Picture (Otherwise 8-bit/pixel) (ESP 2-Bit)

Bit 16 Enable Sub-Picture (ESP)

Bit 15 Reserved (R)

Bit 14 Enable Graphic 2-to-1 Horizontal Shrink (EGHS 2-1)

Bit 13 Enable Graphic 4-to-3 Horizontal Shrink (EGHS 4-3)

Bit 12 Enable Graphic Vertical Shrink (EGVS)

Bit 11 Enable Graphic Vertical Scale Factor to 80H (EGVSF)

Bit 10 Enable Graphic Horizontal Replication (EGHR)

Bit 9 Enable Graphic Vertical Interpolation (EGVI)

Bit 8 Enable Graphic 3-Line Flicker Reduction (EGFR)

Bit 7 Enable Video Window II 420i UV Swap (EVWII 420i)

Bit 6 Enable Video Window II 2-to-1 Horizontal Shrink (EVWII 2-1)

Bit 5 Enable Video Window II 4-to-3 Horizontal Shrink (EVWII 4-3)

Bit 4 Enable Video Window II Vertical Shrink (EVWIIVS)

Bit 3 Enable Video Window I 420i UV Swap (EVWI 420i)

Bit 2 Enable Video Window I 2-to-1 Horizontal Shrink (EVWI 2-1)

Bit 1 Enable Video Window I 4-to-3 Horizontal Shrink (EVWI 4-3)

Bit 0 Enable Video Window I Vertical Shrink (EVWIVS)

VPR40: Graphic Scale Factor

Read/Write Address: VP_Base+40h/3?5h, Index e8, e9, ea, eb
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GRAPHIC INITIAL ODD FIELD VERTICAL								**GRAPHIC INITIAL EVEN FIELD VERTICAL**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRAPHIC HORIZONTAL SCALE FACTOR								**GRAPHIC VERTICAL SCALE FACTOR**							

Bit 31:24 Graphic Initial Odd Field Vertical Scale Factor

Bit 23:16 Graphic Initial Even Field Vertical Scale Factor

Bit 15:8 Graphic Horizontal Scale Factor (GHSF)

$$GHSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Graphic Vertical Scale Factor (GVSF)

$$GVSF = \left(1 - \frac{Source}{Destination}\right) * 256$$

VPR44: Graphic Data Source Starting Address for Odd Field

Read/Write Address: VP_Base+44h/3?5h, Index ec, ed, ee
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**GRAPHIC DATA SOURCE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRAPHIC DATA SOURCE															

Bit 31:20 Reserved

Bit 19:0 Graphic Data Source Starting Address for Odd Field

VPR48: Video Window I Chroma Data Source Starting Address

Read/Write Address: VP_Base+48h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**VIDEO WINDOW I**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I															

Bit 31:20 Reserved

Bit 19:0 Video Window I Chroma Data Source Starting Address

VPR4C: Video Window II Chroma Data Source Starting Address

Read/Write Address: VP_Base+4Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**VIDEO WINDOW II**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II															

Bit 31:20 Reserved

Bit 19:0 Video Window II Chroma Data Source Starting Address

VPR50: Sub-Picture Data Source Starting Address

Read/Write Address: VP_Base=50h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SUB-PICTURE DATA SOURCE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB-PICTURE DATA SOURCE															

Bit 31:20 Reserved

Bit 19:0 Sub-picture Data Source Starting Address

VPR54: FIFO Priority Control

Read/Write Address: VP_Base+54h/3?5h, Index f0, f1, f2, f3
Power-on Default: 07216543h

This register specifies FIFO priority controls for graphics, Flat Panel Read Frame Buffer FIFO1, Video Window I, Video Window II, Flat Panel Write Frame Buffer, Capture Window and Flat Panel Read Frame Buffer FIFO2. Graphics FIFO has the highest priority and Flat Panel Read FIFO2 has the lowest priority as default.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERRP	**EDE1**	**EDE2**	**EHIF**	**EHIF MIF**	**FPR FIFO2**			**R**	**CWFIFO**			**R**	**FPW FIFO**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**VWII FIFO**			**R**	**VWI FIFO**			**R**	**FPR FIFO1**			**R**	**GFIFO**		

Bit 31 Enable Round Robin Priority Arbitration (ERRP)

Bit 30 Enable DE1 Burst of 4 Data (EDE1)

Bit 29 Enable DE2 Burst of 4 Data (EDE2)

Bit 28 Enable HIF Master burst of 4 Data (EHIF)

Bit 27 Enable HIF MIF Burst of 4 Data (EHIF MIF)

Bit 26:24 Flat Panel Read FIFO2 priority select (FPR FIFO2
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last) (default)

Bit 23 Reserved (R)

Bit 22:20 Capture Window FIFO priority select (CWFIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd) (default)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 19 Reserved (R)

Bit 18:16 Flat Panel Write FIFO priority select (FPW FIFO)
000 = request is off
001 = highest priority (1st) (default)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 15 Reserved (R)

Bit14:12 Video Window II FIFO priority select (VWII FIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th) (default)
111 = lowest priority (last)

Bit 11 Reserved (R)

Bit 10:8 Video Window I FIFO priority select (VWI FIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th) (default)
110 = next priority (6th)
111 = lowest priority (last)

Bit 7 Reserved (R)

Bit 6:4 Flat Panel Read FIFO1 priority select (FPR FIFO1)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th) (default)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 3 Reserved

Bit 2:0 Graphics FIFO priority select (GFIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd) (default)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

VPR58: FIFO Empty Request level Control

Read/Write Address: VP_Base+58h/3?5h, Index f4, f5
Power-on Default: 00000444h

This register specifies FIFO empty request level for graphics FIFO, Video Window I, and Video Window II. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty. For LCD Read FIFO1/FIFO2 and LCD Write FIFO request level controls, they are located in FPR4A register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VWII FIFO**			**R**	**VWI FIFO**			**R**	**GFIFO**		

Bit 31:11 Reserved

Bit 10:8 Video Window II FIFO Empty request level Select (VWII FIFO)
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 7 Reserved (R)

Bit 6:4 Video Window I FIFO Empty request level Select (VWI FIFO)
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 3 Reserved (R)

Bit 2:0 Graphics FIFO Empty request level Select (GFIFO)
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

VPR5C: YUV to RGB Conversion Constant

Read/Write Address: VP_Base+5Ch
Power-on Default: EDEDEDh
This register specifies the YUV to RGB conversion constant.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUMA Y ADJUSTMENT								**RED CONVERSION CONSTANT**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN CONVERSION CONSTANT								**BLUE CONVERSION CONSTANT**							

Bit 31:24 Luma Y Adjustment

Bit 23:16 Red Conversion Constant

Bit 15:8 Green Conversion Constant

Bit 7:0 Blue Conversion Constant

VPR60: Current Scan Line Position

Read Only Address: VP_Base+60h
Power-on Default: Undefined

This register specifies the current scan line position.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**CURRENT SCAN LINE**										

Bit 31:11 Reserved

Bit 10:0 Current Scan Line. This register returns the number for current scan line.

VPR64: Signature Analyzer Control and Status

Read/Write Address: VP_Base+64h
Power-on Default: Undefined

This register specifies controls and status for signature analyzer as well as the analyzer signature.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ANALYZER SIGNATURE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												**SAE**	**SAR**	**SASS**	

Bit 31:16 Analyzer Signature. These bits are Ready Only.

Bit 15:4 Reserved

Bit 3 Signature Analyzer Enable/Stop. Software needs to set this bit = 1 as a "ENABLE" control bit in order to enable signature analyzer. Once the analysis is completed, the hardware will reset this bit = 0 as a "STOP" status bit. (SAE)
0 = Stop (analysis is completed)
1 = Enable (analysis is in progress)

Bit 2 Signature Analyzer Reset/Normal. Software needs to set this bit = 1 as a (SAR)

"RESET" control bit to reset signature shift register to "0" before turning on signature analyzer. In the next vertical sync pulse after bit 3 and bit 2 have been set to "11", bit 2 will be automatically reset to "0" as a "NORMAL" status bit.
0 = Normal (disable reset to signature analyzer)
1 = Reset (enable reset to signature analyzer)

Bit 1:0 Signature Analyzer Source Select. These bits selects the input source for the signature analyzer. (SASS)
00 = Source is Red output from Multimedia RAMDAC
01 = Source is Green output from Multimedia RAMDAC
1x = Source is Blue output from Multimedia RAMDAC

VPR70: Sub Picture Color Look Up Register 0

Read/Write Address: VP_Base+70h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 0															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 0

VPR74: Sub Picture Color Look Up Register 1

Read/Write Address: VP_Base+74h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 1**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 1															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 1

VPR78: Sub Picture Color Look Up Register 2

Read/Write Address: VP_Base+78h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 2															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 2

VPR7C: Sub Picture Color Look Up Register 3

Read/Write Address: VP_Base+7Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 3**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 3															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 3

VPR80: Sub Picture Color Look Up Register 4

Read/Write Address: VP_Base+80h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 4**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 4															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 4

VPR84: Sub Picture Color Look Up Register 5

Read/Write Address: VP_Base+84h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 5**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 5															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 5

VPR88: Sub Picture Color Look Up Register 6

Read/Write Address: VP_Base+88h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 6**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 6															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 6

VPR8C: Sub Picture Color Look Up Register 7

Read/Write Address: VP_Base+8Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 7**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 7															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 7

VPR90: Sub Picture Color Look Up Register 8

Read/Write Address: VP_Base+90h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 8**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 8															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 8

VPR94: Sub Picture Color Look Up Register 9

Read/Write Address: VP_Base+94h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 9**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 9															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 9

VPR98: Sub Picture Color Look Up Register A

Read/Write Address: VP_Base+98h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP A**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP A															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register A

VPR9C: Sub Picture Color Look Up Register B

Read/Write Address: VP_Base+9Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP B**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP B															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register B

VPRA0: Sub Picture Color Look Up Register C

Read/Write Address: VP_Base+A0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP C**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP C															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register C

VPRA4: Sub Picture Color Look Up Register D

Read/Write Address: VP_Base+A4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP D**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP D															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register D

VPRA8: Sub Picture Color Look Up Register E

Read/Write Address: VP_Base+A8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP E**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP E															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register E

VPRAC: Sub Picture Color Look Up Register F

Read/Write Address: VP_Base+ACh
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP F**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP F															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register F

VPRB0: Sub Picture Top/Left Boundary

Read/Write Address: VP_Base+B0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**SUB PICTURE TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**SUB PICTURE LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Sub Picture Top Boundary

Bit 15:11 Reserved

Bit 10:0 Sub Picture Left Boundary

VPRB4: Sub Picture Bottom/Right Boundary

Read/Write Address: VP_Base+B4h

Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					SUB PICTURE BOTTOM BOUNDARY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SUB PICTURE RIGHT BOUNDARY										

Bit 31:27 Reserved

Bit 26:16 Sub Picture Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Sub Picture Right Boundary

VPRB8: Sub Picture Source Data Address Offset and Line Width

Read/Write Address: VP_Base+B8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						SUB PICTURE SOURCE DATA LINE									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SUB PICTURE SOURCE DATA ADDRESS OFFSET									

Bit 31:26 Reserved

Bit 25:16 Sub Picture Source Data Line Width

Bit 15:10 Reserved

Bit 9:0 Sub Picture Source Data Address Offset

VPRC0: Video Window I U/V Scale Factor

Read/Write Address: VP_Base+C0h
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							EVWI	VIDEO WINDOW I UV INITIAL ODD							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I UV INITAL EVEN								VIDEO WINDOW I UV VERTICAL							

Bit 31:25 Reserved

Bit 24 Enable Video Window I UV Vertical Shrink (EVWI)

Bit 23:16 Video Window I UV Initial Odd Field Vertical Scale Factor

Bit 15:8 Video Window I UV Initial Even Field Vertical Scale Factor

Bit 7:0 Video Window I UV Vertical Scale Factor

VPRC4: Video Window II Scale Factor

Read/Write Address: VP_Base+C4h
Power-On Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							**EVWII**	**VIDEO WINDOW II UV INITIAL ODD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II UV INITIAL EVEN								**VIDEO WINDOW II UV VERTICAL**							

Bit 31:25 Reserved

Bit 24 Enable Video Window II UV Vertical Shrink (EVWII)

Bit 23:16 Video Window II UV Initial Odd Field Vertical Scale Factor

Bit 15:8 Video Window II UV Initial Even Field Vertical Scale Factor

Bit 7:0 Video Window II UV Vertical Scale Factor

Capture Processor Control Registers

The Capture Processor Control Registers specify the control registers for Capture Processor The Capture Processor Control Registers can only be accessed through memory-mapped.

CPR00: Capture Port Control

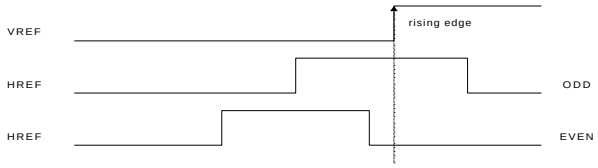
Read/Write Address: CP_Base+00h
Power-on Default: 00h
This register specifies the capture port which can be used for video capture and video playback.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**EMO**	**FDMS**	**VREF**	**HREF**	**EHF**		**EVR**		**EHR**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDI		**FSE**			**IDCE**	**DBE**	**CC**	**FIS**	**IS**	**CBS**	**CFO**	**VIS**	**BUF2**	**BUF1**	**VCE**

Bit 31:26 Reserved

Bit 25 External Memory Only Select (Read Only). This register bit definition is opposite from the MD[23] definition in the Table 3: Power on Configuration. (EMO)
0 = Normal. Allow both internal and external memory access depends on MD[2]/MCR62[2] setting.
1 = External Memory Access Only

Bit 24 Field Detect Method Select (FDMS)
0 = Falling edge of VSYNC
1 = Rising edge of VSYNCt



Bit 23 VREF Polarity (VREF)
0 = "High" active
1 = "Low" active

Bit 22 HREF Polarity (HREF)
0 = "High" active
1 = "Low" active

Bit 21:20 Enable Horizontal Filtering (EHF)
00 = no filtering
01 = 2-tap filtering
10 = 3-tap filtering
11 = 4-tap filtering

Bit 19:18 Enable Vertical Reduction (EVR)
00 = no reduction
01 = 2 to 1 reduction
10 = 4 to 1 reduction
11 = reserved

Bit 17:16 Enable Horizontal Reduction (EHR)
00 = no reduction
01 = 2 to 1 reduction
10 = 4 to 1 reduction
11 = reserved

Bit 15:14 Video Capture Input Data Format (VDI)
00 = YUV 4:2:2
01 = YUV 4:2:2 (with byte swapping)
10 = RGB 5:5:5
11 = RGB 5:6:5

Bit 13:11 Frame Skip Enable (FSE)
000 = no skip
001 = skip every other frame
010 = skip even frame
011 = skip odd frame
100 = capture 2 and skip 1 frame
101 = capture 3 and skip 1 frame
110 = capture 1 and skip 2 frame

111 = capture 1 and skip 3 frame

Bit 10 Interlace Data Capture Enable (IDCE)
0 = Disable (non-interlace)
1 = Enable (interlace data. even field will be captured into buffer1 and odd field will be captured into buffer2) When this bit is set to 1, double buffer mode needs to be also enabled (bit 9 =1).

Bit 9 Double Buffer Enable (DBE)
0 = Disable. Use buffer1 addressed by VPR48.
1 = Enable. Use buffer1 and buffer2 addressed by VPR48 and VPR4C.

Bit 8 Capture Control (CC)
0 = Continuous Capture
1 = Conditional Capture. Capture is controlled by bit 1 or bit 2 of this register.

Bit 7 Field Input Status (Read Only) (FIS)
0 = even field
1 = odd field

Bit 6 Interlace Status (Read Only) (IS)
0 = non-interlace
1 = interlace

Bit 5 Current Buffer Status (Read Only) (CBS)
0 = Buffer 1 is the current buffer used
1 = Buffer 2 is the current buffer used

Bit 4 Current Frame Capture Status (Read Only) (CFO)
0 = Skip the current frame
1 = Capture the current frame

Bit 3 VSYNC Input Status (Read Only) (VIS)
0 = VSYNC pulse is inactive
1 = VSYNC pulse is active

Bit 2 Buffer 2 Status/Control Bit. This bit is used for software to read back the status of the current frame. Software needs to preset this bit to 1 when programming the Buffer 2 starting address in VPR4C. This bit can be set by drawing engine, and it can also be reset by video capture unit. If continuous capture is selected (bit 8 =0), this bit will be ignored. (BUF2)
0 = Idle or Capture has completed
1 = Capture in progress

Bit 1 Buffer 1 Status/Control Bit. This bit is used for software to read back the status of the current frame. Software needs to preset this bit to 1 when programming the Buffer 1 starting address in VPR48. This bit can be set by drawing engine, and it can also be reset by video capture unit. If continuous capture is selected (bit 8 =0), this bit will be ignored. (BUF1)
0 = Idle or Capture has completed
1 = Capture in progress

Bit 0 Video Capture Enable. When Video Capture is enabled, all video port I/O pins except for "BLANK" pin will become input pins only. This bit can also be accessed through I/O register space 3?5, index FF, bit [0]. (VCE)
0 = Disable
1 = Enable

CPR04: Video Source Clipping Control

Read/Write Address: CP_Base+04h
Power-on Default: Undefined

This register specifies top and left clipping of video source.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO SOURCE TOP CLIPPING**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO SOURCE LEFT CLIPPING**									

Bit 31:26 Reserved

Bit 25:16 Video Source Top Clipping, # of line to drop

Bit 15:10 Reserved

Bit 9:0 Video Source Left Clipping, # of pixel to drop

CPR08: Video Source Capture Size Control

Read/Write Address: CP_Base+08h
Power-on Default: Undefined

This register specifies video source capture size.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO SOURCE HEIGHT**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO SOURCE WIDTH**										

Bit 31:27 Reserved

Bit 26:16 Video Source Height

Bit 15:11 Reserved

Bit 10:0 Video Source Width

CPR0C: Capture Port Buffer I Source Start Address

Read/Write Address: CP_Base+0Ch
Power-on Default: Undefined

This register specifies video source start address for Buffer I of Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											**CAPTURE PORT I**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE PORT I															

Bit 31:21 Reserved

Bit 20:0 Capture Port Buffer I source start address, in 64-bit segment

CPR10: Capture Port Buffer II Source Start Address

Read/Write Address: CP_Base+10h
Power-on Default: Undefined

This register specifies video source start address for Buffer II of Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											**CAPTURE PORT II**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE PORT II															

Bit 31:21 Reserved

Bit 20:0 Capture Port Buffer II source start address, in 64-bit segment.

CPR14: Capture Port Source Offset Address

Read/Write Address: CP_Base+14h
Power-on Default: Undefined

This register specifies video source offset address for Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**CAPTURE PORT SOURCE**										

Bit 31:11 Reserved

Bit 10:0 Capture Port Source Address Offset, in 64-bit segment

CPR18: Capture FIFO Empty Request level Control

Read/Write Address: CP_Base+18h
Power-on Default: 00000006h

This register specifies Capture FIFO empty request level. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**CAPTURE WINDOW**		

Bit 31:3 Reserved

Bit 2:0 Capture Window FIFO Empty request level Select
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty
101 = 8 or more empty
110 = 10 or more empty (default)
111 = 12 or more empty

Chapter 23: Motion Comp Video Registers

Table 28: Motion Comp Video Registers Quick Reference

Motion Comp Bus Master CMD Control Registers

MCR00: Motion Comp Enable

Read/Write Address: MCR_Base + Offset
Power-On Default:

7	6	5	4	3	2	1	0
RESERVED							**MCE**

Bit 7:1 Reserved

Bit 0 Motion Comp Enable (MCE)

MCR04: Slot 0 Y Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT0 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT0 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot0, Y Data Source Starting Address

MCR08: Slot1 Y Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT1 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT1 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot1, Y Data Source Starting Address

MCR0C: Slot2 Y Data Source

Read/Write Address: MCR_Base + Offset

Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT2 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT2 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot2, Y Data Source Starting Address

MCR10: Slot3 Y Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT3 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT3 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot3, Y Data Source Starting Address

MCR14: Slot0 UV Interleave Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT0 UV INTERLEAVE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT0 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot0, UV Interleave Data Source Starting Address

MCR18: Slot1 UV Interleave Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												SLOT1 UV INTERLEAVE			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT1 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot1, UV Interleave Data Source Starting Address

MCR1C: Slot2 UV Interleave

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												SLOT2 UV INTERLEAVE			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT2 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot2, UV Interleave Data Source Starting Address

MCR20: Slot3 UV Interleave Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												SLOT3 UV INTERLEAVE			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT3 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot3, UV Interleave Data Source Starting Address

MCR24: Y Data Source Line Offset

Read/Write Address: MCR_Base + Offset
Power-On Default:

7	6	5	4	3	2	1	0
OFFSET							

Bit 8:0 Y Data Source Line Offset (row pitch)

MCR28: UV Interleave Data Source Line Offset

Read/Write Address: MCR_Base + Offset
Power-On Default:

7	6	5	4	3	2	1	0
UV INTERLEAVE DATA SOURCE LINE OFFSET							

Bit 8:0 UV Interleave Data Source Line Offset (row pitch)

Chapter 24: PCI Bus Master Control Registers

Table 29: PCI Bus Master Control Registers Quick Reference

Motion Compensation ICMD Control Registers

Table of Entry Register

Read/Write Address: ICMD_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don't Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: ICMD_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: ICMD_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: ICMD_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: ICMD_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS)

Motion Compensation IDCT Control Registers

Table of Entry Register

Read/Write Address: IDCT_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don't Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: IDCT_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: IDCT_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: IDCT_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: IDCT_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS)

Table of Entry Register

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don't Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS) Motion Compensation ICMD Control Registers

Starting Address

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 14:
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**STARTING ADDRESS**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTING ADDRESS															

Bit 31:20 Reserved

Bit 19:0 Starting Address for Master Transfer

Width and Offset

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 18:
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**WIDTH FOR MASTER TRANSFER**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**OFFSET FOR MASTER TRANSFER**									

Bit 31:26 Reserved

Bit 25:16 Width for Master Transfer

Bit 15:10 Reserved

Bit 9:0 Offset for Master Transfer

Plane Selection

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 1C:
Power-on Default: 00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**EY**	**EU**	**EV**

Bit 31:3 Reserved

Bit 2 Enable Y-Plane Transfer

Bit 1 Enable U-Plane Transfer

Bit 0 Enable V Plane Transfer

Texture 3D Bus Master Control Registers

Table of Entry Register

Read/Write Address: Text3D_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don't Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: Text3D_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: Text3D_Reg_Base + Offset

Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: Text3D_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: Text3D_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS)

Chapter 25: 3D Registers

Table 30: Summary of Registers

Address	Description	Format
All Registers are 32-bit		
3D Control Registers		
DPR80	Reserved	
DPR84	Reserved	
DPR88	Reserved	
DPR8C	Reserved	
DPR90	Reserved	
DPR94 [15:0]	Z Initial Value	
DPR98	Reserved	
DPR9C [15:8]	Alfa_test	
DPR9C [7:0]	Morph A	
DPRA0 [23:0]	Dest_Comp_Color	R, G, B
DPRA4 [23:0]	Dest_CC Mask	
DPRA8 [23:0]	SRC_CC Mask	
DPRAC	Reserved	
DPRB0	Reserved	
DPRB4	Reserved	
DPRB8	Reserved	
DPRBC [23:0]	Text2 Blend Mode*	
DPRC0 [31]	Texture2 AGP Memory	
DPRC0 [30:28]	Reserved	
DPRC0 [27:0]	Texture2 Base Addr	*
DPRC4 [21:0]	3D Display Addr	Quad Word Address
DPRC8 [23:0]	Text1 Blend Mode	
DPRCC [31]	Texture1 AGP Memory	

Table 30: Summary of Registers (Continued)

Address	Description	Format
All Registers are 32-bit		
DPRCC [30]	Flush Cache	
DPRCC [29:28]	Reserved	
DPRCC [27:0]	Texture1 Base Addr	
DPRD0 [31:22]	Reserved	
DPRD0 [21:0]	Z_Base Address	
DPRD4 [21:0]	FB_Base	
DPRD8 [27:16]	3D fb_stride	
DPRD8 [11:0]	Z_stride *	
DPRDC [31:0]	3D_Cmd_Set_0	
DPRE0 [31:0]	3D_Cmd_Set_1	
DPRE4 [31:0]	3D_Cmd_Set_2	
DPRE8 [23:0]	Src_comp_color	R, G, B
DPREC [23:0]	Fog_color	R, G, B
DPRF0	Reserved	
DPRF4 [23:0]	Reserved	
DPRF8 [31:0]	Reserved	
DPRFC [31:0]	3D Test CMD	
D3D Vertex Registers		
DPR100 [31:0]	X0	iEEE S1E8M23
DPR104 [31:0]	Y0	iEEE S1E8M23
DPR108 [31:0]	Z0	iEEE S1E8M23
DPR10C [31:0]	Wi0	iEEE S1E8M23
DPR110 [31:0]	Cd_0	ARGB8888
DPR114 [31:0]	Cs_1	ARGB8888
DPR118 [31:0]	Swi0	iEEE S1E8M23
DPR11C [31:0]	Twi0	iEEE S1E8M23
DPR120 [10:0]	Go_0	

Table 30: Summary of Registers (Continued)

Address	Description	Format
All Registers are 32-bit		
DPR124 [31:0]	X1	iEEE S1E8M23
DPR128 [31:0]	Y1	iEEE S1E8M23
DPR12C [31:0]	Z1	iEEE S1E8M23
DPR130 [31:0]	Wi1	iEEE S1E8M23
DPR134 [31:0]	Cd_1	ARGB8888
DPR138 [10:0]	Cs_1	ARGB8888
DPR13C [31:0]	Swi1	iEEE S1E8M23
DPR140 [31:0]	Twi1	iEEE S1E8M23
DPR144 [10:0]	Go_1	
DPR148 [31:0]	X2	iEEE S1E8M23
DPR14C [31:0]	Y2	iEEE S1E8M23
DPR150 [31:0]	Z2	iEEE S1E8M23
DPR154 [31:0]	Wi2	iEEE S1E8M23
DPR158 [31:0]	Cd_2	ARGB8888
DPR15C [31:0]	Cs_2	ARGB8888
DPR160 [31:0]	Swi1	iEEE S1E8M23
DPR164 [31:0]	Twi2	iEEE S1E8M23
DPR168 [10:0]	Go_2	
DPR184	Reserved	
DPR188	Reserved	
DPR18C	Reserved	
Open GL Vertex Registers		
DPR100 [31:0]	X0	iEEE S1E8M23
DPR104 [31:0]	Y0	iEEE S1E8M23
DPR108 [31:0]	Z0	iEEE S1E8M23
DPR10C [31:0]	Wi0	iEEE S1E8M23
DPR110 [31:0]	R0	iEEE S1E8M23
DPR114 [31:0]	G0	iEEE S1E8M23
DPR118 [31:0]	B0	iEEE S1E8M23
DPR11C [31:0]	A0	iEEE S1E8M23
DPR120 [31:0]	Swi0	iEEE S1E8M23
DPR124 [31:0]	Twi0	iEEE S1E8M23
DPR128 [31:0]	Rs0	
DPR12C [31:0]	Gs0	iEEE S1E8M23
DPR130 [31:0]	Bs0	iEEE S1E8M23

Table 30: Summary of Registers (Continued)

Address	Description	Format
All Registers are 32-bit		
DPR134 [31:0]	As0	iEEE S1E8M23
DPR138 [10:0]	Go_0	iEEE S1E8M23
DPR140 [31:0]	X1	iEEE S1E8M23
DPR144 [31:0]	Y1	iEEE S1E8M23
DPR148 [31:0]	Z1	iEEE S1E8M23
DPR14C [31:0]	Wi1	iEEE S1E8M23
DPR150 [31:0]	R1	iEEE S1E8M23
DPR154 [12:0]	G1	
DPR158 [31:0]	B1	iEEE S1E8M23
DPR15C [31:0]	A1	iEEE S1E8M23
DPR160 [31:0]	Swi1	iEEE S1E8M23
DPR164 [10:0]	Twi1	iEEE S1E8M23
DPR168 [31:0]	Rs1	iEEE S1E8M23
DPR16C [31:0]	Gs1	iEEE S1E8M23
DPR170 [31:0]	Bs1	iEEE S1E8M23
DPR174 [31:0]	As1	iEEE S1E8M23
DPR178 [31:0]	G0_1	iEEE S1E8M23
DPR17C [31:0]	Twi2	iEEE S1E8M23
DPR180 [31:0]	X2	
DPR184 [31:0]	Y2	
DPR188 [31:0]	Z2	
DPR18C [31:0]	Wi2	
DPR190 [31:0]	R2	
DPR194 [31:0]	G2	
DPR198 [31:0]	B2	
DPR19C [31:0]	A2	
DPR1A0 [31:0]	Swi2	
DPR1A4 [31:0]	Twi2	
DPR1A8 [31:0]	Rs1	
DPR1AC [31:0]	Gs1	
DPR1B0 [31:0]	Bs1	
DPR1B4 [31:0]	As1	
DPR1B8 [31:0]	Go_2	
Rendering Registers		
DPR200 [23:0]	Xstart	S11.12

Table 30: Summary of Registers (Continued)

Address	Description	Format
All Registers are 32-bit		
DPR204 [23:0]	Xend1	S11.12
DPR208 [23:0]	Xend2	S11.12
DPR20C [10:0]	Ystart	11.0
DPR210 [11:0]	cnt1	
DPR214 [11:0]	cnt2	
DPR218 [23:0]	dXdY0	S11.12
DPR21C [23:0]	dXdY1	S11.12
DPR220 [23:0]	dXdy2	S11.12
DPR224 [9:0]	Xincr1	10.0
DPR228 [15:0]	rstart	S8.7
DPR22C [15:0]	gstart	S8.7
DPR230 [15:0]	bstart	S8.7
DPR234 [15:0]	drdx	S8.7
DPR238 [15:0]	dgdx	S8.7
DPR23C [15:0]	dbdx	S8.7
DPR240 [15:0]	drd1	S8.7
DPR244 [15:0]	dgd1	S8.7
DPR248 [15:0]	dbd1	S8.7
DPR24C [31:0]	zstart	S15.16
DPR250 [15:0]	astart	S8.7
DPR254 [15:0]	fstart	S8.7
DPR258 [31:0]	dzdx	S15.16
DPR25C [15:0]	dadx	S8.7
DPR260 [15:0]	sdfdx	S8.7
DPR264 [31:0]	dzd1	S15.16
DPR268 [15:0]	dad1	S8.7
DPR26C [15:0]	sdfd1	S8.7
DPR270 [31:0]	sstart	S19.12
DPR274 [31:0]	tstart	S19.12
DPR278 [26:0]	wstart	S6.20
DPR27C [31:0]	dsdx	S19.12
DPR280 [31:0]	dtdx	S19.12
DPR284 [26:0]	dwdx	S6.20
DPR288 [31:0]	dsd1	S19.12
DPR28C [31:0]	dtd1	S19.12

Table 30: Summary of Registers (Continued)

Address	Description	Format
All Registers are 32-bit		
DPR290 [26:0]	dwd1	S6.20
DPR294 [31:0]	dsdy	S19.12
DPR298 [31:0]	dtdy	S19.12
DPR29C [26:0]	dwdy	S6.20
DPR2A0 [15:0]	srstart	S8.7 Specular
DPR2A4 [15:0]	sgstart	S8.7 Specular
DPR2A8 [15:0]	sbstart	S8.7 Specular
DPR2AC [15:0]	sdrdx	S8.7 Specular
DPR2B0 [15:0]	sdgdx	S8.7 Specular
DPR2B4 [15:0]	sdbdx	S8.7 Specular
DPR2B8 [15:0]	sdrd1	S8.7 Specular
DPR2BC [15:0]	sdgd1	S8.7 Specular
DPR2C0 [15:0]	sdbd1	S8.7 Specular
DPR2C4	Reserved	
DPR2C8	Reserved	
DPR2CC	Reserved	
DPR2D0	Reserved	
DPR2D4	Reserved	
DPR2D8	Reserved	
DPR2DC	Reserved	
DPR2E0	Reserved	
DPR2E4	Reserved	
DPR2E8	Reserved	
DPR2EC	Reserved	
DPR2F0	Reserved	
DPR2F4	Reserved	
DPR2F8	Reserved	
DPR2FC [31]	GO_L2R (when writing to this register EW is activated, 0: R2L, 1:L2R	
Global Fog Factor - Look-up Table (512 x 8)		
DPR300 [31:0]	Fog3210	
.....		
DPR4FC [31:0]	Last 4 Fog	

Note: A. The Global fog space lookup table RAM will be shared for:
1. Global fog as 512x8 LUT
2. 256x16 texture palette

B. There are 2 sources that can write to the LUT
1. CPU through Write Buffer to LUT

C. The RAM's write port could be 32-bit (from host) and read is 64-bit. There is flip-flop at input and output. At the 64-bit output, the palette will use index bit [2:1] to select the right 16-bit data, and for the fog the index bit [0] to select the right byte as fog factor.

D. 3D command set bit [31:30] will select 8 bits out from Z's 16-bit
00:Z [15:8] as index for fog LUT-default
01:Z [11:4] as index for fog LUT-default
10:Z [7:0] as index for fog LUT-default

Table 31: 3D Registers Quick Reference

3D_Command_Set_0

Read Write Address: 0DCh
Power-on Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MFE	**Z BUFFER**			**ZUE**	**ZE**	**ME**	**TE**	**MLF**	**RESERVED**					**TEXTURE 1**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE 0		**TFM**			**TCF**			**TEXTURE SIZE**							

Bit 31 Magnification Filer Enable* (MFE)
0 = magnification filter same as texture filter mode
1 = magnification filter use CMD0 [23]

Bit 30:28 Z Buffer Compare Mode
000 = Z never pass
001 = pass if Zi > Zzb
010 = pass if Zi = Zzb
011 = pass if Zi >= Zzb
100 = pass if Zi < Zzb
101 = pass if Zi!= Zzb
110 = pass if Zi <= Zzb
111 = Z always passes

Bit 27 Z Update Enable (ZUE)
0 = do not update Z buffer
1 = update z-buffer with new pixel z value if z compare pass
Z is 16Bit per pixel same as MS D3D. This Bit valid only when Z is enable

Bit 26 Z Enable (ZE)
0 = Z buffer disable - no hardware Z fetch and compare
1 = Z buffer enable

Bit 25 Mipmap Enable (ME)
0: single map texture
1: mipmap texture

Bit 24 Texture Enable (TE)
0 = Texture mapping off
1 = Texture mapping on

Bit 23 Magnification Linear Filter* (MLF)
0 = Nearest for magnification map
1 = Linear (Bilinear) for magnification map
This bit is valid only when the magnification filter is enabled (CMD0 [31] =1)

Bit 22:18 Reserved

Bit 17:16 Texture 2 Address Mode*
00 = NONE use texture border color for outside range
01 = D3DTADDR_WRAP: wrapping around both U and V coordinate
10 = D3DTADDR_CLAMP: Max (u,v) = 1.0. Min (u,v) = 0.0
11 = DEDTADDR_MIRROR: 1.1 becomes .9, 1.7 becomes .3
2.2 becomes .2 and 2.8 becomes .8

Bit 15:14 Texture 1 Address Modes
00 = NONE use texture border color for outside range
01 = D3DTADDR_WRAP: wrapping around both U and V coordinate
10 = D3DTADDR_CLAMP: Max (u,v) = 1.0. Min (u,v) = 0.0
11 = DEDTADDR_MIRROR: 1.1 becomes .9, 1.7 becomes .3
2.2 becomes .2 and 2.8 becomes .8

Bit 13:11 Texture Filtering Modes (TFM)
000 = D3DFILTER_NEAREST:PS point sampling of texture = floor(u,v)
001 = D3DFILTER_LINEAR: BL bilinear filtering
010 = D3DFILTER_MIPNEAREST: NMN 1 mipmap + pointsample
011 = D3DFILTER_LINEAR_MIPNEAREST: NML bilinear on selected mipmap
100 = D3DFILTER_MIPLINEAR: LMN linear on 2 mipmap's nearest
101 = D3DFILTER_LINEARMIPLINEAR: LML trilinear
(110) = Reserved
111 = Reserved

Bit 10:8 Texture Color Format (TCF)
000 = ARGB8888
001 = ARGB4444
010 = ARGB1555
011 = YUYV16/RGB565
100 = CI8
101 = Compress Texture DXT1
110 = Compress Texture DXT2
111 = Compress Texture DXT3

Bit 7:0 Texture1 Size. 2**m X 2**n is the largest mipmap texture rectangular
7:4 = m. where 2**m is the dimension x of rectangular texture
3:0 = n. where 2**n is the dimension y of rectangular

3D_Command_Set_1

Read Write Address: 0E0h
Power-on Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OGL	**PSR**	**DSE**	**RESERVED**		**SO**	**DE**	**DMAC**		**FP PIXEL**		**RESERVED**		**GLOBAL FOG**		**FC**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC	**CKP**	**TFM**	**DESTINATION BLENDING**				**SOURCE BLEND**				**ABE**	**R**	**3D DRAW**		

Bit 31 Open GL/D3D Vertex selection (OGL)
This Bit to determine the vertex address either in D3D space or OpenGL space as shown in the vertex registers table
0 = D3D vertex address mode
1 = OpenGL vertex address mode

Bit 30 Point Sample Round Up for texture mapping (PSR)
0: Floor on S, T- current MicroSoft D3D
1: Floor on S +.5, T +.5;

Bit 29 Disable Setup Engine (DSE)
0 = Enable setup (default)
1 = Reset setup engine: for SU by pass and vertex or render registers read

Bit 28:27 Reserved

Bit 26 Specular On (SO)
0 = Specular off
1 = Specular on

Bit 25 Dither Enable. This Bit to add dithering to internal 24-bit to 16-bit color conversion. (DE)
0: Dither off
1: Dither on

Bit 24:23 DMA Control (DMAC)

00: 2D 3D command & DMA (default)	- with mask header
01: Vertex DMA	- group# and mask
10: MBit DMA	- no mask for hbltw
11: Address, data pair DMA	- no mask

Notes:
1. When select Vertex DMA, internal vertex register will generate the vertex address and host address will be ignored. This Vertex DMA supports both master and slave mode for register write though hbltw port space
2. Vertex Register read also need to set the Vertex DMA bits, and CPU need to supply the Vertex address which means Slave mode only.
3. Before starting an vertex_DMA, this DMA control bit has to set to 00 because internal address counter rely on those two Bit to reset.
4. After finish the DMA transfer, this 2-bit register has to reset back to 00 or 2D engine would not work because 2D registers would not be decoded.
5. Refer to DMA Mask on Page 25 - 1 for details.

Bit 22:21 FB Pixel Format
00: 565 RGB
01: 1555 ARGB
10: 8888 ARGB
11: Reserved

Bit 20:19 Reserved

Bit 18:17 Global Fog LUT index select (from Z):

00&11:	Z_15:7 as global fog LUT index;
01:	Z_12:4 "
10:	Z_8:0"

Bit 16:15 Fog Control (FC)
0x = fog disable
10 = local fog (vertex fog)
11 = global fog

Bit 14 Source Color Key Polarity (CKP)
0: inclusive transparent - within the color low and color high range transparent
1: exclusive transparent - outside the color low and color high range transparent

Bit 13 Source Color Key Transparency Enable (CKT)
0: Disable Color Key comparison. Pixel write enable
1: Enable Color Key comparison. Pixel write base on compared result.
Note: This is texture color compare against compare color register (E8)

Bit 12:9 Destination Blending Factors

0000: ZERO	(0, 0, 0, 0)
0001: One	(1, 1, 1, 1)
0010: SRC_COLOR	(Rs, Gs, Bs, As)
0011: INV_SRC_COLOR	(1 - Rs, 1- Gs, 1 - Bs, 1 - As)
0100: SRC_ALPHA	(As, As, As, As)
0101: INV_SRC_ALPHA	(1 - As, 1 - As, 1 - As,1 - As)
0110: Dst_Alpha	(Ad, Ad, Ad, Ad)
0111: INV_DST_ALPHA	(1- Ad, 1 - Ad, 1 - Ad, 1 - Ad)
1000: DST_COLOR	(Rd, Gd, Bd, Ad)
1001: INV_DST_COLOR	(1 - Rd, 1- Gd, 1 - Bd, 1 - Ad)

Bit 8:5 Source Blend Factors

0000: Zero	(0, 0, 0, 0)
0001: One	(1, 1, 1, 1)
0010: DST_COLOR	(Rd, Gd, Bd, Ad)
0011: INV_DST_COLOR	(1 - Rd, 1- Gd, 1 - Bd, 1 - Ad)
0100: SRC_ALPHA	(As, As, As, As)
0101: INV_SRC_ALPHA	(1 - As, 1 - As, 1 - As,1 - As)
0110: Dst_Alpha	(Ad, Ad, Ad, Ad)
0111: INV_DST_ALPHA	(1- Ad, 1 - Ad, 1 - Ad, 1 - Ad)
1000: SRC_ALPHA_SAT	(f, f, f, 1) where f = min(As, 1 - Ad)
1001: SRC_COLOR	(Rs, Gs, Bs, As)
1010: INV_SRC_COLOR	(1 - Rs, 1- Gs, 1 - Bs, 1 - As)

Bit 4 Alpha Blending Enable (Enable Source/Destination Blending) (ABE)
0 = Disable Alpha Blending. No Source/Destination blending
1 = Enable Alpha Blending

Bit 3 Reserved (R)

Bit 2:0 3D Draw Command

000 = 3D Triangle; if flat and no Z, 2D will take the span data and do the span fill job.
001 = 3D Line with Y major
010 = 3D Line with X major
- software needs to swap the vertex (X,Y) to (YX) before sending to SU, and the Edge Walker needs to swap back the (YX) to (XY) before sending to span.
011 = 3D Point
100 = Anti alias 3D Triangle;
101 = Anti alias 3D Line with Y major
110 = Anti alias 3D Line with X major
- software needs to swap the vertex (X,Y) to (YX) before sending to SU, and the Edge Walker needs to swap back the (YX) to (XY) before sending to span or else reserved

3D_Command_Set_2

Read Write Address: 0E4h
Power-on Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Z	**FZ**	**IZ**	**ZMAP**	**TEXTURE2 SIZE**								**CK**	**ALPHA TEST**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							**LOD BIAS**				**LCE**	**LOD CLAMP LEVEL**			

Bit 31 Z with Sign bit (Z)
0 = Z format is 16-bit positive value
1 = Z is S15 (one sign plus 15 value) 16-bit 2's complement value

Bit 30 Flush Z cache - one cycle pulse (FZ)
Set this bit to 1 to flush the internal Z cache. Internal logic will set back to 0 for normal cache operation
0 = Normal operation mode
1 = Invalidate the cache

Bit 29 Initialize Z - one cycle pulse (IZ)
Set this bit to 1 to initial Z to Z value (R94) in null cycle. Internal logic will set this bit back to 0 for normal operation
0 = Normal operation mode
1 = Initialize Z to Z value at zero cycle

Bit 28 Z-map bypass (ZMAP)
0 = Normal zero cycle Z operation
1 = Bypass zero cycle Z clear operation (need 2D to do Z clear)

Bit 27:20 *Texture2 size - 2**m X52**n is the largest mipmap texture rectangular
[23:20] = m - where 2**m is the dimension of X of rectangular texture
[19:16] = n - where 2**n is the dimension Y of rectangular

Bit 19 Destination color key transparency enable (CK)
0 = Disable color key comparison. Pixel write enable
1 = Enable color key comparison. Pixel write base on compared result.

Note: This is FB color compare against compare color register (A0)

Bit 18:16 Alpha Test Mode
000 = Alpha always pass (similar to disable alpha test) - default
001 = pass if As>Aref
010 = pass if As = Aref
011 = pass if As>=Aref
100 = pass if As<Aref
101 = pass if As! = Aref
110 = pass if As <= Aref
111 = Alpha never passes
Note: Aref at register 9C_[15:8]

Bit 15:9 Reserved

Bit 8:5 LOD Bias - default 0
Hardware LOD calculation will be offset by this register

Bit 4 LOD Clamp Enable (LCD)
0 = No LOD clamp - normal operation
1 = Maximum LOD level will be clamp at bit [3:0]

Bit 3:0 LOD Clamp Level - Valid only when bit [4] = 1
Maximum LOD level that texture engine could reach.

3D_Test Command

Read Write Address: 0FCh
Power-on Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**PDA**	**CDA**	**R**	**FTE**	**FPE**	**FT**	**FD**	**FZ**	**R**	**SS**	**LS**	**IR**	**STE**

Bit 31:13 Reserved

Bit 12 Select 3D display address as panel display address (PDA)
0 = CRT normal display mode - use CRT_0C and CRT_0D as display address
1 = Select 3D display address register (0C4h) as panel address

Bit 11 Select 3D display address as CRT display address (CDA)
0 = CRT normal display mode - use CRT0C and CRT0D as display address
1 = Select 3D display address register (0C4h) as CRT display address

Bit 10 Reserved (R)

Bit 9 Force triangle engine ready for both (FTE)

1. Accepting data from SU
2. Span ready for pixel engine

Bit 8 Force pixel engine ready for both (FPE)
l. Accept spand data
2. Z and D for memory write

Bit 7 Force texture ready in both to accept spand and data for filtering (FT)

Bit 6 Force Destination ready in (FD)
1. Accept span
2. Ready for alpha blending
3. Ready to write out the data to memory. Destination always ready when this bit is set to 1

Bit 5 Force Z ready in both (FZ)
1. Accept spand
2. Data ready for Z compare. Z is always ready when this bit is set to 1.

Bit 4 Reserved (R)

Bit 3 All seq used in setup (SS)
0 = Skip according to which feature is on
1 = All UC sequence will be executed no matter what features are on

Bit 2 Latedone used in setup for debug purpose (LS)
0 = New vertex data will be loaded whenever current vertex register is ready for next one
1 = Vertex register will not load until last UC instruction is executed.

Bit 1 Select internal rendering register B/A for read (IR)
0 = Select rendering register A
1 = Select rendering register B

Bit 0 Stop triangle engine (for CPU read rendering register) (STE)
0 = Normal operation mode
1 = Stop triangle engine operation
This bet set to 1 will block the triangle engine from kickoff. All rendering registers would not be changed by triangle engine.

Go Register in Vertex

Read Write Address: 120, 144, and 168 in D3D vertex; 138, 178, and 1B8 in Open GL vertex
Power-on Default: 0h

Note: This register is spread to 3 different locations, and is connected to the same physical register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**PCO**	**TT**	**SHADING**		**FCS**		**IR**	**STE**

Bit 31:8 Reserved

Bit 7 Perspective correction off (PCO)
0 = Perspective correction on
1 = Perspective correction off

Bit 6 Two Texture (TT)
0 = Single texture triangle
1 = Two texture triangle

Bit 5:4 Shading select
00: Gouraud
01: Flat
1X: Reserved

Bit 3:2 Flat color selection (FCS)
00: Vertex 0 diffuse color as flat color
01: Vertex 1 diffuse color as flat color
10: Vertex 2 diffuse color as flat color
11: Reserved (default vertex 0)

Bit 1 ALL_GO (AG)
0: reset to 0 by setup engine
1: active the setup engine
This bit set means all the vertex information have loaded into the vertex registers and is ready for Setup Engine to kickoff. This bit is reset by setup engine when setup read it or reach RE_GO.

Bit 0 XY_GO (XYG)
0: reset to 0 by setup engine
1: active the setup engine
This bit set means Vertex's XY coordinate has been loaded and Setup Engine is ok to kickoff. This bit is reset by setup engine when setup read it or reach RE_GO.

Z Base Register

Read Write Address: D0
Power-on Default: Don’t care

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Z BUFFER		**RESERVED**								**BASE ADDRESS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE ADDRESS															

Bit 31:30 Z Buffer
0x = Local Z buffer
10 = AGP Z buffer
11 = PCI system Z buffer

Bit 29:22 Reserved

Bit 21:0 Base address in 64 bit as a unit (21 bit cover 32MB space)
Note: write to this register will cause flush Z cache

Texture1 Base Register

Read Write Address: CC
Power-on Default: FC [bit 30] = 0, or else Don't Care

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
T1	**FC**	**RESERVED**		**TEXTURE BASE ADDRESS**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE BASE ADDRESS															

Bit 31 Texture1 in AGP memory: when this bit is set - texture1 is located at AGP memory. The physical address of AGP base is specified in bit [27:0] (T1)

Bit 30 Flush cache: when this bit is 1 - the internal cache will be reset. This bit 1 and new write to this register will generate a cache reset pulse. (FC)

Bit 29:28 Reserved

Bit 27:0 Texture base address in 128-bit (16-byte) as a unit (cover 4GB space)

Texture2 Base Register*

Read Write Address: C0
Power-on Default: Don't Care

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
T2	**RESERVED**			**TEXTURE BASE ADDRESS**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE BASE ADDRESS															

Bit 31 Texture2 in AGP memory: when this bit is set - texture1 is located at AGP memory. The physical address of AGP base is in AGP physical address register (T2)

Bit 30:28 Reserved

Bit 27:0 Texture base address in 128-bit (16-byte) as a unit (cover 4GB space)

Texture1 Blending Mode

Read Write Address: C8
Power-on Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		**ALPHA BLENDING MODE**				**AA1S**			**AA1C**	**AA1A**	**AA2S**			**AA2C**	**AA2A**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**CLOCK BLENDING MODE**				**CA1S**			**CA1C**	**CA1A**	**CA2S**			**CA1C**	**CA1A**

Bit 31:30 Reserved

Bit 29:26 Alpha blending mode
0000: SELECT ARG1 //default
0001: SELECT ARG2
0010: MODULATE //multiply
0011: MODULATE2X //multiply and shift 1 bits
0100: MODULATE4X //multiply and shift 2 bits
0101: ADD //add arg2 together
0101: ADDSIGNED //add with -0.5 bias
//***Linear alpha blend:
0111: BLENDDIFFUSEALPHA //alpha from diffuse alpha
1000: BLENDTEXTUREALPHA //alpha from texture alpha
1001: BLENDFACTORALPHA //alpha from morphing register
//Linear alpha blend with pre-multiplied arg1 input: Arg1 = Arg2* (1-Alpha)
1010: BLENDTEXTUREALPHAM //texture alpha
else: reserved

Bit 25:23 Alpha argument 1 selection (AA1S)
000: diffuse alpha
001: specular alpha
010: texture alpha
011: select texture factor - morph alpha

1xx: reserved

Bit 22 Alpha argument 1 complement (AA1C)
0 = non complement the input alpha
1 = invert the input alpha and color RGB

Bit 21 Alpha argument 1 alpha replicate (AA1A)
0 = color components no change
1 = replicate alpha to color components

Bit 20:18 Alpha argument 2 selection (AA2S)
000: diffuse alpha
001: specular alpha
010: texture alpha
011: select texture factor - morph alpha
1xx: reserved

Bit 17 Alpha argument 2 complement (AA2C)
0 = non-complement the input alpha
1 = invert the input alpha and color RGB

Bit 16 Alpha argument 2 alpha replicate (AA2A)
0 = color components no change
1 = replicate alpha to color components

Bit 15:14 Reserved

Bit 13:10 Color blending mode
0000: SELECT ARG1 //default
0001: SELECT ARG2
0010: MODULATE //multiply
0011: MODULATE2X //multiply and shift 1 bits
0100: MODULATE4X //multiply and shift 2 bits
0101: ADD //add arg2 together
0110: ADDSIGNED //add with -0.5 bias
//***Linear alpha blend:
0111: BLENDDIFFUSEALPHA //alpha from diffuse alpha
1000: BLENDTEXTUREALPHA //alpha from texture alpha
1001: BLENDFACTORALPHA //alpha from morphing register
//Linear alpha blend with pre-multiplied arg1 input: Arg1 = Arg2* (1-Alpha)
1010: BLENDTEXTUREALPHAM //texture alpha
else: reserved

Bit 9:7 Color argument 1 selection (CA1S)
000: diffuse color
001: specular color
010: texture color
011: select texture factor - diffuse color
1xx: reserved

Bit 6 Color argument 1 complement (CA1C)
0 = non complement the input color
1 = invert the input color

Bit 5 Color argument 1 alpha replicate (CA1A)
0 = color components no change
1 = replicate alpha to color components

Bit 4:2 Color argument 2 selection (CA2S)
000: diffuse color
001: specular color
010: texture color
011: select texture factor - diffuse color
1xx: reserved

Bit 1 Color argument 1 complement (CA1C)
0 = non complement the input color
1 = invert the input color

Bit 0 Color argument 1 alpha replicate (CA1A)
0 = color components no change
1 = replicate alpha to color components

2D3D DMA Registers

Table of Entry Address

Read Write Address: 3000
Power-on Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY ADDRESS														**RESERVED**	

Bit 31:2 Table of entry address

Bit 1:0 Reserved (R)

DMA Physical Address

Read Write Address: 3004
Power-on Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

PHYSICAL DATA MEMORY ADDRESS	DON'T CARE

Bit 31:2 Physical data memory address

Bit 1:0 Don't care

DMA Block Size/Page Size

Read Write Address: 3008
Power-on Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PAGE SIZE REMAINING - READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAGE SIZE - 64-BIT AS A UNIT SPACE															

Bit 31:16 Page size remaining - read only

Bit 1:0 Page size - 64-bit as a unit space

DMA Total Transfer Size of 64-Bit Data

Read Write Address: 300C
Power-on Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMT	A	DON'T CARE												TTS	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL TRANSFER SIZE															

Bit 31 Enable master transfer (EMT)

Bit 30 Address (A)
0 = Use table of entry address
1 = Use Physical Address

Bit 29:18 Don't care

Bit 17:0 Total transfer size - maximum in double word transfer size 1MB (TTS)

Chapter 26: TV Encoder Registers

Table 32: TV Encoder Registers Quick Reference

Summary of Registers	Page
Common Register	
Mode Register	26 - 2
Closed Captioning Registers	
Closed Captioning Enable Register	26 - 2
Closed Captioning Line Number Register	26 - 3
Closed Captioning 1st and 2nd byte Data for Odd Field	26 - 3
Closed Captioning 1st and 2nd byte Data for Even Field	26 - 4
Closed Captioning Status Register	26 - 4

Register Descriptions

The following are the descriptions for each registers.

Common Register

Mode Register

Read/Write Address: 3?5h, Index: 60h
Power-on Default: 00h

This register controls main function as follows.

7	6	5	4	3	2	1	0
DON'T CARE		**GL**	**OV**	**BL**	**VIDEO MODE**		

Bit 7:6 Don't Care. These Bits are permanently set to logic 0

Bit 5 Genlock control (GL)
This Bit controls genlock On/Off. When the genlock is on, sub-carrier is aligned by the horizontal sync for every four or eight fields.
0: On
1: Off

Bit 4 Override control (OV)
This Bit switches the video mode select source.
0: Mode pins are selected
1: Mode register Bits are selected

Bit 3 Blank Level control (BL)
This Bit switches are the black setup level
0: Black level is 7.5 IRE
1: Black level is 0 IRE

Bit 2:0 Video Mode select
These Bits switch the video mode when (OV) is 1.
000: NTSC CCIR
001: NTSC Square Pixel
010: NTSC 4Fsc
100: PAL CCIR
101: PAL Square pixel

Closed Captioning Registers

Closed Captioning Enable Register

Read/Write Address: 3?5h, Index: 61h

Power-on Default: 00h

This register controls the closed captioning function On/Off as follows. If this function is enabled and a new data is not written (the field status is 1), a null data (80 hex) will be output.

7	6	5	4	3	2	1	0
DON'T CARE						**CCE**	

Bit 7:2 Don't Care. These Bits are permanently set to logic 0

Bit 1:0 Closed captioning enable (CCE)
These Bits control the closed captioning On/Off for each field
00: Disable
01: Enable Odd field only
10: Enable Even field only
11: Enable both fields

Closed Captioning Line Number Register

Read/Write Address: 3?5h, Index: 62h
Power-on Default: 11h

This register controls closed captioning line number as follows:

7	6	5	4	3	2	1	0
DON'T CARE			**CLOSED CAPTIONING LINE NUMBER**				

Bit 7:5 Don't Care. These Bits are permanently set to logic 0

Bit 4:0 Closed Captioning Line Number Select
These Bits set the line number for the closed captioning data.
For NTSC mode, the actual line number will be CCL + 4 and CCL +263 +4
For PAL mode, the actual line number will be CCL +1 and CCL + 313+1

Closed Captioning 1st and 2nd byte Data for Odd Field

Read/Write Address: 3?5h, Index: 63h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 1st BYTE ODD FIELD							

Bit 7:0 Closed Captioning 1st Byte Odd Field

Read/Write Address: 64h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 2nd BYTE ODD FIELD							

Bit 7:0 Closed Captioning 2nd Byte Odd Field

The value at Closed Captioning 1st byte will be output as a 1st closed captioning data of the odd filed. And the value at Closed Captioning 2nd byte will be output as a 2nd one. When one of these bytes is written, the odd status Bit OST will be cleared.

Closed Captioning 1st and 2nd byte Data for Even Field

Read/Write Address: 3?5h, Index: 65h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 1st BYTE EVEN FIELD							

Bit 7:0 Closed Captioning 1st Byte Even Field

Read/Write Address: 66h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 2nd BYTE EVEN FIELD							

Bit 7:0 Closed Captioning 2nd Byte Even Field

The value at Closed Captioning 1st byte will be output as a 1st closed captioning data of the even filed. And the value at Closed Captioning 2nd byte will be output as a 2nd one. When one of these bytes is written, the even status Bit EST will be cleared.

Closed Captioning Status Register

Read Only Address: 3?5h, Index: 67h
Power-on Default: 03h

This register shows the closed captioning status of each field. If these Bits are set to 1, existed data was sent out, and suitable for writing a new data to each closed captioning data registers. These Bits are cleared on new data writing for each field

7	6	5	4	3	2	1	0
DON'T CARE						**OST**	**EST**

Bit 7:2 Don't Care. These Bits are permanently set to logic 0

Bit 1 Closed Captioning Odd filed status (OST)
This Bit shows the odd field status. When set to 1, the data was sent out.
0: The data is not sent
1: The data is sent and ready for writing next data

Bit 0 Closed Captioning Even Field Status (EST)
This Bit shows the even field status. When set to 1, the data was sent out.
0: The data is not sent
1: The data was sent and ready for writing next data.

Chapter 27: Electrical Specifications

Absolute Maximum Ratings

Table 33: Absolute Maximum Ratings

Specification	Maximum rating
Ambient temperature (TA)	0° C to 75° C
Storage temperature	-40° C to 125° C
Voltage on I/O pins with respect to VSS	- 0.5V to VDD + 5%
Operating power dissipation	TBD
Core DC Power supply voltage	2.5V ± 5%

DC Specifications

Table 34: Digital DC Specification

Name	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-		0.8	V
V_{IH}	Input High Voltage	2.0		-	V
V_{OL}	Output Low Voltage	-		0.4	V
V_{OH}	Output High Voltage	2.4		VDD+0.5	V
I_{OZL}	Output Tri-state Current	-		10	µA
I_{OZH}	Output Tri-state Current	-		10	µA
I_{OZL} (Pull up pins)	Output Tri-state Current	-130		-10	µA
I_{OZH} (Pull up pins)	Output Tri-state Current	-		10	µA
I_{OZL} (Pull down pins)	Output Tri-state Current	-		10	µA
I_{OZH} (Pull down pins)	Output Tri-state Current	10		130	µA
C_{IN}	Input Capacitance			10	pF
C_{OUT}	Output Capacitance			50	pF
I_{CC*}	Power Supply Current		6		mA

Table 35: Recommended DC Operating Voltages

Supply Voltage	Value	Notes
Digital Core	2.5V +/- 5%	
Digital Core (GL Parts)	2.0V +/- 5%	In ReduceOn mode
I/O	3.3V +/- 5%	
Host Interface (HVDD)	3.3V +/- 5%	
Analog DAC (AVDD)	3.3V +/- 5%	
PLL (CVDD)	2.5V +/- 5%	
Flat Panel (FPVDD)	3.3V +/- 5%	

Note: 1. The low voltage parts (GL) is identical to the regular parts. The only difference is that the low voltage parts go through a more rigorous test flow to guarantee a low voltage operation.
2. The low voltage part can be a substitute for the regular part.

Table 36: LVDS Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS (CMOS/TTL) DC Specifications						
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	$OV \leq V_{IN} \leq Vcc$			±10	μA
LVDS Driver DC Specifications						
V_{OD}	Differential Output Voltage	RL = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in VOD between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in VOC between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = OV, RL = 100 Ω			-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN = 0V, V_{OUT} = 0V to Vcc				

Note: LVDS transmitter licensed from Thine Electronics, Inc.

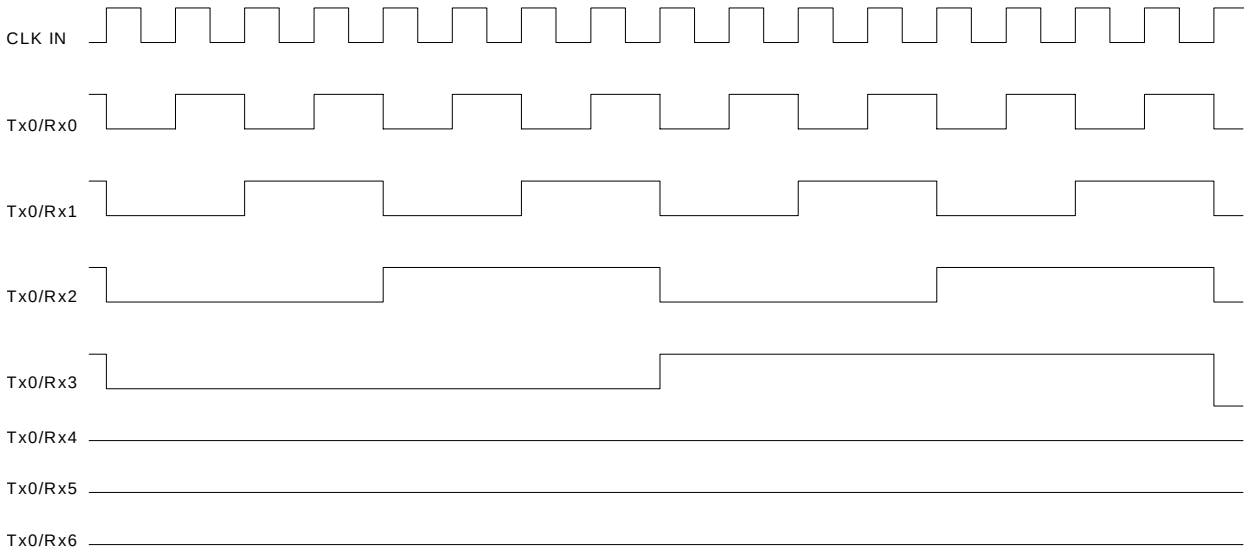


Figure 45: 16 Grayscale Pattern

Table 37: RAMDAC Characteristics

Parameter	Min	Typical	Max	Unit
Resolution Each DAC	-	8		Bits
LSB Size	-	54.7		µA
Output Full Scale Current	-	14.0		mA
Integral Linearity Error	0	-	1	LSB
Differential Linearity Error	0	-	1	LSB
DAC to DAC Mismatch	0	-	5%	
Power Supply Rejection Ratio	0	-	0.5	% /% AVDD
Output Compliance	0	-	1.2	V
Output Capacitance	-	-	10	pF
Glitch Energy	-	30	-	pV-Sec

Table 38: RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC Supply Voltage	3.17	3.3	3.47	V
CVDD	PLL Supply Voltage	2.38	2.50	2.63	V
VREF	Internal DAC voltage reference	1.1	1.235	1.35	V

AC Specifications

Table 39: RAMDAC AC Specifications

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	3		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Setting Time	15		ns	
DAC-to-DAC Output Skew	2	15	ns	3

Note: 1. Measured from the 50% of VCLK to the 50% point of full scale transaction
2. Measured from 10% to 90% full scale
3. With DAC outputs equally loaded

Parameter	I_{OUT} (mA)	VOUT (V)	BLANK	Input Data
White	14.0	0.7	1	FFh
Data	Data	Data	1	Data
Black	0	0	1	00h
~BLANK	0	0	0	Don't Care

Note: Condition for V_{OUT} is a 50 Ohm terminated load, use of the internal VREF and RFSC = 1.2 K Ohms.

AC Timing Specifications

Power On Reset

Table 40: Power-on Reset and Configuration Reset Timing

Symbol	Parameter	Min	Max	Unit
t1	Reset active from VCC stable	5	-	ms
t2	Reset active from external oscillator stable	0	-	
t3	Reset active from ~PWRDN signal stable	2	-	ms
t4	Internal Power On ~RESET from VCC stable	-	200	ns
t5	External ~RESET to internal Power On ~RESET inactive	-	20	ms
t6	External ~RESET Pulse Width		-	ns
t7	Configuration cycle setup time	20	-	ns
t8	Configuration cycle hold time	5		

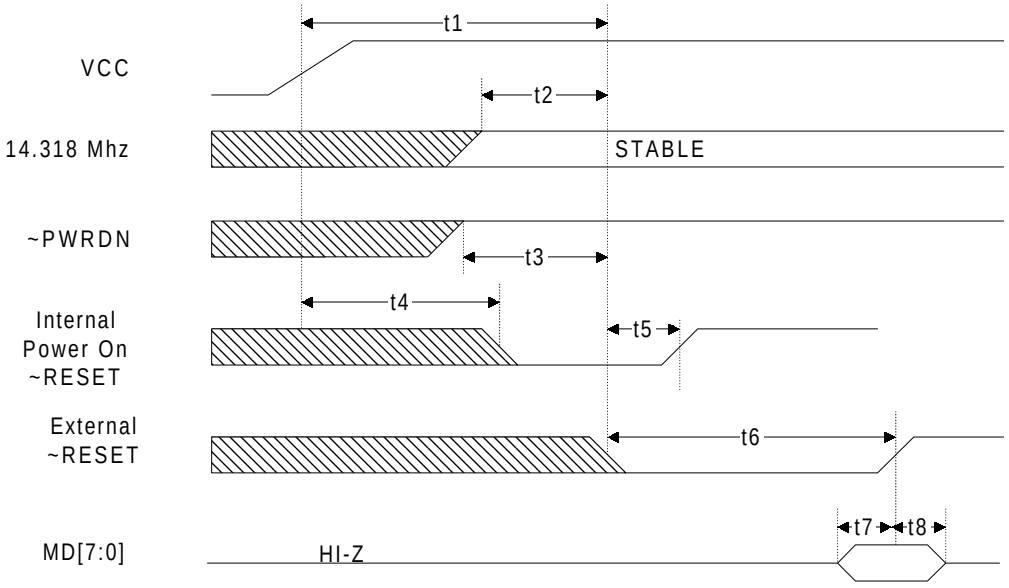


Figure 46: Power-on Reset and Reset Configuration Timing

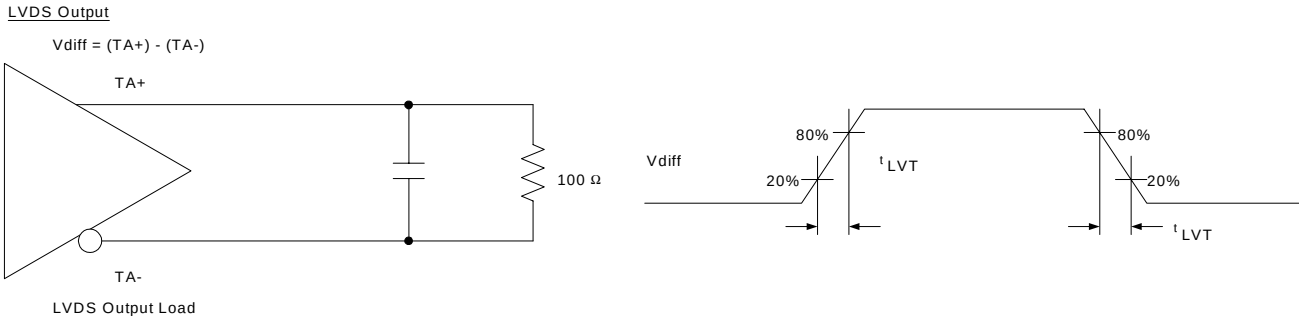


Figure 47: LVDS Transmitter Device Transition Times

Table 41: Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{LVT}	LVDS Transition Time		0.6	1.5	ns

PCI Bus Cycles

Table 42: PCI Bus Timing (33 MHz)

Symbol	Parameter	Min	Max	Unit
t1	~FRAME setup to CLK	7	-	ns
t2	AD[31:0] (address) setup to CLK	7	-	ns
t3	AD[31:0] (address) hold from CLK	0	-	ns
t4	AD[31:0] (Read Data) valid from CLK	2	11	ns
t5	AD[31:0] (Read Data) hold from CLK	0	-	ns
t6	AD[31:0] (Write Data) setup to CLK	7	-	ns
t7	AD[31:0] (Write Data) hold from CLK	0	-	ns
t8	C/~BE[3:0] (Command) setup to CLK	7	-	ns
t9	C/~BE[3:0] (Command) hold from CLK	0	-	ns
t10	C/~BE[3:0] (Byte Enable) hold from CLK	0	-	ns
t11	~TRDY High-Z to High from CLK	2	-	ns
t12	~TRDY active from CLK	2	11	ns
t13	~TRDY inactive from CLK	2	11	ns
t14	~TRDY High before High-Z	1T	-	CLK
t15	~IRDY setup to CLK	7	-	ns
t16	~IRDY hold from CLK	0	-	ns
t17	~DEVSEL active from CLK	2	11	ns
t18	~DEVSEL inactive from CLK	2	11	ns
t19	~DEVSEL High before High-Z	1T	-	CLK

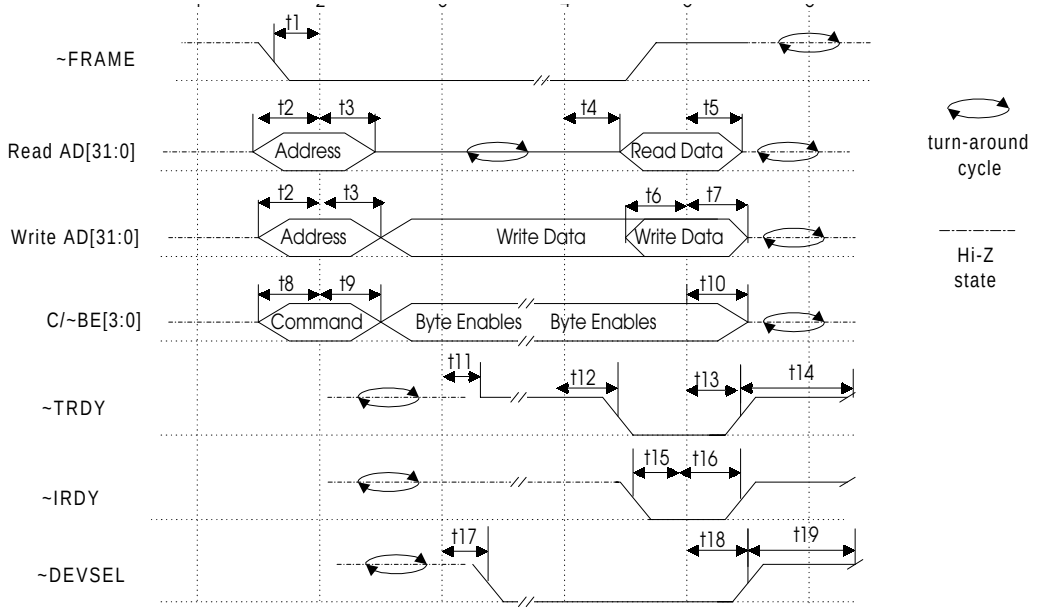


Figure 48: PCI Bus Timing Diagram

AGP BUS Cycles

Table 43: AGP 1X mode BUS Timing

Symbol	PARAMETER	Min Spec	Max Spec	units
t cyc	CLK Cycle Time	15.0	30.0	ns
t valc	CLK to control signal (Output) valid delay	1.0	5.5	ns
t vald	CLK to data (Output) valid delay	1.0	6.0	ns
t on	Float to Active (Output) Delay	1.0	6.0	ns
t off	Active to Float (Output) Delay	1.0	14.0	ns
t suc	Control signals (Input) setup time to CLK	6.0	-	ns
t sud	Data (Input) setup time to CLK	5.5	-	ns
t h	Control signals (Input) hold time to CLK	0.0	-	ns

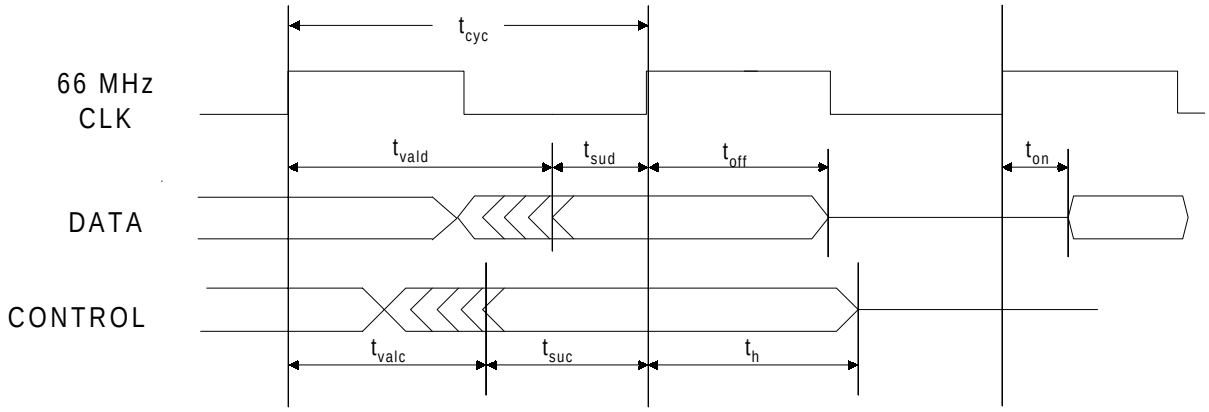


Figure 49: AGP Bus Timing Diagram

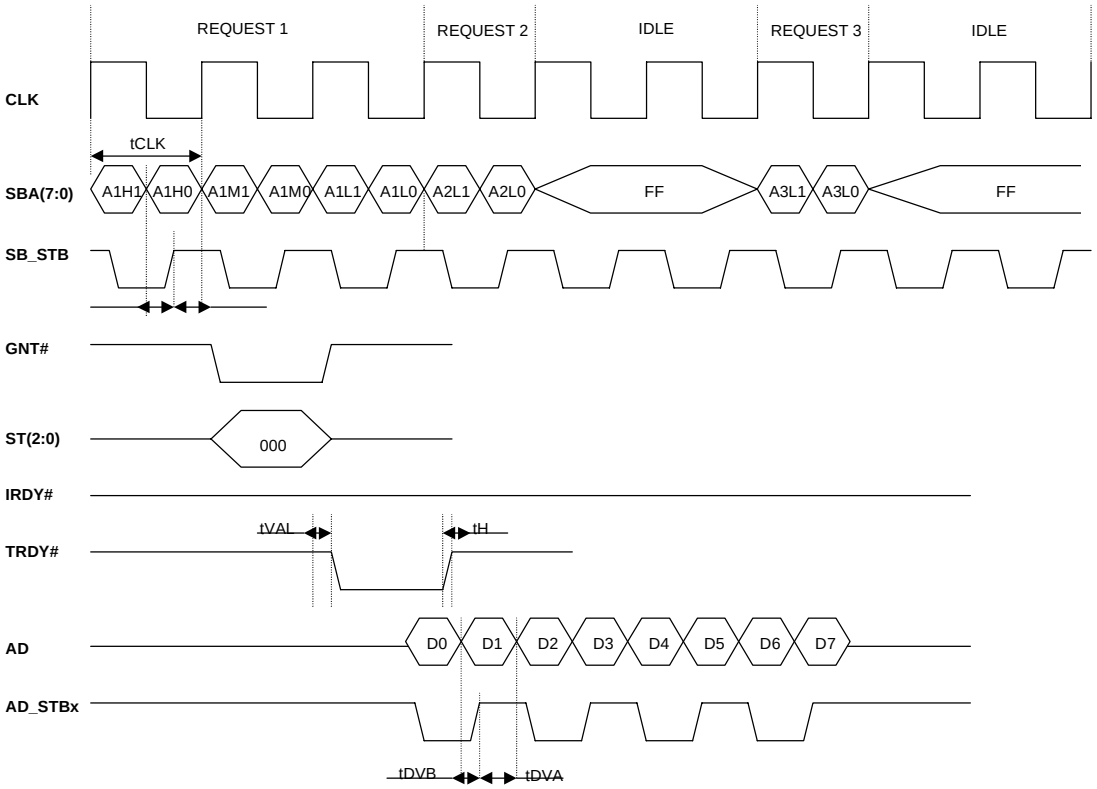


Figure 50: AGP 2X Read Request with Return Data (4Qw)

Table 44: AGP 2X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tCLK	Clock	-	15
TDVB	Data valid before	1.7	
tDVA	Data valid after	1.7	
TVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

Synchronous DRAM (SDRAM) and SGRAM Cycles

Table 45: SDRAM/SGRAM Memory Read Timing

Symbol	Parameter	Min	Max	Unit
t1	SDCK Cycle Time	12		ns
t2	SDCK High Time	4		ns
t3	SDCK Low Time	4		ns
t4	SDCKEN hold time	3.5		ns
t5	SDCKEN setup time	3.5		ns
t6	Command (˜CS, ˜RAS, ˜CAS, ˜WE, DSF, DQM) setup time	3.5		ns
t7	Command (˜CS, ˜RAS, ˜CAS, ˜WE, DSF, DQM) hold time	3.5		ns
t8	Address/BA setup time	3.5		ns
t9	Address/BA hold time	2.5		ns
t10	Access time from SDCK		T-2	ns
t11	Data Out hold time from SDCK	4		ns
t12	Data In setup time from SDCK	3.5		ns
t13	Data In hold time from SDCK	3.5		ns
t14	Active to READ, WRITE delay	3T		
t15	Read Latency	3T		
t16	Write recovery time	2T		

Note: T = SDCK clock period

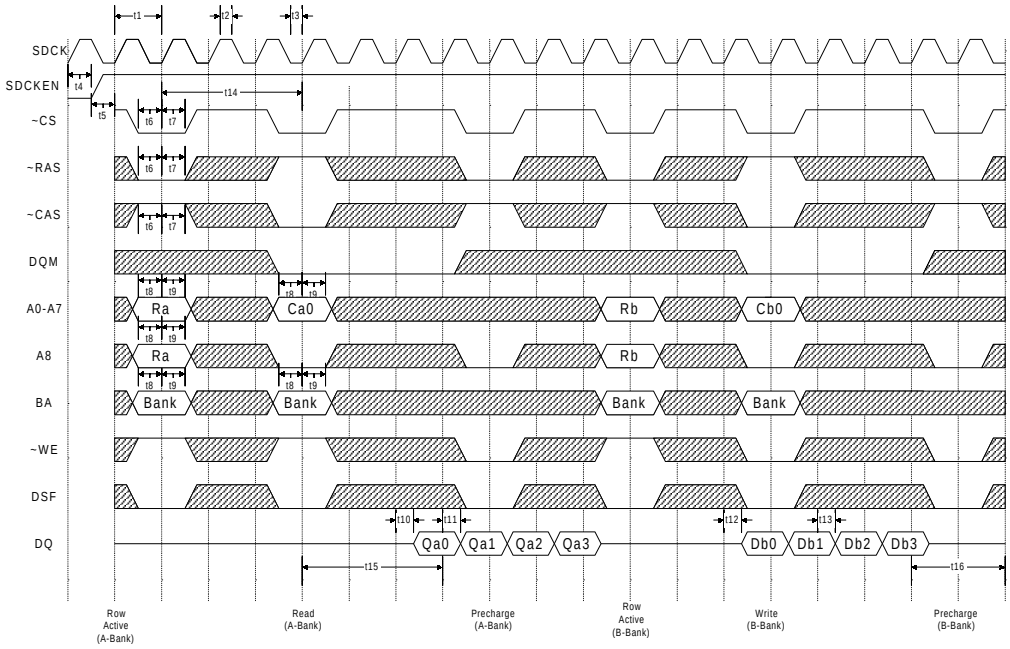


Figure 51: SDRAM/SGRAM Read and Write Cycles

Flat Panel Interface Cycle Timing

Table 46: Color TFT Interface Timing

Symbol	Parameter	Min	Max	Unit
t1	TFT FPSCLK Cycle Time	12		ns
t2f	FDATA setup to FPSCLK falling edge	0.5T-2		ns
t3f	FDATA hold from FPSCLK falling edge	0.5T-2		ns
t4f	DE setup to FPSCLK falling edge	0.5T-4		ns
t5f	DE hold from FPSCLK falling edge	0.5T-4		ns
t2r	FDATA setup to FPSCLK rising edge	0.5T-2		ns
t3r	FDATA hold from FPSCLK rising edge	0.5T-2		ns
t4r	DE VSYNC setup to FPSCLK rising edge	0.5T-4		ns
t5r	DE VSYNC hold from FPSCLK rising edge	0.5T-4		ns
t6	FHSYNC Pulse Width	8	16	T
t7	FVSYNC Pulse Width	1		FHSYNC

Note: T = pixel clock rate on LCD

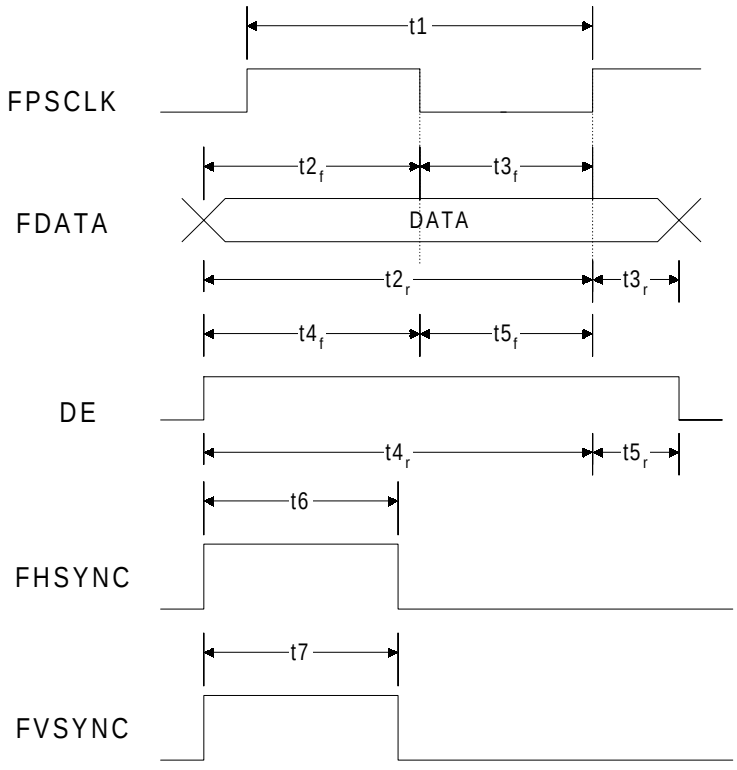


Figure 52: TFT Interface Timing

Table 47: Color DSTN Interface Timing

		16-Bit		24-Blt		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t1	DSTN FPSCLK High Time	2.5T-3	3T+3			ns
t2	DSTN FPSCLK Low Time	2.5T-3	3t+3			ns
t3	FDATA setup to FPSCLK falling edge	2.5T-5				ns
t4	FDATA hold from FPSCLK falling edge	2.5T-5				ns
t5	LP Pulse Width	16T	32T			ns
t6	FP setup to LP falling edge	20T				ns
t7	FP hold from LP falling edge	4T				ns
t8	DSTN FPSCLK active from LP falling edge	16T				ns
t9	DSTN FPSCLK inactive to LP rising edge	8T				ns

Note: T = pixel clock rate on LCD

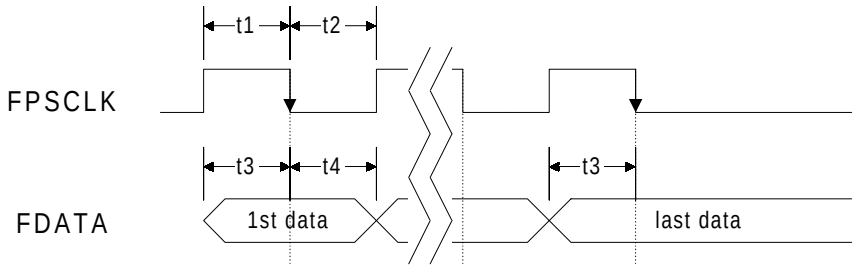


Figure 53: DSTN Interface (Clock and Data) Timing

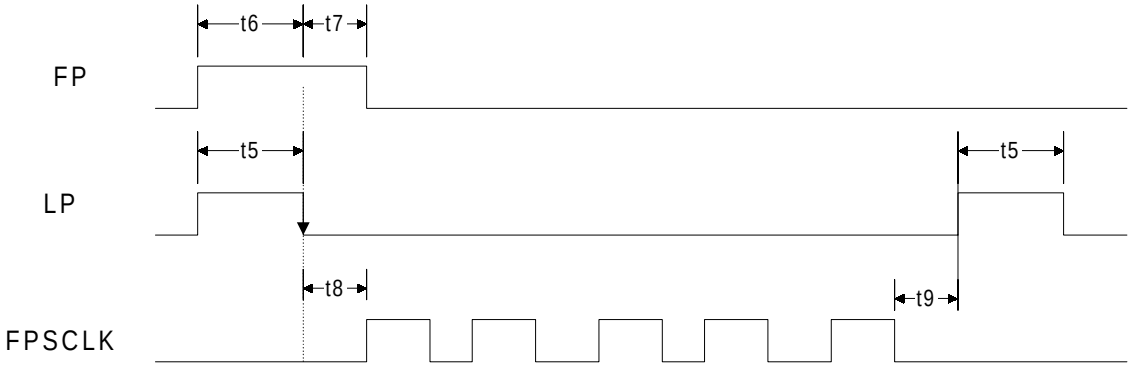


Figure 54: DSTN Interface (Control and Clock) Timing

Chapter 28: Mechanical Dimensions

Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.20	2.33	2.50	0.087	0.092	0.098
A1	—	0.60	—	—	0.024	—
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	—	0.75	—	—	0.030	—
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	—	24.13	—	—	0.950	—
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	17.95	18.00	18.05	0.707	0.709	0.711
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	—	24.13	—	—	0.950	—
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	17.95	18.00	18.05	0.707	0.709	0.711
e	—	1.27	—	—	0.050	—
ddd	—	—	0.15	—	—	0.006
θ	30° TYP			30° TYP		

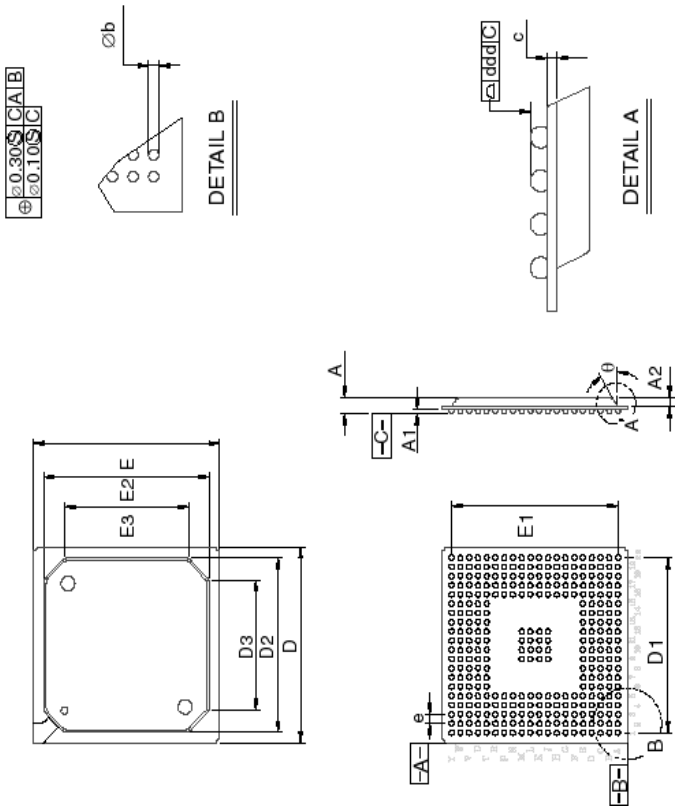


Figure 55: 316 BGA Mechanical Dimensions

Appendix A: Video Modes

This appendix lists the various tables of video modes supported under various configurations of Lynx3DM+: CRT only, LCD only, or simultaneous. The parameters listed in the following tables define the standard capabilities of the Lynx3DM+ when it is used with the Silicon Motion's Video BIOS.

Abbreviations used:
Txt: text mode
Gr: graphics mode

Standard IBM Compatible VGA Modes

The table details the standard VGA modes supported in CRT only.

Table 48: Standard IBM Compatible VGA Modes

Mode # (Hex)	Type	Colors	Alpha	Resolution	Font	Clock MHz	Hsync KHz	Vsync Hz	Memory Min	Buffer Start
0,1	Txt	16	40x25	320x200	8x8	25.175	31.55	70.3	256K	B8000
0,1*	Txt	16	40x25	320x350	8x14	25.175	31.55	70.3	256K	B8000
0,1+	Txt	16	40x25	360x400	9x16	28.322	31.34	69.8	256K	B8000
2,3	Txt	16	80x25	640x200	8x8	25.175	31.55	70.3	256K	B8000
2,3*	Txt	16	80x25	640x350	8x14	25.175	31.55	70.3	256K	B8000
2,3+	Txt	16	80x25	720x400	9x16	28.322	31.34	69.8	256K	B8000
4,5	Gr	4	40x25	320x200	8x8	25.175	31.55	70.3	256K	B8000
6	Gr	2	80x25	640x200	8x8	25.175	31.55	70.3	256K	B8000
7	Txt	Mono	80x25	720x350	9x14	28.322	31.34	69.8	256K	B8000
7+	Txt	Mono	80x25	720x400	9x16	28.322	31.34	69.8	256K	B8000
D	Gr	16	40x25	320x200	8x8	25.175	31.55	70.3	256K	A0000
E	Gr	16	80x25	640x200	8x8	25.175	31.55	70.3	256K	A0000
F	Gr	Mono	80x25	640x350	8x14	25.175	31.55	70.3	256K	A0000
10	Gr	16	80x25	640x350	8x14	25.175	31.55	70.3	256K	A0000
11	Gr	2	80x30	640x480	8x16	25.175	31.55	60.1	256K	A0000
12	Gr	16	80x30	640x480	8x16	25.175	31.55	60.1	256K	A0000
13	Gr	256	40x25	320x200	8x8	25.175	31.55	70.3	256K	A0000

NOTE: For Modes 3 and 7, 8-dot Fonts are used on the LCD.

VESA Super VGA Modes

VESA extended video modes are supported by the LYNX family BIOS (subject to the constraints of the video subsystem hardware) as follows:

Table 49: VESA Super VGA Modes

VESA Mode # (Hex)	Extended Mode	Type	Colors	Alpha	Resolution	Font	Memory Min	Buffer Start
(Min.)	Buffer Start							
101	50	Gr	256	80x30	640x480	8x16	512K	A0000
102	6A	Gr	16	100x75	800x600	8x8	256K	A0000
103	55	Gr	256	100x75	800x600	8x8	512K	A0000
104	6B	Gr	16	128x48	1024x768	8x16	512K	A0000
105	60	Gr	256	128x48	1024x768	8x16	1M	A0000
107	65	Gr	256	160x64	1280x1024	8x16	2M	A0000
111	52	Gr	64K	80x30	640x480	8x16	1M	A0000
112	53	Gr	16M	80x30	640x480	8x16	1M	A0000
114	57	Gr	64K	100x75	800x600	8x8	1M	A0000
115	58	Gr	16M	100x75	800x600	8x8	2M	A0000
117	62	Gr	64K	128x100	1024x768	8x8	2M	A0000
118	63	Gr	16M	128x100	1024x768	8x8	4M	A0000
11A	67	Gr	64K	160x128	1280x1024	8x8	4M	A0000
11B	68	Gr	16M	160x128	1280x1024	8x8	4M	A0000

Low Resolution Modes

The LYNX family BIOS supports low-resolution modes from 320x200 to 640x400 in 8/16-bit colors for DirectDraw. The low resolution modes are defined as follows:

Table 50: Low Resolution Modes

Mode # (Hex)	Type	Colors	Resolutions	Vsync (Hz)	Video Memory	Buffer Start
40	Gr	256	320x200	70	1MB	A0000
41	Gr	64K	320x200	70	1MB	A0000
42	Gr	256	320x240	75, 60	1MB	A0000
43	Gr	64K	320x240	75, 60	1MB	A0000
44	Gr	256	400x300	75, 60	1MB	A0000
45	Gr	64K	400x300	75, 60	1MB	A0000
46	Gr	256	512x384	75	1MB	A0000
47	Gr	64K	512x384	75	1MB	A0000
48	Gr	256	640x400	70	1MB	A0000
49	Gr	64K	640x400	70	1MB	A0000

NOTE: For modes 320x240 and 400x300, default refresh rate is set to 60Hz and optimal is set to 75Hz.

640 by 480 Resolution Modes

Table 51: 640 x 480 Extended Modes

Mode # (Hex)	VESA Mode # (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
50	101	Gr	256	80x30	8x16	25.175	31.5	60.0	512 KB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
52	111	Gr	64K	80x30	8x16	25.0	31.5	60.0	1MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
53	112	Gr	16M (24-bit)	80x30	8x16	25.0	31.5	60.0	1MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
54		Gr	16M (32-bit)	80x30	8x16	25.0	31.5	60.0	2MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz.

800 by 600 Resolution Modes

Table 52: 800x600 Extended Modes

Mode # (Hex)	Vesa Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
6A	6A	Gr	16	100x75	8x8	40.0	37.9+	60.3+	256KB	A0000
55	103	Gr	256	100x75	8x8	40.0	37.9+	60.3+	512KB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
57	114	Gr	64K	100X75	8X8	40.0	37.9+	60.3+	1MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
58	115	Gr	16M (24-bit)	100X75	8X8	40.0	37.9+	60.3+	2MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
59		Gr	16M (32-bit)	100X75	8X8	40.0	37.9+	60.3+	2MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz.

1024 by 768 Resolution Modes

Table 53: 1024x768 Extended Modes

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
6B	104	Gr	16	128x48	8x16	65.0	48.4 -	60.0 -	512KB	A0000
60	105	Gr	256	128x48	8x16	65.0	48.4 -	60.0 -	1MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
62	117	Gr	64K	128x48	8x16	65.0	48.4 -	60.0 -	2MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
63	118	Gr	16M (24-bit)	128x48	8x16	65.0	48.4 -	60.0 -	4MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
64		Gr	16M (32-bit)	128x48	8x16	65.0	48.4 -	60.0 -	4MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz

1280 by 1024 Resolution Modes

Table 54: 1280x1024 Extended Modes

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
65	107	Gr	256	160x64	8x16	78.8	46.4	86.8i+	2 MB	A0000
						108	64	60.0		
						135	79.98	75.0		
67	11A	Gr	64K	160x64	8x16	78.8	46.4	86.8i+	4 MB	A0000
						108	64	60.0		
						135	79.98	75.0		
68		Gr	16M (24-bit)	160x64	8x16	78.8	46.4	86.8i+	4 MB	A0000
						108	64	60.0		
						135	79.98	75.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz

Appendix B: Popup Icon Consideration

Introduction

The Lynx family of silicon supports both the hardware cursor and popup icon. System BIOS uses the popup icon to display system information, such as: Battery Status, LCD Brightness and more. The display driver for GUI operating system uses the hardware Cursor to increase performance. Since both popup icon and hardware cursor image locations are closely coupled both will be described. This appendix details popup icon support and how to implement the support in system BIOS.

Popup Icon

The popup icon size is 64x64, and can be zoomed up by 2 to become 128x128 popup icon. The popup icon can be programmed to anywhere on the screen display.

Furthermore, the popup icon is supported only through the CRT backend. Thus, when display image is processed through the LCD backend (as in the case of Virtual Refresh mode), there is no popup icon support on the LCD.

For example, in simultaneous mode since a display image is processed through the CRT backend, the popup icon can be displayed on both LCD and CRT. Similarly, in LCD only mode (Standard Refresh mode), popup icon can be displayed on the LCD. However, in Dual Monitor mode (or Virtual Refresh mode) under Windows 98, the popup icon will only be displayed on CRT and not on the LCD.

Icon Pattern Memory Location

The Icon pattern memory location is specified in PHR80 and PHR81 registers. These two registers allocate 2KB off-screen video memory within the maximum physical memory. Silicon Motion assigns the highest 2KB address for the physical memory installed. The lower 1KB is used to store Pop-Up icon image. The upper 1KB is used to store hardware cursor image. (Please also refer to Figure 56)

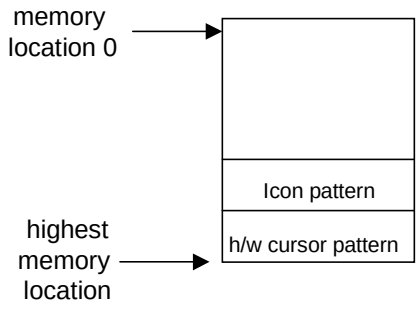


Figure 56: Hardware Cursor and Popup Icon Memory Location

Icon Pattern

Each pixel of the Icon pattern uses 2-bit to select the different color formats. The table below lists the various color selects: transparent, Icon Color1 is defined in POP84 register, Icon Color2 is defined in POP85 register, and Icon Color3 is defined in POP86 register.

Icon Pattern [1:0]	Color Source
00	transparent
01	Icon Color1
10	Icon Color 2
11	Icon Color 3

Furthermore, pixel data is stored in sequential order. For example, Bit[7:6] of a byte in the video memory is the first pixel of the Icon pattern. Bit[5:4] is the second pixel of the Icon pattern.

Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0
1st pixel	2nd pixel	3rd pixel	4th pixel

Each of the popup icon color registers (POP83-85) is defined in the same way described below:

The 8-bit color register is defined to be 3:3:2 for R:G:B respectively as shown on the table below:

7	6	5	4	3	2	1	0
Red			Green			Blue	
2	1	0	2	1	0	1	0

The Lynx family of silicon will take the 8-bit Icon color and convert it into 24-bit Icon color internally. For example, R2R1R0G2G1G0B1B0 will be expanded to R2R1R0R0R0R0R0R0G2G1G0G0G0G0G0G0B1B0B0B0B0B0B0B0.

Icon Control

Register POP82 controls the popup icon enable and size.

POP82[7] controls Popup Icon Enable
0 = Disable
1 = Enable

POP82[6] controls Popup Icon Size
0 = 64x64
1 = 128x128

Video BIOS Function Call

Video BIOS has call services for popup icon. The table below lists the available video BIOS function calls. For more detail information, please refer to the Lynx family BIOS specification.

Function Definition	AX	BX	CH	CL	DX	ES:SI
Icon Control	5F10	0		0 = disable		

Function Definition	AX	BX	CH	CL	DX	ES:SI
1 = enable						
Icon Size	5F10	1		0 = 64x64		
1 = 128x128						
Icon Location	5F10	2	X start	X start	Y start	
Icon Color1	5F10	3	1	Color Value		
Icon Color2	5F10	3	2	Color Value		
Icon Color3	5F10	3	3	Color Value		
Load Icon Pattern	5F10	5				Pattern Address

Furthermore, there is a sample code (pop8.exe) which shows how to use the video BIOS function call to set up popup icon image. Please request this sample code from your local technical support staff.

Appendix C: SMI Handler Programming Consideration

Introduction

The Lynx family of silicon is designed for notebook systems. Notebook systems require support of SMM (system management mode) for handling system-wide functions, such as: power management, system hardware control, and proprietary OEM-design code. This application note describes consideration for system BIOS when implementing SMI (System management interrupt) handler for the Lynx family of silicon.

Background

SMM is a special-purpose operating mode provided for handling system-wide functions. The main benefit of SMM is that it offers an easily isolated processor environment that operates transparently to the operating system or software applications.

When SMM is invoked through SMI, the processor saves the current state of the processor, then switches to a separate operating environment contained in the system management RAM. While in SMM, the processor executes a SMI handler code to perform operations such as power down HD when it is idle or displaying an OEM-design message on the screen. When the SMI handler has completed its operations, it executes a resume instruction. This instruction causes the processor to reload the saved context of the processor, switch back to protected or real mode, and resume executing the interrupted operating-system program or interrupted application programs.

System BIOS Consideration

The video BIOS provides an alternate INT 10h entry to allow SMI handlers to execute VGA BIOS function calls. This entry point bypasses the STI (Set Interrupt Flag) instruction at the beginning of the standard interrupt handler.

Int10 Vector Entry

The standard interrupt handler INT10 vector is located in 0000:0040h. This INT10 handler will issue STI instruction.

Alternate INT10 Entry

The alternate INT10 entry is specified within the content of location C000:0034h. This alternate INT10 handler entry does not issue STI.

Note: For system BIOS from Phoenix, there is a function named: PmModifyInt10Vector that can be used to modify the INT10 vector.

Video BIOS service calls read/modify the I/O and memory-mapped registers. The memory-mapped registers are accessed through A000-B000 range in real mode or SMM; they are video processor registers, drawing engine registers and capture port registers. Due to the fact that A000-B000 range is reserved for power management under SMM mode, special consideration is necessary:

There are two methods as listed below:

1. **Exit SMM**
   Exit SMM when calling video BIOS services or accessing memory-mapped registers. Upon completion, it is ok to resume back to SMM.

2. **Map Power Management Data to another location**
   The default area for storing the power management data is A000-B000. In order to allow video BIOS services to access A000-B000 area, system BIOS can map the A000-B000 data to another location, such as D000-E000.

Appendix D: Programming USR [3:0] Pins

Application Notes for control of USR [3:0] Pins

*GPR 72 is General Purpose Register 72 with address 3C5h and index 72h
GPR 73 is General Purpose Register 73 with address 3C5h and index 73h

USR0

GPR72 [4]	GPR72 [0]	USR0 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR0 is in input state, the input status can be read from GRP72[2].

USR1

GPR72 [5]	GPR72 [1]	USR1 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR1 is in input state, the input status can be read from GRP72[3].

USR2

GPR73 [5]	GPR73 [1]	USR1 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR2 is in input state, the input status can be read from GRP73[2]. When toggling USR2 as an input pin, it will generate a hardware interrupt. The status of the interrupt can be read at bit 2 of SCR1C register.

USR3

GPR73 [5]	GPR73 [1]	USR1 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR3 is in input state, the input status can be read from GRP73[3]. When toggling USR3 as an input pin, it will generate a hardware interrupt. The status of the interrupt can be read at bit 3 of SCR1C register.

Appendix E: Monitor & TV Defect

CRT Monitor Detect

To simplify the monitor detect procedure SM722 implemented four new registers (ccr7a, ccr7b, ccr7c, ccr7d) and detect circuitry. As for R, G, B corresponds to ccr7a, ccr7b, ccr7c data and ccr7d_[7] as enable. When all these registers are programmed properly, and without waiting for sync period the users can read back the register 3c2_[4] to determine if the monitor is connected.

3c2_[4] = 0; No monitor detect
3c2_[4] = 1; Color monitor detect

TV Detect

To simplify the TV monitor detect procedure SM722 also uses registers (ccr7a, ccr7b, ccr7c, ccr7d), and TV monitor detect circuitry.

For Y = {ccr7a,00} as 10 bit data
For C = {ccr7b,00} as 10 bit data
For CVBS = {ccr7c,00} as 10 bit data

With ccr7d_[7] as enable and all these registers are programmed properly the users can read back the register ccr7d_[6] to determine SVHS monitor's status.

Ccr7d_[6] = 0; No TV monitor detect
Ccr7d_[6] = 1; TV monitor detect

With ccr7d_[7] as enable and all these registers are programmed properly the users can read back the register ccr7d_[5] to determine CVBS monitor's status.

Ccr7d_[5] = 0; No TV monitor detect
Ccr7d_[5] = 1; TV monitor detect

Appendix F: CRT Timing Register Summary

CRT Timing Register Summary

Table 55: CRT Timing and LCD Shadow Register Summary

Parameter	CRT Register Bits						
	[10]	[9]	[8]	[7]	[6]	[5]	[4:0]
H Total				CRT00[7]	CRT00[6]	CRT00[5]	CRT00[4:0]
H Total Shadow				SVR40[7]	SVR40[6]	SVR40[5]	SVR40[4:0]
H Display End				CRT01[7]	CRT01[6]	CRT01[5]	CRT01[4:0]
H Blank Start				CRT02[7]	CRT02[6]	CRT02[5]	CRT02[4:0]
H Blank Start Shadow				SVR41[7]	SVR41[6]	SVR41[5]	SVR41[4:0]
H Blank End				CRT33[6]	CRT33[5]	CRT05[7]	CRT03[4:0]
H Blank End Shadow						SVR44[7]	SVR42[4:0]
H Sync Start				CRT04[7]	CRT04[6]	CRT04[5]	CRT04[4:0]
H Sync Start Shadow				SVR43[7]	SVR43[6]	SVR43[5]	SVR43[4:0]
H Sync End							CRT05[4:0]
H Sync End Shadow							SVR44[4:0]
V Total	CRT30[3]	CRT07[5]	CRT07[0]	CRT06[7]	CRT06[6]	CRT06[5]	CRT06[4:0]
V Total Shadow		SVR4A[5]	SVR4A[0]	SVR45[7]	SVR45[6]	SVR45[5]	SVR45[4:0]
V Sync Start	CRT30[0]	CRT07[7]	CRT07[2]	CRT10[7]	CRT10[6]	CRT10[5]	CRT010[4:0]
V Sync Start Shadow		SVR4A[7]	SVR4A[2]	SVR48[7]	SVR48[6]	SVR48[5]	SVR48[4:0]
V Sync End							CRT011[3:0]
V Sync End Shadow							SVR49[3:0]
V Display End	CRT30[2]	CRT07[6]	CRT07[1]	CRT12[7]	CRT12[6]	CRT12[5]	CRT012[4:0]
V Blank Start	CRT30[1]	CRT09[5]	CRT07[3]	CRT15[7]	CRT15[6]	CRT15[5]	CRT015[4:0]
V Blank Start Shadow		SVR4B[5]	SVR4A[3]	SVR46[7]	SVR46[6]	SVR46[5]	SVR46[4:0]
V Blank End	CRT36[2]	CRT33[4]	CRT33[3]	CRT16[7]	CRT16[6]	CRT16[5]	CRT016[4:0]
V Blank End Shadow				SVR47[7]	SVR47[6]	SVR47[5]	SVR47[4:0]
Line Compare				CRT18[7]	CRT18[6]	CRT18[5]	CRT018[4:0]
Offset				CRT13[7]	CRT13[6]	CRT13[5]	CRT013[4:0]

Note: Bits shown in bold text are SMI extended registers

Appendix G: 2D/3D Bus Master DMA Data Stream Format

2D3D Bus Master - DMA Data Stream Format

DMA data format is always in Mask-Data pair. It could be one 32-bit Mask followed by one 32-bit data, or more sets of 32-bit data depending on the setting in the mask.

DMA 32-bit Mask

Vertex Data DMA Mask Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**DMA CONTROL**		**VS**		**FVF FORMAT**				**RESERVED**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**PC**	**DT**	**RESERVED**		**GCS**		**GCFC**		**ALL**	**XY**

Bit 31:30 DMA Data Type
00: Vertex data
01: 2D/3D registers/commands
10: Host blit write data
11: Low level engine (wait, flush, flip,...etc.)*

Bit 29:28 DMA Control
x1: End of A DMA buffer
1x: End of A DMA block
Each DMA buffer could contain several DMA blocks. Each DMA block (max 4K byte) consists of a number of DMA mask/data pairs.

Hardware DMA operation sequence:
1. Fetch the first DMA mask;
2. Fetch the DMA data defined by the present DMA mask and fetch the next DMA mask;
3. Load/check the next DMA mask:
   a) If end-of- DMA buffer then DMA is done; or
   b) If end-of-block (go to step 1); or
   c) Else (go to step 2)

Bit 27:26 DMA head - Vertex selection (VS)
00 data for vertex 0
01 data for vertex 1
10 data for vertex 2
11 data contains 3 vertices (v0, v1 and v2) for list or first triangle in the strip or fan

Bit 25:22 DMA head - FVF Format - there are 5 groups
xxxx include x, y, z
1xxx include diffuse color
x1xx include specular color
xx1x include texture 1 (Wi1, U1, V1)
xxx1 include texture 2, (U2, V2)*

Bit 21:10 Reserved

Bit 9 Go command - Perspective correction off when = 1 (PC)

Bit 8 Go command - Dual textures when = 1 (DT)

Bit 7:6 Reserved

Bit 5:4 Go command shading (GCS)
00: Gouraud shading
01: Flat shading
1x: Reserved

Bit 3:2 Go command flat color section (GCFC)
00: Vertex 0's diffuse color as flat color
01: Vertex 1's diffuse color as flat color
10: Vertex 2's diffuse color as flat color
11: Reserved

Bit 1 All_go

Bit 0 XY_go

* Not supported for SM722

2D/3D Register Mask Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**1**	**DMA CONTROL**		**PCI OFFSET**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI OFFSET				**DWORD COUNT**											

Bit 31:30 DMA Data Type
00: Vertex data
01: 2D/3D registers/commands
10: Host blit write data
11: Low level engine (wait, flush, flip,...etc.)*

Bit 29:28 DMA Control

x1: End of A DMA buffer
1x: End of A DMA block

Bit 27:12 PCI offset - 16 bits

Bit 11:0 Dword count - number of consecutive DW in the following DMA data

Host Blit Write Data Mask Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	**0**	**DMA CONTROL**		**RESERVED**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit 31:30 DMA Data Type
00: Vertex data
01: 2D/3D registers/commands
10: Host blit write data
11: Low level engine (wait, flush, flip,...etc.)*

Bit 29:28 DMA Control
x1: End of A DMA buffer
1x: End of A DMA block

Bit 27:0 Reserved

Appendix H: Lynx3DM+ New Features

Introduction

This chapter includes a description of the additional features added to the Lynx3DM+ compared to Lynx3DM.

This Lynx3DM+ chapter includes the following components:

- New features
- New registers
- Errata fixed from Lynx3DM
- Pin descriptions

New Feature

The original Lynx3DM part used MCB technology developed by Silicon Motion. The MCB technology married the logic die and the memory die to provide a robust and highly integrated part. The Lynx3DM+ provides more integration by integrating an 112MHz LVDS transmitter resulting in both space and power saving. This saving is especially important in low form factor battery sensitive notebooks.

LVDS features:

- 28:4 Data channel compression at up to 392 MB/sec throughput
- Wide Frequency Range: 32 - 112 MHz suited for SVGA, VGA and SXGA
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- On chip Input Jitter filtering
- PLL requires No external Components

LVDS Data Input Select:

There are two different ways that LVDS inputs are mapped: Generic and Hitachi listed below

Generic	T1[6:0]	T2[6:0]	T3[6:0]	T4[6:0]
24-bit TFT	G[0], R[5:0]	B[1:0], G[5:1]	DE, Vsync, Hsync, B[5:2]	0, B[7:6], G[7:6], R[7:6]

Hitachi	T1[6:0]	T2[6:0]	T3[6:0]	T4[6:0]
24-bit TFT	G[2], R[7:2]	B[3:2], G[7:3]	DE, Vsync, Hsync, B[:4]	0, B[1:0], G[1:0], R[1:0]

New Registers

- Lynx3DM+ device number is 720 revision CA

- FPR33[4] is used to select panel to drive the digital panel interface (Please refer to Figure 3 at the end of this document for more detail explanation)
  0 = FP1 interface drives the digital panel interface
  1 = FP2 (virtual) interface drives the digital panel interface
  (Note: only FP1 interface connects to the LVDS interface)

- FPR4E[5] is used to enable/disable the digital panel output
  0 = Normal. Digital Panel interface connected. (default)
  1 = Digital Panel interface is not connected. Fpdata[23:0] pad is in tri-state mode.

- FPR33[6] is used to select between these two ways:
  0 = Generic TFT 24-bit or 18-bit LVDS mapping
  1 = Hitachi TFT 24-bit LVDS mapping (for Hitachi 18-bit LVDS panel, this bit should be set to 0)

- FPR33[7]: enable LVDS module
  0 = LVDS module in power down mode
  1 = LVDS module is power-on.

- CRT Vertical Blank End Control added one more bit for SXGA panel
  V. Blank End Control Bits: {CR36[2], CR33[4:3], CR16[7:0]}

Lynx3DM+ Pin Descriptions

The Lynx3DM+ is provided in a 316 BGA package.

The following table, Table 57, provides a brief description of the new BGA balls of the Lynx3DM+ that are different from Lynx3DM. Signal names with ~ preceding are active "LOW" signals, whereas signal names without ~ preceding are active "HIGH" signals. Also, the following abbreviations are used for Pin Type.

I	-	INPUT SIGNAL
O	-	Output Signal
I/O	-	Input or Output Signal

Note: All Outputs and I/O signals are tri-stated except all analog outputs including LVDS. Internal pull-up for I/O pad are all 100KO?resistor. Internal pull-down for I/O pad are all 100KO resistor.

Table 56: New Pin Descriptions for Lynx3DM+

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max.Load (pF)	Description
LVDS Interface					
TX0+/-	O				LVDS Channel 1 Output
TX1+/-	O				LVDS Channel 2 Output
TX2+/-	O				LVDS Channel 3 Output
TX3+/-	O				LVDS Channel 4 Output
TXCLK+/-	O				LVDS Clock Output
VCC and GROUND Pins					
PLLVDD					LVDS PLL Power Supply, 2.5V
PLLVSS					LVDS PLL Ground
LVDD					LVDS Power Supply, 2.5V
LVSS					LVDS Ground
Others					
RS[12:2]					Reserve pins
BA0					Memory Bank 0 select (Reserved)

Table 57: Numerical SM722 BGA Pin List

(NOTE: signals which are in BOLD have different definitions from Lynx3DM)

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
A1	MD12	MD12				MVDD
A2	MD3	MD3	{ROM}			MVDD
A3	MD4	MD4	ROMD4			MVDD
A4	MD5	MD5	ROMD5			MVDD
A5	MD7	MD7	ROMD7			MVDD
A6	MD31	MD31				MVDD
A7	MD17	MD17				MVDD
A8	MD28	MD28				MVDD
A9	MD20	MD20				MVDD
A10	MD25	MD25				MVDD
A11	MD22	MD22				MVDD
A12	AD0	AD0				HVDD
A13	AD4	AD4				HVDD
A14	AD7	AD7				HVDD
A15	AD9	AD9				HVDD
A16	AD12	AD12				HVDD
A17	AD14	AD14				HVDD
A18	PAR	PAR				HVDD
A19	~FRAME	~FRAME				HVDD
A20	C/~BE2	C/~BE2				HVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
B1	MD2	MD2	ROMD2			MVDD
B2	MD0	MD0	ROMD0			MVDD
B3	MD11	MD11				MVDD
B4	MD9	MD9				MVDD
B5	MD8	MD8				MVDD
B6	~DQM3	~DQM3				MVDD
B7	MD30	MD30				MVDD
B8	MD18	MD18				MVDD
B9	MD27	MD27				MVDD
B10	MD21	MD21				MVDD
B11	MD24	MD24				MVDD
B12	AD1	AD1				HVDD
B13	AD5	AD5				HVDD
B14	C/~BE0	C/~BE0				HVDD
B15	AD10	AD10				HVDD
B16	AD13	AD13				HVDD
B17	C/~BE1	C/~BE1				HVDD
B18	~TDRY	~TDRY				HVDD
B19	~STOP	~STOP				HVDD
B20	AD16	AD16				HVDD
C1	MD15	MD15				MVDD
C2	MD1	MD1	ROMD1			MVDD
C3	MD13	MD13				MVDD
C4	MD10	MD10				MVDD
C5	MD6	MD6	ROMD6			MVDD
C6	~DQM2	~DQM2				MVDD
C7	MD16	MD16				MVDD
C8	MD29	MD29				MVDD
C9	MD19	MD19				MVDD
C10	MD26	MD26				MVDD
C11	MD23	MD23				MVDD
C12	AD3	AD3				HVDD
C13	AD6	AD6				HVDD
C14	AD8	AD8				HVDD
C15	AD11	AD11				HVDD
C16	AD15	AD15				HVDD
C17	~DEVSEL	~DEVSEL				HVDD
C18	~IDRY	~IDRY				HVDD
C19	AD17	AD17				HVDD
C20	AD18	AD18				HVDD
D1	~CS0	~CS0				MVDD
D2	~DQM1	~DQM1				MVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
D3	MD14	MD14				MVDD
D4	VCCA	VCCA				
D5	VSS	VSS				
D6	**MIVDD**	**MVDD**				
D7	VSS	VSS				
D8	**MIVDD**	**MVDD**				
D9	VSS	VSS				
D10	VSS	VSS				
D11	AD2	AD2				HVDD
D12	HVDD	HVDD				
D13	VSS	VSS				
D14	HVDD	HVDD				
D15	VDD	VDD				
D16	VSS	VSS				
D17	HVDD	HVDD				
D18	AD19	AD19				HVDD
D19	AD20	AD20				HVDD
D20	AD21	AD21				HVDD
E1	~WE	~WE				MVDD
E2	BA	BA				MVDD
E3	~DQM0	~DQM0				MVDD
E4	VSS	VSS				
E5	~RBF	~RBF				
E6	**Reserved**	**BA0**				
E7	RS2	RS2				
E8	~AGP_BUSY	~AGP_BUSY				HVDD
E9	~STOP_AGP	~STOP_AGP				HVDD
E10	~PIPE	~PIPE				HVDD
E11	ST0	ST0				HVDD
E12	ST1	ST1				HVDD
E13	ST2	ST2				HVDD
E14	SBA7	SBA7				HVDD
E15	SBA6	SBA6				HVDD
E16	SBA5	SBA5				HVDD
E17	VSS	VSS				
E18	AD22	AD22				HVDD
E19	AD23	AD23				HVDD
E20	IDSEL	IDSEL				HVDD
F1	MA5	MA5				MVDD
F2	~CAS	~CAS				MVDD
F3	~RAS	~RAS				MVDD
F4	MVDD	MVDD				

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
F5	VCCA	VCCA				
F16	SBA4	SBA4				HVDD
F17	HVDD	HVDD				
F18	C/~BE3	C/~BE3				HVDD
F19	AD24	AD24				HVDD
F20	AD25	AD25				HVDD
G1	MA7	MA7				MVDD
G2	MA3	MA3				MVDD
G3	MA4	MA4				MVDD
G4	VSS	VSS				
G5	**VSSA**	**VSS**				
G16	SBA3	SBA3				HVDD
G17	VDD	VDD				
G18	AD26	AD26				HVDD
G19	AD27	AD27				HVDD
G20	AD28	AD28				HVDD
H1	MA1	MA1				MVDD
H2	MA8	MA8				MVDD
H3	MA2	MA2				MVDD
H4	MA6	MA6				MVDD
H5	MA10	MA10				MVDD
H16	SBA2	SBA2				HVDD
H17	VSS	VSS				
H18	AD29	AD29				HVDD
H19	AD30	AD30				HVDD
H20	AD31	AD31				HVDD
J1	SDCKEN	SDCKEN				MVDD
J2	SDCK	SDCK				MVDD
J3	MA9	MA9				MVDD
J4	MA0	MA0				MVDD
J5	VDD	VDD				
J9	VSS	VSS				
J10	VSS	VSS				
J11	AVSS3	AVSS3				
J12	IREF2	IREF2				
J16	SBA1	SBA1				HVDD
J17	HVDD	HVDD				
J18	~REQ	~REQ				HVDD
J19	~GNT	~GNT				HVDD
J20	CLK	CLK				HVDD
K1	VCCA	VCCA				
K2	~ROMEN	~ROMEN				MVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
K3	DSF	DSF				MVDD
K4	VCCA	VCCA				
K5	~PME	~PME				HVDD
K9	VSS	VSS				
K10	VSS	VSS				
K11	VSS	VSS				
K12	AVDD3	AVDD3				
K16	SBA0	SBA0				HVDD
K17	VSS	VSS				
K18	~RST	~RST				HVDD
K19	~INTA	~INTA				HVDD
K20	REFCLK	REFCLK				HVDD
L1	MD55	MD55				MVDD
L2	MD56	MD56				MVDD
L3	MD54	MD54				MVDD
L4	VSS	VSS				
L5	VSS	VSS				
L9	**FDATA29**	**RS5**				
L10	**FDATA32**	**RS6**				
L11	**FDATA26**	**RS7**				
L12	CVBS	CVBS	{EXT CLK}			
L16	SB_STB	SB_STB				HVDD
L17	MCKIN/ LVDSCK	MCKIN/ LVDSCK	MCKIN			HVDD
L18	~PDOWN	~PDOWN				HVDD
L19	~CLKRUN/ ACTIVITY	~CLKRUN/ ACTIVITY				HVDD
L20	~EXCKEN	~EXCKEN				HVDD
M1	MD57	MD57				MVDD
M2	MD53	MD53				MVDD
M3	MD58	MD58				MVDD
M4	VCCA	VCCA				
M5	**FDATA47**	**RS3**				
M9	**FDATA31**	**RS8**				
M10	**FDATA33**	**RS9**				
M11	**FDATA28**	**RS10**				
M12	**FDATA25**	**RS11**				
M16	VSS	VSS				
M17	PALCK	PALCK				
			{ZV IN}		{TESTMODE1}	
M18	VREF	VREF	VS		TD19	VPVDD
M19	HREF	HREF	HREF	{External TV encoder}	TD18	VPVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
M20	BLANK	BLANK		TVCLK	TD17	VPVDD
N1	MD52	MD52				MVDD
N2	MD59	MD59				MVDD
N3	MD51	MD51				MVDD
N4	VSS	VSS				
N5	**FDATA46**	**RS4**				
N16	AD_STB0	AD_STB0				HVDD
N17	P4	P4	UV4		TD4	VPVDD
N18	P1	P1	UV1		TD1	VPVDD
N19	P0	P0	UV0		TD0	VPVDD
N20	PCLK	PCLK	PCLK		TD16	VPVDD
P1	MD60	MD60				MVDD
P2	MD50	MD50				MVDD
P3	MD61	MD61				MVDD
P4	MVDD	MVDD				
P5	VSS	VSS				
P16	AD_STB1	AD_STB1				HVDD
P17	Y	Y	{ZV IN}			
P18	P5	P5	UV5		TD5	VPVDD
P19	P3	P3	UV3		TD3	VPVDD
P20	P2	P2	UV2		TD2	VPVDD
R1	MD49	MD49				MVDD
R2	MD62	MD62				MVDD
R3	MD48	MD48				MVDD
R4	~DQM7	~DQM7				MVDD
R5	VCCA	VCCA				
R16	**FDATA36**	**LVDD**				
R17	VPVDD	VPVDD				
R18	P8	P8	Y0		TD8	VPVDD
R19	P7	P7	UV7		TD7	VPVDD
R20	P6	P6	UV6		TD6	VPVDD
T1	MD63	MD63				MVDD
T2	~DQM6	~DQM6	{ROM}			MVDD
T3	MD39	MD39	ROMA7			MVDD
T4	VSS	VSS				
T5	FPVDD	FPVDD				
T6	VCCA	VCCA				
T7	VSS	VSS				
T8	**FDATA45**	**PLLVDD**				
T9	**FDATA44**	**TX3+**				**LVDD**
T10	**FDATA43**	**TXCLK+**				**LVDD**
T11	**FDATA42**	**TXCLK-**				**LVDD**

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
T12	**FDATA41**	**TX2-**				**LVDD**
T13	**FDATA40**	**TX1+**				**LVDD**
T14	**FDATA39**	**TX0+**				**LVDD**
T15	**FDATA38**	**TX0-**				**LVDD**
T16	**FDATA37**	**LVSS**				
T17	C	C	{ZV IN}			
T18	P12	P12	Y4		TD12	VPVDD
T19	P10	P10	Y2		TD10	VPVDD
T20	P9	P9	Y1		TD9	VPVDD
			{ROM}			
U1	MD40	MD40	ROMA8			MVDD
U2	MD38	MD38	ROMA6			MVDD
U3	MD41	MD41	ROMA9			MVDD
U4	MD43	MD43	ROMA11			
U5	MVDD	MVDD				
U6	**FDATA35**	**RS12**	**{DSTN}**			
U7	FDATA22	FDATA22	UD10			FPVDD
U8	**FDATA34**	**PLVSS**				
U9	FPVDD	FPVDD				
U10	**FDATA30**	**TX3-**				**LVDD**
U11	**FDATA27**	**TX2+**				**LVDD**
U12	FPVDD	FPVDD				
U13	**FDATA24**	**TX1-**				**LVDD**
U14	FPVDDEN	FPVDDEN				FPVDD
U15	CVSS	CVSS				
U16	AVSS1	AVSS1	{I2C/DDC}	{USR CFG}		
U17	USR0/SCL	USR0/SCL	SCL (Prim)	USR0		VPVDD
U18	TEST1	TEST1	{ZV IN}		TEST1	VPVDD
U19	P13	P13	Y5		TD13	VPVDD
U20	P11	P11	Y3		TD11	VPVDD
			{ROM}			
V1	MD37	MD37	ROMA5			MVDD
V2	MD42	MD42	ROMA10			MVDD
V3	MD34	MD34	ROMA2			MVDD
V4	MD33	MD33	ROMA1			MVDD
V5	~DQM5	~DQM5	{DSTN}			MVDD
V6	FPSCLK	FPSCLK	XCK			FPVDD
V7	FDATA23	FDATA23	UD11			FPVDD
V8	FDATA19	FDATA19	UD7			FPVDD
V9	FDATA16	FDATA16	UD4			FPVDD
V10	FDATA13	FDATA13	UD1			FPVDD
V11	FDATA8	FDATA8	LD8			FPVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
V12	FDATA5	FDATA5	LD5			FPVDD
V13	FDATA2	FDATA2	LD2			FPVDD
V14	VBIASEN	VBIASEN				FPVDD
V15	CVDD	CVDD				
V16	RVSS	RVSS				
V17	BLUE	BLUE	{I2C/DDC}	{USR CFG}		
V18	USR1/SDA	USR1/SDA	SDA (Prim)	USR1		VPVDD
V19	TEST0	TEST0	{ZV IN}		TEST0	VPVDD
V20	P14	P14	Y6		TD14	VPVDD
			{ROM}			
W1	MD36	MD36	ROMA4			MVDD
W2	MD46	MD46	ROMA14			MVDD
W3	MD45	MD45	ROMA13			MVDD
W4	MD47	MD47	ROMA15			MVDD
				{DSTN}		
W5	LP/FHSYNC	LP/FHSYNC		LP		FPVDD
W6	M/ DE	M/ DE		M/DE		FPVDD
W7	FDATA21	FDATA21		UD9		FPVDD
W8	FDATA18	FDATA18		UD6		FPVDD
W9	FDATA15	FDATA15		UD3		FPVDD
W10	FDATA12	FDATA12		UD0		FPVDD
W11	FDATA9	FDATA9		LD9		FPVDD
W12	FDATA6	FDATA6		LD6		FPVDD
W13	FDATA3	FDATA3		LD3		FPVDD
W14	FDATA0	FDATA0		LD0		FPVDD
W15	CRTHSYNC	CRTHSYNC				VPVDD
W16	**RVDD**	**VDD**				
W17	IREF	IREF				
W18	RED	RED	{ZV IN}			
W19	P15	P15	Y7		TD15	VPVDD
			{I2C/DDC}	{USR CFG}		
W20	USR2	USR2	SCL	USR2/ NTSCPAL		VPVDD
			{ROM}			
Y1	MD35	MD35	ROMA3			MVDD
Y2	MD44	MD44	ROMA12			MVDD
Y3	MD32	MD32	ROMA0			MVDD
Y4	~DQM4	~DQM4		{DSTN}		MVDD
Y5	FP/ FVSYNC	FP/ FVSYNC		FP		FPVDD
Y6	FPEN	FPEN		FPEN		FPVDD
Y7	FDATD20	FDATD20		UD8		FPVDD
Y8	FDATA17	FDATA17		UD5		FPVDD
Y9	FDATA14	FDATA14		UD2		FPVDD

#	SM721 Name	SM722 Name	{Function1}	{Function2}	{Function3}	VDD
Y10	FDATA11	FDATA11		LD11		FPVDD
Y11	FDATA10	FDATA10		LD10		FPVDD
Y12	FDATA7	FDATA7		LD7		FPVDD
Y13	FDATA4	FDATA4		LD4		FPVDD
Y14	FDATA1	FDATA1		LD1		FPVDD
Y15	CRTVSYNC	CRTVSYNC				FPVDD
Y16	CKIN	CKIN				
Y17	AVDD	AVDD				
Y18	GREEN	GREEN				
Y19	AVSS2	AVSS2	{I2C/DDC2}	{USR CFG}		
Y20	USR3	USR3	SDA	USR3/TVONOFF		VPVDD

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