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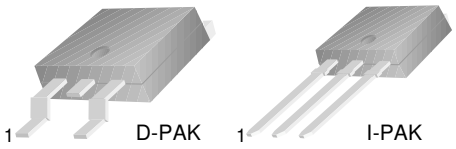
Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

MJD350

High Voltage Power Transistors
D-PAK for Surface Mount Applications

- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I-PAK, "- I" Suffix)



1.Base 2.Collector 3.Emitter

PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	- 300	V
V_{CEO}	Collector-Emitter Voltage	- 300	V
V_{EBO}	Emitter-Base Voltage	- 3	V
I_C	Collector Current (DC)	- 0.5	A
I_{CP}	Collector Current (Pulse)	- 0.75	A
P_C	Collector Dissipation (T_C = 25°C)	15	W
	Collector Dissipation (T_a = 25°C)	1.56	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	- 65 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
V_{CEO}(sus)	* Collector-Emitter Sustaining Voltage	I_C = 1mA, I_B = 0	-300		V
I_{CEO}	Collector Cut-off Current	V_{CB} = -300V, I_E =0		-0.1	mA
I_{EBO}	Emitter Cut-off Current	V_{EB} = -3V, I_C = 0		-0.1	mA
h_{FE}	* DC Current Gain	V_{CE} = -10V, I_C = -50mA	30	240	

* Pulse Test: PW≤300μs, Duty Cycle≤2%

Typical Characteristics

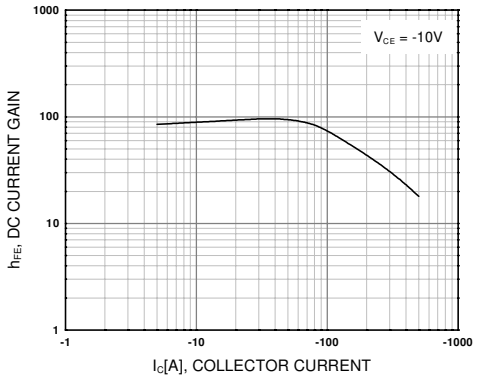


Figure 1. DC current Gain

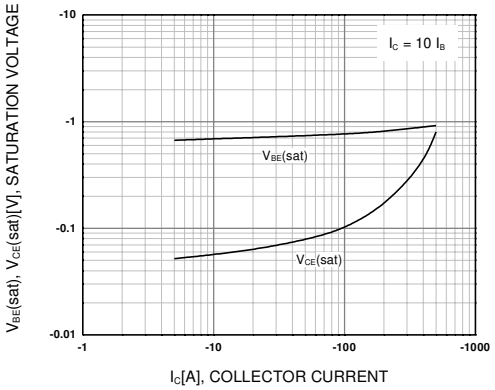


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

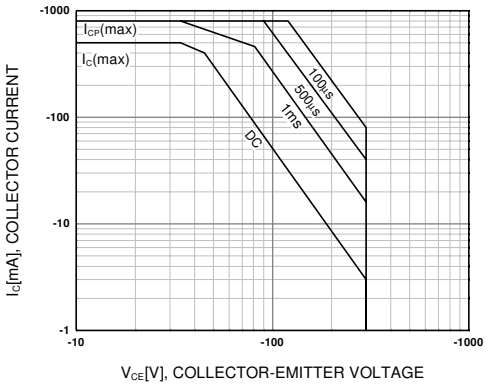


Figure 3. Safe Operating Area

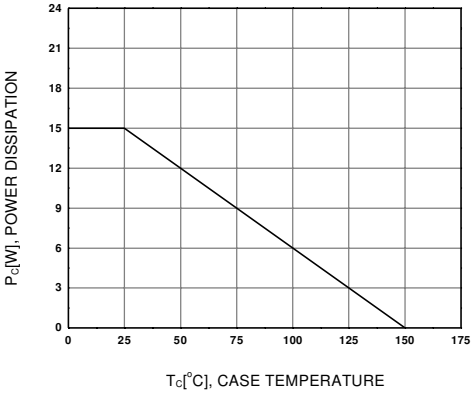
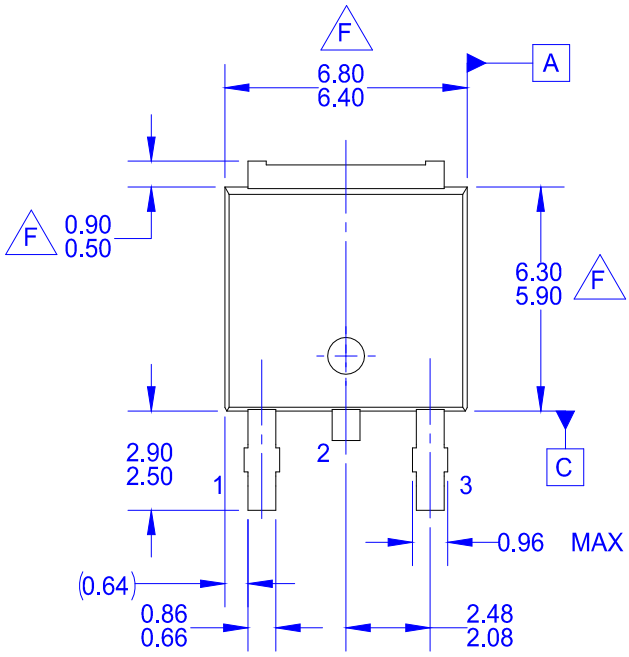
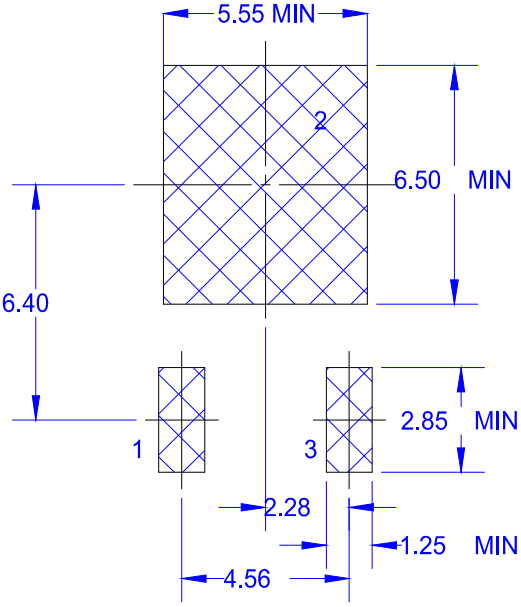
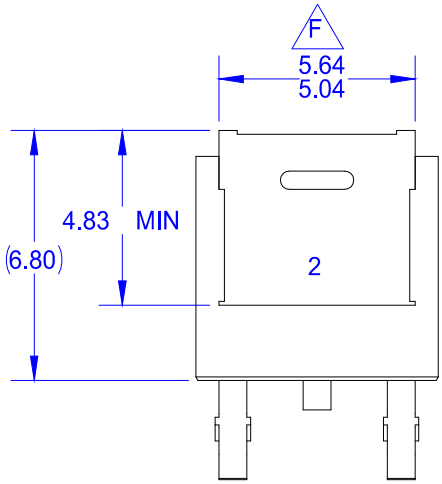


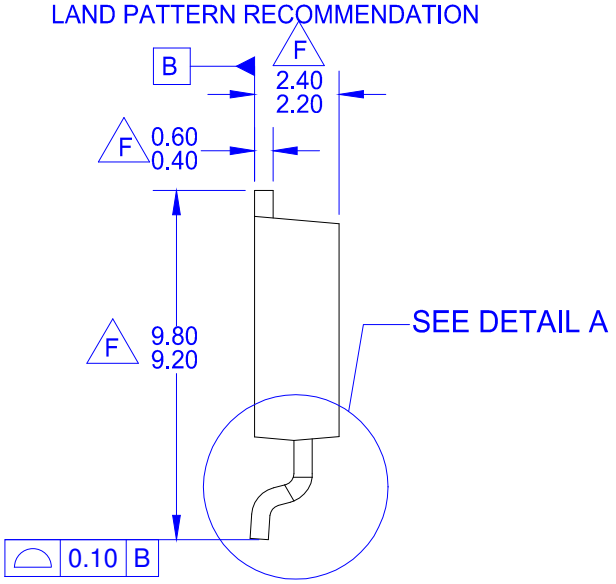
Figure 4. Power Derating

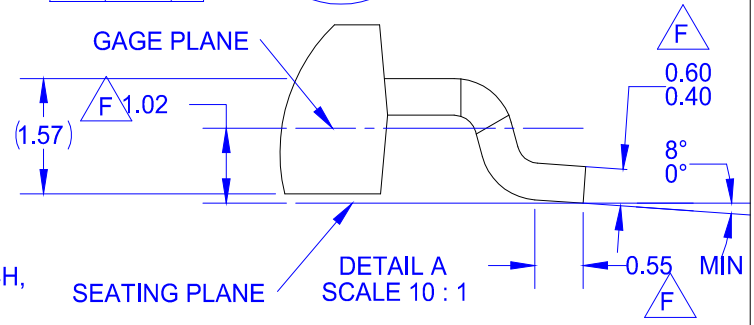




LAND PATTERN RECOMMENDATION







NOTES:UNLESS OTHERWISE SPECIFIED

A) NOT COMPLIANT TO JEDEC TO-252 VARIATION AB
B) ALL DIMENSION ARE IN MILLIMETER
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,MOLD FLASH, AND TIE BAR EXTRUSIONS
D) LAD PATTERN PER IPC7351A ATANDARD TO228P991X239-3N
E) DRAWING FILE NAME:MKT-TO252D03REV4.
F) DOES NOT COMPLY JEDEC STANDARD VALUE.
G) FAIRCHILD SEMICONDUCTOR.

FAIRCHILD

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