

DS92001 3.3V B/LVDS-BLVDS Buffer

Check for Samples: [DS92001](#)

FEATURES

- **Single +3.3 V Supply**
- **Receiver Inputs Accept LVDS/CML/LVPECL Signals**
- **TRI-STATE Outputs**
- **Receiver Input Threshold $\lt; \pm 100\text{ mV}$**
- **Fast Propagation Delay of 1.4 ns (typ)**
- **Low Jitter 400 Mbps Fully Differential Data Path**
- **Compatible with BLVDS 10-bit SerDes (40MHz)**
- **Compatible with ANSI/TIA/EIA-644-A LVDS Standard**
- **Available in SOIC and Space Saving WSON Package**
- **Industrial Temperature Range**

DESCRIPTION

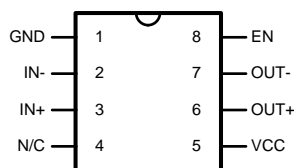
The DS92001 B/LVDS-BLVDS Buffer takes a BLVDS input signal and provides a BLVDS output signal. In many large systems, signals are distributed across backplanes. One of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS92001 has edge transitions optimized for multidrop backplanes where the switching frequency is in the 200 MHz range or less. The output edge rate is critical in some systems where long stubs may be present, and utilizing a slow transition allows for longer stub lengths.

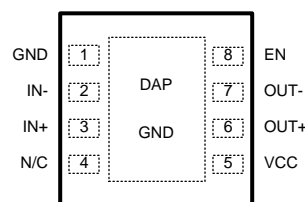
The DS92001, available in the WSON package, will allow the receiver inputs to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range allows the DS92001 to receive differential signals from LVPECL, CML as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-BLVDS or CML-BLVDS translator.

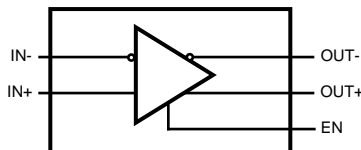
Connection and Block Diagrams



**Figure 1. SOIC Package Number D0008A
Top View**



**Figure 2. WSON Package Number NGK0008A
Top View**



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Table 1. Functional Operation

| BLVDS Inputs [IN+] – [IN-] | BLVDS Outputs | |
|-------------------------------|---------------|-----------|
| | OUT+ | OUT- |
| $VID \geq 0.1V$ | H | L |
| $VID \leq -0.1V$ | L | H |
| $-0.1V \leq VID \leq 0.1V$ | Undefined | Undefined |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | | |
|---|---------------------|------------------------------|
| Supply Voltage (V_{CC}) | | -0.3V to +4V |
| LVC MOS/LVTTL Input Voltage (EN) | | -0.3V to ($V_{CC} + 0.3V$) |
| B/LVDS Receiver Input Voltage (IN+, IN-) | | -0.3V to +4V |
| BLVDS Driver Output Voltage (OUT+, OUT-) | | -0.3V to +4V |
| BLVDS Output Short Circuit Current | | Continuous |
| Junction Temperature | | +150°C |
| Storage Temperature Range | | -65°C to +150°C |
| Lead Temperature Range Soldering (4 sec.) | | +260°C |
| Maximum Package Power Dissipation at 25°C | D Package | 726 mW |
| | Derate D Package | 5.8 mW/°C above +25°C |
| | NGK Package | 2.44 W |
| | Derate NGK Package | 19.49 mW/°C above +25°C |
| ESD Ratings | (HBM, 1.5kΩ, 100pF) | ≥2.5kV |
| | (EIAJ, 0Ω, 200pF) | ≥250V |

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

| | Min | Typ | Max | Units |
|---|-----|-----|-----|-------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Receiver Differential Input Voltage (V_{ID}) with $V_{CM}=1.2V$ | 0.1 | | 2.4 | V |
| Operating Free Air Temperature | -40 | +25 | +85 | °C |
| B/LVDS Input Rise/Fall 20% to 80% | | 2 | 20 | ns |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|------------------------------|------|--|-------|
| LVC MOS/LVTTL DC SPECIFICATIONS (EN) | | | | | | |
| V _{IH} | High Level Input Voltage | | 2.0 | | V _{CC} | V |
| V _{IL} | Low Level Input Voltage | | GND | | 0.8 | V |
| I _{IH} | High Level Input Current | V _{IN} = V _{CC} or 2.0V | | +7 | +20 | μA |
| I _{IL} | Low Level Input Current | V _{IN} = GND or 0.8V | -10 | ±1 | +10 | μA |
| V _{CL} | Input Clamp Voltage | I _{CL} = -18 mA | | -0.6 | -1.5 | V |
| BLVDS OUTPUT DC SPECIFICATIONS (OUT) | | | | | | |
| V _{OD} | Differential Output Voltage ⁽¹⁾ | R _L = 27Ω | 250 | 350 | 500 | mV |
| | | R _L = 50Ω | 350 | 450 | 600 | mV |
| ΔV _{OD} | Change in Magnitude of V _{OD} for Complimentary Output States | R _L = 27Ω or 50Ω See Figure 3 and Figure 4 | | | 20 | mV |
| V _{OS} | Offset Voltage | R _L = 27Ω or R _L = 50Ω | 1.1 | 1.25 | 1.375 | V |
| ΔV _{OS} | Change in Magnitude of V _{OS} for Complimentary Output States | See Figure 3 | | 2 | 20 | mV |
| I _{OZ} | Output TRI-STATE Current | EN = 0V, V _{OUT} = V _{CC} or GND | -20 | ±5 | +20 | μA |
| I _{OFF} | Power-Off Leakage Current | V _{CC} = 0V or Open Circuit, V _{OUT} = 3.6V | -20 | ±5 | +20 | μA |
| I _{OS1} | Output Short Circuit Current ⁽³⁾ | EN = V _{CC} , V _{CM} = 1.2V, V _{ID} = 200mV, V _{OUT+} = 0V, or V _{ID} = -200mV, V _{CM} = 1.2V, V _{OUT-} = 0V | | -30 | -60 | mA |
| | | V _{ID} = -200mV, V _{CM} = 1.2V, V _{OUT+} = V _{CC} , or V _{ID} = 200mV, V _{CM} = 1.2V, V _{OUT-} = V _{CC} | | 53 | 80 | mA |
| I _{OSD} | Differential Output Short Circuit Current ⁽³⁾ | EN = V _{CC} , V _{ID} = 200mV , V _{CM} = 1.2V, V _{OD} = 0V (connect true and complement outputs through a current meter) | | 30 | 42 | mA |
| B/LVDS RECEIVER DC SPECIFICATIONS (IN) | | | | | | |
| V _{TH} | Differential Input High Threshold ⁽⁴⁾ | V _{CM} = +0.05V, +1.2V or +3.25V | | -30 | -5 | mV |
| V _{TL} | Differential Input Low Threshold ⁽⁴⁾ | | -70 | -30 | | mV |
| V _{CMR} | Common Mode Voltage Range ⁽⁴⁾ | | V _{ID} /2 | | V _{CC} - V _{ID} /2 | V |
| I _{IN} | Input Current | V _{IN} = V _{CC} | V _{CC} = 3.6V or 0V | 1.5 | 20 | μA |
| | | V _{IN} = 0V | | 1.5 | 20 | μA |
| ΔI _{IN} | Change in Magnitude of I _{IN} | V _{IN} = V _{CC} | | 1 | 6 | μA |
| | | V _{IN} = 0V | | 1 | 6 | μA |
| SUPPLY CURRENT | | | | | | |
| I _{CCD} | Total Dynamic Supply Current (includes load current) | EN = V _{CC} , R _L = 27Ω or 50Ω, C _L = 15 pF, Freq. = 200MHz 50% duty cycle, V _{ID} = 200mV, V _{CM} = 1.2V | | 50 | 65 | mA |
| I _{CCZ} | TRI-STATE Supply Current | EN = 0V, Freq. = 200MHz 50% duty cycle, V _{ID} = 200mV, V _{CM} = 1.2V | | 36 | 46 | mA |

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID}, V_{OD}, V_{TH}, V_{TL}, and ΔV_{OD}. V_{OD} has a value and direction. Positive direction means OUT+ is a more positive voltage than OUT-.
- (2) All typical are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
- (3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.
- (4) The parameters are specified by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|---|-------|-----|-----|-------|
| LVDS OUTPUT AC SPECIFICATIONS (OUT) | | | | | | |
| t_{PHLD} | Differential Propagation Delay High to Low ⁽²⁾ | $V_{ID} = 200\text{mV}$, $V_{CM} = 1.2\text{V}$, $R_L = 27\Omega$ or 50Ω , $C_L = 15\text{pF}$ See Figure 5 and Figure 6 | 1.0 | 1.4 | 2.0 | ns |
| t_{PLHD} | Differential Propagation Delay Low to High ⁽²⁾ | | 1.0 | 1.4 | 2.0 | ns |
| t_{SKD1} | Pulse Skew $ t_{PLHD} - t_{PHLD} $ (measure of duty cycle) ⁽³⁾⁽⁴⁾ | | 0 | 20 | 200 | ps |
| t_{SKD3} | Part-to-Part Skew ⁽³⁾⁽⁵⁾ | | 0 | 200 | 300 | ps |
| t_{SKD4} | Part-to-Part Skew ⁽³⁾⁽⁶⁾ | | 0 | | 1 | ns |
| t_{LHT} | Rise Time ⁽³⁾⁽²⁾ 20% to 80% points | $R_L = 50\Omega$ or 27Ω , $C_L = 15\text{pF}$ See Figure 5 and Figure 7 | 0.350 | 0.6 | 1.0 | ns |
| t_{HLT} | Fall Time ⁽³⁾⁽²⁾ 80% to 20% points | | 0.350 | 0.6 | 1.0 | ns |
| t_{PHZ} | Disable Time (Active High to Z) | $R_L = 50\Omega$, $C_L = 15\text{pF}$ See Figure 8 and Figure 9 | | 3 | 25 | ns |
| t_{PLZ} | Disable Time (Active Low to Z) | | | 3 | 25 | ns |
| t_{PZH} | Enable Time (Z to Active High) | | | 100 | 120 | ns |
| t_{PZL} | Enable Time (Z to Active Low) | | | 100 | 120 | ns |
| t_{DJ} | LVDS Data Jitter, Deterministic (Peak-to-Peak) ⁽⁷⁾ | $V_{ID} = 300\text{mV}$; PRBS = $2^{23} - 1$ data; $V_{CM} = 1.2\text{V}$ at 400Mbps (NRZ) | | | 78 | ps |
| t_{RJ} | LVDS Clock Jitter, Random ⁽⁷⁾ | $V_{ID} = 300\text{mV}$; $V_{CM} = 1.2\text{V}$ at 200MHz clock | | | 36 | ps |
| f_{MAX} | Maximum specified frequency ⁽⁸⁾ | $V_{ID} = 200\text{mV}$, $V_{CM} = 1.2\text{V}$ | 200 | 300 | | MHz |

- (1) All typical are given for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, unless otherwise stated.
- (2) Propagation delay, rise and fall times are specified by design and characterization to 200MHz. Generator for these tests: $50\text{MHz} \leq f \leq 200\text{MHz}$, $Z_o = 50\Omega$, $t_r, t_f \leq 0.5\text{ns}$. Generator used was HP8130A (300MHz capability).
- (3) The parameters are specified by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.
- (4) t_{SKD1} ; $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel (a measure of duty cycle).
- (5) t_{SKD3} ; Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range. This parameter specified by design and characterization.
- (6) t_{SKD4} ; Part to Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as $|Max - Min|$ differential propagation delay.
- (7) The parameters are specified by design. The limits are based on statistical analysis of the device performance over the PVT range with the following test equipment setup: Agilent 86130A used as stimulus, 5 feet of RG142B cable with DUT test board and Agilent 86100A (digital scope mainframe) with Agilent 86122A (20GHz scope module). Data input jitter pk to pk = 22 picoseconds; Clock input jitter = 24 picoseconds; t_{DJ} measured 100 picoseconds, t_{RJ} measured 60 picoseconds.
- (8) f_{MAX} test: Generator (HP8133A or equivalent), Input duty cycle = 50%. Output criteria: $V_{OD} \geq 200\text{mV}$, Duty Cycle better than 45/55%. This specification is specified by design and characterization. A minimum is specified, which means that the device will operate to specified conditions from DC to the minimum specified AC frequency. The typical value is always greater than the minimum specification.

DC Test Circuits

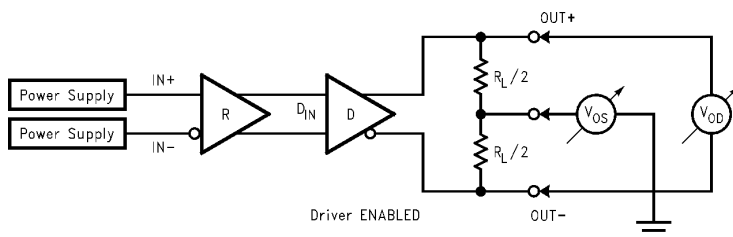


Figure 3. Differential Driver DC Test Circuit

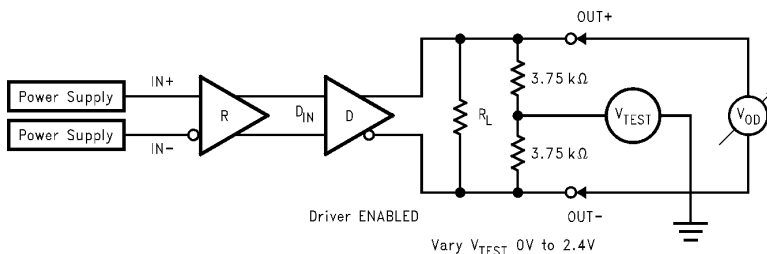


Figure 4. Differential Driver Full Load DC Test Circuit

AC Test Circuits and Timing Diagrams

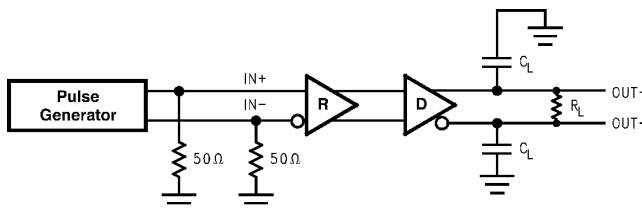


Figure 5. BLVDS Output Load

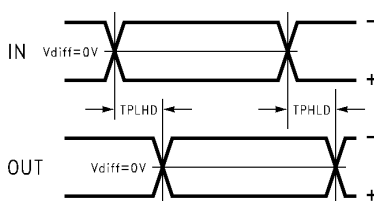


Figure 6. Propagation Delay Low-to-High and High-to-Low

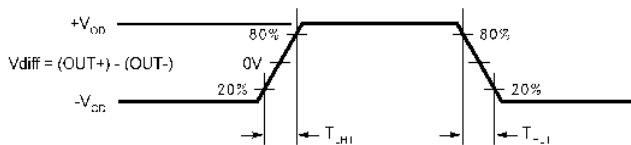


Figure 7. BLVDS Output Transition Time

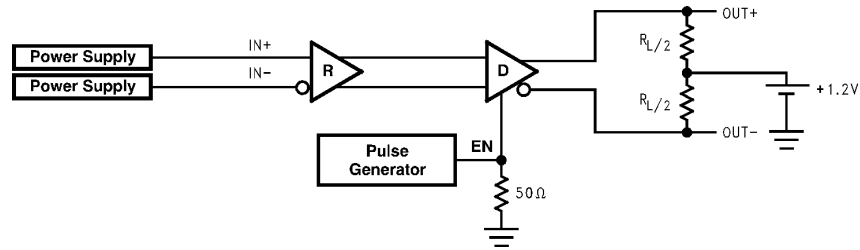


Figure 8. TRI-STATE Delay Test Circuit

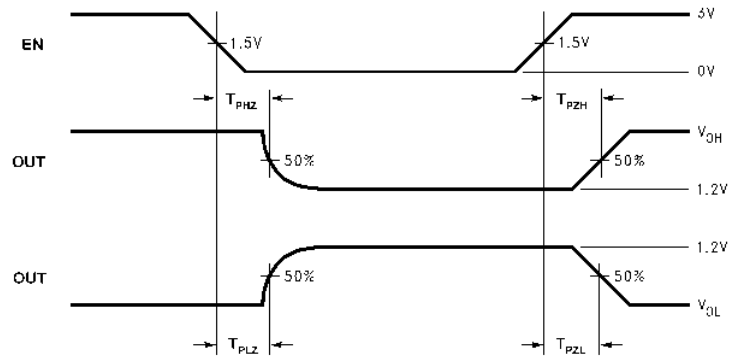


Figure 9. Output active to TRI-STATE and TRI-STATE to active output time

PIN DESCRIPTIONS

| Pin Name | Pin # | Input/Output | Description |
|-----------------|-------|--------------|---|
| GND | 1 | P | Ground |
| IN - | 2 | I | Inverting receiver B/LVDS input pin |
| IN+ | 3 | I | Non-inverting receiver B/LVDS input pin |
| N/C | 4 | NA | "NO CONNECT" pin |
| V _{CC} | 5 | P | Power Supply, 3.3V ± 0.3V. |
| OUT+ | 6 | O | Non-inverting driver BLVDS output pin |
| OUT - | 7 | O | Inverting driver BLVDS output pin |
| EN | 8 | I | Enable pin. When EN is LOW, the driver is disabled and the BLVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL levels. |
| GND | DAP | P | WSON Package Ground |

Typical Applications

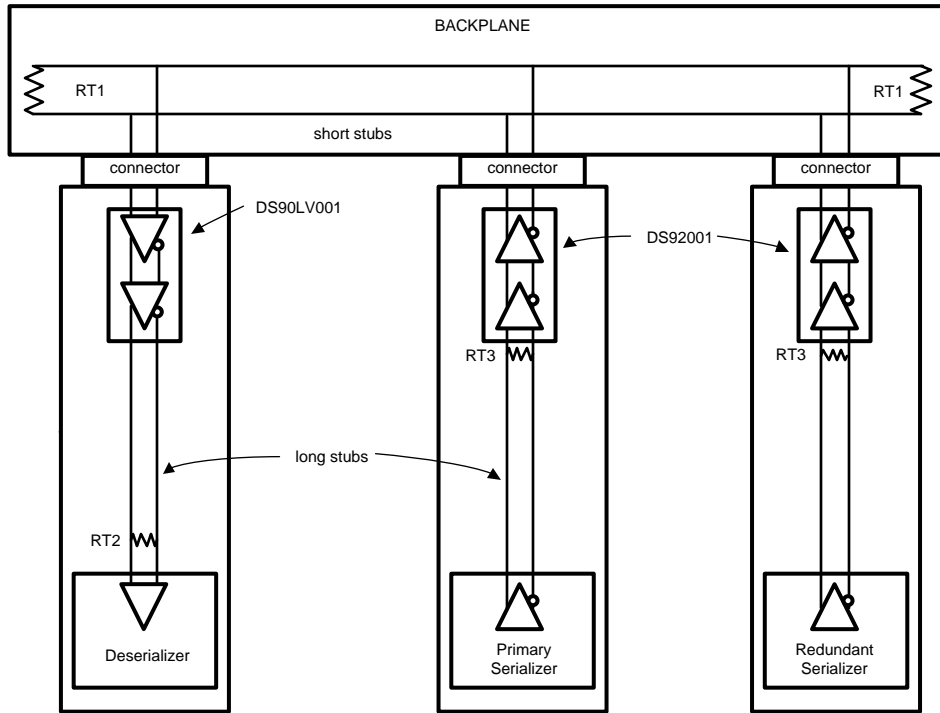


Figure 10. Backplane Stub-Hider Application

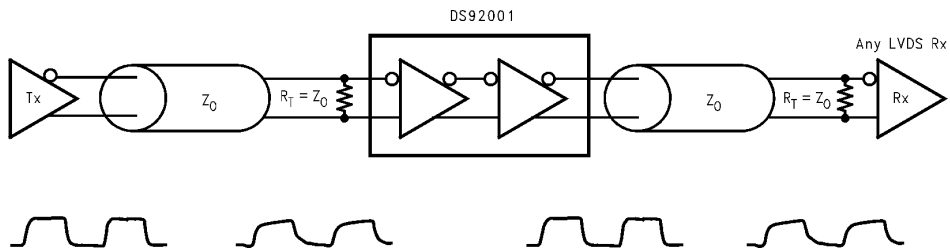


Figure 11. Cable Repeater Application

APPLICATION INFORMATION

The DS92001 can be used as a "stub-hider." In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on the individual cards. See [Figure 10](#). Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the designer would like. The DS92001, available in the WSON package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS92001. This very small WSON package is a 75% space savings over the SOIC package.

The DS92001 may also be used as a repeater as shown in [Figure 11](#). The signal is recovered and redriven at full strength down the following segment. The DS92001 may also be used as a level translator, as it accepts LVDS, BLVDS, and LVPECL inputs.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 μ F and 0.01 μ F capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 μ F (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

For PC board considerations for the WSON package, please refer to application note AN-1187 "Leadless Leadframe Package" (Literature Number SNOA401). It is important to note that to optimize signal integrity (minimize jitter and noise coupling), the WSON thermal land pad, which is a metal (normally copper) rectangular region located under the package as seen in [Figure 12](#), should be attached to ground and match the dimensions of the exposed pad on the PCB (1:1 ratio).

Top View

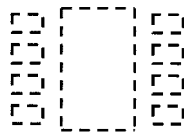


Figure 12. WSON Thermal Land Pad and Pin Pads

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω for point-to-point links. Multidrop (driver in the middle) or multipoint configurations are typically terminated at both ends. The termination value may be lower than 100Ω due to loading effects and in the 50Ω to 100Ω range. Remember that the current mode outputs need the termination resistor to generate the differential voltage.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

REVISION HISTORY

| Changes from Revision E (April 2013) to Revision F | Page |
|--|-------------------|
| • Changed layout of National Data Sheet to TI format | 9 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DS92001TLD/NOPB | ACTIVE | WSON | NGK | 8 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | 92001 | Samples |
| DS92001TMA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | 92001 TMA | Samples |
| DS92001TMAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | 92001 TMA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

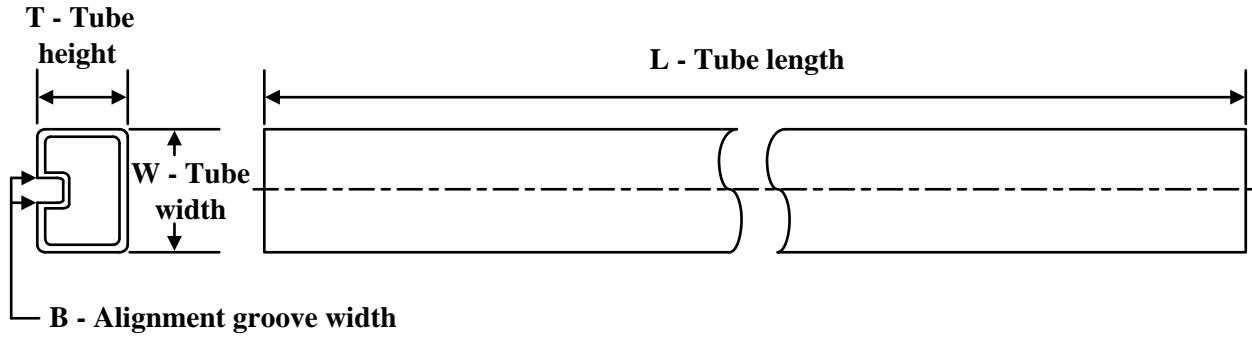

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS92001TLD/NOPB | WSON | NGK | 8 | 1000 | 178.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q1 |
| DS92001TMAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

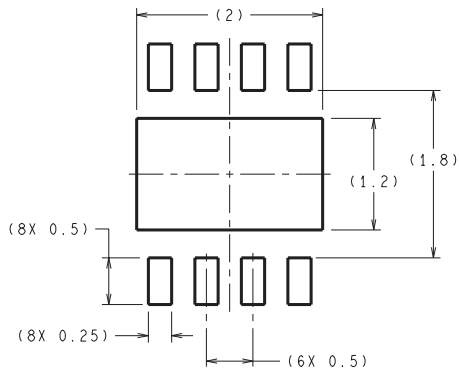
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS92001TLD/NOPB | WSON | NGK | 8 | 1000 | 367.0 | 367.0 | 35.0 |
| DS92001TMAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

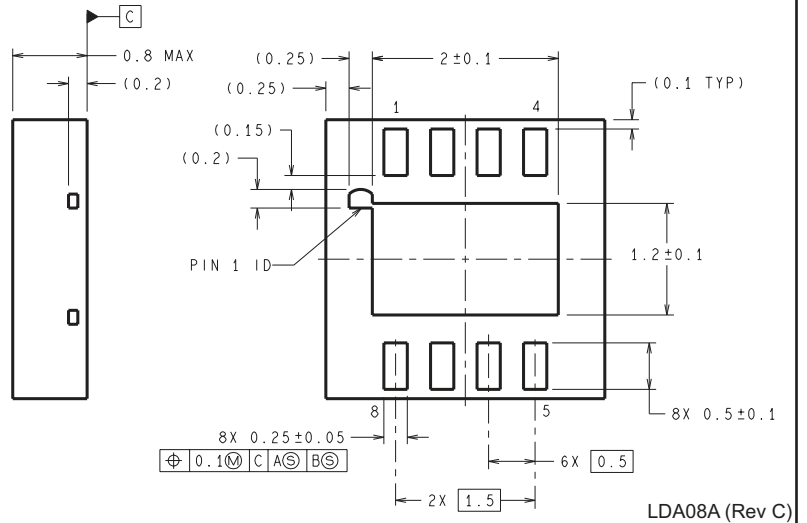
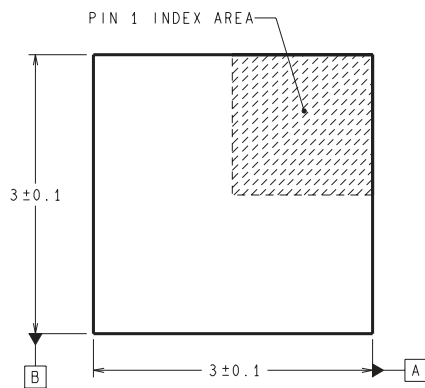
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DS92001TMA/NOPB | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |

NGK0008A



DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



LDA08A (Rev C)



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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