Murata Power Solutions

D1U54-D-450-12-HxxC Series

54mm 1U Front End DC-DC Power Supply Converter

FEATURES

- 450W output power
- 93% efficiency at 50% load
- 12Vdc main output
- 5Vdc standby output options
- <1U height:
  54.5mm x 228.6mm x 40mm
  (2.15" x 9.0" x 1.57")
- Card Edge DC Output and Signal I/O Connector
- DC Input Terminal Block
- 14.8 Watts per cubic inch power density
- N+1 redundancy capable, including hot plugging
- Active (digital) current sharing on 12Vdc main output; ORING FET are included for both standby and main outputs
- Overvoltage, Overcurrent, Overtemperature protection
- Internal cooling fan (variable speed)
- PMBus™/I2C interface with status indicators
- RoHS compliant
- Two Year Warranty

RoHS COMPLIANT

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For full details go to
www.murata-ps.com/rohs

PMBus

PRODUCT OVERVIEW

The D1U54-D-450-12-HxxC series power modules are very high efficiency, 450 watt DC input front end supplies, with a 12Vdc main output and a standby output. An active (digital) current share characteristic is provided to allow units to operate in parallel and share load current. The power supply may be hot plugged; recovers from overtemperature faults, and has status LEDs on the front panel in addition to hardware signal logic and PMBus™ status signals. The low profile 1U package and 14.8W/cubic inch power density make them ideal for delivering reliable, efficient power to networking equipment, workstations, storage systems and other 12Vdc distributed power architectures.

These models are intended to complement the appropriate D1U54P-W-450-12-HxxC AC input variant.

ORDERING GUIDE

Part Number	Murata Internal Part Number	Power Output -48 to -60Vdc	Main Output	Standby Output	Airflow
D1U54-D-450-12-HA3C	M1920	450W	12Vdc	5Vdc	Front to Back
D1U54-D-450-12-HA4C	M1919			5Vdc	Back to front

INPUT CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Units
DC Input Voltage Operating Range		-44	-53	-72	Vdc
Turn-on Input Voltage	Ramp Up	-40.5	-43	-43.5	
Turn-off Input Voltage	Ramp Down	-36.5	-38	-39.5	
Input Current @ VIN = -53Vdc	450W		9.5		Adc
DC Input Inrush Peak Current	Cold start (25°C) between 0 to 200ms			25	Apk
Efficiency (-54Vdc)	20% FL		89		%
	50% FL		93		
	100% FL		90		
Reverse polarity protection	Reversed input cables; no internal/external fuse failure	+40		+72	Vdc

OUTPUT VOLTAGE CHARACTERISTICS

Nominal Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
Main 12Vdc	Output Set Point Accuracy	50% load; Tamb = 25C	11.96	12.00	12.04	Vdc
	Line & Load Regulation	Combined regulation	-2.0%		+2.0%	
	Ripple & Noise[1,2]	20MHz Bandwidth			120	mV P-P
	Output Current	-40Vdc to -72Vdc DC input	0		37.5A	A
	Load Capacitance		500		4000	µF
5VSB	Voltage Set Point			5.0		Vdc
	Line & Load Regulation		4.76		5.24	
	Ripple Voltage & Noise[1,2]	20MHz Bandwidth			120	mV P-P
	Output Current		0		2	A
	Load Capacitance		0		3000	µF

[1] Ripple and noise are measured at the output connector, with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. A short coaxial cable to the measurement 'scope input, is used.

[2] Measurements assume the use of the minimum load capacitance as specified for the main 12Vdc output and a minimum load of 5%. Below 5% loading the overall voltage deviation shall be within ±2.5%.

Certificate and Test Report

OUTPUT CHARACTERISTICS

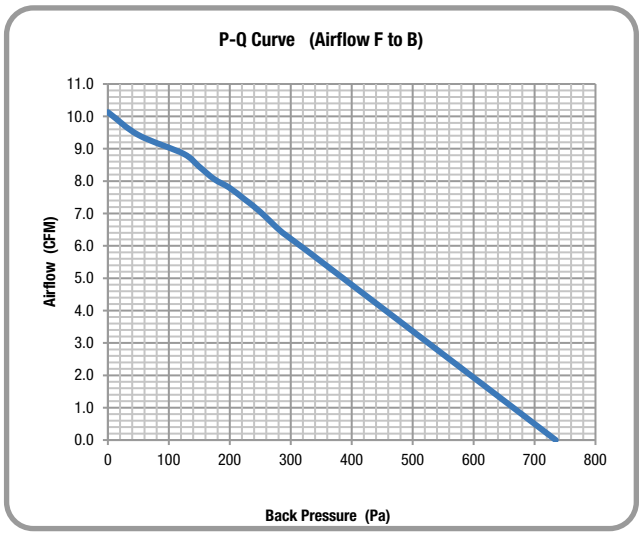
Parameter	Conditions	Min.	Typ.	Max.	Units
Startup Time	AC ramp up			3	s
Transient Response	Main 12V, 50% load step, 1A/µs di/dt			5	%
	Standby output, 50% load step, 1A/µs di/dt			500	µs
Current sharing accuracy (Main 12Vdc output)	>10% load; (* percentage of full load)			±5*	%
Hot Swap Transients				±5	%
Holdup Time (Total Effective Hold Up - See Timing Waveforms)	Full DC Input Source Range; 100% load	2		-	ms

ENVIRONMENTAL CHARACTERISTICS

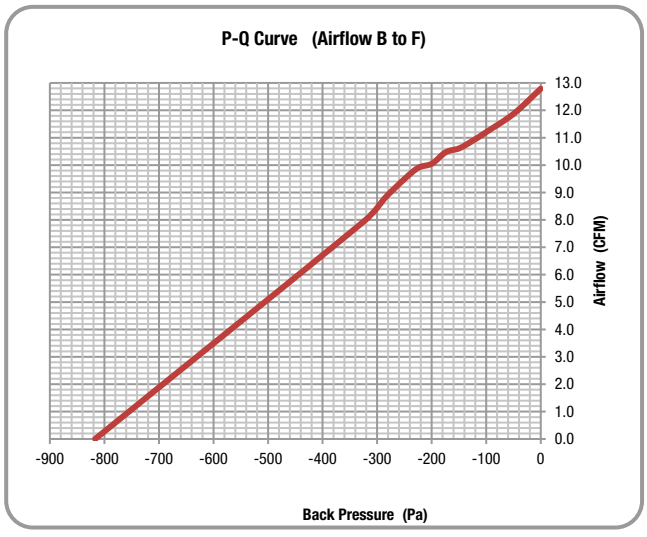
Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature Range		-40		70	°C
Operating Temperature Range	-40 to -72Vdc, 450W	-5		50	
Operating Humidity	Noncondensing; +45°C	5		90	%
Storage Humidity		5		95	
Altitude (without derating at 40°C)				3000	m
Shock	30G non-operating				
Operational Vibration	Sine sweep; 5-200Hz, 2G; random vibration, 5-500Hz, 1.11G				
MTBF (Target)	Per Telcordia SR-332 Issue 3 M1C3 at 40°C		620K		hrs
Safety Approval Standards	CAN/CSA C22.2 No 60950-1:2007 + A2:2014 UL 60950-1:2014 IEC60950-1:2005 +A2:2013 EN 60950-1:2006+A2:2013 CCC: GB4943.1-2011; GB/T9254-2008; GB17625.1-2012				
Input Fuse	Power Supply has internal 25A/250V fast blow fuse on the DC input negative line				
Weight	1.51 lbs (0.684 kg)				

TYPICAL AIRFLOW; PRESSURE VS. FLOW (PQ) CURVES

D1U54-D-450-12-Hx3C



D1U54-D-450-12- Hx4C



Notes:
1. The above curves represent provisional performance based upon a similar product using a 20mm thickness fan; these curves will be updated on later revisions of this datasheet.
2. Curves recorded at room ambient (circa 25°C).
3. Curves generated with intermal fan running at 100% duty cycle while variying back pressure.

PROTECTION CHARACTERISTICS

Output	Parameter	Conditions	Min.	Typ.	Max.	Units
	Overtemperature (intake)[1]	Autorestart with 4°C hysteresis for recovery (warning issued at 70°C)		75		°C
12V	Overvoltage	Latching	13.5		14.5	Vdc
	Overcurrent (target)	The output shall shutdown when an overcurrent condition is detected. It will auto restart after 1sec; however if the overcurrent condition is redetected the output will once again shutdown. The output will once again re-start, however if the overcurrent condition persists it will latch of after the fifth unsuccessful attempt. To reset the latch it will be necessary to toggle the PS_ON_L signal or recycle the incoming DC source.	38		47	Adc
5VSB	Overvoltage	Latching	5.4		6.0	Vdc
	Overcurrent	The output shall shutdown when an overcurrent is detected. It will auto restart after 2sec; however if the overcurrent is re-detected the output will once again shutdown. This cycle will occur indefinitely while the overcurrent condition persists.	2.2		3.5	Adc

[1]As measured by the internal intake air temperature sensor;

ISOLATION CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Insulation Safety Rating/Test Voltage	Input to Output - Reinforced	1000			Vdc
Isolation	Output to Chassis	500			Vdc

EMISSIONS AND IMMUNITY

Characteristic	Standard	Compliance
Input Current Harmonics	IEC/EN 61000-3-2	Complies
Voltage Fluctuation and Flicker	IEC/EN 61000-3-3	Complies
Conducted Emissions	FCC 47 CFR Part 15 CISPR 22/EN55022	Class A with 6dB margin
ESD Immunity	IEC/EN 61000-4-2	Level 4 criteria A
Radiated Field Immunity	IEC/EN 61000-4-3	Level 3 criteria B
Electrical Fast Transients/Burst Immunity	IEC/EN 61000-4-4	Level 3 criteria A
Surge Immunity	IEC/EN 61000-4-5	Level 3, Criteria A (normal performance), common mode 2kV 12ohm, differential mode 1kV 2ohms
RF Conducted Immunity	IEC/EN 61000-4-6	Level 3 criteria A
Magnetic Field Immunity	IEC/EN 61000-4-8	3 A/m criteria B
Voltage Dips and Interruptions – Target (TBC)	-----	-53Vin, 80% load, Dip 100% Duration 4ms; Performance Criteria A (normal performance maintained)

STATUS INDICATORS AND CONTROL SIGNALS

INPUT LED

Condition	LED Status
Input Voltage Present	Solid Green
Input Voltage fault or warning	Blinking Green
Input off	Off

POWER LED

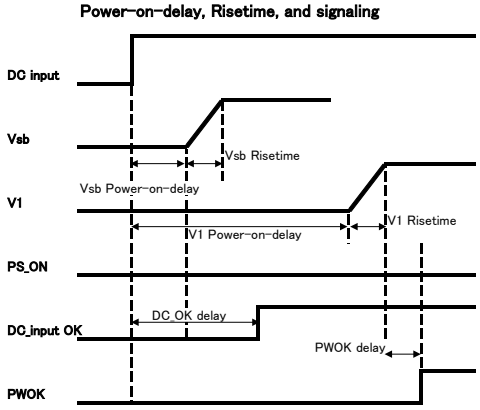
Condition	LED Status
Output Fault indication concurrent PMBus Status_x registers	Solid Amber
Output Warning, indication, concurrent PMBus Status_x registers	Blinking Amber
Standby, 12Vdc Main output off, Vstby On	Blinking Green
Power Good 12Vdc Main output on, Vstby On	Solid Green
Power Off 12Vdc Main output off, Vstby Off	Off

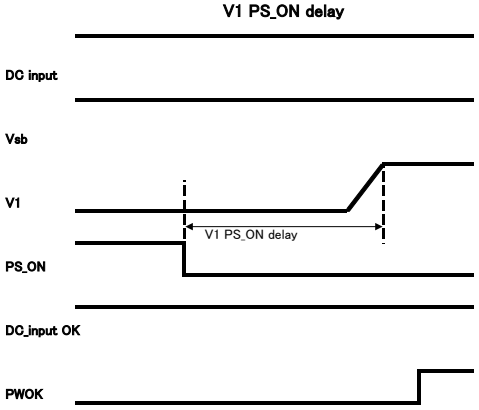
STATUS AND CONTROL SIGNALS			
Signal Name	I/O	Description	Interface Details
INPUT_OK (DC Source)	Output	The signal output is driven high when input source is available and within acceptable limits. The output is driven low to indicate loss of input power. There is a minimum of 1ms pre-warning time before the signal is driven low prior to the PWR_OK signal going low. The power supply must ensure that this interface signal provides accurate status when DC input power is lost.	Pulled up internally via 10K to V_{DD}*. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
PW_OK (Output OK)	Output	The signal is asserted, driven high, by the power supply to indicate that all outputs are valid. If any of the outputs fail then this output will be hi-Z or driven low. The output is driven low to indicate that the Main output is outside of lower limit of regulation.	Pulled up internally via 10K to V_{DD}*. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
SMB_ALERT (FAULT/WARNING)	Output	The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed.	Pulled up internally via 10K to V_{DD}*. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
PRESENT_L (Power Supply Absent)	Output	The signal is used to detect the presence (installation) of a PSU by the host system. The signal is connected to PSU logic +VSB_Return within the power module.	Passive connection to +VSB_Return. A logic low <0.8Vdc
PS_ON (Power Supply Enable/Disable	Input	This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +VSB_Return. In the low state the signal input shall not source more than 1mA of current. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions.	Pulled up internally via 10K to V_{DD}*. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
PS_KILL	Input	This signal is used during hot swap to disable the main output during hot swap extraction. The input is pulled up internally to V_{DD}* (within the power supply). The signal is provided on a short (lagging pin) and should be connected to +VSB_Return.	Pulled up internally via 10K to V_{DD}*. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
ADDR (Address Select)	Input	An analog input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications. Connection of a suitable resistor to +VSB_Return, in conjunction with an internal resistor divider chain, will configure the required address (see ADDR Address Selection: #ADDRSelect)	DC voltage between the limits of 0 and +3.3Vdc.
SCL (Serial Clock)	Both	A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	V_{IL} is 0.8V maximum V_{OL} is 0.4V maximum when sinking 3mA V_{IH} is 2.1V minimum
SDA (Serial Data)	Both	A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	V_{IL} is 0.8V maximum V_{OL} is 0.4V maximum when sinking 3mA V_{IH} is 2.1V minimum
V1_SENSE V1SENSE_RTN	Input	Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required then the voltage can be configured for local sense by: 1. V1_SENSE directly connected to power gold fingers P9-P16 (inclusive) 2. V1_SENSE_RTN directly connected to gold fingers P1 to P8 (inclusive)	Compensation for a up to 0.12Vdc total connection drop (output and return connections).
ISHARE	Bi-Directional Digital Bus	The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit).	Analogue voltage: +8V maximum; 10K to +12V_RTN

*VDD is an internal voltage rail derived from VSB and an internal housekeeping rail ("diode ORed") and is compatible with the voltage tolerances of VSB).

TIMING SPECIFICATIONS

Turn-On Delay & Output Rise Time:



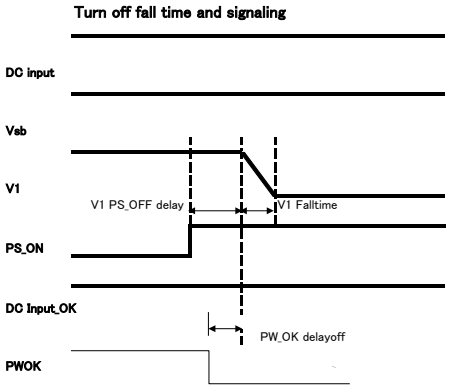


1. The turn-on delay after application of DC input within the operating range shall as defined in the following tables.
2. The output rise times shall be measured from 10% of the nominal output to the lower limit of the regulation band as defined in the following tables.

Time	Min	Max
Vsb Rise time	2ms	170ms
V1 Rise time	10ms	220ms
Vsb Power-on-delay	300ms	1600ms
V1 Power-on-delay	400ms	2000ms
V1 PS_ON delay	100ms	300ms
V1 PWOK delay	300ms	450ms
DCOK (Input) detect	270ms	1000ms

TIMING SPECIFICATIONS

Turn-Off (Shutdown by PS_ON)

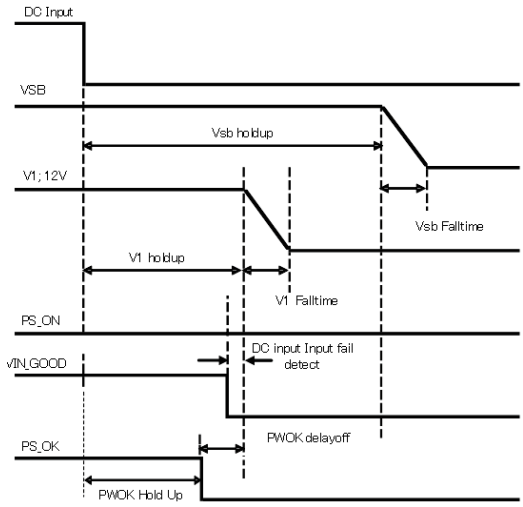


Turn-Off Timing	Min	Max	Notes
V1 Fall time	-	-	Must be monotonic
V1 PS_OFF delay	0ms	6.0ms	
PW_OK delay off	1.2ms		

1. Note this characteristic is applicable for the main 12Vdc output shutdown from PS_ON pulled high.

TIMING SPECIFICATIONS

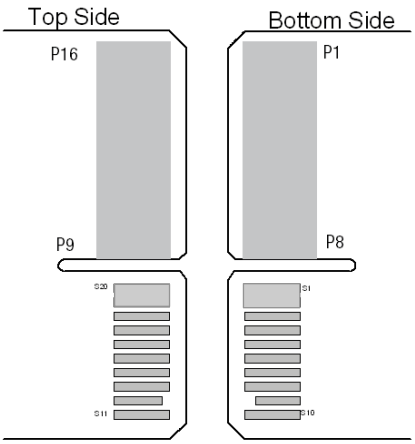
Power Removal Holdup



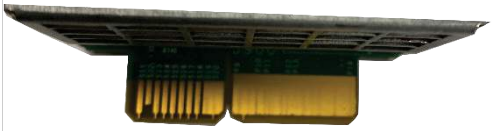
Power Removal Timing	Min	Max	Notes
Vsb holdup	17ms	50ms	+VSB Full Load
V1 holdup (Total Effective)	1.8ms	-	100% load
DC (Input) fail detect	400µs	1ms	
PWOK delay off	1.0ms		100% load
PWOK Hold Up	0.8ms		

OUTPUT CONNECTOR & SIGNAL INTERFACE

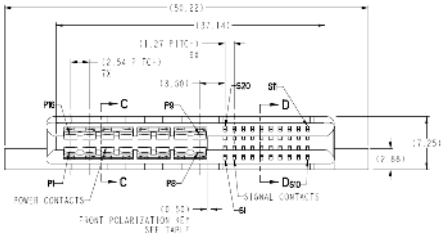
Gold Finger Layout & Pin Assignment Map	Photos	Mating Connector: FCI 10126933080820xALF; "Straddle" Connector



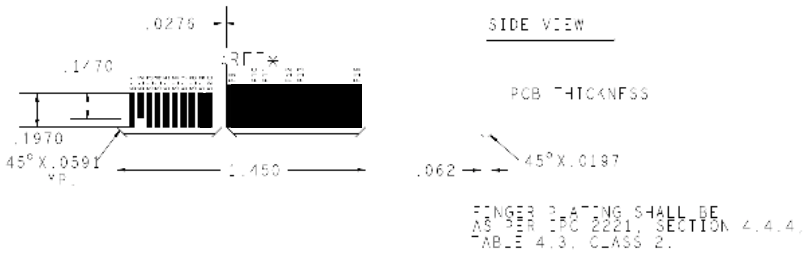
Top View



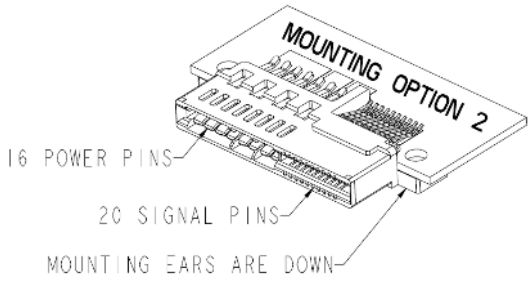
Bottom View



Note: Gold Fingers S9 (PS_KILL) and S12 (PS PRESENT/L) are "last to make; fist to break" short pins. Dimensions as follows:



HOST BOARD MOUNTING PROPOSED ORIENTATION



OUTPUT CONNECTOR PIN ASSIGNMENTS - D1U54-D-450-12-HxxC

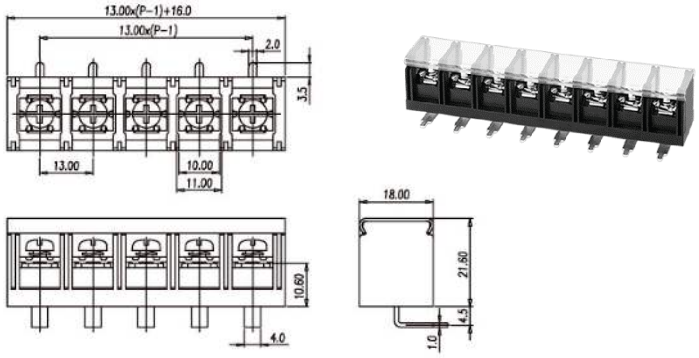
(Power Supply Gold Finger/Card

Pin#	Signal Name	Description/Comment
P1-P8 inclusive	V1 (+12VOUT)	+12V Main Output
P9-P16 inclusive	V1 (+12VOUT) RTN/PGND)	+12V Main Output Return
S1	+VSB (+5V)	Standby Output
S2	+VSB (+5V)	Standby Output
S3	Reserved	No User Connection
S4	ISHARE	Active (Analogue) Current Share Bus
S5	SDA	I^2C Serial Data Line
S6	SCL	I^2C Serial Clock Line
S7	SMB_ALERT	Alert signal to host system
S8	PS_ON_L	Remote On/Off (Enable/Disable)
S9	PS_KILL	Power Supply “kill”; short pin
S10	DCOK/L	DC Input Source Present & “OK”
S11	PW_OK	Power “OK”
S12	PS PRESENT/L	Power Module Present; short pin
S13	Reserved	No User Connection
S14	Reserved	No User Connection
S15	V1_SENSE_R	-VE Remote Sense Return
S16	V1_SENSE	+VE Remote Sense
S17	ADDR	Address Protocol Selection; (select address by use of the appropriate pull down resistor – see table below)
S18	Reserved	No User Connection
S19	+VSB (+5V)	Standby Output
S20	+VSB (+5V)	Standby Output

INPUT TERMINAL BLOCK

Dinkle Enterprise DT-7C-B14W-02

A two positon barrier style terminal block is probided for conneciton to DC input supply.



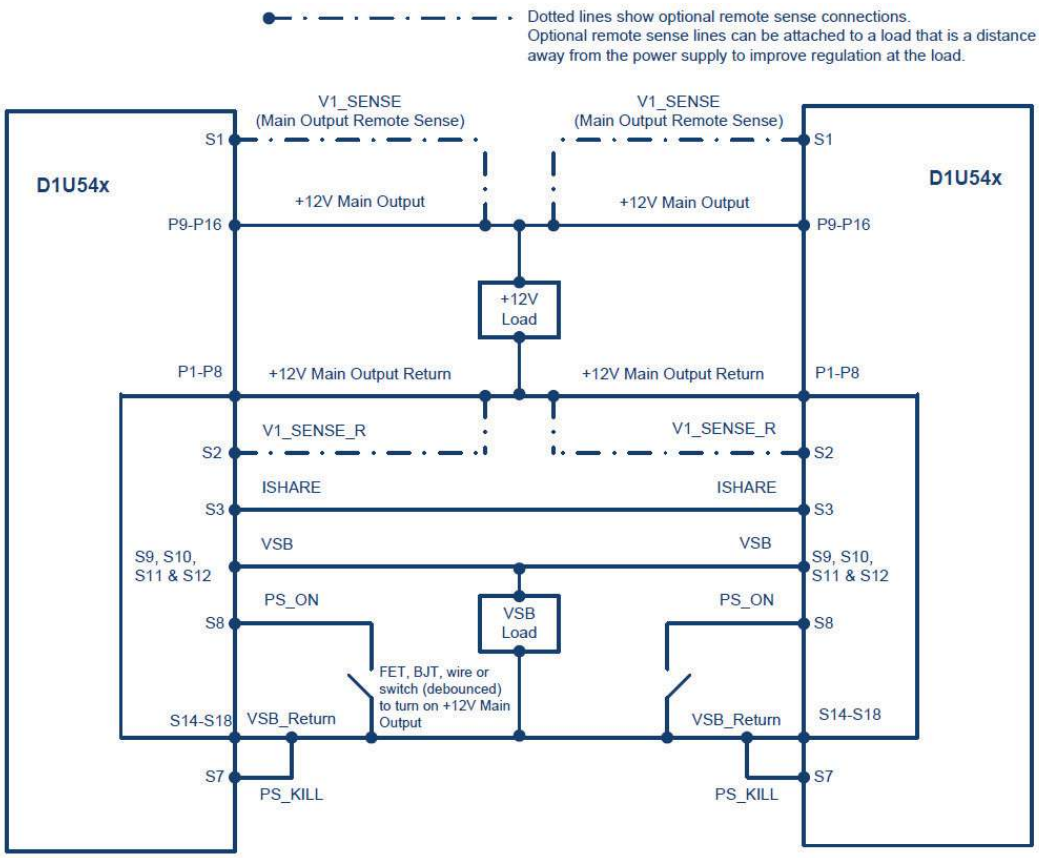
ADDR ADDRESS SELECTION

ADDR pin (A3) resistor to GND (K-ohm)*	Power Supply Main Controller (Serial Communications Slave Address)	Power Supply External EEPROM (Serial Communications Slave Address)
0.82	0xB0	0xA0
2.7	0xB2	0xA2
5.6	0xB4	0xA4
8.2	0xB6	0xA6
15	0xB8	0xA8
27	0xBA	0xAA
56	0xBC	0xAC
180	0xBE	0xAE

* The resistor shall be +/-5% tolerance

#BackToADDRSig

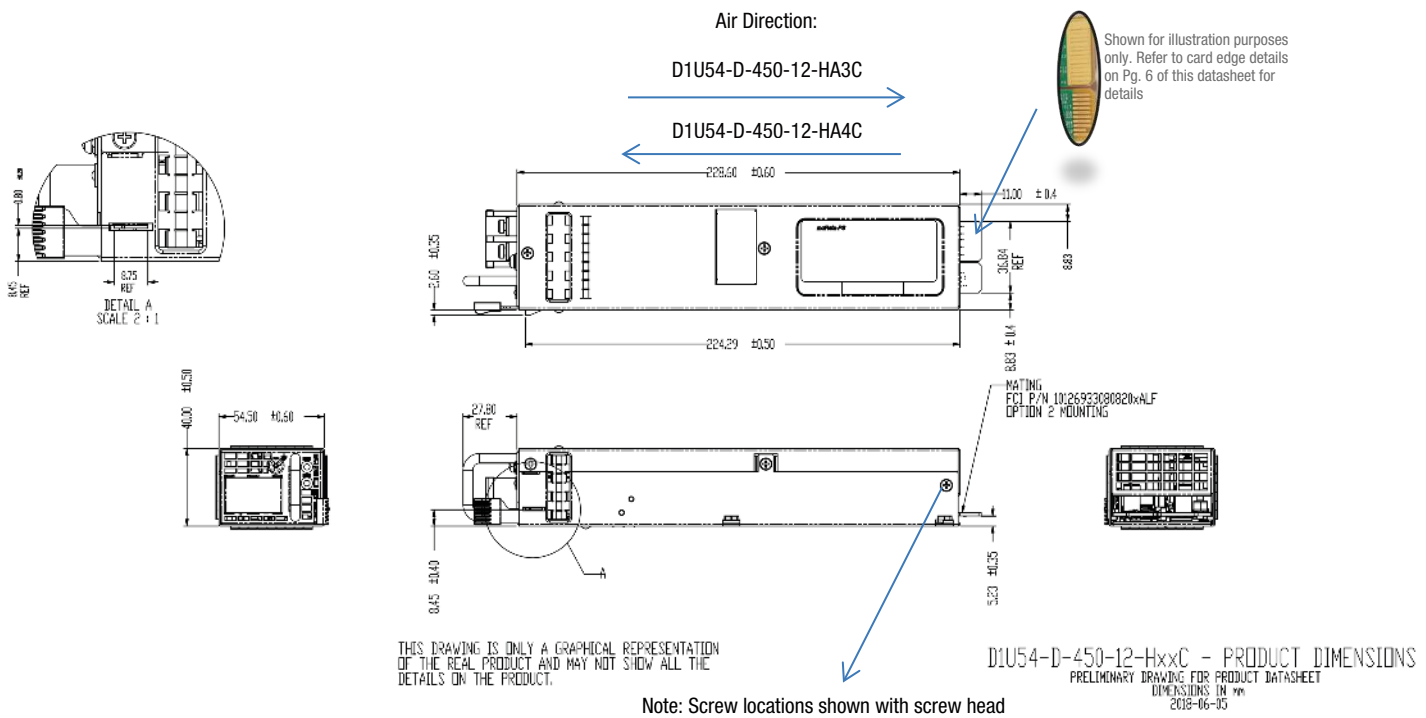
WIRING DIAGRAM FOR OUTPUT



CURRENT SHARE NOTES

1. Main Output: Current sharing is achieved using the active current share method details.)
2. Current sharing can be achieved with or without the remote (V_SENSE) connected to the common load.
3. +VSB Outputs can be tied together for redundancy but total combined output power must not exceed the rated standby power. The +VSB output has an internal ORing MOSFET for additional redundancy/internal short protection.
4. The current sharing pin is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load. For two units sharing the same load this would read 4VDC for perfect current sharing (i.e. 50% load per unit).
5. The load for both the main 12Vdc and the VSB rails at initial startup shall not be allowed to exceed the capability of a single unit. The load can be increased after a delay of 3sec (minimum), to allow all sharing units to achieve steady state regulation.

MECHANICAL DIMENSIONS



1. DC input Input Terminal Block is a Dinkle Enterprise DT-7C-B14W-02
2. Dimensions: 2.15" x 9.0" x 1.57" (54.5mm x 228.6mm x 40.0mm)
3. This drawing is a graphical representation of the product and may not show all fine details.
4. Reference File: I:\Eng_wip\UserPDDwg\1919\D1U54-D-650-12-HBxC_DRAWING FOR PRODUCT DATASHEET

OPTIONAL ACCESSORIES

Description	Part Number
12V D1U54P Output Connector Card	D1U54P-12-EDGE

APPLICATION NOTES

Document Number	Description	Link
ACAN-73	D1U54P-54-CONC-EDGE Output Connector Card	Link to ACAN-73
ACAN-74	D1U54P-x Communication Protocol	Link to ACAN-74

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ISO 9001 REGISTERED